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Kind regards,

Team Nexperia

# PHP101NQ03LT

## N-channel TrenchMOS logic level FET

Rev. 04 — 2 March 2009

**Product data sheet** 

### 1. Product profile

#### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

#### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Simple gate drive required due to low gate charge
- Suitable for logic level gate drive sources

### 1.3 Applications

■ DC-to-DC convertors

#### 1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	-	30	V
I <sub>D</sub>	drain current	$T_{mb} = 25 \text{ °C}; V_{GS} = 10 \text{ V};$ see <u>Figure 1</u> ; see <u>Figure 3</u>	-	-	75	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>	-	-	166	W
Dynamic	characteristics					
$Q_{GD}$	gate-drain charge	$V_{GS} = 5 \text{ V}; I_D = 50 \text{ A};$ $V_{DS} = 15 \text{ V}; T_j = 25 \text{ °C};$ see Figure 11	-	8	-	nC
Static ch	aracteristics					
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C}; \text{ see } \underline{\text{Figure 9}};$ $\text{see } \underline{\text{Figure 10}}$	-	4.5	5.5	mΩ



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
• •••		-	Ompinioa oatinio	Grupino dymbor
1	G	gate		
2	D	drain	mb	D
3	S	source		
3 mb	D	mounting base; connected to drain		mbb076 S
			SOT78 (TO-220AB; SC-46)	

## 3. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
PHP101NQ03LT	TO-220AB; SC-46	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78			

## **Limiting values**

Table 4. **Limiting values** 

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	30	V
$V_{DGR}$	drain-gate voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}; R_{GS} = 20 \text{ k}\Omega$	-	30	V
$V_{GS}$	gate-source voltage		-20	20	V
I <sub>D</sub>	drain current	$V_{GS} = 10 \text{ V}; T_{mb} = 100 \text{ °C}; \text{ see } \frac{\text{Figure 1}}{\text{Model}}$	-	75	Α
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; see <u>Figure 1</u> ; see <u>Figure 3</u>	-	75	Α
I <sub>DM</sub>	peak drain current	$t_p \le 10 \mu\text{s}; \text{ pulsed};  T_{\text{mb}} = 25 ^{\circ}\text{C}; \text{ see } \frac{\text{Figure 3}}{}$	-	240	А
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>	-	166	W
T <sub>stg</sub>	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
$V_{GSM}$	peak gate-source voltage	pulsed; $\delta = 25 \text{ %}; t_p \le 50 \text{ µs}; T_j \le 150 \text{ °C}$	-25	25	V
Source-dr	ain diode				
Is	source current	T <sub>mb</sub> = 25 °C	-	75	А
I <sub>SM</sub>	peak source current	$t_p \le 10 \ \mu s$ ; pulsed; $T_{mb} = 25 \ ^{\circ}C$	-	240	А
Avalanche	ruggedness				
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $I_D$ = 43 A; $V_{sup} \le$ 15 V; unclamped; $t_p$ = 0.19 ms; $R_{GS}$ = 50 $\Omega$	-	185	mJ

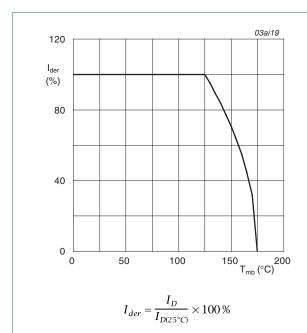


Fig 1. Normalized continuous drain current as a function of mounting base temperature

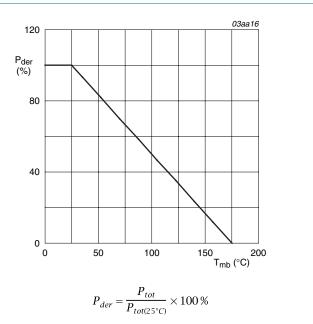
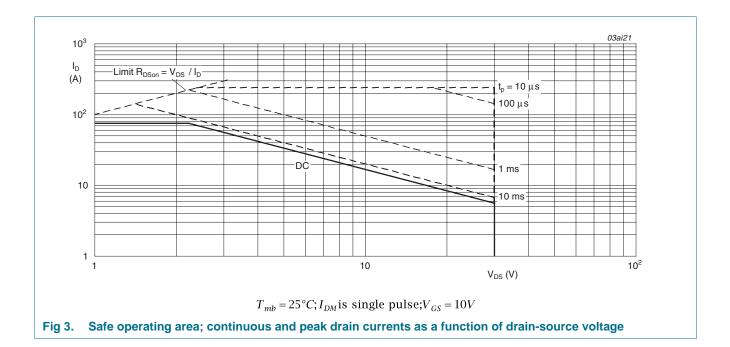


Fig 2. Normalized total power dissipation as a function of mounting base temperature

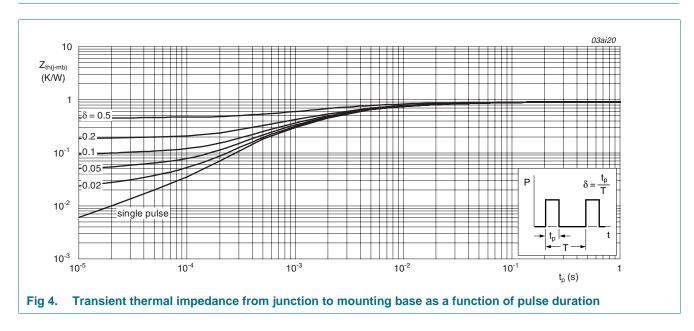
**Product data sheet** 



#### 5. Thermal characteristics

Table 5. Thermal characteristics

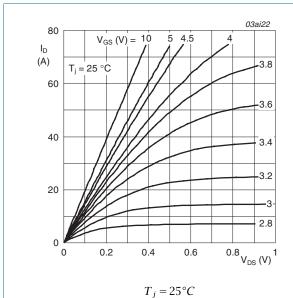
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in free air	-	60	-	K/W
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	see Figure 4	-	-	0.19	K/W



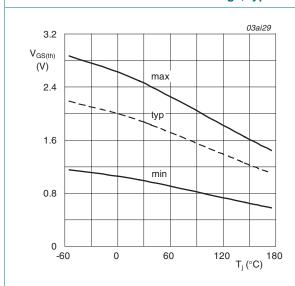
### 6. Characteristics

Table 6. Characteristics

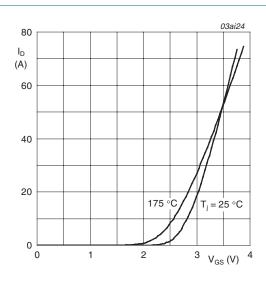
Table 0.						
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	aracteristics					
V <sub>(BR)DSS</sub>		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	27	-	-	V
	breakdown voltage	$I_D = 250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = 25 \ ^{\circ}C$	30	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$ ; $T_j = -55$ °C; see <u>Figure 7</u> ; see <u>Figure 8</u>	-	-	2.9	V
		$I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$ ; $T_j$ = 175 °C; see <u>Figure 7</u> ; see <u>Figure 8</u>	0.6	-	-	V
		$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ °C}$ ; see <u>Figure 7</u> ; see <u>Figure 8</u>	1	1.9	2.5	V
I <sub>DSS</sub>	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.05	1	μΑ
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 ^{\circ}\text{C}$	-	-	500	μΑ
I <sub>GSS</sub>	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; see <u>Figure 9</u> ; see <u>Figure 10</u>	-	4.5	5.5	mΩ
		$V_{GS} = 5 \text{ V}$ ; $I_D = 25 \text{ A}$ ; $T_j = 175 \text{ °C}$ ; see Figure 9; see Figure 10	-	10.5	13.5	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 9</u> ; see <u>Figure 10</u>	-	5.8	7.5	mΩ
Dynamic	characteristics					
Q <sub>G(tot)</sub>	total gate charge	$I_D = 50 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 5 \text{ V};$	-	23	-	nC
Q <sub>GS</sub>	gate-source charge	T <sub>j</sub> = 25 °C; see <u>Figure 11</u>	-	10.5	-	nC
$Q_{GD}$	gate-drain charge		-	8	-	nC
C <sub>iss</sub>	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	2180	-	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; see <u>Figure 12</u>	-	600	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	225	-	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 15 \text{ V}; R_L = 0.6 \Omega; V_{GS} = 4.5 \text{ V};$	-	23	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 5.6 \Omega; T_j = 25 \text{ °C}; I_D = 25 \text{ A}$	-	90	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	37	-	ns
t <sub>f</sub>	fall time		-	33	-	ns
Source-d	rain diode					
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C};$ see <u>Figure 13</u>	-	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S = 10 \text{ A}$ ; $dI_S/dt = -100 \text{ A/}\mu\text{s}$ ; $V_{GS} = 0 \text{ V}$ ;	-	37	-	ns
Q <sub>r</sub>	recovered charge	$V_{DS} = 25 \text{ V}; T_j = 25 \text{ °C}$	-	33	-	nC



Output characteristics: drain current as a function of drain-source voltage; typical values

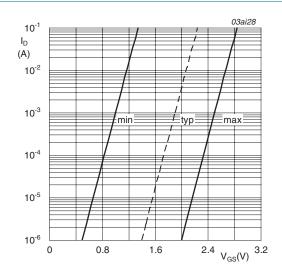


 $I_D = 1mA; V_{DS} = V_{GS}$ Gate-source threshold voltage as a function of Fig 7. junction temperature



 $T_j = 25$ °C and 175°C;  $V_{DS} > I_D \times R_{DSon}$ 

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



 $T_{j} = 25^{\circ}C; V_{DS} = 5V$ 

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Sub-threshold drain current as a function of Fig 8. gate-source voltage

**Product data sheet** 

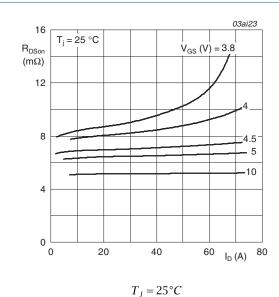
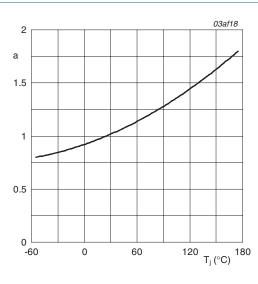


Fig 9. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature

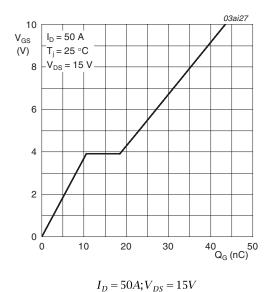
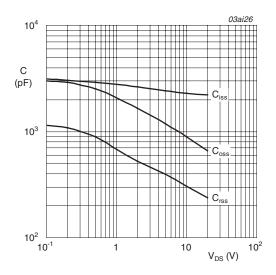


Fig 11. Gate-source voltage as a function of gate charge; typical values

**Product data sheet** 

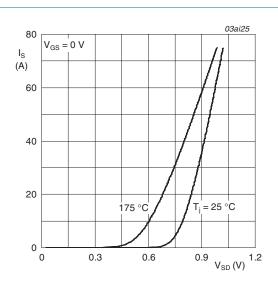
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 $V_{GS} = 0V; f = 1MHz$ 

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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 $T_j = 25 \,^{\circ} C \text{ and } 175 \,^{\circ} C; V_{GS} = 0V$ 

Fig 13. Source current as a function of source-drain voltage; typical values

### 7. Package outline

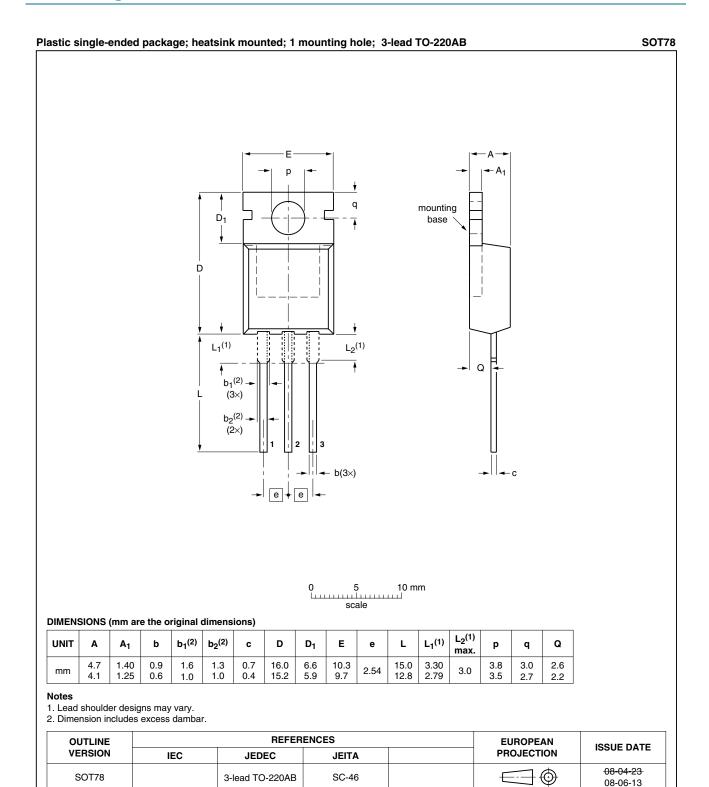


Fig 14. Package outline SOT78 (TO-220AB)

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## 8. Revision history

#### Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHP101NQ03LT_4	20090302	Product data sheet	-	PHP_PHU101NQ03LT_3
Modifications:		f this data sheet has been NXP Semiconductors.	en redesigned to comply	with the new identity
	<ul> <li>Legal texts h</li> </ul>	ave been adapted to the	e new company name w	here appropriate.
PHP_PHU101NQ03LT_3	20051117	Product data sheet	CPCN # 200309016	PHP_PHU101NQ03LT-02
PHP_PHU101NQ03LT-02 (9397 750 10927)	20030225	Product data	-	PHP_PHD_PHB_PHU101 NQ03LT-01
PHP_PHD_PHB_PHU101 NQ03LT-01 (9397 750 09307)	20020220	Product data	-	-

### 9. Legal information

#### 9.1 Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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## PHP101NQ03LT

### N-channel TrenchMOS logic level FET

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