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Kind regards,

Team Nexperia

CBT3244A

Octal bus switch with quad output enables

Rev. 02 — 15 September 2005 Product data sheet

1. General description

The CBT3244A provides eight bits of high-speed TTL-compatible bus switching in a standard '244 device pinout. The low ON-state resistance of the switch allows connections to be made with minimal propagation delay.

The CBT3244A device is organized as two 4-bit low-impedance switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is LOW, the switch is on and data can flow from port A to port B, or vice versa. When $\overline{OE}$ is HIGH, the switch is open and high-impedance state exists between the two ports.

The CBT3244A is characterized for operation from −40 °C to +85 °C.

2. Features

- Standard '244-type pinout
- 5 Ω switch connection between two ports
- TTL compatible control input levels
- Package options include:
  - plastic small outline (SO20)
  - shrink small outline (SSOP20)
  - shrink small outline, QSOP (SSOP20)
  - thin shrink small outline (TSSOP20)
  - depopulated heatsink very thin quad flat package, no leads (DHVQFN20)
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

PHILIPS

3. Ordering information

Table 1: Ordering information

$T_{amb} = -40\,°C$ to $+85\,°C$

Type number	Topside mark	Package		
		Name	Description	Version
CBT3244ABQ	CT3244A	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
CBT3244APW	CT3244A	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
CBT3244ADS	CT3244ADS	SSOP20 [1]	plastic shrink small outline package; 20 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT724-1
CBT3244ADB	CT3244A	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
CBT3244AD	CBT3244AD	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

[1] Also known as QSOP20.

Standard packing quantities and other packaging data are available at *www.standardics.philips.com/packaging*.

4. Functional diagram

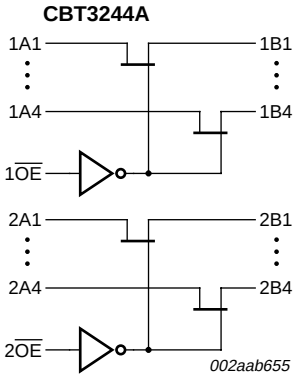


Fig 1. Logic diagram of CBT3244A

5. Pinning information

5.1 Pinning

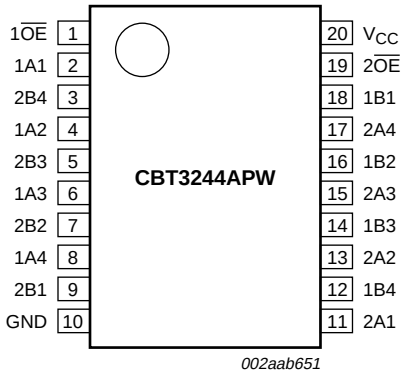


Fig 2. Pin configuration for TSSOP20

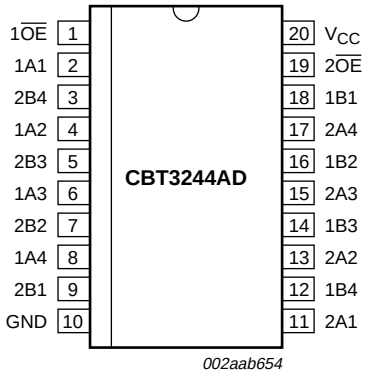


Fig 3. Pin configuration for SO20

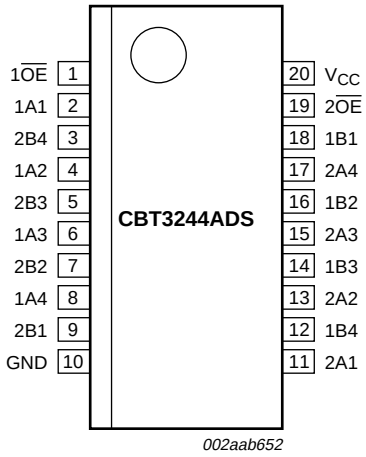


Fig 4. Pin configuration for SSOP20 (QSOP)

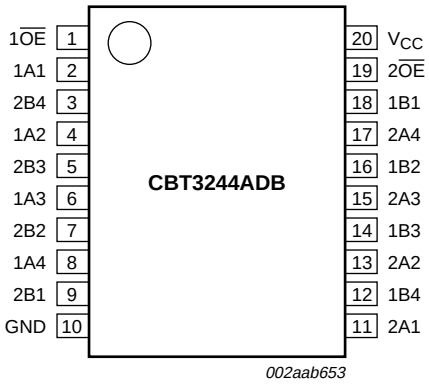
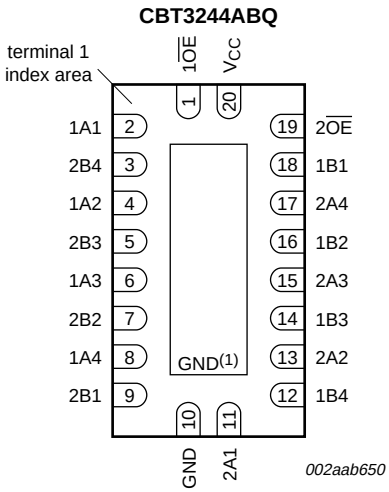


Fig 5. Pin configuration for SSOP20



Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It cannot be used as a supply pin or input.

Fig 6. Pin configuration for DHVQFN20

5.2 Pin description

Table 2: Pin description

Symbol	Pin	Description
$1\overline{OE}$	1	output enable (active LOW)
1A1, 1A2, 1A3, 1A4	2, 4, 6, 8	inputs
2A1, 2A2, 2A3, 2A4	11, 13, 15, 17	inputs
1B1, 1B2, 1B3, 1B4	18, 16, 14, 12	outputs
2B1, 2B2, 2B3, 2B4	9, 7, 5, 3	outputs
GND	10	ground (0 V)
$2\overline{OE}$	19	output enable (active LOW)
V_{CC}	20	positive supply voltage

6. Functional description

Refer to Figure 1 “Logic diagram of CBT3244A”.

6.1 Function table

Table 3: Function selection

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF state

Inputs		Outputs	
$1\overline{OE}$	$2\overline{OE}$	1An, 1Bn	2An, 2Bn
L	L	1An = 1Bn	2An = 2Bn
L	H	1An = 1Bn	Z
H	L	Z	2An = 2Bn
H	H	Z	Z

7. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). [1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V		-	–18	mA
V_I	input voltage		[2]	–1.2	+7.0	V
I_{OK}	output clamping current	$V_O < 0$ V		-	–50	mA
V_O	output voltage	output in OFF or HIGH state	[2]	–0.5	+7.0	V
I_O	output current	output in LOW state		-	128	mA
T_{stg}	storage temperature			–65	+150	°C

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

[2] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5: Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_{IH}	HIGH-state input voltage		2.0	-	-	V
V_{IL}	LOW-state input voltage		-	-	0.8	V
T_{amb}	ambient temperature	operating in free-air	–40	-	+85	°C

9. Static characteristics

Table 6: Static characteristics

T_{amb} = –40 °C to +85 °C

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_I = –18 mA	-	-	–1.2	V
I_{LI}	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V	-	-	±1	µA
I_{CC}	quiescent supply current	V_{CC} = 5.5 V; I_O = 0 mA; V_I = V_{CC} or GND	-	1	3	µA
ΔI_{CC} [2]	additional quiescent supply current (per input)	V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND	-	-	2.5	mA
C_i	input capacitance (control pins)	V_I = 3 V or 0 V; $n\overline{OE}$ = V_{CC}	-	3	-	pF
C_{io}	input/output capacitance	$n\overline{OE}$ = V_{CC} = 5.0 V	-	3	-	pF
R_{on} [3]	ON-state resistance	V_{CC} = 4.5 V; V_I = 0 V; I_I = 64 mA	-	4	7	Ω
		V_{CC} = 4.5 V; V_I = 0 V; I_I = 30 mA	-	4	7	Ω
		V_{CC} = 4.5 V; V_I = 2.4 V; I_I = 15 mA	-	8	15	Ω

[1] All typical values are at V_{CC} = 5 V; T_{amb} = 25 °C.

[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

[3] Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two (A or B) terminals.

10. Dynamic characteristics

Table 7: Dynamic characteristics

T_{amb} = –40 °C to +85 °C; V_{CC} = 5.0 V ± 0.5 V; GND = 0 V; C_L = 50 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PD}	propagation delay [1]	from nAn input to nBn output, or from nBn input to nAn output	-	-	0.25	ns
t_{en}	enable time [2]	from $n\overline{OE}$ input to nAn or nBn output	1.0	-	5.6	ns
t_{dis}	disable time [3]	from $n\overline{OE}$ input to nAn or nBn output	1.0	-	6.0	ns

[1] This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical ON-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

[2] Output enable time to HIGH and LOW level.

[3] Output disable time from HIGH and LOW level.

10.1 AC waveforms

V_M = 1.5 V; V_I = GND to 3.0 V

t_{PLZ} and t_{PHZ} are the same as t_{dis}.

t_{PZL} and t_{PZH} are the same as t_{en}.

t_{PLH} and t_{PHL} are the same as t_{PD}.

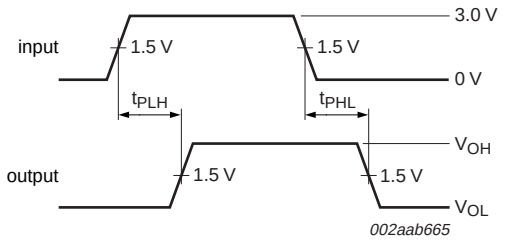
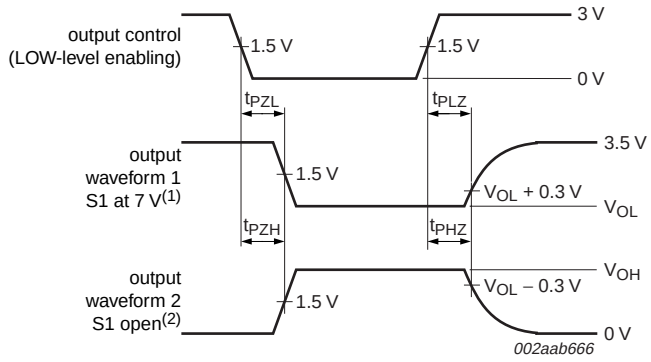


Fig 7. Input to output propagation delays

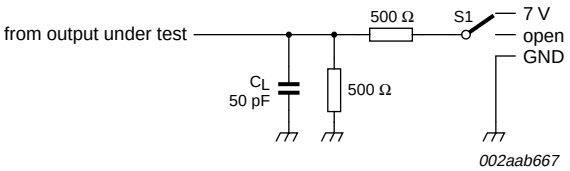


(1) Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.

(2) Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

Fig 8. 3-state output enable and disable times

11. Test information



Test data are given in Table 8.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns.

The outputs are measured one at a time with one transition per measurement.

C_L = load capacitance includes jig and probe capacitance.

R_L = load resistance.

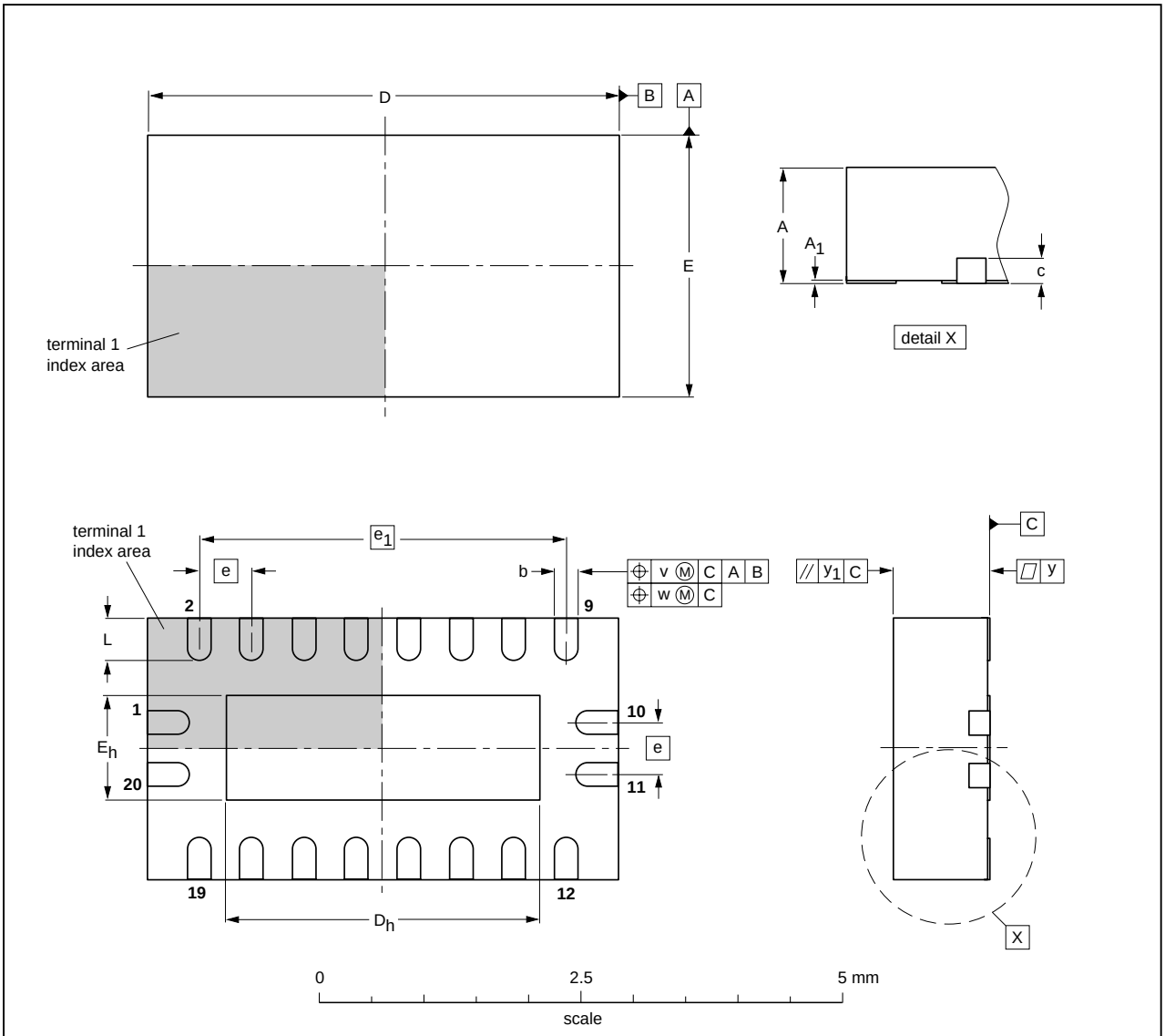
Fig 9. Test circuit

Table 8: Test data

Test	Load		Switch
	C_L	R_L	
t_{PD}	50 pF	500 Ω	open
t_{PLZ}/t_{PZL}	50 pF	500 Ω	7 V
t_{PHZ}/t_{PZH}	50 pF	500 Ω	open

12. Package outline

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm **SOT764-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.6 4.4	3.15 2.85	2.6 2.4	1.15 0.85	0.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

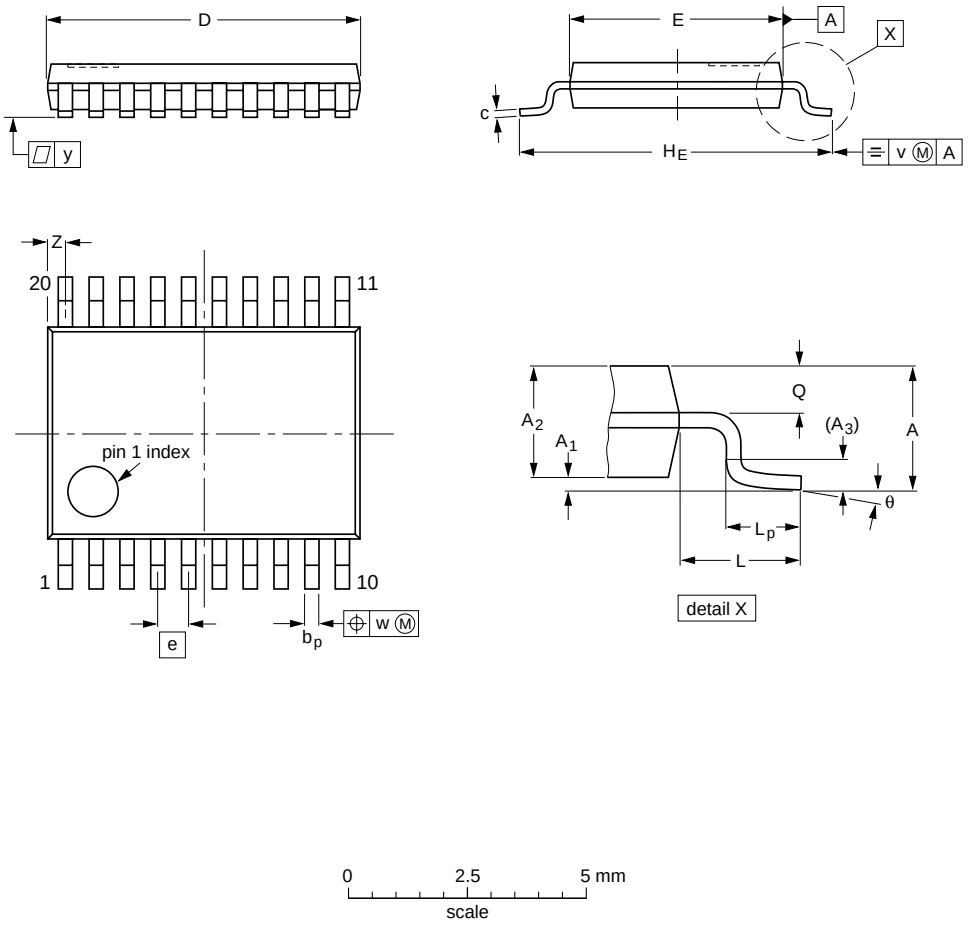
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT764-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 10. Package outline SOT764-1 (DHVQFN20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

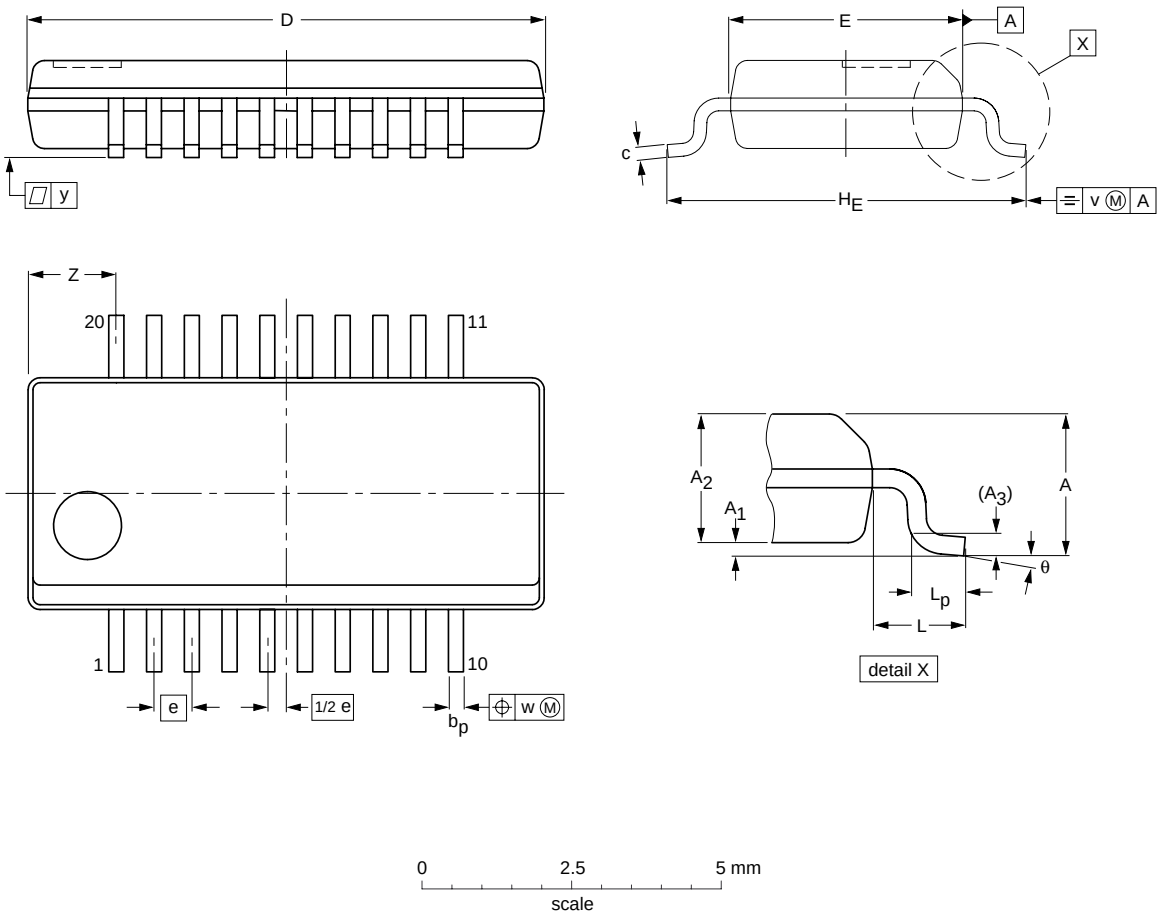
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT360-1 (TSSOP20)

SSOP20: plastic shrink small outline package; 20 leads; body width 3.9 mm; lead pitch 0.635 mm **SOT724-1**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.73	0.25 0.10	1.55 1.40	0.25	0.31 0.20	0.25 0.18	8.8 8.6	4.0 3.8	0.635	6.2 5.8	1	0.89 0.41	0.25	0.18	0.1	1.67 1.28	8^o 0^o

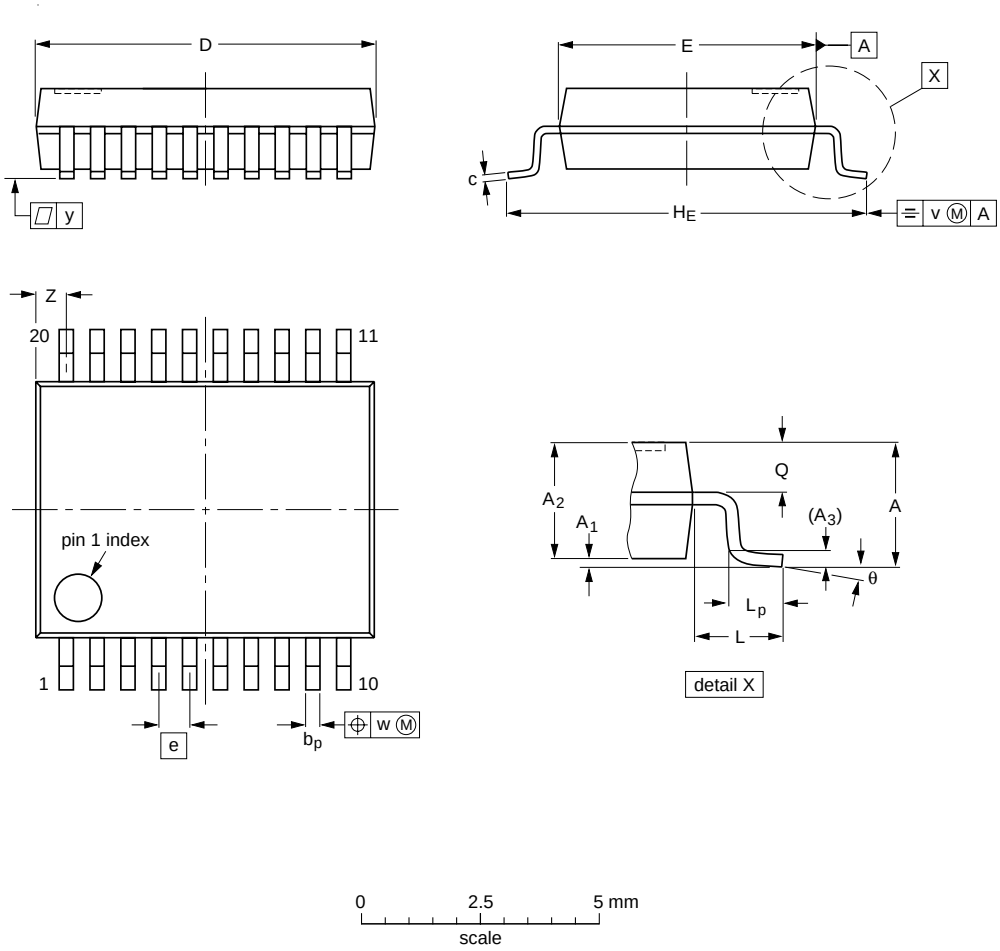
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT724-1		MO-137				~~01-07-04~~ 03-02-18

Fig 12. Package outline SOT724-1 (SSOP20) (QSOP20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8^o 0^o

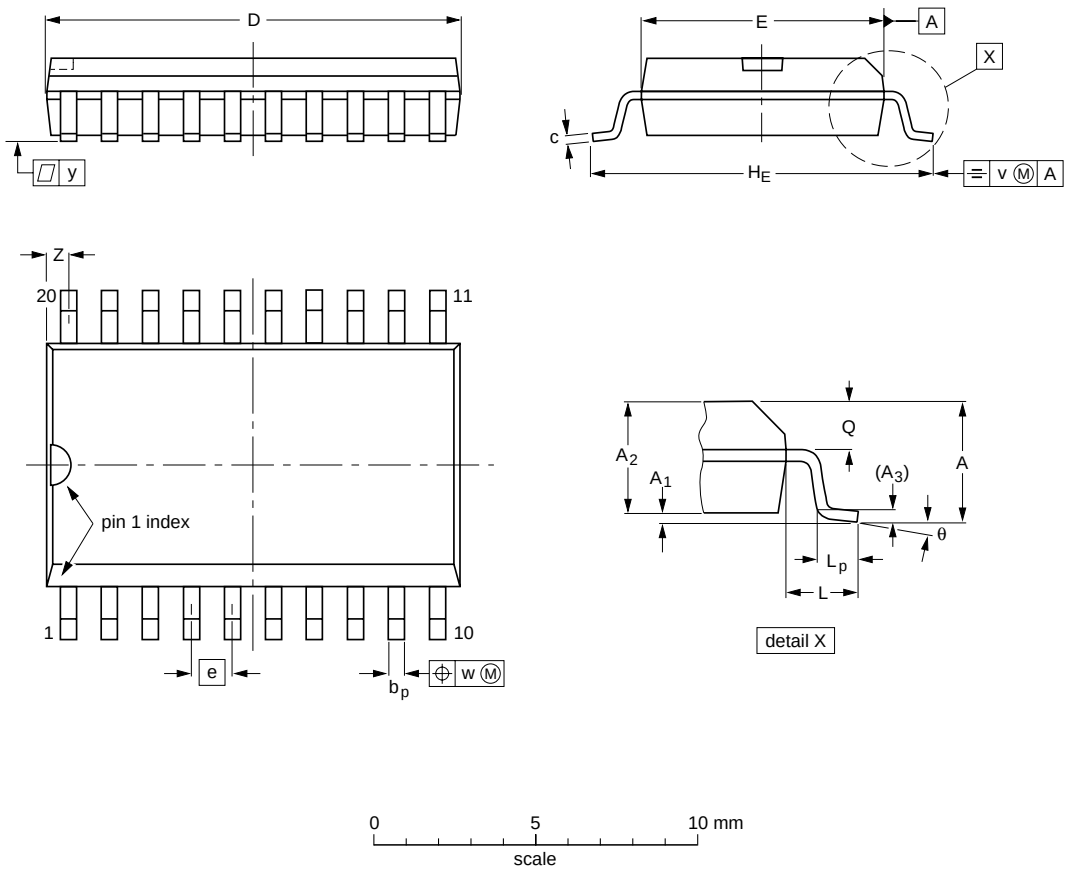
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT339-1 (SSOP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 14. Package outline SOT163-1 (SO20)

13. Soldering

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

13.5 Package related soldering information

Table 9: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

14. Abbreviations

Table 10: Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

15. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
CBT3244_2	20050915	Product data sheet	-	9397 750 13362	CBT3244A_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • added DHVQFN20 package option (affects Section 2 “Features”, Section 3 “Ordering information”, Section 5 “Pinning information”, and Section 12 “Package outline” • Section 2 “Features” on page 1, 6th bullet: changed from ‘exceeds 1000 V HBM ...’ to ‘exceeds 2000 V HBM ...’ • added Section 14 “Abbreviations” on page 16				
CBT3244A_1	20040526	Product data sheet	-	9397 750 13281	-

16. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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21. Contents

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