

74HC4515

4-to-16 line decoder/demultiplexer with input latches; inverting

Rev. 3 — 2 July 2018

Product data sheet

1 General description

The 74HC4515 is a 4-to-16 line decoder/demultiplexer having four binary weighted address inputs (A0 to A3) with latches, a latch enable input (LE), an enable input (\bar{E}) and 16 inverting outputs ($\bar{Q}0$, to $\bar{Q}15$).

When LE is HIGH, the selected output is determined by the data on An. When LE goes LOW, the last data present at An are stored in the latches and the outputs remain stable. When \bar{E} is LOW, the selected output, determined by the contents of the latch, is LOW. When \bar{E} is HIGH, all outputs are HIGH. The enable input \bar{E} does not affect the state of the latch. When the device is used as a demultiplexer, \bar{E} is the data input and A0 to A3 are the address inputs.

Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2 Features and benefits

- Inverting outputs
- CMOS input levels
- 16-line demultiplexing capability
- Decodes 4 binary-coded inputs into 16 mutually-exclusive outputs
- Complies with JEDEC standard no. 7 A
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3 Applications

- Digital multiplexing
- Address decoding
- Hexadecimal/BCD decoding

4 Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC4515D	-40 °C to +125 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

5 Functional diagram

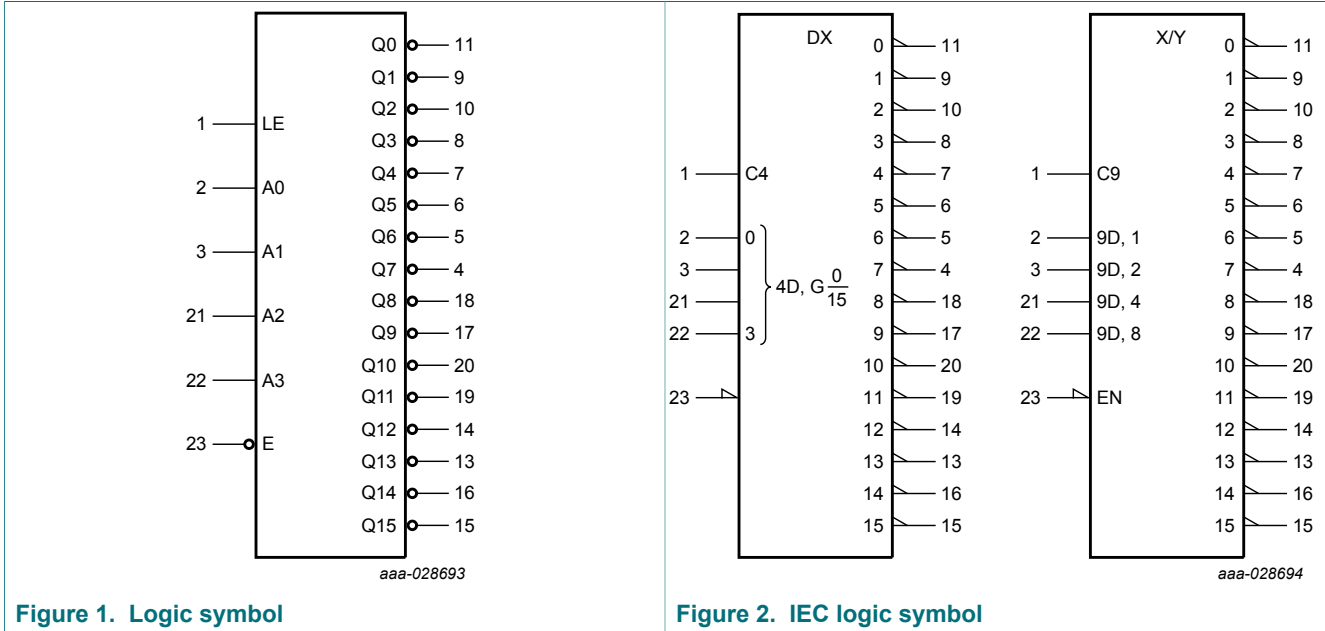


Figure 1. Logic symbol

Figure 2. IEC logic symbol

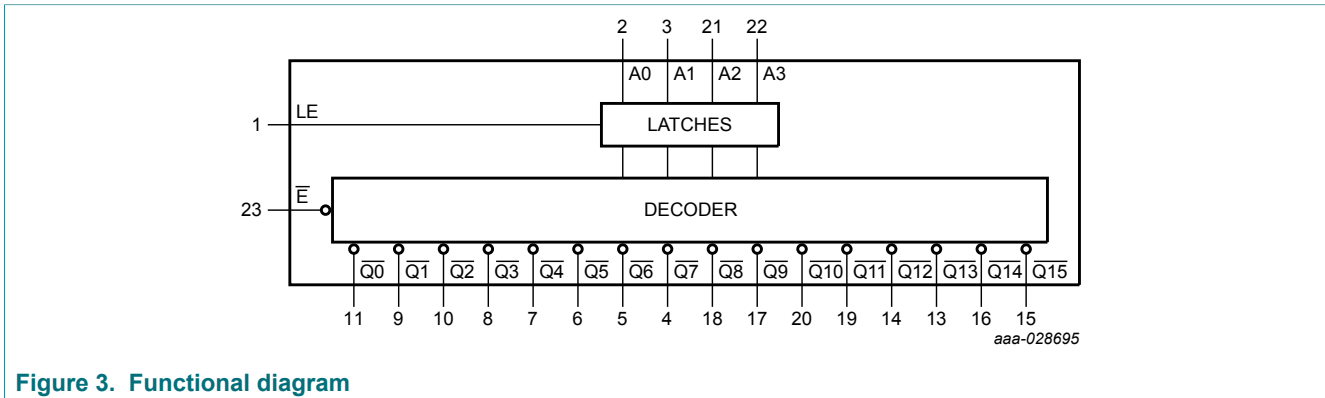


Figure 3. Functional diagram

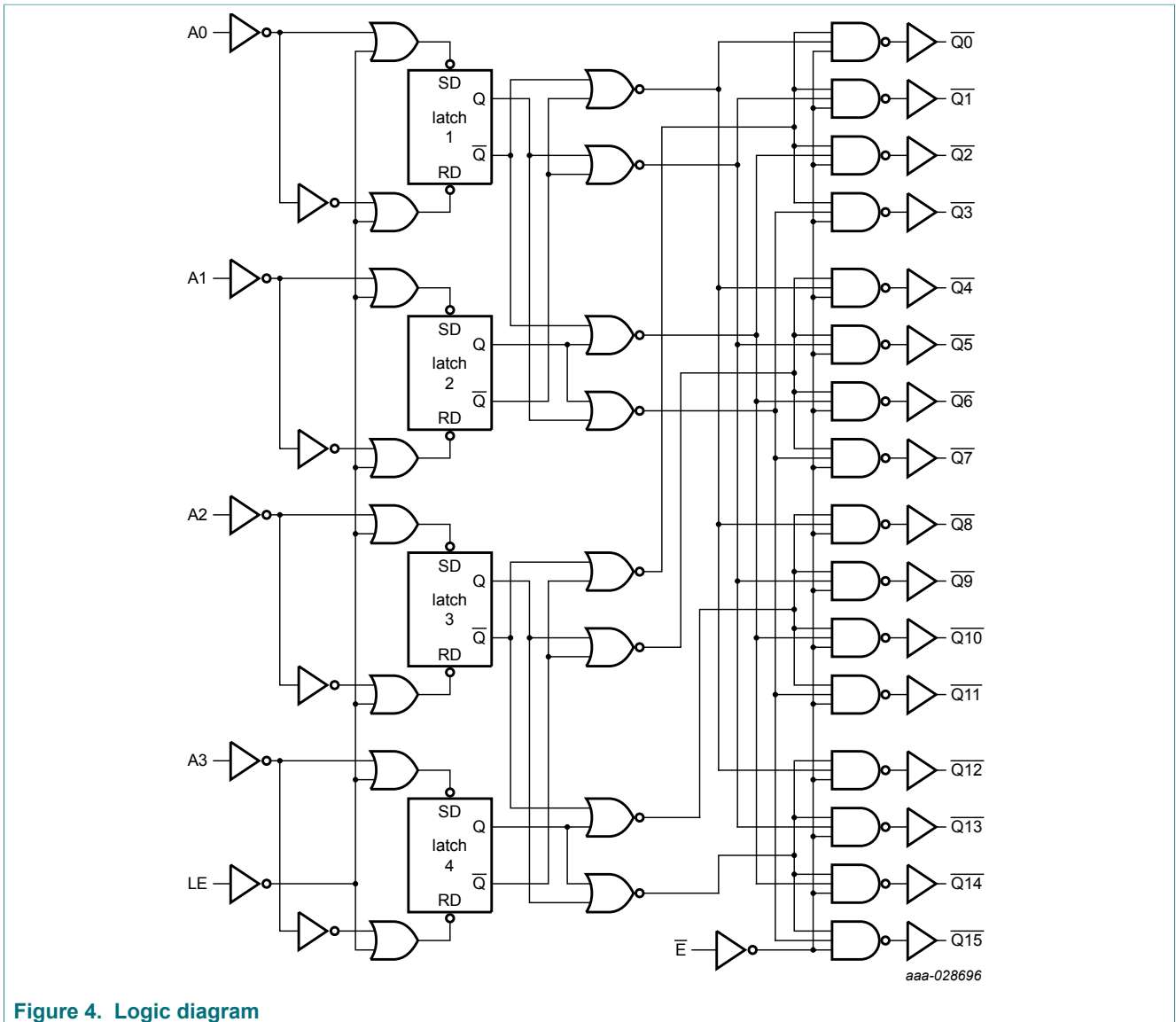


Figure 4. Logic diagram

6 Pinning information

6.1 Pinning

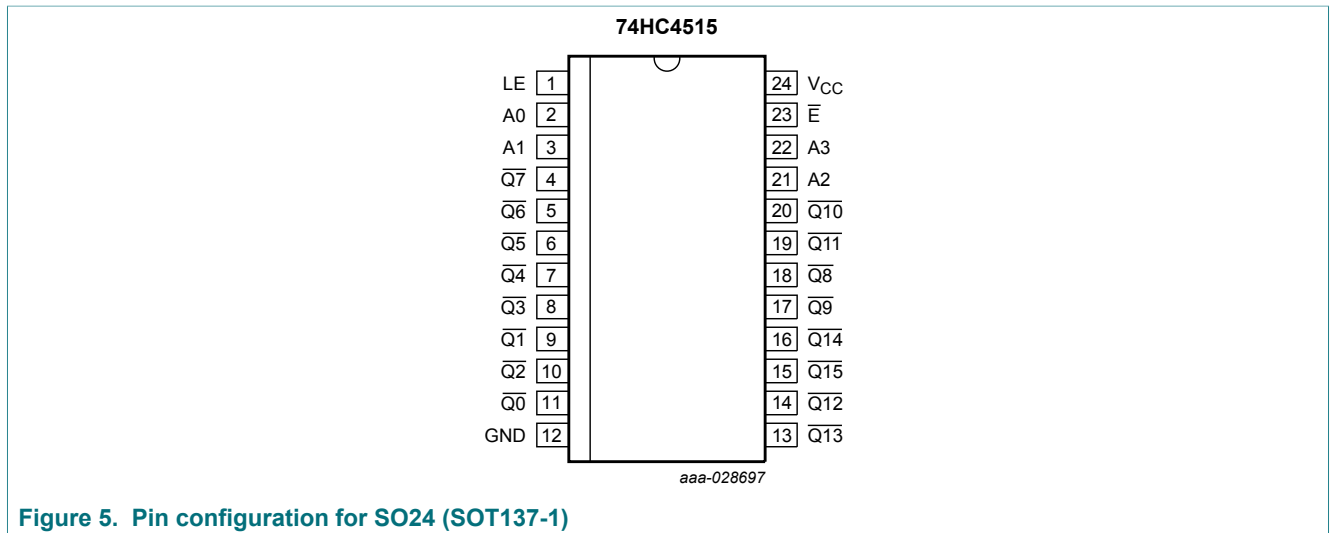


Figure 5. Pin configuration for SO24 (SOT137-1)

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
LE	1	latch enable input (active HIGH)
\bar{E}	23	enable input (active LOW)
$\bar{Q}0, \bar{Q}1, \bar{Q}2, \bar{Q}3, \bar{Q}4, \bar{Q}5, \bar{Q}6, \bar{Q}7, \bar{Q}8, \bar{Q}9, \bar{Q}10, \bar{Q}11, \bar{Q}12, \bar{Q}13, \bar{Q}14, \bar{Q}15$	11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15	multiplexer outputs (active LOW)
A0, A1, A2, A3	2, 3, 21, 22	address inputs
GND	12	ground (0 V)
V _{CC}	24	supply voltage

7 Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Inputs ^[1]					Outputs															
E	A0	A1	A2	A3	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10	Q11	Q12	Q13	Q14	Q15
H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
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L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

[1] LE = HIGH

8 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	± 25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	SO24	[1]	500	mW

[1] P_{tot} derates linearly with 8 mW/K above 70 °C.

9 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		2.0	5.0	6.0	V
V _I	input voltage		0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	V
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	ns/V
		V _{CC} = 4.5 V	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	ns/V
T _{amb}	ambient temperature		-40	-	+125	°C

10 Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} (°C)						Unit	
			+25			-40 to +85		-40 to +125		
			Min	Typ	Max	Min	Max	Min		Max
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
	I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V	
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
	I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V	

4-to-16 line decoder/demultiplexer with input latches; inverting

Symbol	Parameter	Conditions	T _{amb} (°C)						Unit	
			+25			-40 to +85		-40 to +125		
			Min	Typ	Max	Min	Max	Min		Max
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

11 Dynamic characteristics

Table 7. Dynamic characteristics

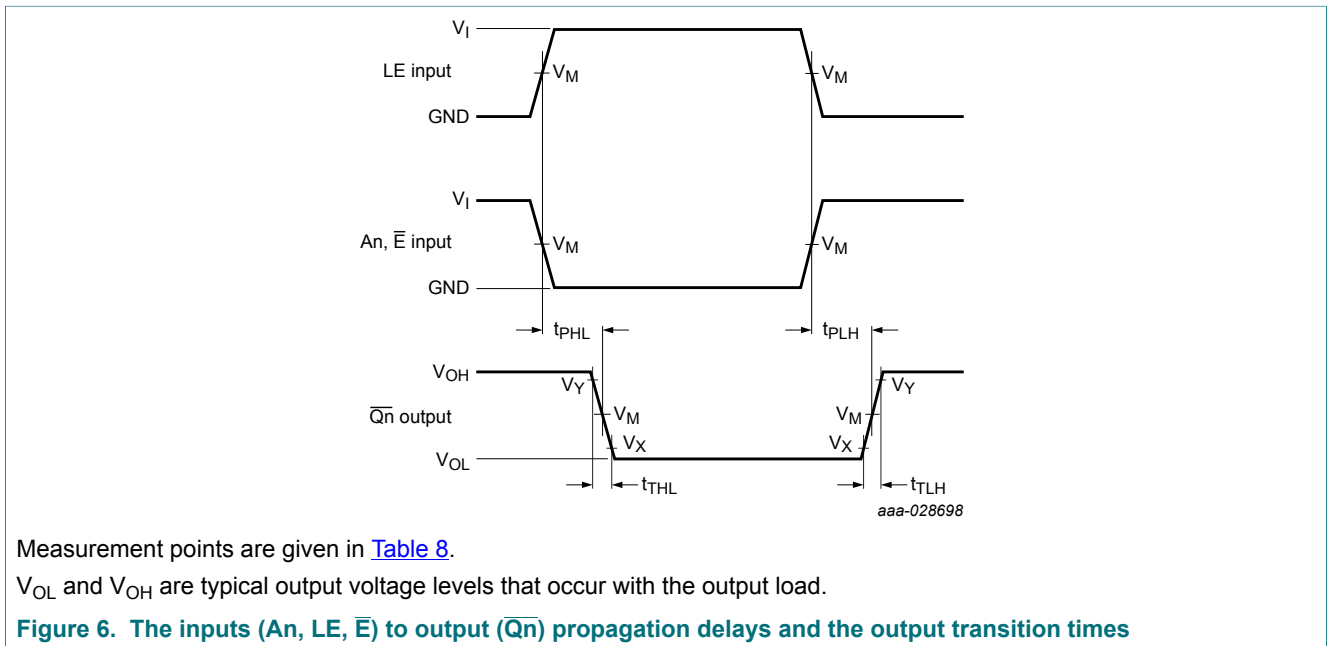
Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 8.

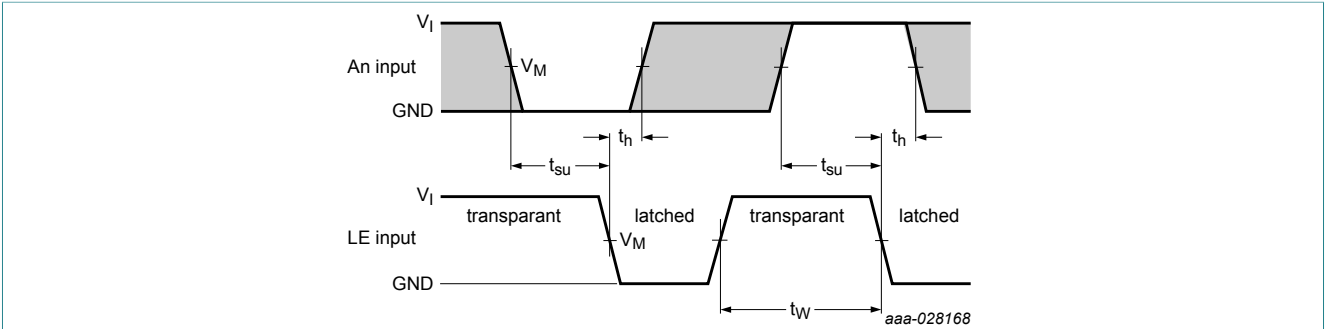
Symbol	Parameter	Conditions	T _{amb} (°C)						Unit	
			+25			-40 to +85		-40 to +125		
			Min	Typ	Max	Min	Max	Min		Max
t _{pd}	propagation delay	An to \overline{Qn} ; see Figure 6 ^[1]								
		V _{CC} = 2.0 V	-	80	250	-	315	-	375	ns
		V _{CC} = 4.5 V	-	29	50	-	63	-	75	ns
		V _{CC} = 5 V; C _L = 15 pF	-	25	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	23	43	-	54	-	64	ns
		LE to \overline{Qn} ; see Figure 6								
		V _{CC} = 2.0 V	-	66	225	-	280	-	340	ns
		V _{CC} = 4.5 V	-	24	45	-	56	-	68	ns
		V _{CC} = 6.0 V	-	19	38	-	48	-	58	ns
		\overline{E} to \overline{Qn} ; see Figure 6								
		V _{CC} = 2.0 V	-	50	175	-	220	-	265	ns
		V _{CC} = 4.5 V	-	18	35	-	44	-	53	ns
V _{CC} = 6.0 V	-	14	30	-	37	-	45	ns		
t _t	transition time	\overline{Qn} ; see Figure 6 ^[2]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t _w	pulse width	LE HIGH; see Figure 7								
		V _{CC} = 2.0 V	75	14	-	95	-	110	-	ns
		V _{CC} = 4.5 V	15	5	-	19	-	22	-	ns
		V _{CC} = 6.0 V	13	4	-	16	-	19	-	ns

Symbol	Parameter	Conditions	T _{amb} (°C)						Unit	
			+25			-40 to +85		-40 to +125		
			Min	Typ	Max	Min	Max	Min		Max
t _{su}	set-up time	An to LE; see Figure 7								
		V _{CC} = 2.0 V	90	28	-	115	-	135	-	ns
		V _{CC} = 4.5 V	18	10	-	23	-	27	-	ns
		V _{CC} = 6.0 V	15	8	-	20	-	23	-	ns
t _h	hold time	An to LE; see Figure 7								
		V _{CC} = 2.0 V	0	-11	-	0	-	0	-	ns
		V _{CC} = 4.5 V	0	-4	-	0	-	0	-	ns
		V _{CC} = 6.0 V	0	-3	-	0	-	0	-	ns
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} ^[3]	-	44	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PLH} and t_{PHL}
- [2] t_t is the same as t_{TLH} and t_{THL}
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of load switching outputs;
 Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

11.1 Waveforms and test circuit





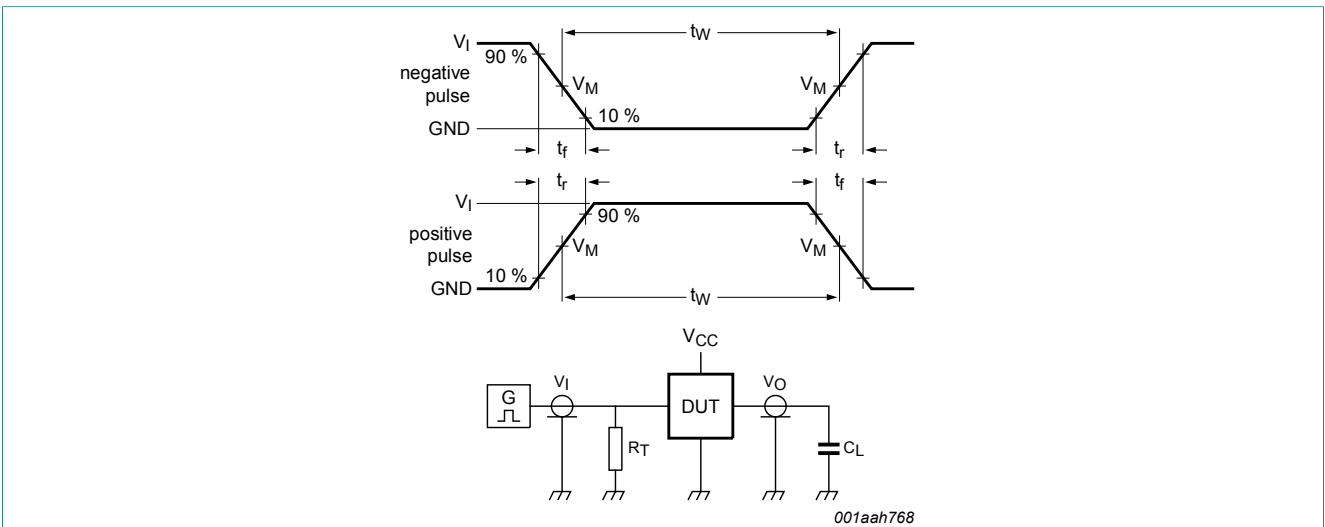
Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 7. Data set-up and hold times for An input to LE input and LE input pulse width

Table 8. Measurement points

Input	Output			
V_I	V_M	V_M	V_X	V_Y
GND to V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$



Test data is given in [Table 9](#).

Definitions for test circuit:

R_T = Termination resistance; should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

Figure 8. Test circuit for measuring switching times

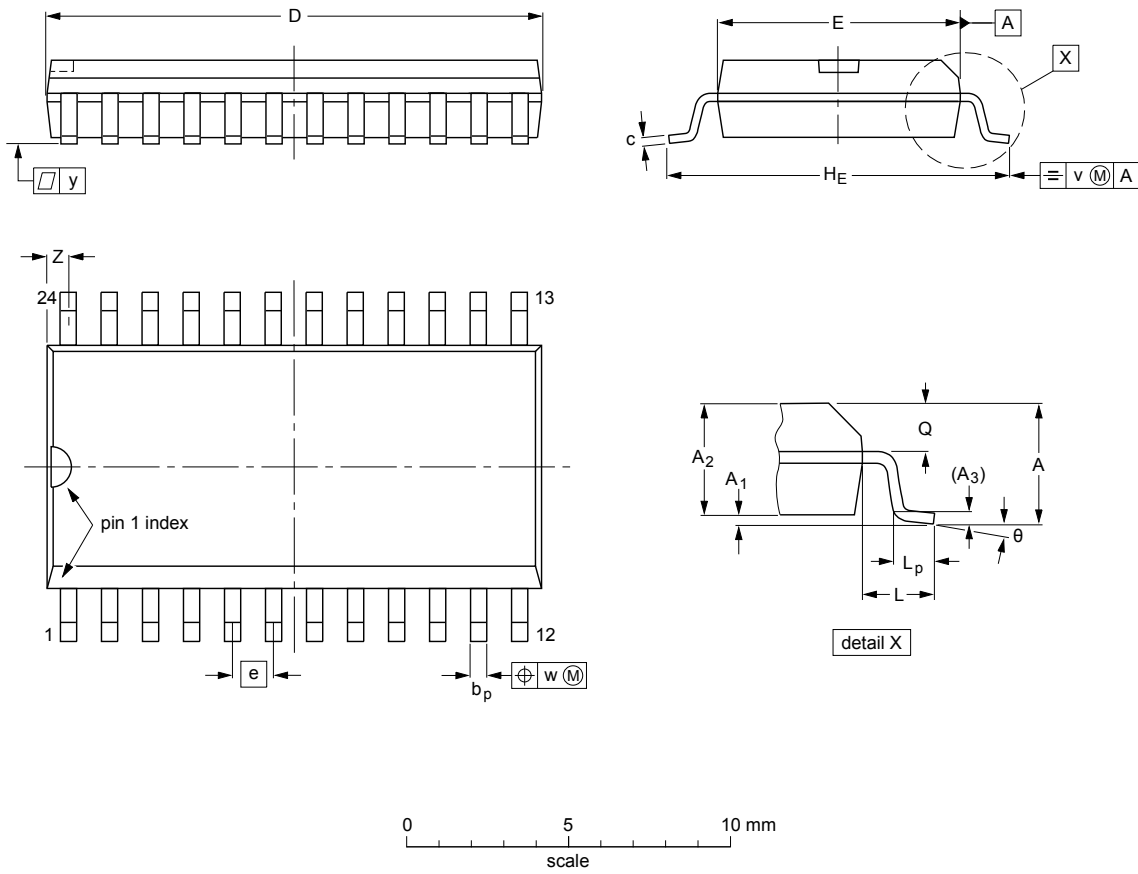
Table 9. Test data

Input		Load
V_I	t_r, t_f	C_L
GND to V_{CC}	6 ns	15 pF, 50 pF

12 Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				99-12-27 03-02-19

Figure 9. Package outline SOT137-1 (SO24)

13 Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC4515 v.3	20180702	Product data sheet	-	74HC_HCT4515 v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type numbers 74HCT4515D (SOT137-1), 74HC4515N (SOT101) and 74HCT4515N (SOT101) removed. 			
74HC_HCT4515 v.2	19930901	Product specification	-	74HC_HCT4515 v.1

15 Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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