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Kind regards,

Team Nexperia

DATA SHEET

74ALVCH16646

16-bit bus transceiver/register (3-State)

Product specification

1998 Sep 03

IC24 Data Handbook

16-bit bus transceiver/register (3-State)

74ALVCH16646

FEATURES

- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through pin-out architecture
- Low inductance, multiple V_{CC} and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- Output drive capability 50Ω transmission lines @ 85°C
- All inputs have bushold circuitry

DESCRIPTION

The 74ALVCH16646 consists of 16 non-inverting bus transceiver circuits with 3-State outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the 'A' or 'B' bus will be clocked in the internal registers, as the appropriate clock (CP_{AB} or CP_{BA}) goes to a HIGH logic level. Output enable (OE) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the 'A' or 'B' register, or in both. The select source inputs (S_{AB} and S_{BA}) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when OE is active (LOW). In the isolation mode (OE = HIGH), 'A' data may be stored in the 'B' register and/or 'B' data may be stored in the 'A' register.

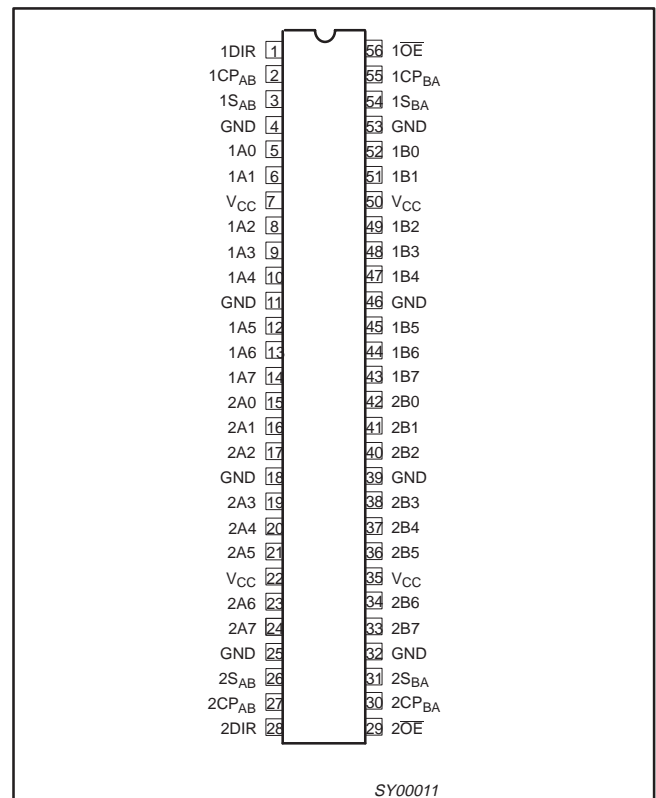
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, 'A' or 'B' may be driven at a time.

To ensure the high impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the

minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; t_r = t_f ≤ 2.5ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t _{PHL} /t _{PLH}	Propagation delay nAx to nBx	V _{CC} = 2.5V, C _L = 30pF V _{CC} = 3.3V, C _L = 50pF		2.6 2.7	ns
C _I	Input capacitance			3.0	pF
C _{PD}	Power dissipation capacitance per channel	V _I = GND to V _{CC} ¹	Outputs enabled	36	pF
			Outputs disabled	4	
F _{max}	Maximum clock frequency	V _{CC} = 2.5V, C _L = 30pF V _{CC} = 3.3V, C _L = 50pF		300 320	MHz

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic TSSOP Type II	-40°C to +85°C	74ALVCH16646 DGG	ACH16646 DGG	SOT364-1

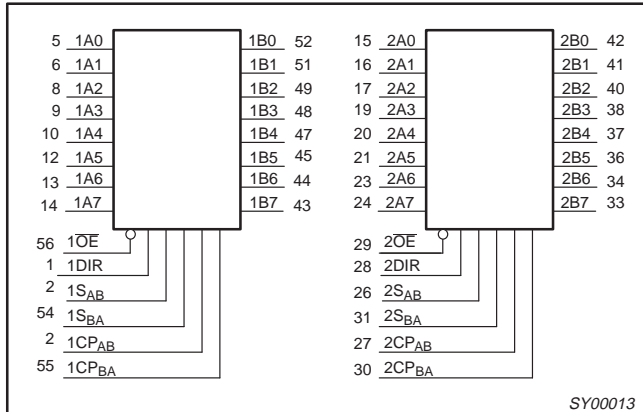
16-bit bus transceiver/register (3-State)

74ALVCH16646

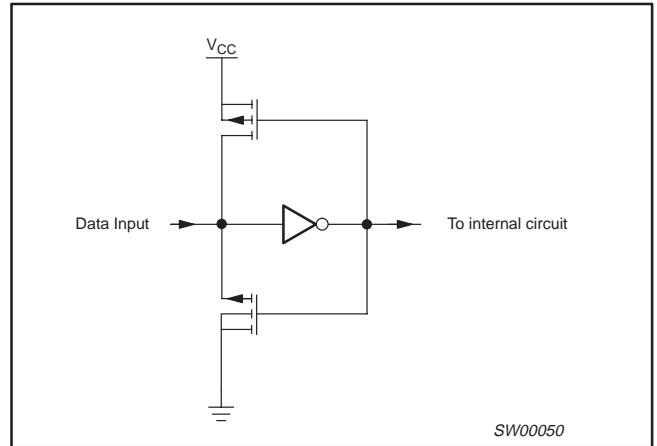
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 28	nDIR	Direction control input
2, 27	nCP _{AB}	Clock input A-to-B
3, 26	nS _{AB}	Select input A-to-B
5, 6, 8, 9, 10, 12, 13, 14	1A0 to 1A7	Data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V _{CC}	Positive supply voltage
15, 16, 17, 19, 20, 21, 23, 24	2A0 to 2A7	Data inputs/outputs
29, 56	nOE	Output enable
30, 55	nCP _{BA}	Clock input B-to-A
31, 54	nS _{BA}	Select input B-to-A
42, 41, 40, 38, 37, 36, 34, 33	2B0 to 2B7	Data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43	1B0 to 1B7	Data inputs/outputs

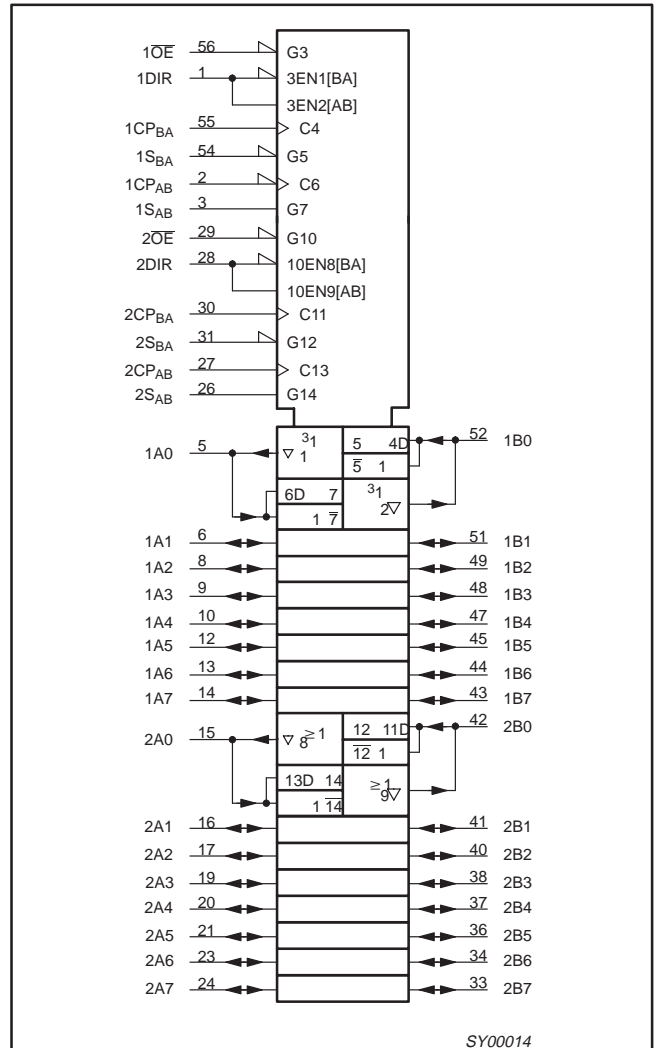
LOGIC SYMBOL



BUSHOLD CIRCUIT



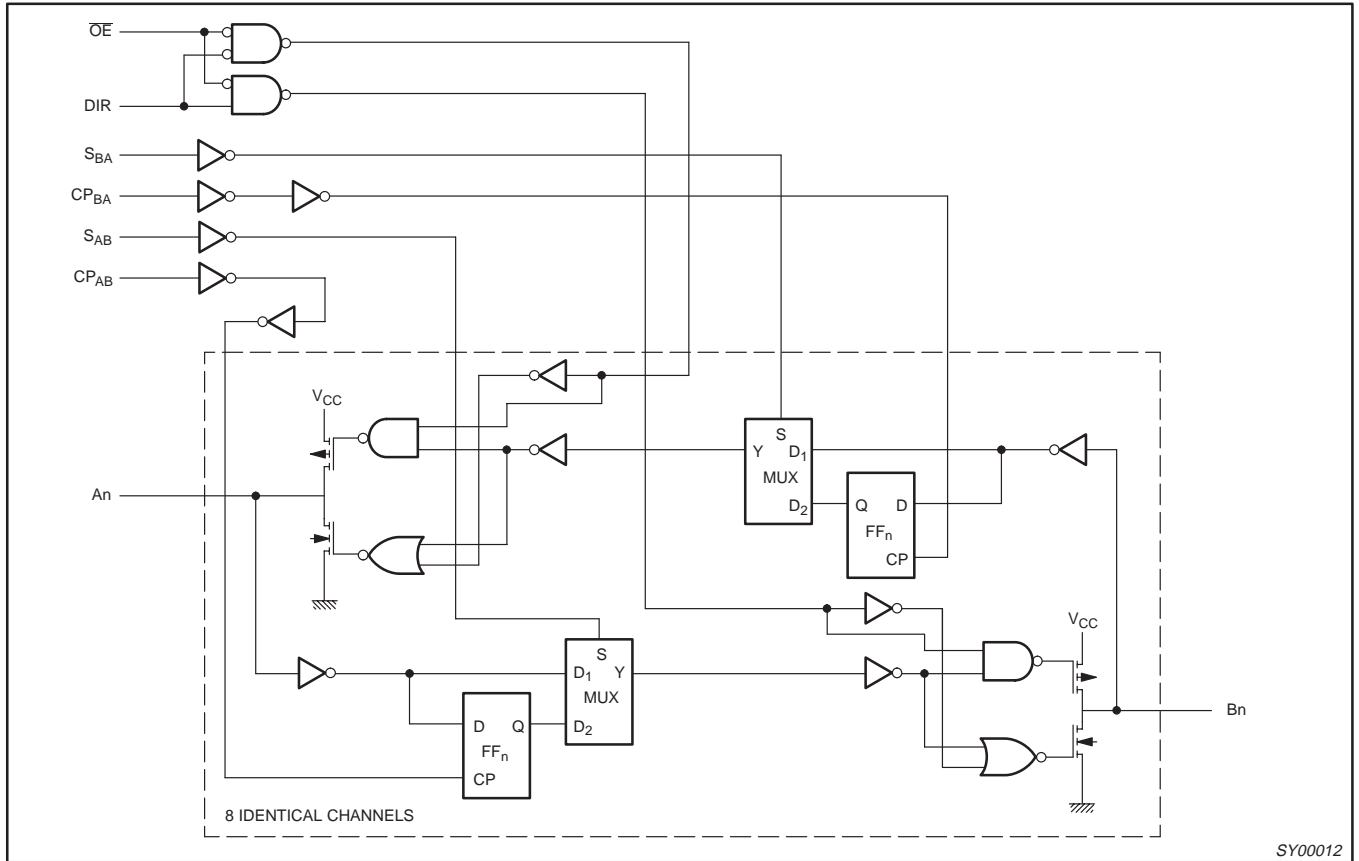
LOGIC SYMBOL (IEEE/IEC)



16-bit bus transceiver/register (3-State)

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LOGIC DIAGRAM (one section)



FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
nOE	nDIR	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
X	X	↑	X	X	X	input	un*	store A, B unspecified*
X	X	X	↑	X	X	un*	input	store B, A unspecified*
H	X	↑	↑	X	X	input	input	store A and B data, isolation
H	X	H or L	H or L	X	X	input	input	hold storage
L	L	X	X	X	L	output	input	real-time B data to A bus
L	L	X	H or L	X	H	output	input	stored B data to A bus
L	H	X	X	L	X	input	output	real-time A data to B bus
L	H	H or L	X	H	X	input	output	stored A data to B bus

* The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

- un = unspecified
- H = HIGH voltage level
- L = LOW voltage level
- X = don't care
- ↑ = LOW-to-HIGH level transition

16-bit bus transceiver/register (3-State)

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		-40	+85	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 2.3$ to $3.0V$ $V_{CC} = 3.0$ to $3.6V$	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage	For control pins ¹	-0.5 to +4.6	V
		For data inputs ¹	-0.5 to $V_{CC} + 0.5$	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	± 50	mA
V_O	DC output voltage	Note 1	-0.5 to $V_{CC} + 0.5$	V
I_O	DC output source or sink current	$V_O = 0$ to V_{CC}	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		± 100	mA
T_{stg}	Storage temperature range		-65 to +150	°C
P_{TOT}	Power dissipation per package -plastic thin-medium-shrink (TSSOP)	For temperature range: -40 to +125 °C	850	mW
		above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	600	

NOTE:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

16-bit bus transceiver/register (3-State)

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 2.3 to 2.7V	1.7	1.2		V
		V _{CC} = 2.7 to 3.6V	2.0	1.5		
V _{IL}	LOW level Input voltage	V _{CC} = 2.3 to 2.7V		1.2	0.7	V
		V _{CC} = 2.7 to 3.6V		1.5	0.8	
V _{OH}	HIGH level output voltage	V _{CC} = 2.3 to 3.6V; V _I = V _{IH} or V _{IL} ; I _O = -100µA	V _{CC} - 0.2	V _{CC}		V
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = -6mA	V _{CC} - 0.3	V _{CC} - 0.08		
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} - 0.6	V _{CC} - 0.26		
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} - 0.5	V _{CC} - 0.14		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} - 0.6	V _{CC} - 0.09		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -24mA	V _{CC} - 1.0	V _{CC} - 0.28		
V _{OL}	LOW level output voltage	V _{CC} = 2.3 to 3.6V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		GND	0.20	V
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = 6mA		0.07	0.40	V
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = 12mA		0.15	0.70	V
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 12mA		0.14	0.40	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 24mA		0.27	0.55	
I _I	Input leakage current	V _{CC} = 2.3 to 3.6V; V _I = V _{CC} or GND		0.1	5	µA
I _{OZ}	3-State output OFF-state current	V _{CC} = 2.7 to 3.6V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND		0.1	10	µA
I _{CC}	Quiescent supply current	V _{CC} = 2.3 to 3.6V; V _I = V _{CC} or GND; I _O = 0		0.2	40	µA
ΔI _{CC}	Additional quiescent supply current	V _{CC} = 2.3V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0		150	750	µA
I _{BHL}	Bus hold LOW sustaining current	V _{CC} = 2.3V; V _I = 0.7V ²	45	-		µA
		V _{CC} = 3.0V; V _I = 0.8V ²	75	150		
I _{BHH}	Bus hold HIGH sustaining current	V _{CC} = 2.3V; V _I = 1.7V ²	-45			µA
		V _{CC} = 3.0V; V _I = 2.0V ²	-75	-175		
I _{BHLO}	Bus hold LOW overdrive current	V _{CC} = 3.6V ²	500			µA
I _{BHHO}	Bus hold HIGH overdrive current	V _{CC} = 3.6V ²	-500			µA

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

16-bit bus transceiver/register (3-State)

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AC CHARACTERISTICS FOR $V_{CC} = 2.3V$ TO $2.7V$ RANGEGND = 0V; $t_r = t_f \leq 2.0ns$; $C_L = 30pF$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 2.5V \pm 0.2V$			
			MIN	TYP	MAX	
t_{PLH}/t_{PHL}	Propagation delay nAx to nBx, nBx to nAx	1	1.0	2.7	4.8	ns
	Propagation delay nCP _{AB} to nBx, nCP _{BA} to nAx	3	1.0	3.4	5.6	
	Propagation delay nS _{AB} to nBx, nS _{BA} to nAx	2	1.0	3.4	6.8	
t_{PZH}/t_{PZL}	3-State output enable time nOE to nAx, nBx	4	1.0	3.3	6.5	ns
t_{PHZ}/t_{PLZ}	3-State output disable time nOE to nAx, nBx	4	1.6	2.8	5.7	ns
t_{PZH}/t_{PZL}	3-State output enable time nDIR to nAx, nBx	5	1.0	3.4	7.8	ns
t_{PHZ}/t_{PLZ}	3-State output disable time nDIR to nAx, nBx	5	1.5	3.0	6.5	ns
t_w	Pulse width HIGH or LOW nCP _{AB} , nCP _{BA}	3	3.3	1.2		ns
t_{SU}	Set up time nAx to nCP _{AB} , nBx to nCP _{BA}	3	1.6	0.2		ns
t_h	Hold time nAx to nCP _{AB} , nBx to nCP _{BA}	3	0.6	0.1		ns
F_{max}	Maximum clock pulse frequency	3	150	300		MHz

NOTE:1. All typical values are at $V_{CC} = 2.5V$ and $T_{amb} = 25^\circ C$.**AC CHARACTERISTICS FOR $V_{CC} = 3.0V$ TO $3.6V$ RANGE AND $V_{CC} = 2.7V$** GND = 0V; $t_r = t_f = 2.5ns$; $C_L = 50pF$

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$			
			MIN	TYP ^{1, 2}	MAX	MIN	TYP ¹	MAX	
t_{PHL}/t_{PLH}	Propagation delay nAx to nBx, nBx to nAx	1	1.0	2.6	3.9	1.0	2.8	4.5	ns
t_{PHL}/t_{PLH}	Propagation delay nCP _{AB} to nBx, nCP _{BA} to nAx	3	1.4	2.9	4.5	1.4	3.1	5.2	ns
t_{PHL}/t_{PLH}	Propagation delay nS _{AB} to nBx, nS _{BA} to nAx	2	1.3	3.1	5.3	1.3	3.5	6.4	ns
t_{PZH}/t_{PZL}	3-State output enable time nOE to nAx, nBx	4	1.0	2.3	5.1	1.0	3.2	6.2	ns
t_{PHZ}/t_{PLZ}	3-State output disable time nOE to nAx, nBx	4	1.0	2.9	4.7	1.0	3.1	5.0	ns
t_{PZH}/t_{PZL}	3-State output enable time nDIR to nAx, nBx	5	1.4	3.0	5.1	1.4	3.4	6.2	ns
t_{PHZ}/t_{PLZ}	3-State output disable time nDIR to nAx, nBx	5	1.4	2.5	5.3	1.4	3.3	6.0	ns
t_w	Pulse width HIGH or LOW nCP _{AB} , nCP _{BA}	3	3.3	0.7		3.3	1.0		ns
t_{SU}	Set up time nAx to nCP _{AB} , nBx to nCP _{BA}	3	1.4	0.3		1.7	0.2		ns
t_h	Hold time nAx to nCP _{AB} , nBx to nCP _{BA}	3	0.7	0.2		0.4	0.1		ns
F_{max}	Maximum clock pulse frequency	3	150	320		150	320		MHz

NOTES:1. All typical values are at $T_{amb} = 25^\circ C$.2. $V_{CC} = 3.3V$

16-bit bus transceiver/register (3-State)

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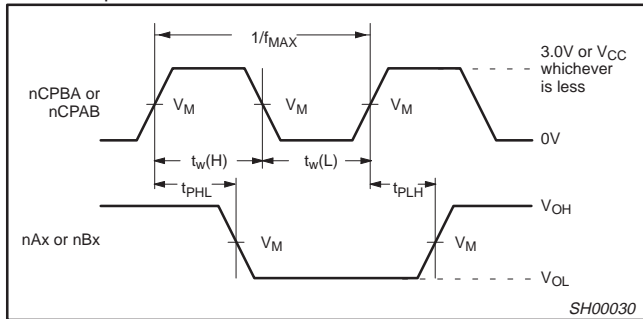
AC WAVEFORMS

V_{CC} = 2.3 TO 2.7 V RANGE

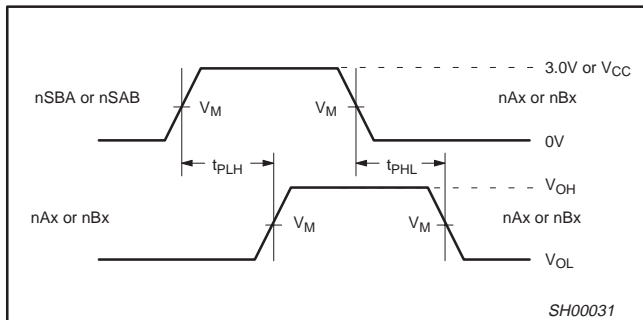
1. V_M = 0.5 V
2. V_X = V_{OL} + 0.15V
3. V_Y = V_{OH} - 0.15V
4. V_I = V_{CC}
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

V_{CC} = 3.0 TO 3.6 V RANGE AND V_{CC} = 2.7 V

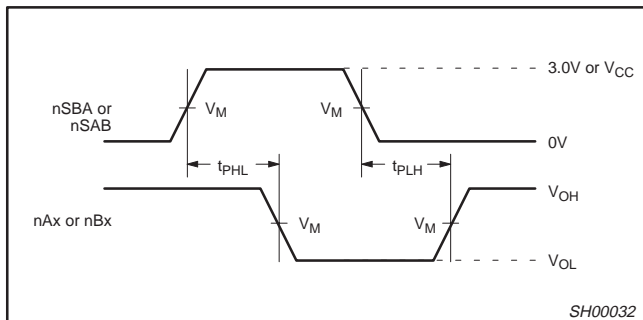
1. V_M = 1.5 V
2. V_X = V_{OL} + 0.3V
3. V_Y = V_{OH} - 0.3V
4. V_I = 2.7 V
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



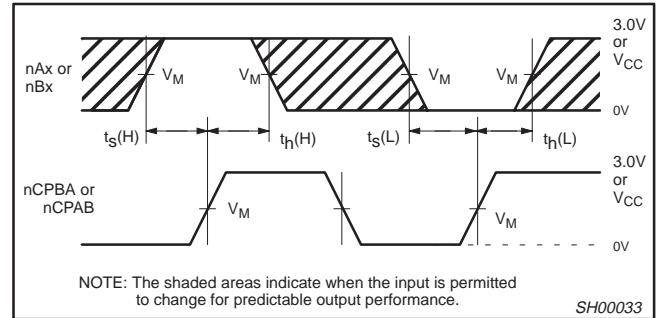
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



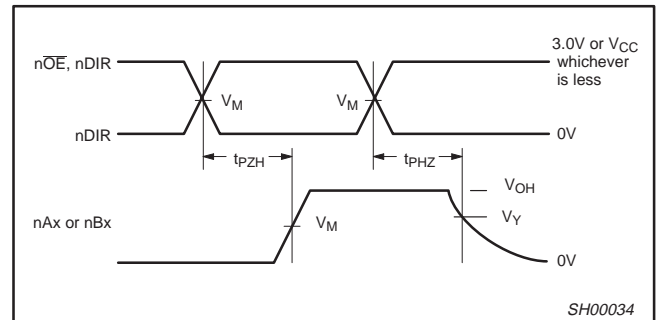
Waveform 2. Propagation Delay, nSAB to nBx or nSBA to nAx, nAx to nBx or nBx to nAx



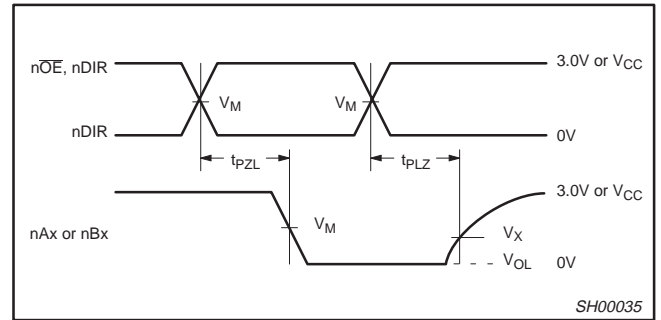
Waveform 3. Propagation Delay, nSBA to nAx or nSAB to nBx



Waveform 4. Data Setup and Hold Times

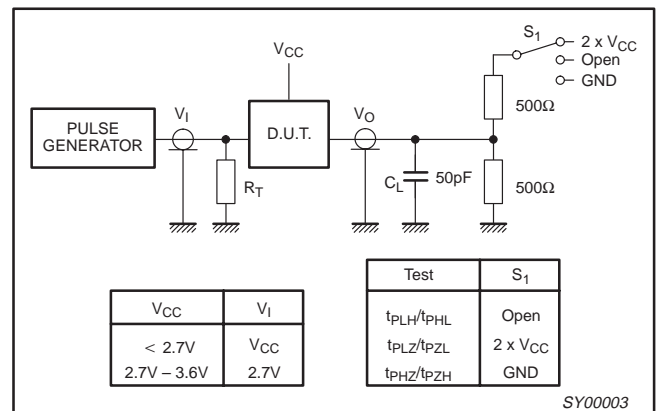


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT

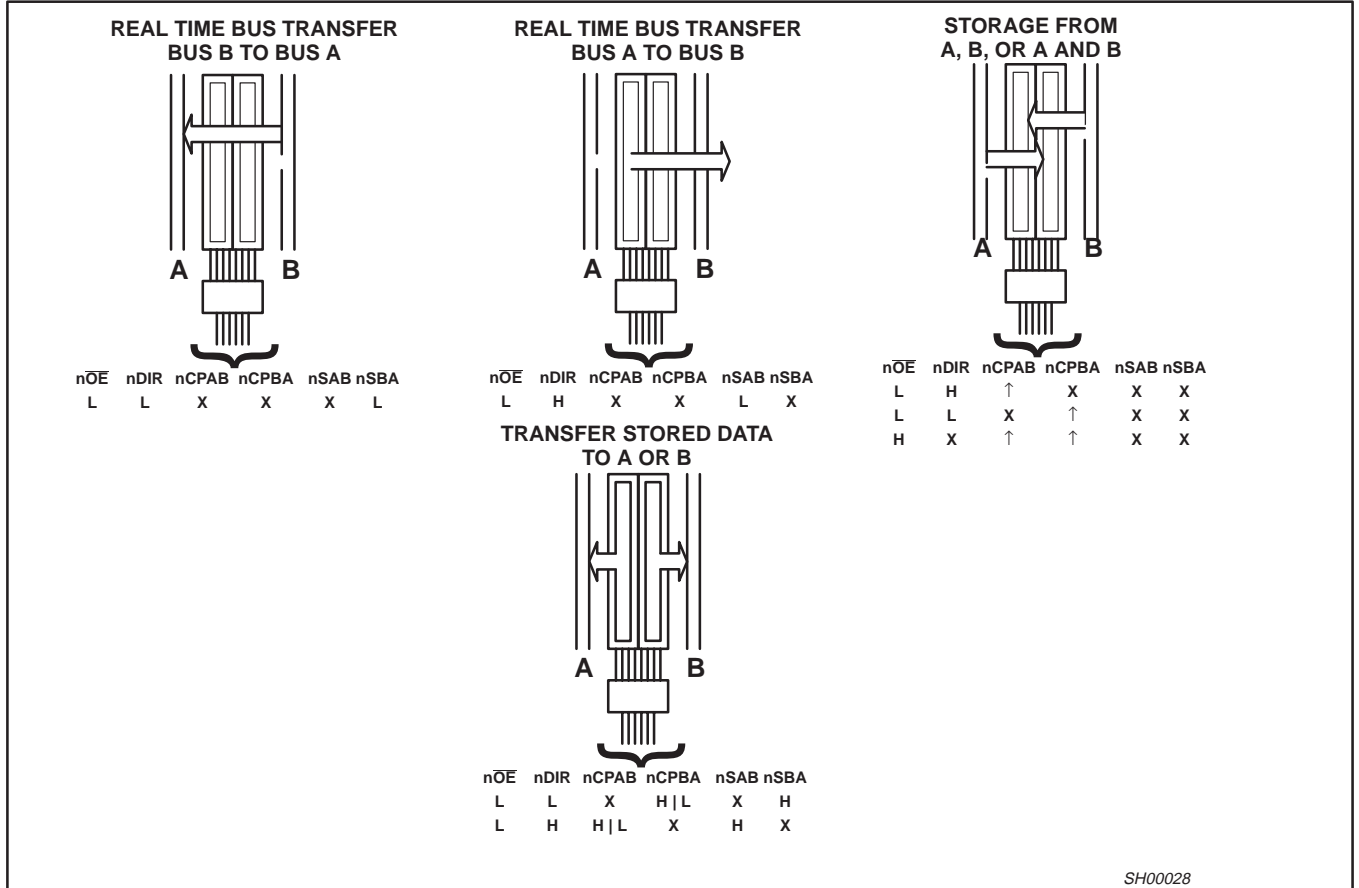


Load circuitry for switching times

16-bit bus transceiver/register (3-State)

74ALVCH16646

APPLICATION INFORMATION

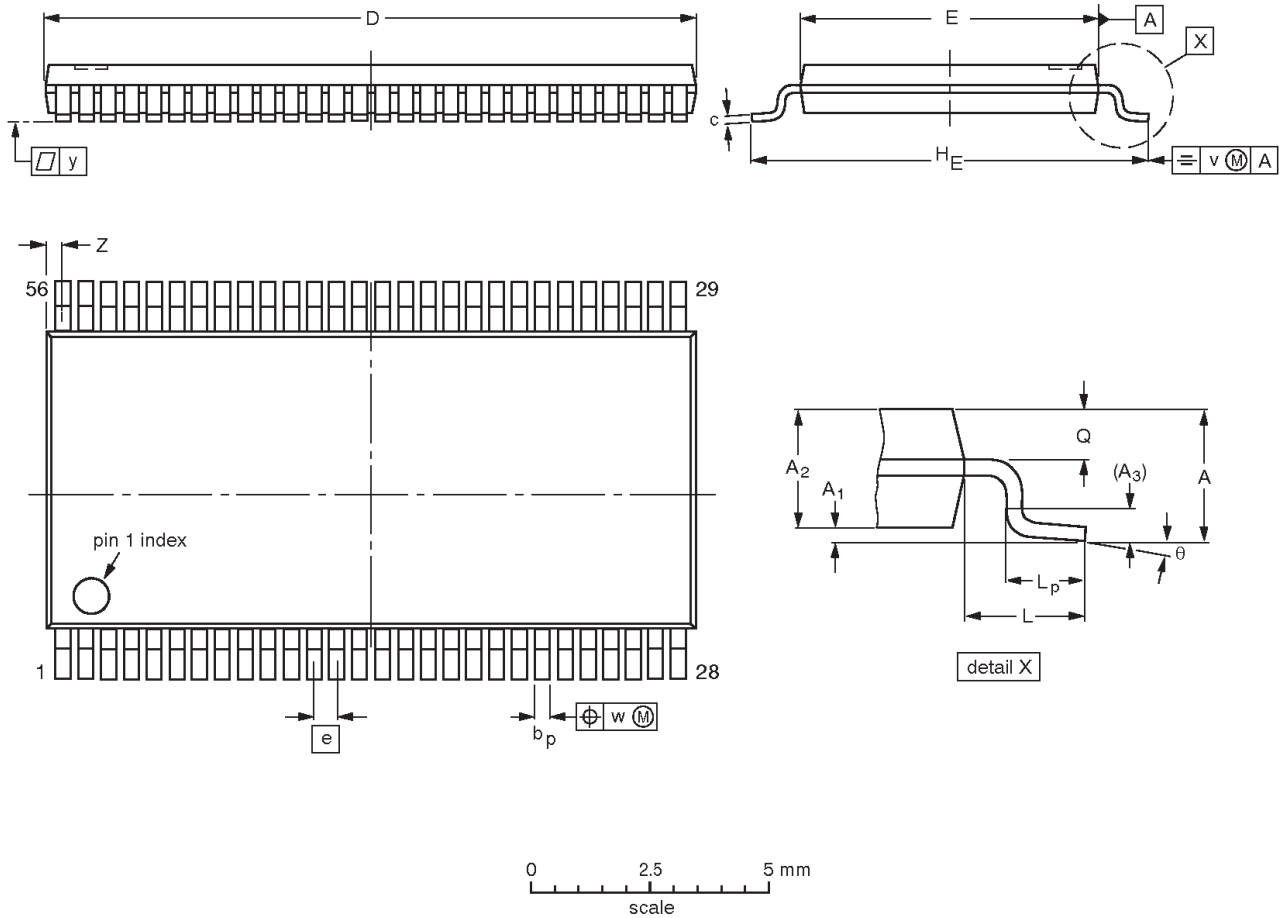


16-bit bus transceiver/register (3-State)

74ALVCH16646

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT364-1		MO-153EE				93-02-03 95-02-10

16-bit bus transceiver/register (3-State)

74ALVCH16646

NOTES

16-bit bus transceiver/register (3-State)

74ALVCH16646

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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