

74LVC74A-Q100

Dual D-type flip-flop with set and reset; positive-edge trigger

Rev. 3 — 18 June 2020

Product data sheet

1. General description

The 74LVC74A-Q100 is a dual edge triggered D-type flip-flop with individual data (nD) inputs, clock (nCP) inputs, set (nSD) and (nRD) inputs, and complementary nQ and nQ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the nQ output on the LOW-to-HIGH transition of the clock pulse. The nD inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation.

Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- 5 V tolerant inputs for interlacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-----------------|-------------------|---------|---|----------|
| | Temperature range | Name | Description | Version |
| 74LVC74AD-Q100 | -40 °C to +125 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74LVC74APW-Q100 | -40 °C to +125 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |

Dual D-type flip-flop with set and reset; positive-edge trigger

| Type number | Package | | | Version |
|-----------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | |
| 74LVC74ABQ-Q100 | -40 °C to +125 °C | DHVQFN14 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm | SOT762-1 |

4. Functional diagram

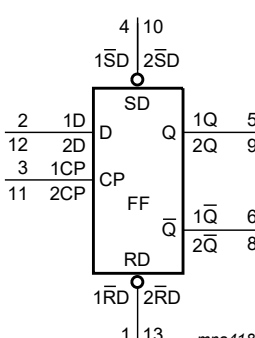


Fig. 1. Logic symbol

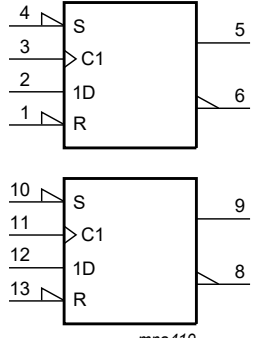


Fig. 2. IEC logic symbol

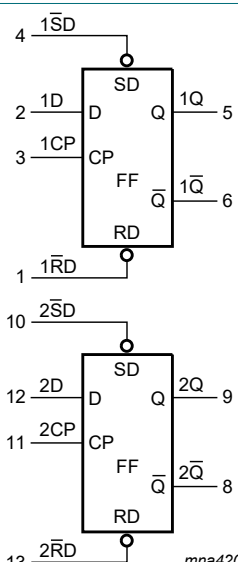
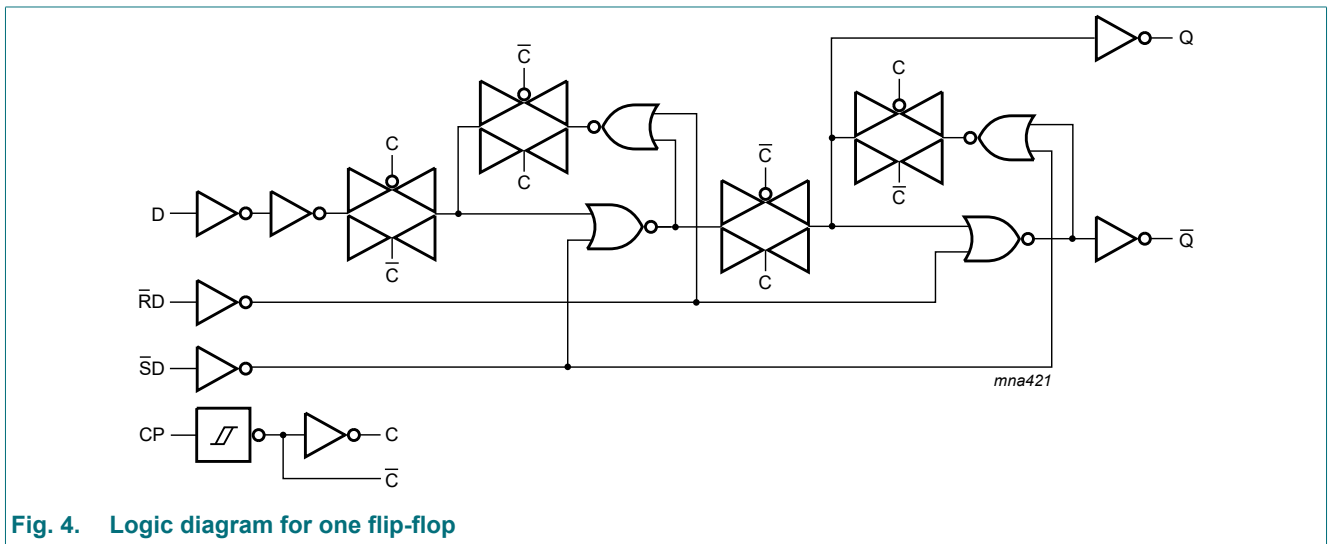
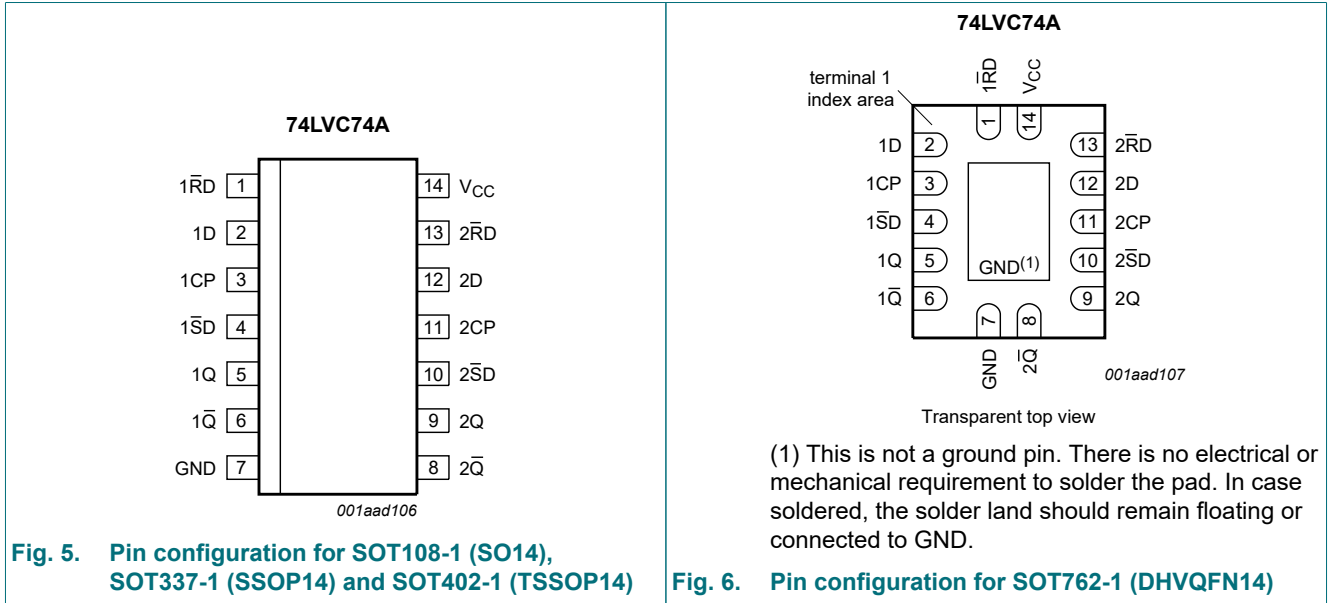


Fig. 3. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|-----|--|
| 1RD | 1 | asynchronous reset-direct input (active LOW) |
| 1D | 2 | data input |
| 1CP | 3 | clock input (LOW-to-HIGH, edge-triggered) |
| 1SD | 4 | asynchronous set-direct input (active LOW) |
| 1Q | 5 | true output |
| 1Q̄ | 6 | complement output |
| GND | 7 | ground (0 V) |
| 2Q̄ | 8 | complement output |
| 2Q | 9 | true output |
| 2SD | 10 | asynchronous set-direct input (active LOW) |
| 2CP | 11 | clock input (LOW-to-HIGH, edge-triggered) |
| 2D | 12 | data input |
| 2RD | 13 | asynchronous reset-direct input (active LOW) |
| V _{CC} | 14 | supply voltage |

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care

| Input | | | | Output | |
|-------|-----|-----|----|--------|-----|
| nSD | nRD | nCP | nD | nQ | nQ̄ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H | H |

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level;

↑ = LOW-to-HIGH transition; Q_{n+1} = state after the next LOW-to-HIGH CP transition

| Input | | | | Output | |
|-------|-----|-----|----|-------------------|--------------------|
| nSD | nRD | nCP | nD | nQ _{n+1} | nQ̄ _{n+1} |
| H | H | ↑ | L | L | H |
| H | H | ↑ | H | H | L |

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|-------------------------------|------|----------------|------|
| V_{CC} | supply voltage | | -0.5 | +6.5 | V |
| I_{IK} | input clamping current | $V_I < 0$ V | -50 | - | mA |
| V_I | input voltage | | -0.5 | +6.5 | V |
| I_{OK} | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V | - | ±50 | mA |
| V_O | output voltage | | -0.5 | $V_{CC} + 0.5$ | V |
| I_O | output current | $V_O = 0$ V to V_{CC} | - | ±50 | mA |
| I_{CC} | supply current | | - | 100 | mA |
| I_{GND} | ground current | | -100 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40$ °C to +125 °C | - | 500 | mW |

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
 For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
 For SOT762-1 (DHFQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 6. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|-------------------------------------|-----------------------------------|------|-----|-----------------|------|
| V _{CC} | supply voltage | for maximum speed performance | 1.65 | - | 3.6 | V |
| | | for low-voltage applications | 1.2 | - | 3.6 | V |
| V _I | input voltage | | 0 | - | 5.5 | V |
| V _O | output voltage | | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | - | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 1.65 V to 2.7 V | 0 | - | 20 | ns/V |
| | | V _{CC} = 2.7 V to 3.6 V | 0 | - | 10 | ns/V |

9. Static characteristics

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|-----------------|---------------------------|--|-----------------------|--------|----------------------|-----------------------|----------------------|------|
| | | | Min | Typ[1] | Max | Min | Max | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 1.2 V | 1.08 | - | - | 1.08 | - | V |
| | | V _{CC} = 1.65 V to 1.95 V | 0.65xV _{CC} | - | - | 0.65xV _{CC} | - | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | - | - | 1.7 | - | V |
| | | V _{CC} = 2.7 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 1.2 V | - | - | 0.12 | - | 0.12 | V |
| | | V _{CC} = 1.65 V to 1.95 V | - | - | 0.35xV _{CC} | - | 0.35xV _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | - | - | 0.7 | - | 0.7 | V |
| | | V _{CC} = 2.7 V to 3.6 V | - | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | |
| | | I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V | V _{CC} - 0.2 | - | - | V _{CC} - 0.3 | - | V |
| | | I _O = -4 mA; V _{CC} = 1.65 V | 1.2 | - | - | 1.05 | - | V |
| | | I _O = -8 mA; V _{CC} = 2.3 V | 1.8 | - | - | 1.65 | - | V |
| | | I _O = -12 mA; V _{CC} = 2.7 V | 2.2 | - | - | 2.05 | - | V |
| | | I _O = -18 mA; V _{CC} = 3.0 V | 2.4 | - | - | 2.25 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | |
| | | I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V | - | - | 0.2 | - | 0.3 | V |
| | | I _O = 4 mA; V _{CC} = 1.65 V | - | - | 0.45 | - | 0.65 | V |
| | | I _O = 8 mA; V _{CC} = 2.3 V | - | - | 0.6 | - | 0.8 | V |
| | | I _O = 12 mA; V _{CC} = 2.7 V | - | - | 0.4 | - | 0.6 | V |
| I _I | input leakage current | V _{CC} = 3.6 V; V _I = 5.5 V or GND | - | ±0.1 | ±5 | - | ±20 | μA |
| | | V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A | - | 0.1 | 10 | - | 40 | μA |

Dual D-type flip-flop with set and reset; positive-edge trigger

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|-----------------|---------------------------|--|------------------|--------|-----|-------------------|------|---------------|
| | | | Min | Typ[1] | Max | Min | Max | |
| ΔI_{CC} | additional supply current | per input pin; $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V};$ $V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}$ | - | 5 | 500 | - | 5000 | μA |
| C_i | input capacitance | $V_{CC} = 0 \text{ V to } 3.6 \text{ V};$ $V_I = \text{GND to } V_{CC}$ | - | 4.0 | - | - | - | pF |

[1] All typical values are measured at $V_{CC} = 3.3 \text{ V}$ (unless stated otherwise) and $T_{amb} = 25 \text{ °C}$.

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 9.

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|--|-------------------|--|------------------|--------|------|-------------------|------|------|
| | | | Min | Typ[1] | Max | Min | Max | |
| t_{pd} | propagation delay | nCP to nQ, n \bar{Q} ; see Fig. 7 [2] | | | | | | |
| | | $V_{CC} = 1.2 \text{ V}$ | - | 15 | - | - | - | ns |
| | | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | 1.0 | 5.0 | 10.3 | 1.0 | 11.9 | ns |
| | | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 1.8 | 2.9 | 5.8 | 1.8 | 6.7 | ns |
| | | $V_{CC} = 2.7 \text{ V}$ | 1.0 | 2.7 | 6.0 | 1.0 | 7.5 | ns |
| | | $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ | 1.0 | 2.6 | 5.2 | 1.0 | 6.5 | ns |
| | | nSD to nQ, n \bar{Q} ; see Fig. 8 | | | | | | |
| | | $V_{CC} = 1.2 \text{ V}$ | - | 15 | - | - | - | ns |
| | | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | 0.5 | 4.0 | 10.6 | 0.5 | 12.2 | ns |
| | | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 1.0 | 2.4 | 6.1 | 1.0 | 7.1 | ns |
| | | $V_{CC} = 2.7 \text{ V}$ | 1.0 | 2.9 | 6.4 | 1.0 | 8.0 | ns |
| | | $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ | 1.0 | 2.2 | 5.4 | 1.0 | 7.0 | ns |
| | | nRD to nQ, n \bar{Q} ; see Fig. 8 | | | | | | |
| | | $V_{CC} = 1.2 \text{ V}$ | - | 15 | - | - | - | ns |
| | | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | 0.5 | 4.1 | 10.7 | 0.5 | 12.4 | ns |
| | | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 1.0 | 2.4 | 6.1 | 1.0 | 7.1 | ns |
| $V_{CC} = 2.7 \text{ V}$ | 1.0 | 3.0 | 6.4 | 1.0 | 8.0 | ns | | |
| $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ | 1.0 | 2.2 | 5.4 | 1.0 | 7.0 | ns | | |
| t_w | pulse width | clock HIGH or LOW; see Fig. 7 | | | | | | |
| | | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | 5.0 | - | - | 5.0 | - | ns |
| | | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 4.0 | - | - | 4.0 | - | ns |
| | | $V_{CC} = 2.7 \text{ V}$ | 3.3 | - | - | 4.5 | - | ns |
| | | $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ | 3.3 | 1.3 | - | 4.5 | - | ns |
| | | set or reset LOW; see Fig. 8 | | | | | | |
| | | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | 5.0 | - | - | 5.0 | - | ns |
| | | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 4.0 | - | - | 4.0 | - | ns |
| | | $V_{CC} = 2.7 \text{ V}$ | 3.3 | - | - | 4.5 | - | ns |
| | | $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ | 3.3 | 1.7 | - | 4.5 | - | ns |

Dual D-type flip-flop with set and reset; positive-edge trigger

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|--------------------|-------------------------------|--|------------------|--------|-----|-------------------|-----|------|
| | | | Min | Typ[1] | Max | Min | Max | |
| t _{rec} | recovery time | set or reset; see Fig. 8 | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 1.5 | - | - | 1.5 | - | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.5 | - | - | 1.5 | - | ns |
| | | V _{CC} = 2.7 V | 1.5 | - | - | 1.0 | - | ns |
| t _{su} | set-up time | nD to nCP; see Fig. 7 | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 3.0 | - | - | 3.0 | - | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 2.5 | - | - | 2.5 | - | ns |
| | | V _{CC} = 2.7 V | 2.2 | - | - | 2.2 | - | ns |
| t _h | hold time | nD to nCP; see Fig. 7 | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 2.0 | - | - | 2.0 | - | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.5 | - | - | 1.5 | - | ns |
| | | V _{CC} = 2.7 V | 1.0 | - | - | 1.0 | - | ns |
| f _{max} | maximum frequency | V _{CC} = 3.0 V to 3.6 V | +1.0 | -3.0 | - | 1.0 | - | ns |
| | | nCP; see Fig. 7 | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 100 | - | - | 80 | - | MHz |
| | | V _{CC} = 2.3 V to 2.7 V | 125 | - | - | 100 | - | MHz |
| t _{sk(o)} | output skew time | V _{CC} = 2.7 V | 150 | - | - | 120 | - | MHz |
| | | V _{CC} = 3.0 V to 3.6 V | 150 | 250 | - | 120 | - | MHz |
| | | V _{CC} = 3.0 V to 3.6 V | - | - | 1.0 | - | 1.5 | ns |
| | | [3] | | | | | | |
| C _{PD} | power dissipation capacitance | per flip-flop; V _I = GND to V _{CC} | [4] | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | - | 12.4 | - | - | - | pF |
| | | V _{CC} = 2.3 V to 2.7 V | - | 16.0 | - | - | - | pF |
| | | V _{CC} = 3.0 V to 3.6 V | - | 19.1 | - | - | - | pF |

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz; f_o = output frequency in MHz

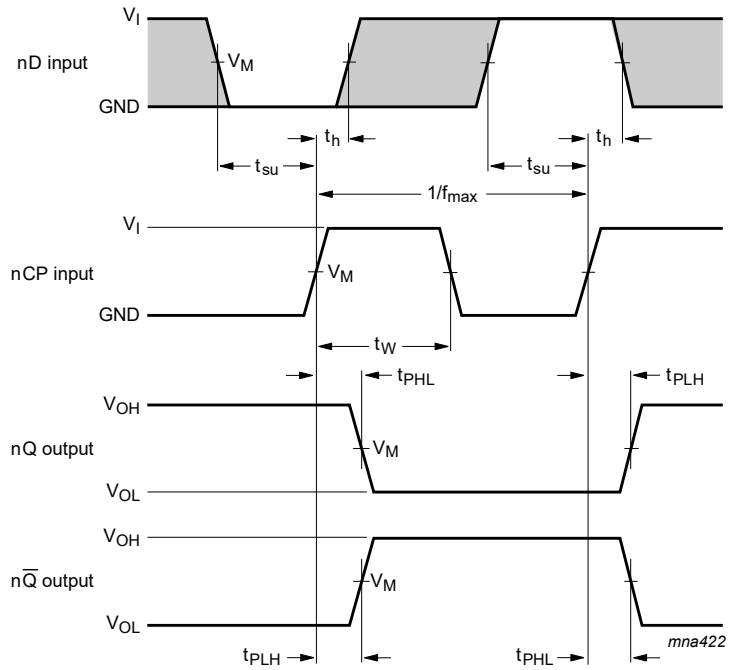
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

Σ(C_L × V_{CC}² × f_o) = sum of the outputs

10.1. Waveforms and test circuit



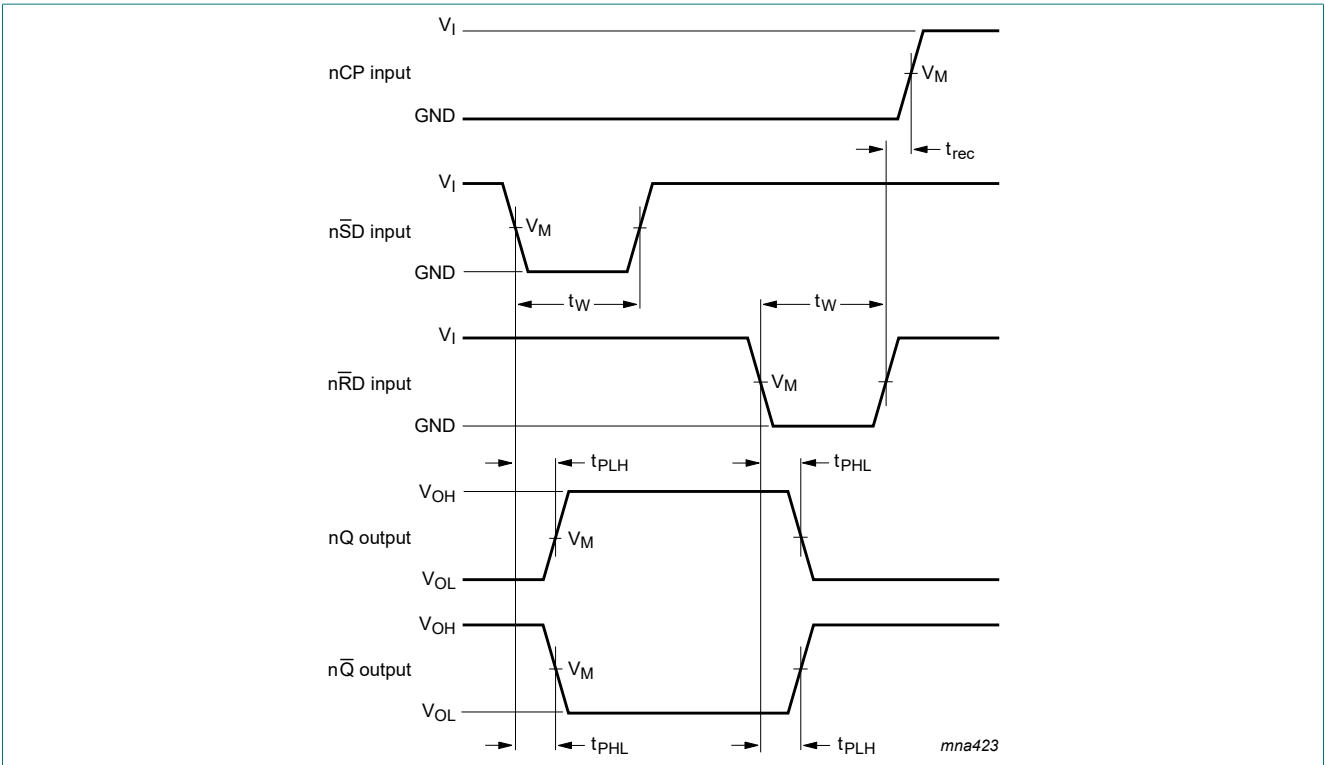
The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in [Table 9](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. The clock input (nCP) to output (nQ, nQ-bar) propagation delays, the clock pulse width, the nD to nCP set-up, the nCP to nD hold times, and the maximum frequency

Dual D-type flip-flop with set and reset; positive-edge trigger



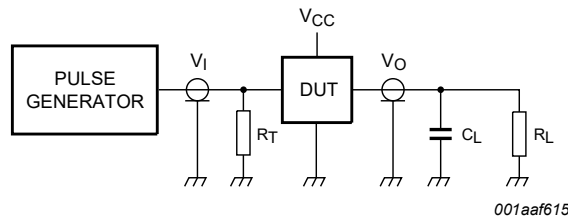
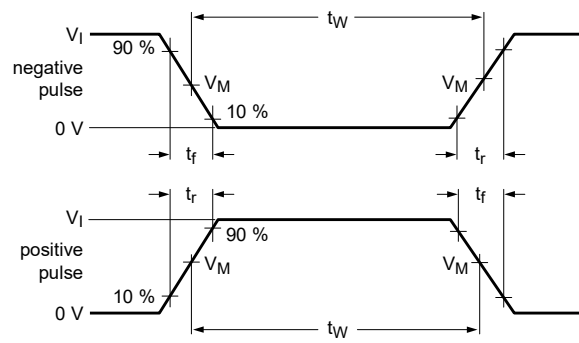
Measurement points are given in [Table 9](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 8. The set ($n\overline{SD}$) and reset ($n\overline{RD}$) input to output (nQ , $n\overline{Q}$) propagation delays, the set and reset pulse widths, and the $n\overline{RD}$ to nCP recovery time

Table 9. Measurement points

| Supply voltage | Input | | Output |
|------------------|----------|---------------------|---------------------|
| V_{CC} | V_I | V_M | V_M |
| 1.2 V | V_{CC} | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |
| 1.65 V to 1.95 V | V_{CC} | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |
| 2.3 V to 2.7 V | V_{CC} | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |
| 2.7 V | 2.7 V | 1.5 V | 1.5 V |
| 3.0 V to 3.6 V | 2.7 V | 1.5 V | 1.5 V |

Dual D-type flip-flop with set and reset; positive-edge trigger



001aaf615

Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig. 9. Test circuit for measuring switching times

Table 10. Test data

| Supply voltage | Input | | Load | |
|------------------|----------|---------------|-------|--------------|
| V_{CC} | V_I | t_r, t_f | C_L | R_L |
| 1.2 V | V_{CC} | ≤ 2 ns | 30 pF | 1 k Ω |
| 1.65 V to 1.95 V | V_{CC} | ≤ 2 ns | 30 pF | 1 k Ω |
| 2.3 V to 2.7 V | V_{CC} | ≤ 2 ns | 30 pF | 500 Ω |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω |

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

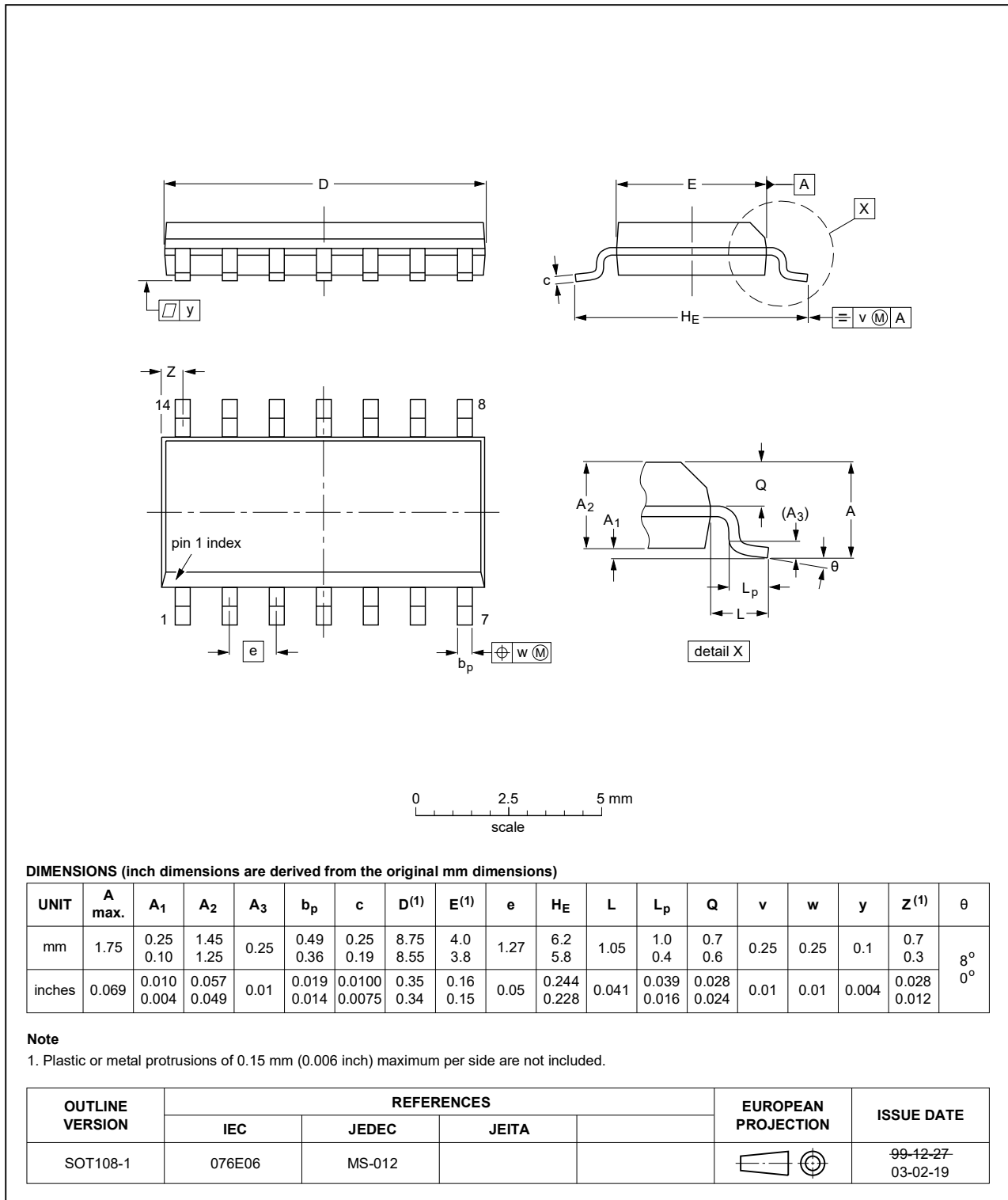


Fig. 10. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

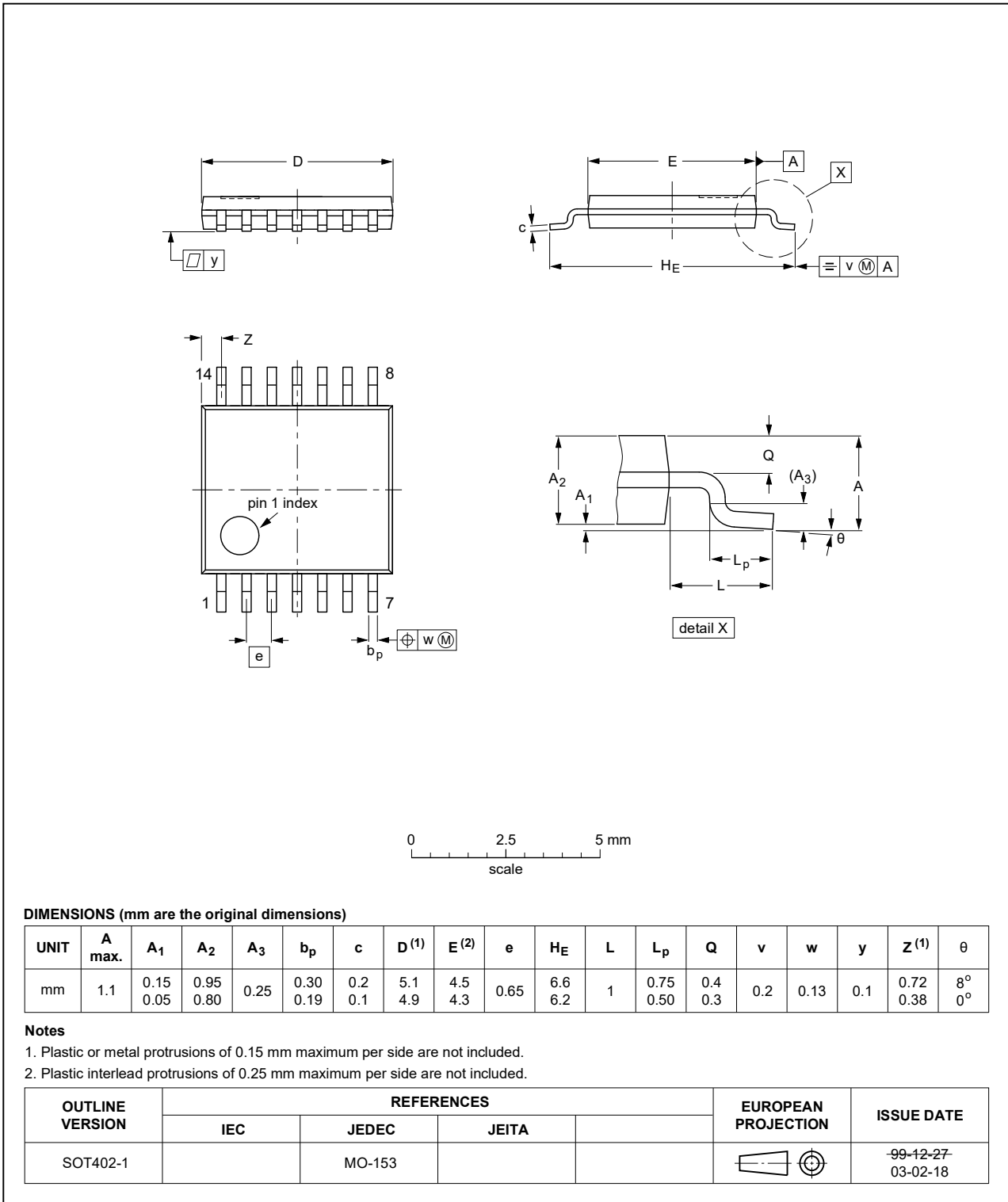


Fig. 11. Package outline SOT402-1 (TSSOP14)

Dual D-type flip-flop with set and reset; positive-edge trigger

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

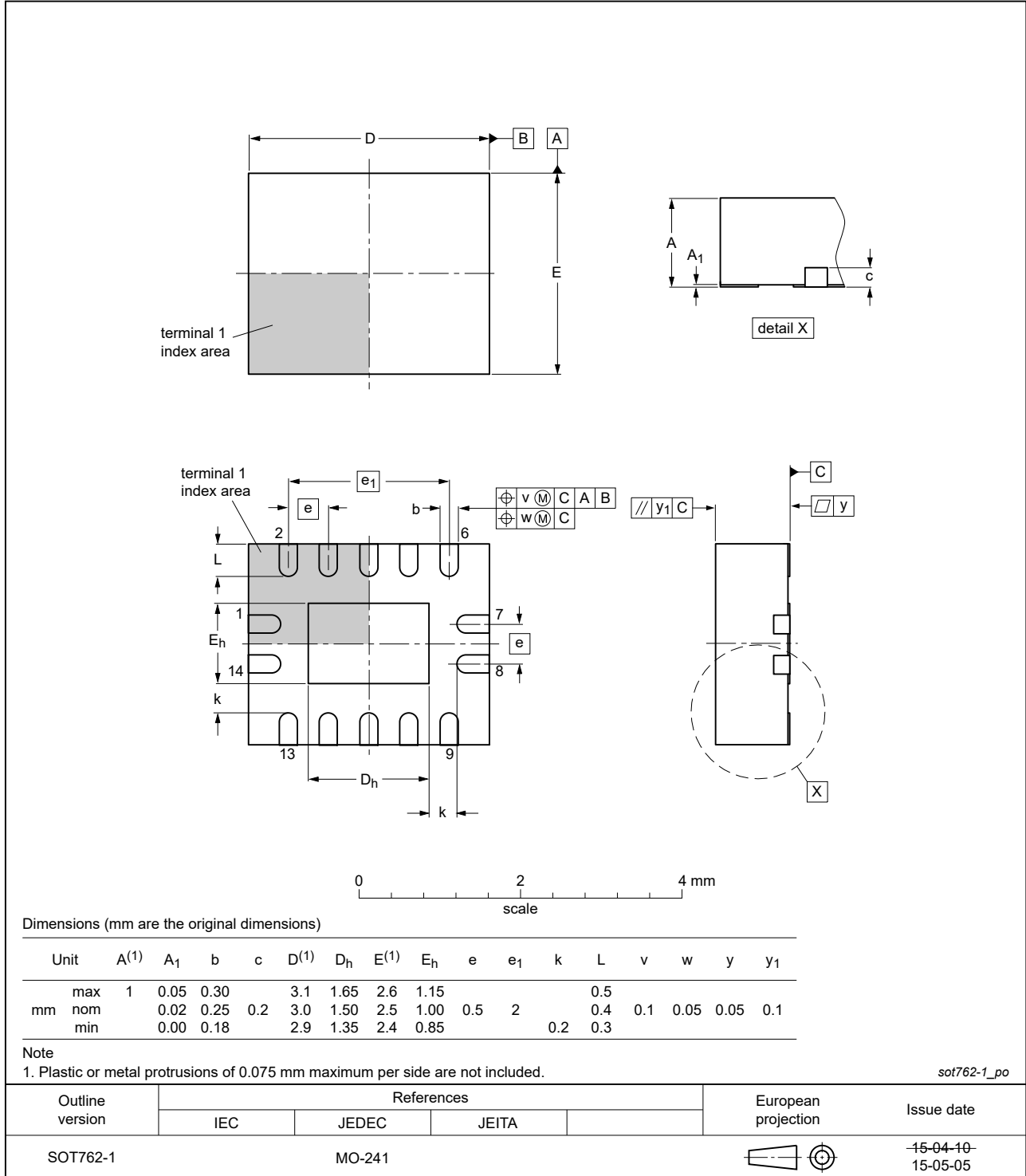


Fig. 12. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 11. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MIL | Military |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 12. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------------|---|--------------------|---------------|-------------------|
| 74LVC74A_Q100 v.3 | 20200618 | Product data sheet | - | 74LVC74A_Q100 v.2 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 1 and Section 2 updated. Table 5: Derating values for P_{tot} total power dissipation have been updated. Table 10 corrected (errata). Package outline drawing of SOT762-1 (Fig. 12) updated. | | | |
| 74LVC74A_Q100 v.2 | 20130405 | Product data sheet | - | 74LVC74A_Q100 v.1 |
| Modifications: | <ul style="list-style-type: none"> #unique_17: removed redundant temperature range. | | | |
| 74LVC74A_Q100 v.1 | 20130326 | Product data sheet | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
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