![ANALOG DEVICES]

Dual, 16 MHz, Rail-to-Rail FET Input Amplifier

Data Sheet **AD823**

FEATURES

Single-supply operation
- **Output swings rail-to-rail**
- **Input voltage range extends below ground**
- **Single-supply capability from 3 V to 36 V**

High load drive
- **Capacitive load drive of 500 pF, G = +1**
- **Output current of 15 mA, 0.5 V from supplies**

Excellent ac performance on 2.6 mA/amplifier
- **−3 dB bandwidth of 16 MHz, G = +1**
- **350 ns settling time to 0.01% (2 V step)**
- **Slew rate of 22 V/µs**

Good dc performance
- **800 µV maximum input offset voltage**
- **2 µV/°C offset voltage drift**
- **25 pA maximum input bias current**

Low distortion: −108 dBc worst harmonic @ 20 kHz
Low noise: 16 nV/√Hz @ 10 kHz
No phase inversion with inputs to the supply rails

APPLICATIONS

Battery-powered precision instrumentation
Photodiode preamps
Active filters
12-bit to 16-bit data acquisition systems
Medical instrumentation

GENERAL DESCRIPTION

The AD823 is a dual precision, 16 MHz, JFET input op amp that can operate from a single supply of 3.0 V to 36 V or from dual supplies of ±1.5 V to ±18 V. It has true single-supply capability with an input voltage range extending below ground in single-supply mode. Output voltage swing extends to within 50 mV of each rail for $I_{OUT} \leq 100$ µA, providing outstanding output dynamic range.

An offset voltage of 800 µV maximum, an offset voltage drift of 2 µV/°C, input bias currents below 25 pA, and low input voltage noise provide dc precision with source impedances up to a Gigaohm. It provides 16 MHz, −3 dB bandwidth, −108 dB THD @ 20 kHz, and a 22 V/µs slew rate with a low supply current of 2.6 mA per amplifier. The AD823 drives up to 500 pF of direct capacitive load as a follower and provides an output current of 15 mA, 0.5 V from the supply rails. This allows the amplifier to handle a wide range of load conditions.

CONNECTION DIAGRAM

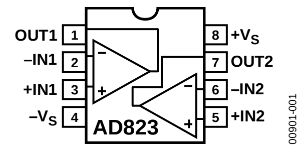

Figure 1. 8-Lead PDIP and SOIC

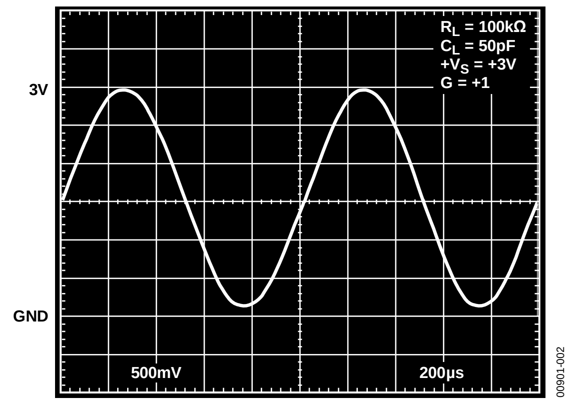

Figure 2. Output Swing, +VS = +3 V, G = +1

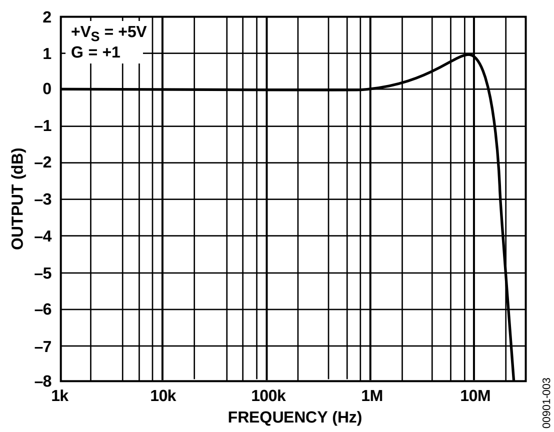

Figure 3. Small Signal Bandwidth, G = +1

This combination of ac and dc performance, plus the outstanding load drive capability, results in an exceptionally versatile amplifier for applications such as A/D drivers, high speed active filters, and other low voltage, high dynamic range systems.

The AD823 is available over the industrial temperature range of −40°C to +85°C and is offered in both 8-lead PDIP and 8-lead SOIC packages.

Rev. E

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

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5/95—Revision 0: Initial Version

SPECIFICATIONS

At T_A = 25°C, $+V_S$ = +5 V, R_L = 2 kΩ to 2.5 V, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth, V_O ≤ 0.2 V p-p	G = +1	12	16		MHz
Full Power Response	V_O = 2 V p-p		3.5		MHz
Slew Rate	G = −1, V_O = 4 V Step	14	22		V/µs
Settling Time					
to 0.1%	G = −1, V_O = 2 V Step		320		ns
to 0.01%	G = −1, V_O = 2 V Step		350		ns
NOISE/DISTORTION PERFORMANCE					
Input Voltage Noise	f = 10 kHz		16		nV/√Hz
Input Current Noise	f = 1 kHz		1		fA/√Hz
Harmonic Distortion	R_L = 600 Ω to 2.5 V, V_O = 2 V p-p, f = 20 kHz		−108		dBc
Crosstalk					
f = 1 kHz	R_L = 5 kΩ		−105		dB
f = 1 MHz	R_L = 5 kΩ		−63		dB
DC PERFORMANCE					
Initial Offset			0.2	0.8	mV
Maximum Offset Over temperature			0.3	2.0	mV
Offset Drift			2		µV/°C
Input Bias Current	V_{CM} = 0 V to 4 V		3	25	pA
at T_{MAX}	V_{CM} = 0 V to 4 V		0.5	5	nA
Input Offset Current			2	20	pA
at T_{MAX}			0.5		nA
Open-Loop Gain	V_O = 0.2 V to 4 V, R_L = 2 kΩ	20	45		V/mV
T_{MIN} to T_{MAX}		20			V/mV
INPUT CHARACTERISTICS					
Input Common-Mode Voltage Range		−0.2 to +3	−0.2 to +3.8		V
Input Resistance			10^{13}		Ω
Input Capacitance			1.8		pF
Common-Mode Rejection Ratio	V_{CM} = 0 V to 3 V	60	76		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing					
I_L = ±100 µA			0.025 to 4.975		V
I_L = ±2 mA			0.08 to 4.92		V
I_L = ±10 mA			0.25 to 4.75		V
Output Current	V_{OUT} = 0.5 V to 4.5 V		16		mA
Short-Circuit Current	Sourcing to 2.5 V		40		mA
	Sinking to 2.5 V		30		mA
Capacitive Load Drive	G = +1		500		pF
POWER SUPPLY					
Operating Range		3		36	V
Quiescent Current	T_{MIN} to T_{MAX}, total		5.2	5.6	mA
Power Supply Rejection Ratio	V_S = 5 V to 15 V, T_{MIN} to T_{MAX}	70	80		dB

At T_A = 25°C, $+V_S$ = +3.3 V, R_L = 2 kΩ to 1.65 V, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth, V_O ≤ 0.2 V p-p	G = +1	12	15		MHz
Full Power Response	V_O = 2 V p-p		3.2		MHz
Slew Rate	G = −1, V_O = 2 V Step	13	20		V/µs
Settling Time					
to 0.1%	G = −1, V_O = 2 V Step		250		ns
to 0.01%	G = −1, V_O = 2 V Step		300		ns
NOISE/DISTORTION PERFORMANCE					
Input Voltage Noise	f = 10 kHz		16		nV/√Hz
Input Current Noise	f = 1 kHz		1		fA/√Hz
Harmonic Distortion	R_L = 100 Ω, V_O = 2 V p-p, f = 20 kHz		−93		dBc
Crosstalk					
f = 1 kHz	R_L = 5 kΩ		−105		dB
f = 1 MHz	R_L = 5 kΩ		−63		dB
DC PERFORMANCE					
Initial Offset			0.2	1.5	mV
Maximum Offset Over temperature			0.5	2.5	mV
Offset Drift			2		µV/°C
Input Bias Current	V_{CM} = 0 V to 2 V		3	25	pA
at T_{MAX}	V_{CM} = 0 V to 2 V		0.5	5	nA
Input Offset Current			2	20	pA
at T_{MAX}			0.5		nA
Open-Loop Gain	V_O = 0.2 V to 2 V, R_L = 2 kΩ	15	30		V/mV
T_{MIN} to T_{MAX}		12			V/mV
INPUT CHARACTERISTICS					
Input Common-Mode Voltage Range		−0.2 to +1	−0.2 to +1.8		V
Input Resistance			10^{13}		Ω
Input Capacitance			1.8		pF
Common-Mode Rejection Ratio	V_{CM} = 0 V to 1 V	54	70		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing					
I_L = ±100 µA			0.025 to 3.275		V
I_L = ±2 mA			0.08 to 3.22		V
I_L = ±10 mA			0.25 to 3.05		V
Output Current	V_{OUT} = 0.5 V to 2.5 V		15		mA
Short-Circuit Current	Sourcing to 1.5 V		40		mA
	Sinking to 1.5 V		30		mA
Capacitive Load Drive	G = +1		500		pF
POWER SUPPLY					
Operating Range		3		36	V
Quiescent Current	T_{MIN} to T_{MAX}, total		5.0	5.7	mA
Power Supply Rejection Ratio	V_S = 3.3 V to 15 V, T_{MIN} to T_{MAX}	70	80		dB

At T_A = 25°C, V_S = ±15 V, R_L = 2 kΩ to 0 V, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth, V_O ≤ 0.2 V p-p	G = +1	12	16		MHz
Full Power Response	V_O = 2 V p-p		4		MHz
Slew Rate	G = −1, V_O = 10 V Step	17	25		V/μs
Settling Time					
to 0.1%	G = −1, V_O = 10 V Step		550		ns
to 0.01%	G = −1, V_O = 10 V Step		650		ns
NOISE/DISTORTION PERFORMANCE					
Input Voltage Noise	f = 10 kHz		16		nV/√Hz
Input Current Noise	f = 1 kHz		1		fA/√Hz
Harmonic Distortion	R_L = 600 Ω, V_O = 10 V p-p, f = 20 kHz		−90		dBc
Crosstalk					
f = 1 kHz	R_L= 5 kΩ		−105		dB
f = 1 MHz	R_L= 5 kΩ		−63		dB
DC PERFORMANCE					
Initial Offset			0.7	3.5	mV
Maximum Offset Over temperature			1.0	7	mV
Offset Drift			2		μV/°C
Input Bias Current	V_{CM} = 0 V		5	30	pA
	V_{CM} = −10 V		60		pA
at T_{MAX}	V_{CM} = 0 V		0.5	5	nA
Input Offset Current			2	20	pA
at T_{MAX}			0.5		nA
Open-Loop Gain	V_O = +10 V to −10 V, R_L = 2 kΩ	30	60		V/mV
T_{MIN} to T_{MAX}		30			V/mV
INPUT CHARACTERISTICS					
Input Common-Mode Voltage Range		−15.2 to +13	−15.2 to +13.8		V
Input Resistance			10^{13}		Ω
Input Capacitance			1.8		pF
Common-Mode Rejection Ratio	V_{CM} = −15 V to +13 V	66	82		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing					
I_L = ±100 μA			−14.95 to +14.95		V
I_L = ±2 mA			−14.92 to +14.92		V
I_L = ±10 mA			−14.75 to +14.75		V
Output Current	V_{OUT} = −14.5 V to +14.5 V		17		mA
Short-Circuit Current	Sourcing to 0 V		80		mA
	Sinking to 0 V		60		mA
Capacitive Load Drive	G = +1		500		pF
POWER SUPPLY					
Operating Range		3		36	V
Quiescent Current	T_{MIN} to T_{MAX}, total		7.0	8.4	mA
Power Supply Rejection Ratio	V_S = 5 V to 15 V, T_{MIN} to T_{MAX}	70	80		dB

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	36 V
Internal Power Dissipation	
PDIP (N)	1.3 W
SOIC (R)	0.9 W
Input Voltage (Common Mode)	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Output Short-Circuit Duration	See Figure 4
Storage Temperature Range N, R	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature Range (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Specification is for device in free air.

Table 5. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead PDIP	90	°C/W
8-Lead SOIC	160	°C/W

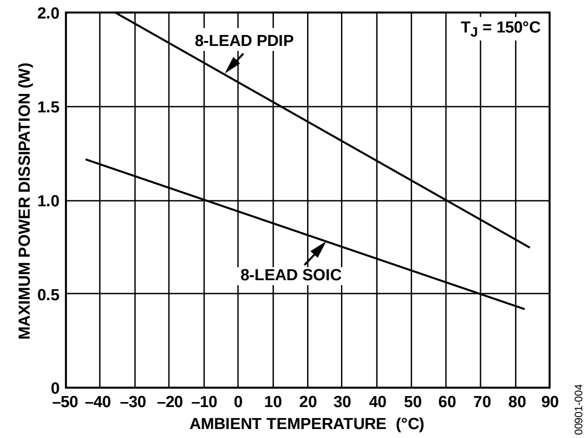
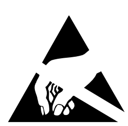


Figure 4. Maximum Power Dissipation vs. Temperature

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

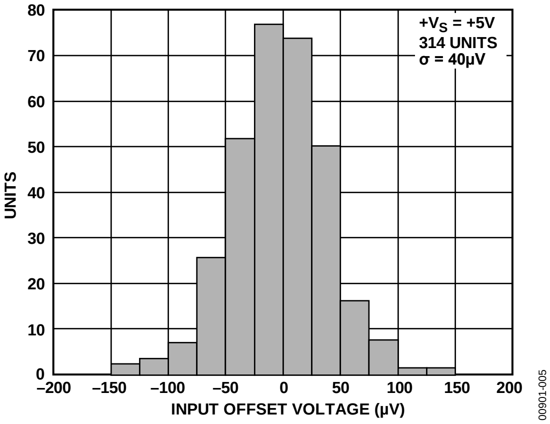


Figure 5. Typical Distribution of Input Offset Voltage

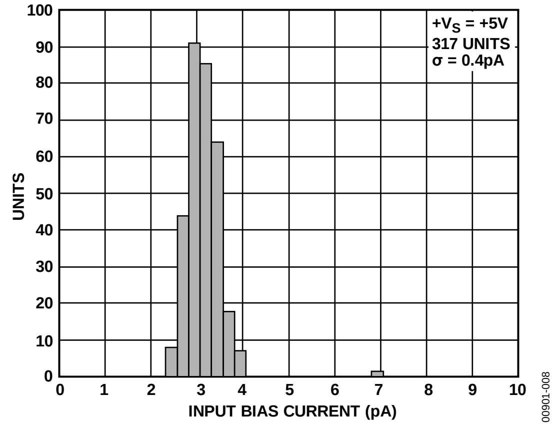


Figure 8. Typical Distribution of Input Bias Current

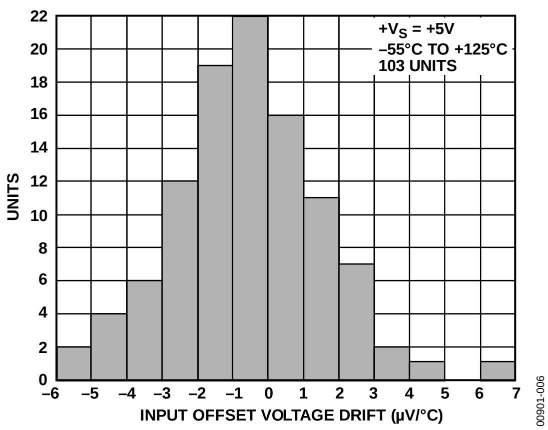


Figure 6. Typical Distribution of Input Offset Voltage Drift

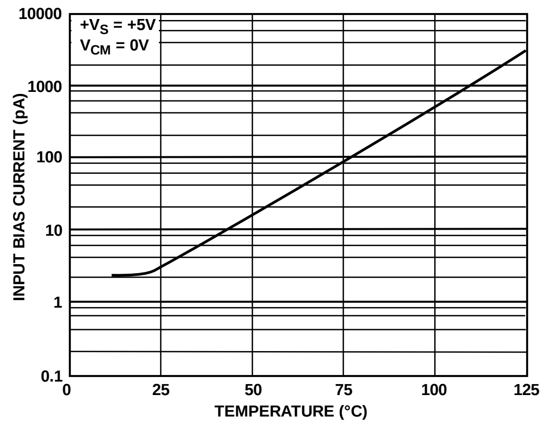


Figure 9. Input Bias Current vs. Temperature

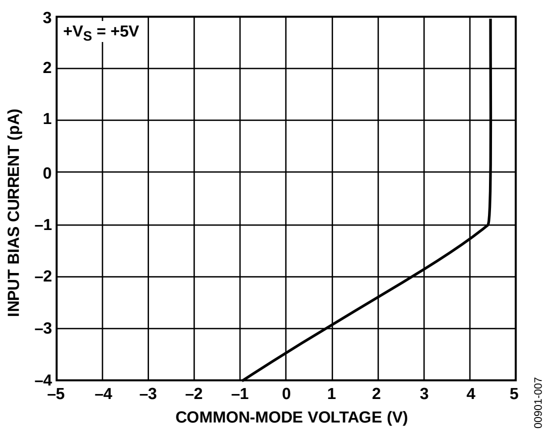


Figure 7. Input Bias Current vs. Common-Mode Voltage

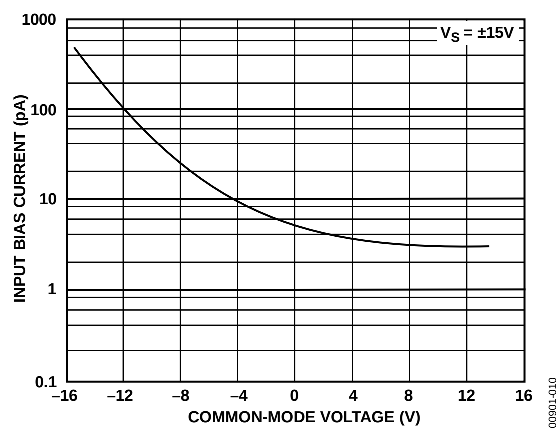


Figure 10. Input Bias Current vs. Common-Mode Voltage

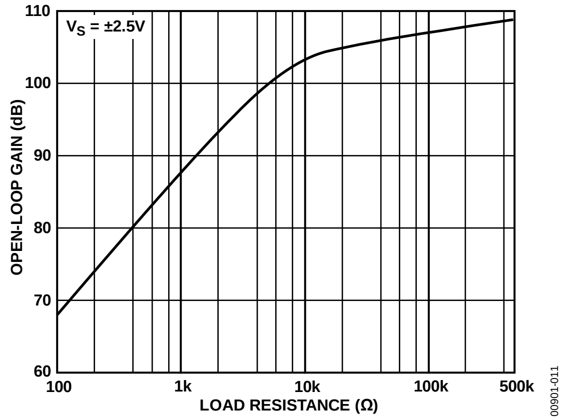


Figure 11. Open-Loop Gain vs. Load Resistance

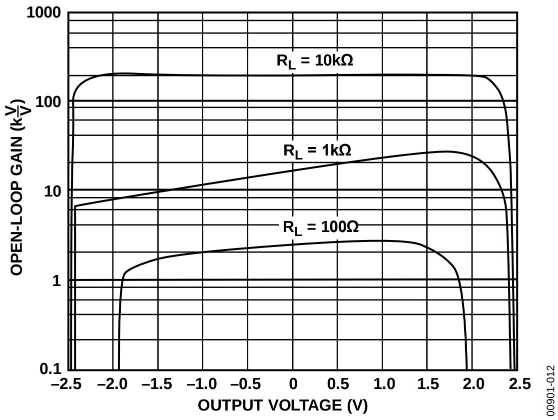


Figure 12. Open-Loop Gain vs. Output Voltage, $V_S = \pm 2.5$ V

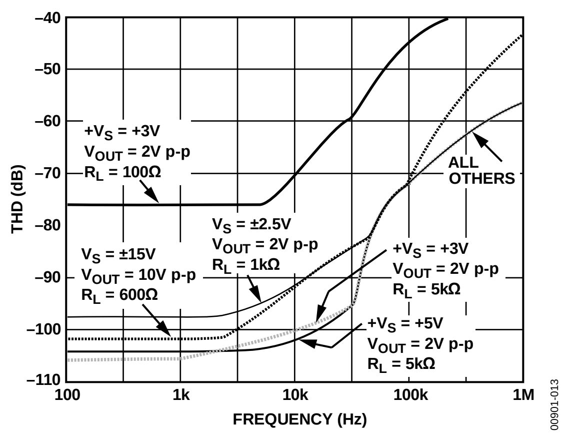


Figure 13. Total Harmonic Distortion vs. Frequency

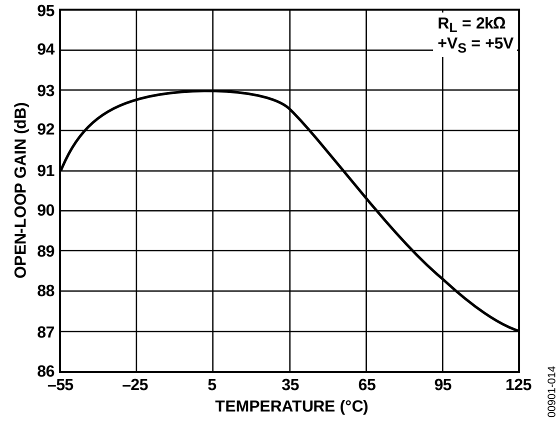


Figure 14. Open-Loop Gain vs. Temperature

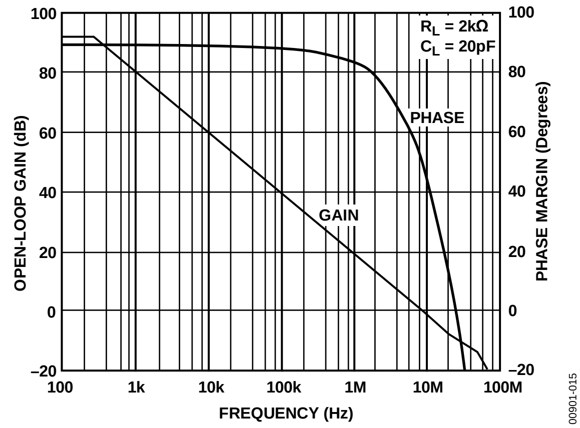


Figure 15. Open-Loop Gain and Phase Margin vs. Frequency

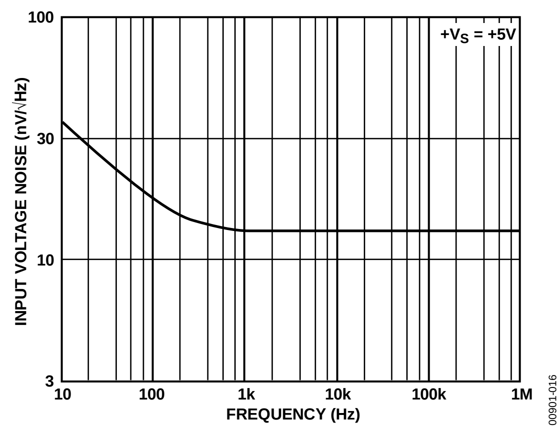


Figure 16. Input Voltage Noise vs. Frequency

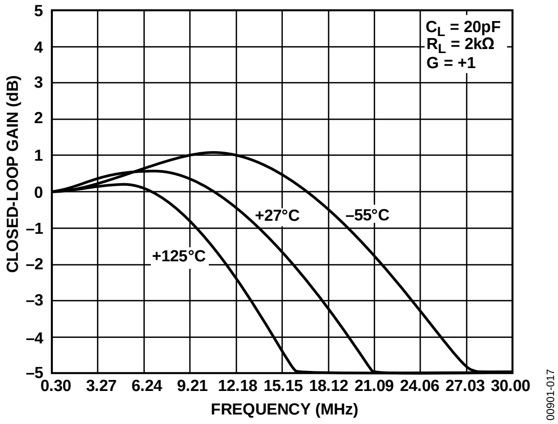


Figure 17. Closed-Loop Gain vs. Frequency

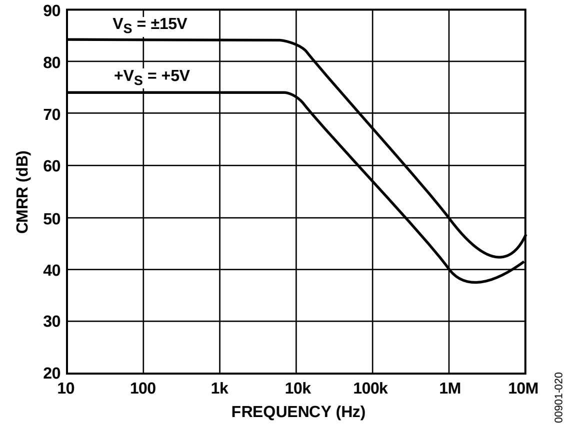


Figure 20. Common-Mode Rejection Ratio vs. Frequency

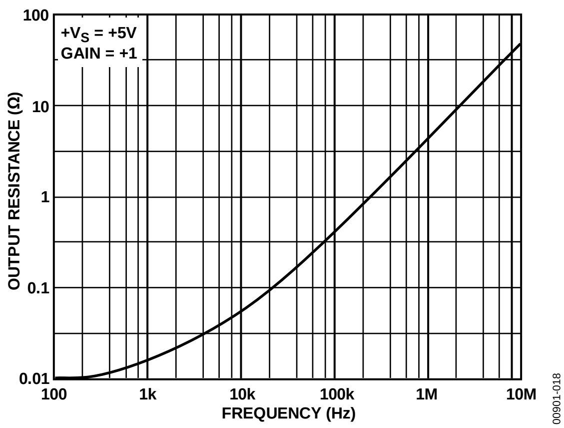


Figure 18. Output Resistance vs. Frequency, $+V_S = +5$ V, Gain = +1

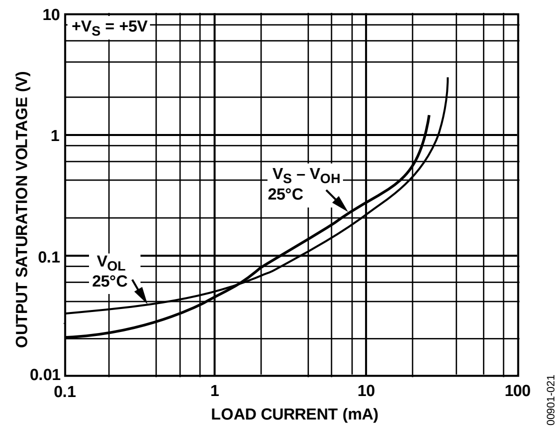


Figure 21. Output Saturation Voltage vs. Load Current

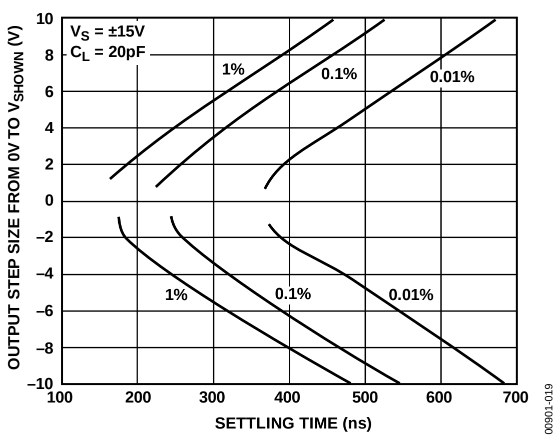


Figure 19. Output Step Size vs. Settling Time (Inverter)

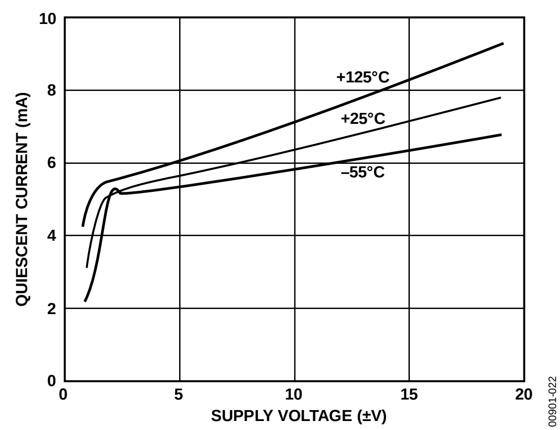


Figure 22. Quiescent Current vs. Supply Voltage

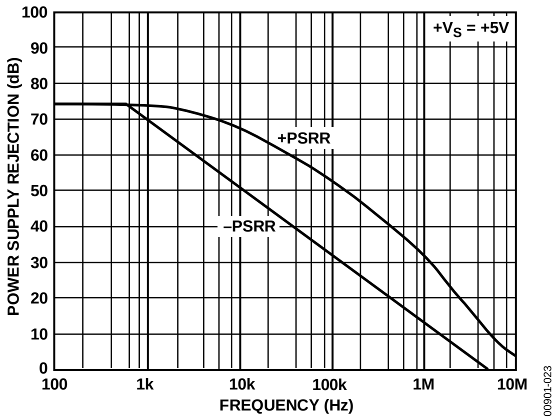


Figure 23. Power Supply Rejection vs. Frequency

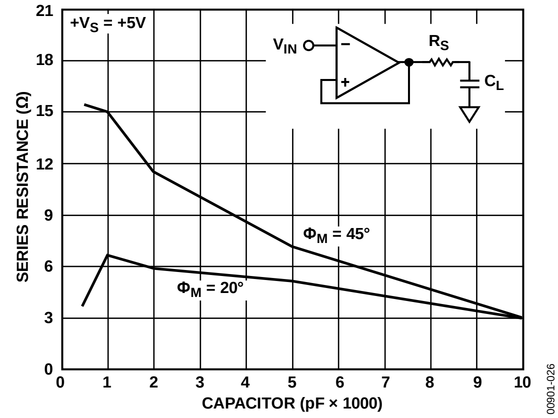


Figure 26. Series Resistance vs. Capacitive Load

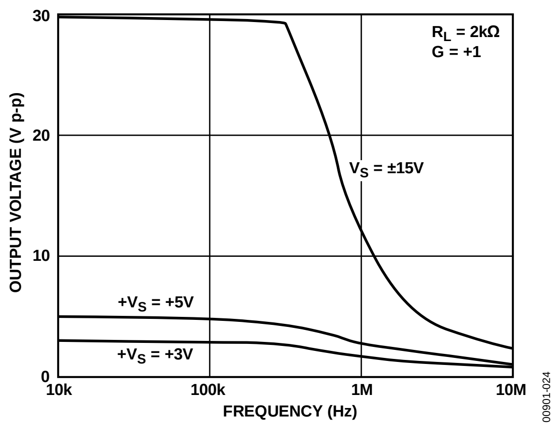


Figure 24. Large Signal Frequency Response

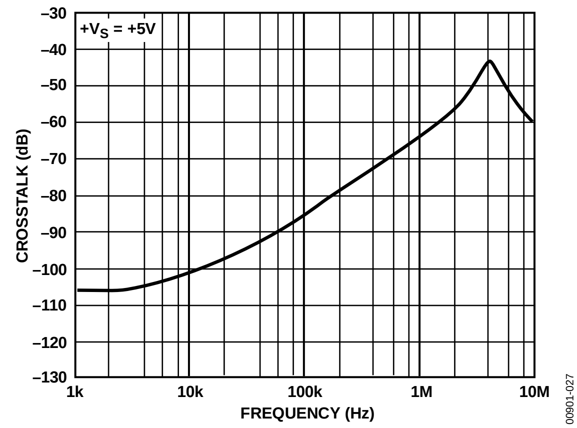


Figure 27. Crosstalk vs. Frequency

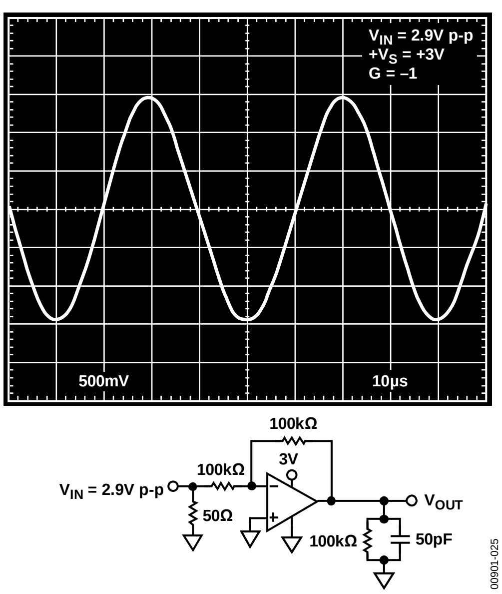


Figure 25. Output Swing, $+V_S = +3$ V, $G = -1$

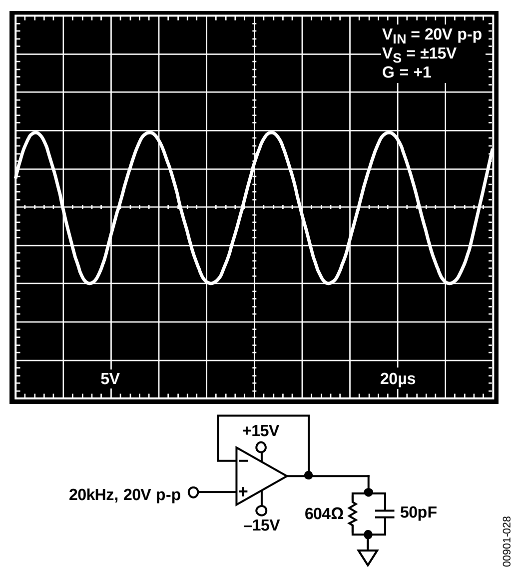


Figure 28. Output Swing, $V_S = \pm 15$ V, $G = +1$

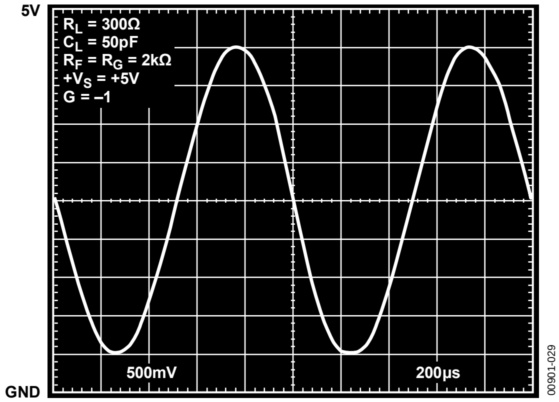


Figure 29. Output Swing, $+V_S = +5$ V, G = −1

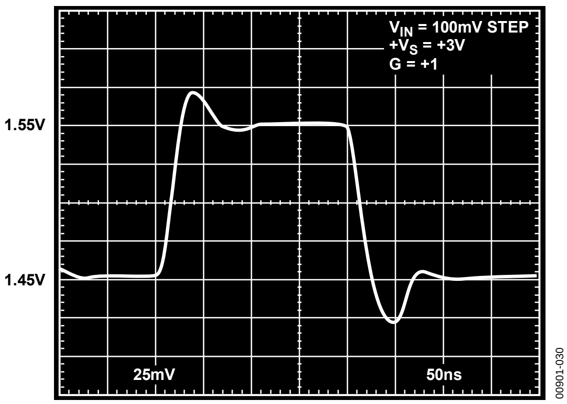


Figure 30. Pulse Response, $+V_S = +3$ V, G = +1

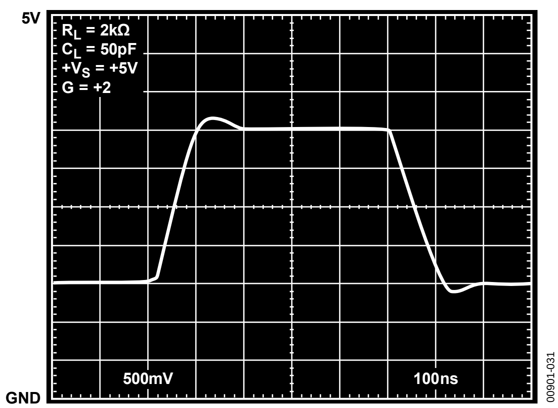


Figure 31. Pulse Response, $+V_S = +5$ V, G = +2

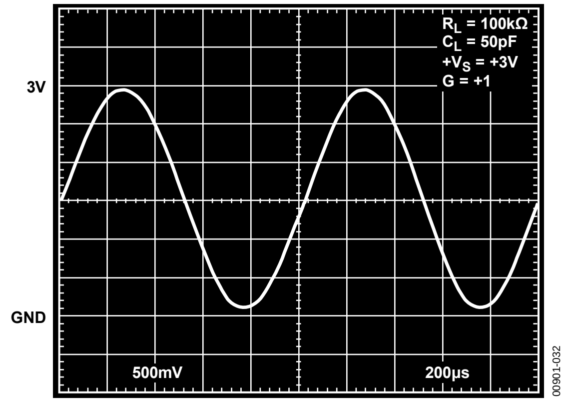


Figure 32. Output Swing, $+V_S = +3$ V, G = +1

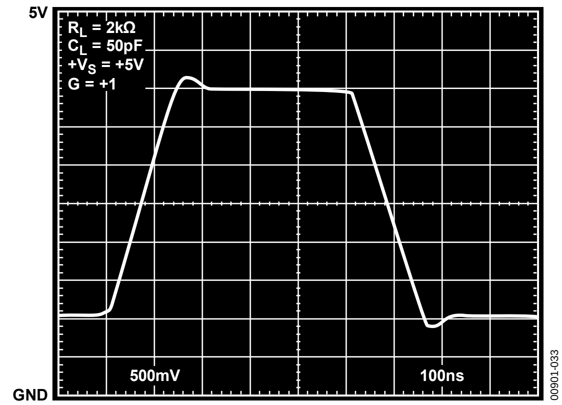


Figure 33. Pulse Response, $+V_S = +5$ V, G = +1

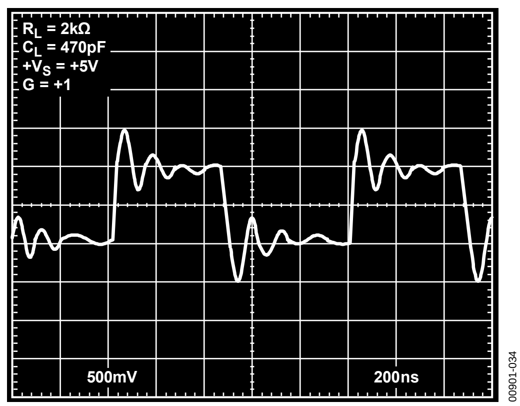


Figure 34. Pulse Response, $+V_S = +5$ V, G = +1, $C_L = 470$ pF

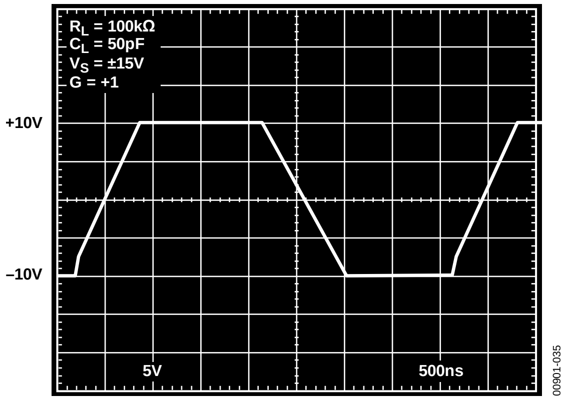


Figure 35. Pulse Response, V_S = ±15 V, G = +1

THEORY OF OPERATION

The AD823 is fabricated on the Analog Devices, Inc. proprietary complementary bipolar (CB) process that enables the construction of PNP and NPN transistors with similar f_T's in the 600 MHz to 800 MHz region. In addition, the process also features N-Channel JFETs that are used in the input stage of the AD823. These process features allow the construction of high frequency, low distortion op amps with picoamp input currents. This design uses a differential output input stage to maximize bandwidth and headroom (see Figure 36). The smaller signal swings required on the S1P/S1N outputs reduce the effect of the nonlinear currents due to junction capacitances and improve the distortion performance. With this design, harmonic distortion of better than −91 dB @ 20 kHz into 600 Ω with V_{OUT} = 4 V p-p on a single 5 V supply is achieved. The complementary common emitter design of the output stage provides excellent load drive without the need for emitter followers, thereby improving the output range of the device considerably with respect to conventional op amps. The AD823 can drive 20 mA with the outputs within 0.6 V of the supply rails. The AD823 also offers outstanding precision for a high speed op amp. Input offset voltages of 1 mV maximum and offset drift of 2 μV/°C are achieved through the use of the Analog Devices advanced thin film trimming techniques.

A nested integrator topology is used in the AD823 (see Figure 37). The output stage can be modeled as an ideal op amp with a single-pole response and a unity-gain frequency set by transconductance g_{m2} and Capacitor C2. R1 is the output impedance of the input stage; g_m is the input transconductance. C1 and C5 provide Miller compensation for the overall op amp. The unity-gain frequency occurs at g_m/C5. Solving the node equations for this circuit yields

$$\frac{V_{OUT}}{Vi} = \frac{A0}{\left(sR1\left[C1\left(A2+1\right)\right]+1\right)\times\left(s\left[\frac{C2}{g_{m2}}\right]+1\right)}$$

where:

$A0 = g_m g_{m2}\, R2R1$ (open-loop gain of op amp).

$A2 = g_{m2}\, R2$ (open-loop gain of output stage).

The first pole in the denominator is the dominant pole of the amplifier and occurs at ~18 Hz. This equals the input stage output impedance R1 multiplied by the Miller-multiplied value of C1. The second pole occurs at the unity-gain bandwidth of the output stage, which is 23 MHz. This type of architecture allows more open-loop gain and output drive to be obtained than a standard 2-stage architecture would allow.

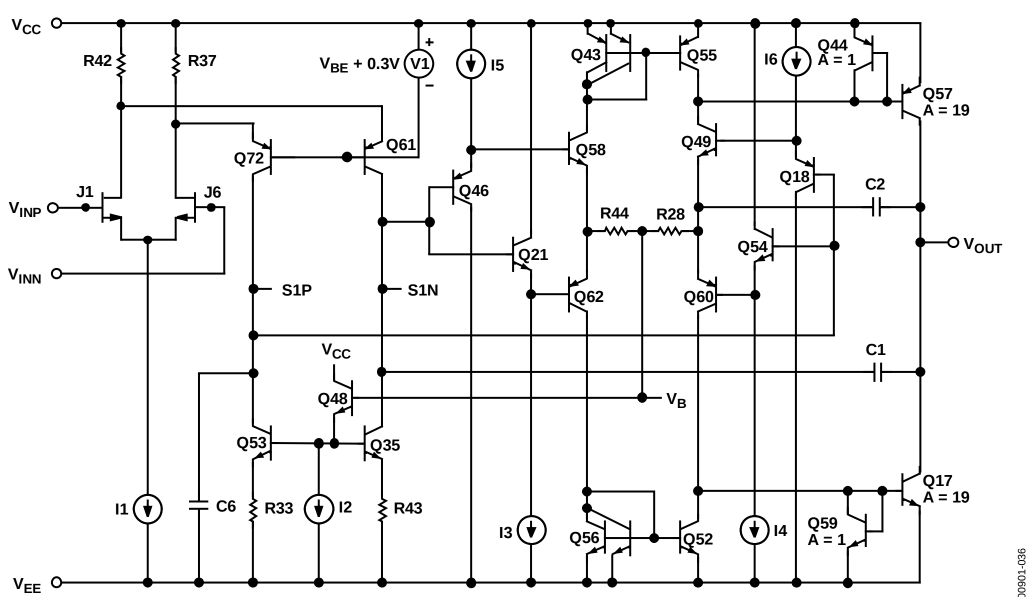


Figure 36. Simplified Schematic

OUTPUT IMPEDANCE

The low frequency open-loop output impedance of the common-emitter output stage used in this design is approximately 30 kΩ. Although this is significantly higher than a typical emitter follower output stage, when it is connected with feedback, the output impedance is reduced by the open-loop gain of the op amp. With 109 dB of open-loop gain, the output impedance is reduced to <0.2 Ω. At higher frequencies, the output impedance rises as the open-loop gain of the op amp drops; however, the output also becomes capacitive due to the integrator capacitors C1 and C2. This prevents the output impedance from ever becoming excessively high (see Figure 18), which can cause stability problems when driving capacitive loads. In fact, the AD823 has excellent cap-load drive capability for a high frequency op amp. Figure 34 shows the AD823 connected as a follower while driving 470 pF direct capacitive load. Under these conditions, the phase margin is approximately 20°. If greater phase margin is desired, a small resistor can be used in series with the output to decouple the effect of the load capacitance from the op amp (see Figure 26). In addition, running the part at higher gains also improves the capacitive load drive capability of the op amp.

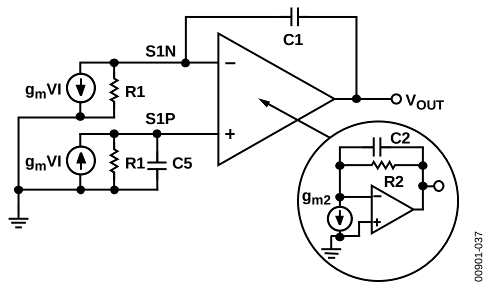


Figure 37. Small Signal Schematic

APPLICATION NOTES

INPUT CHARACTERISTICS

In the AD823, N-Channel JFETs are used to provide a low offset, low noise, high impedance input stage. Minimum input common-mode voltage extends from 0.2 V below $-V_S$ to 1 V < $+V_S$. Driving the input voltage closer to the positive rail causes a loss of amplifier bandwidth and increased common-mode voltage error.

The AD823 does not exhibit phase reversal for input voltages up to and including $+V_S$. Figure 38 shows the response of an AD823 voltage follower to a 0 V to 5 V ($+V_S$) square wave input. The input and output are superimposed. The output polarity tracks the input polarity up to $+V_S$, with no phase reversal. The reduced bandwidth above a 4 V input causes the rounding of the output wave form. For input voltages greater than $+V_S$, a resistor in series with the AD823's noninverting input prevents phase reversal, at the expense of greater input voltage noise. This is illustrated in Figure 39.

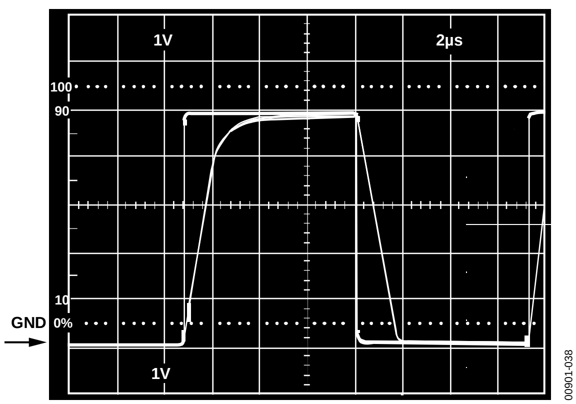


Figure 38. AD823 Input Response: $R_P = 0$, $V_{IN} = 0$ to $+V_S$

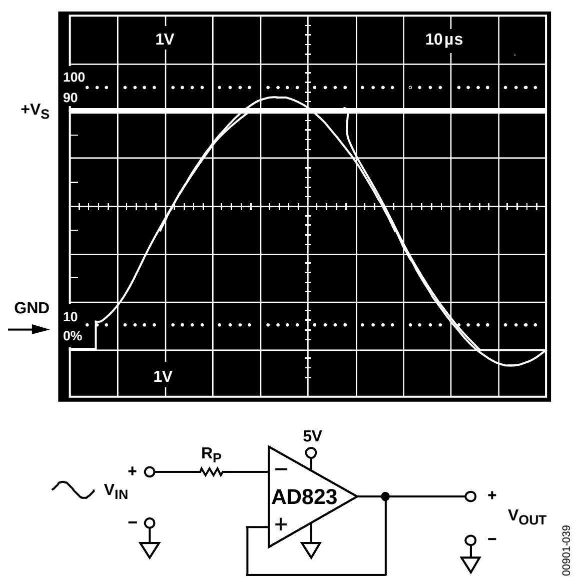


Figure 39. AD823 Input Response:
$V_{IN} = 0$ to $+V_S + 200$ mV, $V_{OUT} = 0$ to $+V_S$, $R_P = 49.9$ kΩ

Because the input stage uses N-Channel JFETs, input current during normal operation is negative; the current flows out from the input terminals. If the input voltage is driven more positive than $+V_S - 0.4$ V, the input current reverses direction as internal device junctions become forward biased. This is illustrated in Figure 7.

A current limiting resistor should be used in series with the input of the AD823 if there is a possibility of the input voltage exceeding the positive supply by more than 300 mV, or if an input voltage is applied to the AD823 when $\pm V_S = 0$. The amplifier becomes damaged if left in that condition for more than 10 seconds. A 1 kΩ resistor allows the amplifier to withstand up to 10 V of continuous overvoltage and increases the input voltage noise by a negligible amount.

Input voltages less than $-V_S$ are a completely different story. The amplifier can safely withstand input voltages 20 V below $-V_S$ as long as the total voltage from the positive supply to the input terminal is less than 36 V. In addition, the input stage typically maintains picoamp level input currents across that input voltage range.

The AD823 is designed for 16 nV/√Hz wideband input voltage noise and maintains low noise performance to low frequencies (see Figure 16). This noise performance, along with the AD823's low input current and current noise, means that the AD823 contributes negligible noise for applications with source resistances greater than 10 kΩ and signal bandwidths greater than 1 kHz.

OUTPUT CHARACTERISTICS

The AD823's unique bipolar rail-to-rail output stage swings within 25 mV of the supplies with no external resistive load. The AD823's approximate output saturation resistance is 25 Ω sourcing and sinking. This can be used to estimate the output saturation voltage when driving heavier current loads. For instance, when driving 5 mA, the saturation voltage to the rails is approximately 125 mV.

If the AD823's output is driven hard against the output saturation voltage, it recovers within 250 ns of the input returning to the amplifier's linear operating region.

A/D Driver

The rail-to-rail output of the AD823 makes it useful as an A/D driver in a single-supply system. Because it is a dual op amp, it can be used to drive both the analog input of the A/D as well as its reference input. The high impedance FET input of the AD823 is well suited for minimal loading of high output impedance devices.

Figure 40 shows a schematic of an AD823 being used to drive both the input and reference input of an AD1672, a 12-bit, 3-MSPS, single-supply ADC. One amplifier is configured as a unity-gain follower to drive the analog input of the AD1672, which is configured to accept an input voltage that ranges from 0 V to 2.5 V.

The other amplifier is configured as a gain of 2 to drive the reference input from a 1.25 V reference. Although the AD1672 has its own internal reference, there are systems that require greater accuracy than the internal reference provides. On the other hand, if the AD1672 internal reference is used, the second AD823 amplifier can be used to buffer the reference voltage for driving other circuitry while minimally loading the reference source.

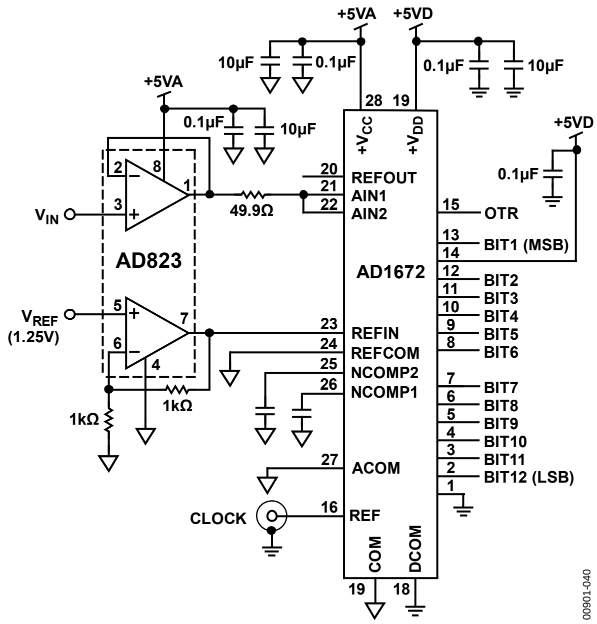


Figure 40. AD823 Driving Input and Reference of the AD1672, a 12-Bit, 3-MSPS ADC

The circuit was tested with a 500 kHz sine wave input that was heavily low-pass filtered (60 dB) to minimize the harmonic content at the input to the AD823. The digital output of the AD1672 was analyzed by performing a fast Fourier transform (FFT).

During the testing, it was observed that at 500 kHz, the output of the AD823 cannot go below ~350 mV (operating with negative supply at ground) without seriously degrading the second harmonic distortion. Another test was performed with a 200 Ω pull-down resistor to ground that allowed the output to go as low as 200 mV without seriously affecting the second harmonic distortion. There was, however, a slight increase in the third harmonic term with the resistor added, but it was still less than the second harmonic.

Figure 41 is an FFT plot of the results of driving the AD1672 with the AD823 with no pull-down resistor. The input amplitude was 2.15 V p-p and the lower voltage excursion was 350 mV. The input frequency was 490 kHz, which was chosen to spread the location of the harmonics.

The distortion analysis is important for systems requiring good frequency domain performance. Other systems may require good time domain performance. The noise and settling time performance of the AD823 provides the necessary information for its applicability for these systems.

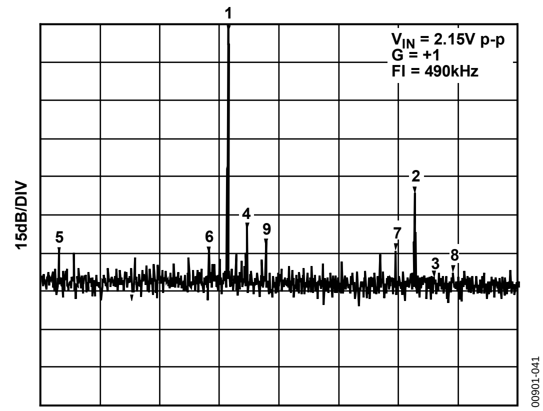


Figure 41. FFT of AD1672 Output Driven by AD823

3 V, Single-Supply Stereo Headphone Driver

The AD823 exhibits good current drive and total harmonic distortion plus noise (THD+N) performance, even at 3 V single supplies. At 20 kHz, THD+N equals −62 dB (0.079%) for a 300 mV p-p output signal. This is comparable to other single-supply op amps that consume more power and cannot run on 3 V power supplies.

In Figure 42, each channel's input signal is coupled via a 1 µF Mylar capacitor. Resistor dividers set the dc voltage at the noninverting inputs so that the output voltage is midway between the power supplies (+1.5 V). The gain is 1.5. Each half of the AD823 can then be used to drive a headphone channel. A 5 Hz high-pass filter is realized by the 500 µF capacitors and the headphones that can be modeled as 32 Ω load resistors to ground. This ensures that all signals in the audio frequency range (20 Hz to 20 kHz) are delivered to the headphones.

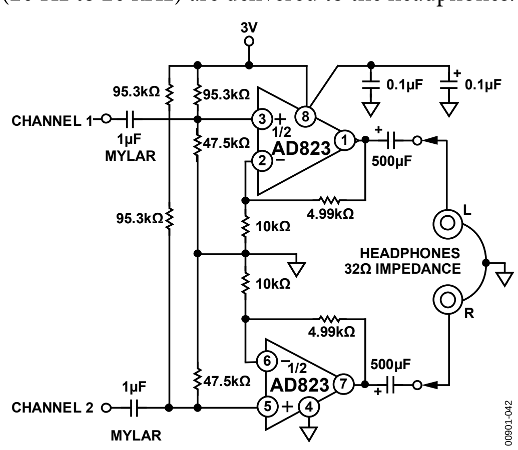


Figure 42. 3 V Single-Supply Stereo Headphone Driver

Second-Order Low-Pass Filter

Figure 43 depicts the AD823 configured as a second-order Butterworth low-pass filter. With the values as shown, the corner frequency equals 200 kHz. Component selection is shown in the following equations:

R1 = R2 = User Selected (*Typical Values*: 10 kΩ to 100 kΩ)

$$C1(farads) = \frac{1.414}{2\pi f_{cutoff} \times R1}$$

$$C2 = \frac{0.707}{2\pi f_{cutoff} \times R1}$$

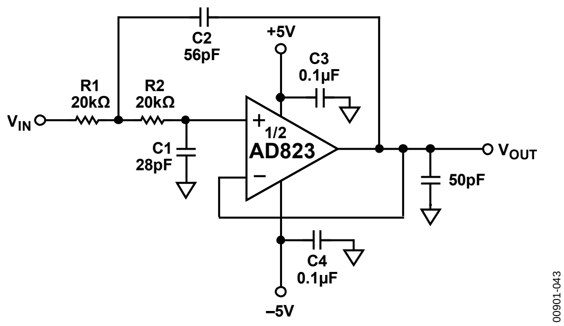


Figure 43. Second-Order Low-Pass Filter

A plot of the filter is shown in Figure 44; better than 50 dB of high frequency rejection is provided.

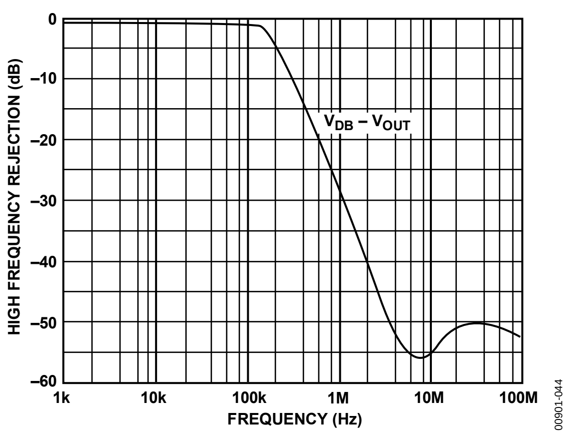


Figure 44. Frequency Response of Filter

Single-Supply Half-Wave and Full-Wave Rectifiers

An AD823 configured as a unity-gain follower and operated with a single supply can be used as a simple half-wave rectifier. The AD823 inputs maintain picoamp level input currents even when driven well below the minus supply. The rectifier puts that behavior to good use, maintaining an input impedance of over 10^{11} Ω for input voltages from within 1 V of the positive supply to 20 V below the negative supply.

The full-wave and half-wave rectifier shown in Figure 45 operates as follows: when V_{IN} is above ground, R1 is bootstrapped through the unity-gain follower A1 and the loop of Amplifier A2. This forces the inputs of A2 to be equal, thus no current flows through R1 or R2, and the circuit output tracks the input. When V_{IN} is below ground, the output of A1 is forced to ground. The noninverting input of Amplifier A2 sees the ground level output of A1; therefore, A2 operates as a unity-gain inverter. The output at Node C is then a full-wave rectified version of the input. Node B is a buffered half-wave rectified version of the input. Input voltage supply to ±18 V can be rectified, depending on the voltage supply used.

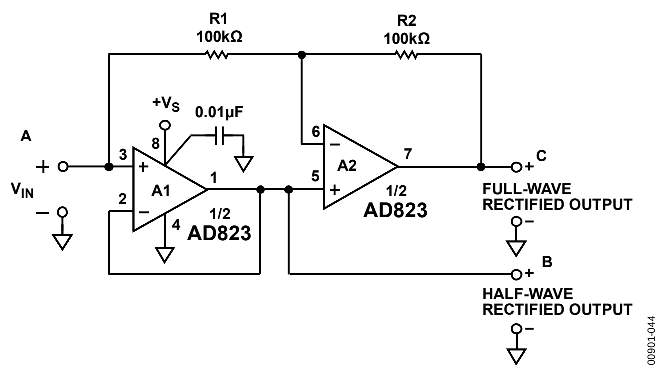


Figure 45. Full-Wave and Half-Wave Rectifier

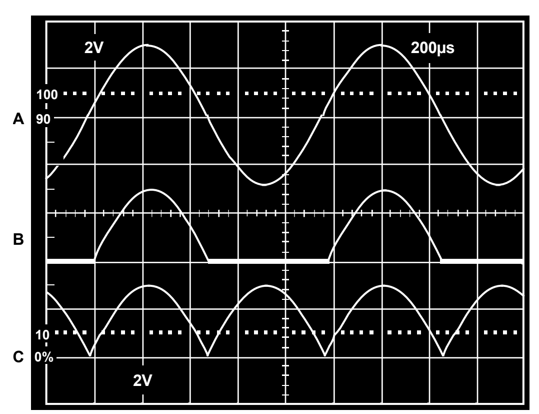
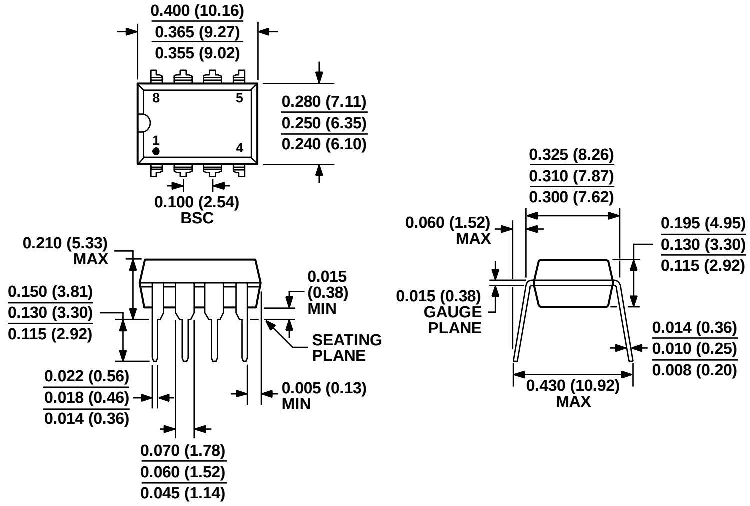


Figure 46. Single-Supply Half-Wave and Full-Wave Rectifier

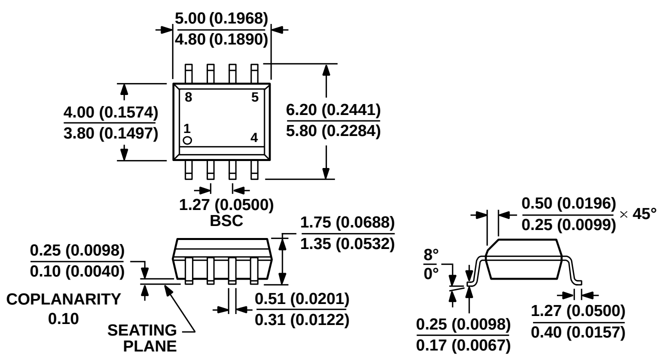
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 47. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 48. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD823ANZ	−40°C to +85°C	8-Lead PDIP	N-8
AD823AR	−40°C to +85°C	8-Lead SOIC_N	R-8
AD823AR-REEL	−40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8
AD823AR-REEL7	−40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8
AD823ARZ	−40°C to +85°C	8-Lead SOIC_N	R-8
AD823ARZ-RL	−40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8
AD823ARZ-R7	−40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8
AD823AR-EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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