

# NCV4296-2C

## Voltage Regulator - Low Dropout, Inhibit

### 30 mA

The NCV4296-2C is a monolithic integrated low dropout voltage regulator with an output current capability of 30 mA available in the TSOP-5 package.

The output voltage is accurate within  $\pm 4.0\%$  with a maximum dropout voltage of 250 mV with an input up to 45 V. Low quiescent current is a feature typically drawing only 160  $\mu\text{A}$  with a 1 mA load. With Inhibit feature, the regulator can be turned off and the device consumes less than 5  $\mu\text{A}$  of quiescent current. This part is ideal for automotive and all battery operated microprocessor equipment.

The regulator is protected against reverse battery, short circuit and thermal overload conditions.

#### Features

- Output Voltage Options: 3.3 V, 5.0 V
- Output Voltage Accuracy:  $\pm 4.0\%$
- Output Current: up to 30 mA
- Low Quiescent Current (typ. 160  $\mu\text{A}$  @ 1 mA)
- Low Dropout Voltage (typ. 65 mV @ 20 mA)
- Wide Input Voltage Operating Range: up to 45 V
- Inhibit Input
- Protection Features:
  - ◆ Current Limitation
  - ◆ Thermal Shutdown
  - ◆ Reverse Polarity Protection and Reverse Bias Protection
- AEC-Q100 Grade 1 Qualified and PPAP Capable
- This is a Pb-Free Device

#### Typical Applications

- Microprocessor Systems Power Supply

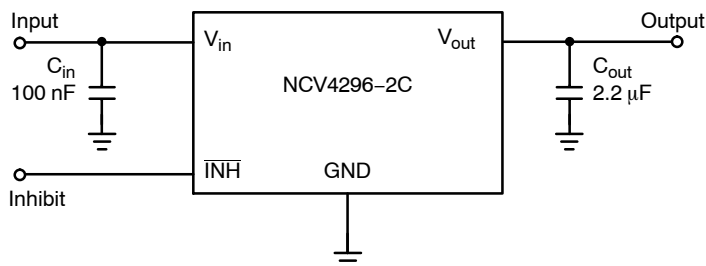
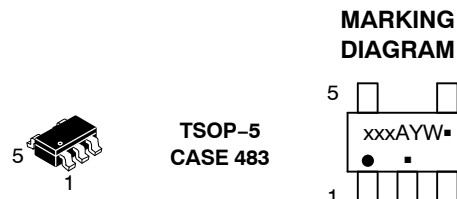


Figure 1. Applications Circuit



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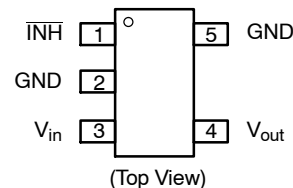
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xxx = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### PIN CONNECTIONS



#### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 10 of this data sheet.

# NCV4296-2C

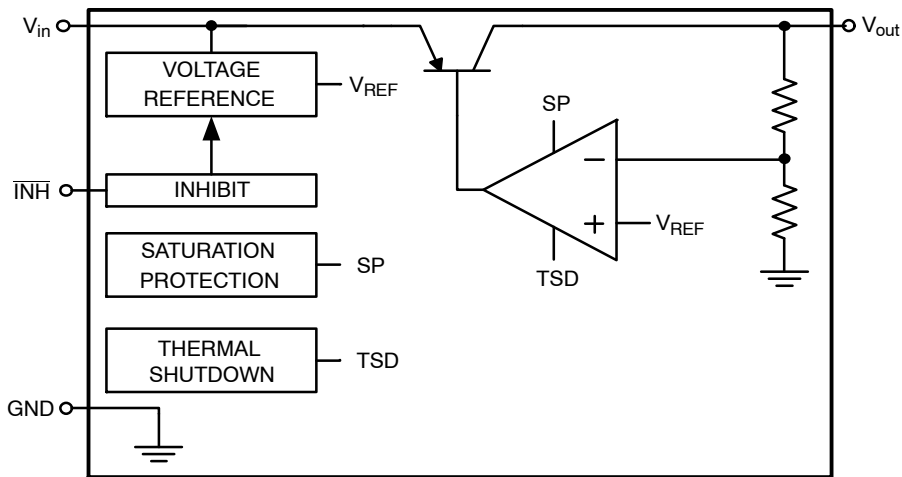


Figure 2. Simplified Block Diagram

## PIN FUNCTION DESCRIPTION

Pin No. TSOP-5	Pin Name	Description
1	$\overline{\text{INH}}$	Inhibit Input. Low level disables the IC.
2	GND	Power Supply Ground.
3	$V_{in}$	Unregulated Positive Power Supply Input. Connect 0.1 $\mu\text{F}$ capacitor to ground.
4	$V_{out}$	Regulated Positive Output Voltage. Connect 2.2 $\mu\text{F}$ capacitor with $\text{ESR} < 7 \Omega$ to ground.
5	GND	Power Supply Ground.

## ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input Voltage DC (Note 1) DC	$V_{in}$	-42	45	V
Input Voltage (Note 2) Load Dump – Suppressed	$U_s$	-	60	V
Output Voltage	$V_{out}$	-6	30	V
Inhibit Input Voltage DC	$V_{\overline{\text{INH}}}$	-42	45	V
Inhibit Input Current Range DC Transient, $-0.3 \text{ V} \leq V_{in} < 45 \text{ V}$ , $t_p < 1 \text{ ms}$	$I_{\overline{\text{INH}}}$	-0.5 -5	- 5	mA
Maximum Junction Temperature	$T_{J(\text{max})}$	-40	150	$^{\circ}\text{C}$
Storage Temperature	$T_{\text{STG}}$	-50	150	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
- Load Dump Test B (with centralized load dump suppression) according to ISO16750-2 standard. Guaranteed by design. Not tested in production. Passed Class A according to ISO16750-1.

## ESD CAPABILITY (Note 3)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	$\text{ESD}_{\text{HBM}}$	-2	2	kV

- This device series incorporates ESD protection and is tested by the following methods:  
ESD Human Body Model tested per AEC-Q100-002 (JS-001-2010)  
Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes  $< 50 \text{ mm}^2$  due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS-002-2014.

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## LEAD SOLDERING TEMPERATURE AND MSL (Note 4)

Rating	Symbol	Min	Max	Unit
Moisture Sensitivity Level	MSL		1	-

4. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

## THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, TSOP-5 Thermal Resistance, Junction-to-Air (Note 5)	$R_{\theta JA}$	136.2	°C/W

5. Values based on copper area of 645 mm<sup>2</sup> (or 1 in<sup>2</sup>) of 1 oz copper thickness and FR4 PCB substrate.

## RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 6)	$V_{in}$	$V_{out, nom} + 0.5$ or 3.5	45	V
Inhibit Input Voltage	$\overline{V_{INH}}$	-0.3	40	V
Junction Temperature	$T_J$	-40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Minimum  $V_{in} = V_{out, nom} + 0.5$  or 3.5, whichever is higher.

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**ELECTRICAL CHARACTERISTICS**  $V_{in} = 13.5\text{ V}$ ,  $V_{INH} > 2.5\text{ V}$ ,  $C_{in} = 0.1\text{ }\mu\text{F}$ ,  $C_{out} = 2.2\text{ }\mu\text{F}$ , for typical values  $T_J = 25^\circ\text{C}$ , for min/max values  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; unless otherwise noted. (Note 7)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
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## REGULATOR OUTPUT

Output Voltage	5.0 V	$V_{in} = 13.5\text{ V}$ , $I_{out} = 1\text{ mA}$ to $30\text{ mA}$ $V_{in} = 6\text{ V}$ to $40\text{ V}$ , $I_{out} = 10\text{ mA}$	$V_{out}$	4.80	5.00	5.20	V
	3.3 V			4.80	5.00	5.20	
Line Regulation		$V_{in} = V_{in, min}$ to $36\text{ V}$ , $I_{out} = 5\text{ mA}$ , $T_J = 25^\circ\text{C}$ $V_{in} = V_{in, min}$ to $36\text{ V}$ , $I_{out} = 5\text{ mA}$	$Reg_{line}$	-	5	20	mV
				-	10	30	
Load Regulation		$I_{out} = 1\text{ mA}$ to $25\text{ mA}$ , $T_J = 25^\circ\text{C}$ $I_{out} = 1\text{ mA}$ to $25\text{ mA}$	$Reg_{load}$	-	3	20	mV
				-	10	30	
Dropout Voltage (Note 8)		$I_{out} = 20\text{ mA}$	$V_{DO}$	-	65	250	mV

## DISABLE AND QUIESCENT CURRENTS

Disable Current		$V_{INH} \leq 0.4\text{ V}$ , $T_J < 85^\circ\text{C}$ $V_{INH} \leq 0.4\text{ V}$	$I_{DIS}$	-	0	1	$\mu\text{A}$
				-	0	5	
Quiescent Current, $I_q = I_{in} - I_{out}$		$I_{out} < 0.1\text{ mA}$ , $T_J < 85^\circ\text{C}$ $I_{out} < 1\text{ mA}$ $I_{out} < 30\text{ mA}$	$I_q$	-	150	170	$\mu\text{A}$
				-	160	200	$\mu\text{A}$
				-	0.8	4	mA
				-			

## CURRENT LIMIT PROTECTION

Current Limit		$V_{out} = V_{out, nom} - 100\text{ mV}$	$I_{LIM}$	30	-	-	mA
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## PSRR

Power Supply Ripple Rejection		$f = 100\text{ Hz}$ , $0.5\text{ V}_{pp}$	PSRR	-	60	-	dB
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## INHIBIT

Inhibit Input Threshold Voltage Low (Off-State) High (On-State)		$V_{out} < 0.1\text{ V}$ $V_{out} > 0.95 \times V_{out, nom}$	$V_{INH}$	0.4	1.76	-	V
				-	1.82	2.2	
Inhibit Input Current Low (Off-State) High (On-State)		$V_{INH} = 0\text{ V}$ $V_{INH} = 5\text{ V}$	$I_{INH\_OFF}$ $I_{INH\_ON}$	-2	-	2	$\mu\text{A}$
				-	6	12	

## THERMAL SHUTDOWN

Thermal Shutdown Temperature (Note 9)			$T_{SD}$	151	175	195	$^\circ\text{C}$
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Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at  $T_A \approx T_J$ . Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
8. Measured when output voltage falls 100 mV below the regulated voltage at  $V_{in} = 13.5\text{ V}$ . If  $V_{out} < 5\text{ V}$ , then  $V_{DO} = V_{in} - V_{out}$ . Maximum dropout voltage value is limited by minimum input voltage  $V_{in} = V_{out, nom} + 0.5\text{ V}$  recommended for guaranteed operation at maximum output current.
9. Values based on design and/or characterization.

TYPICAL CHARACTERISTICS - 5.0 V VERSION

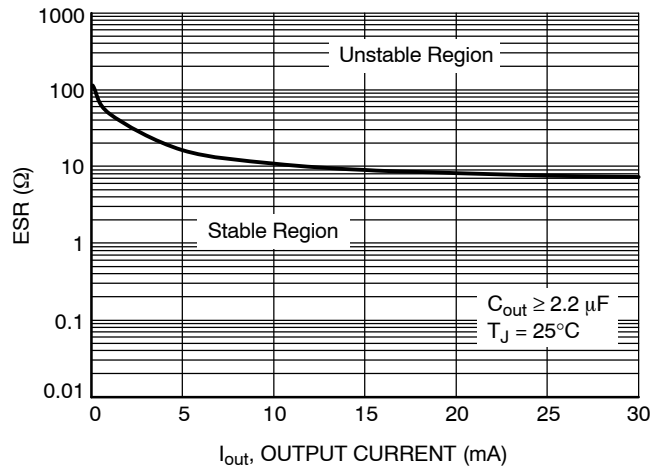


Figure 3. Output Stability with Output Capacitor ESR

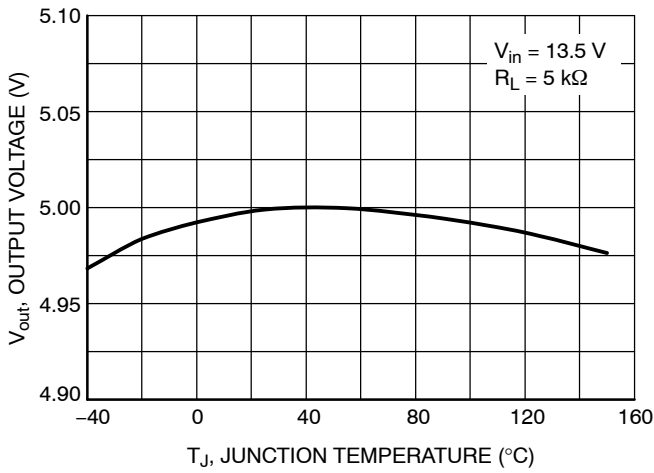


Figure 4. Output Voltage vs. Junction Temperature

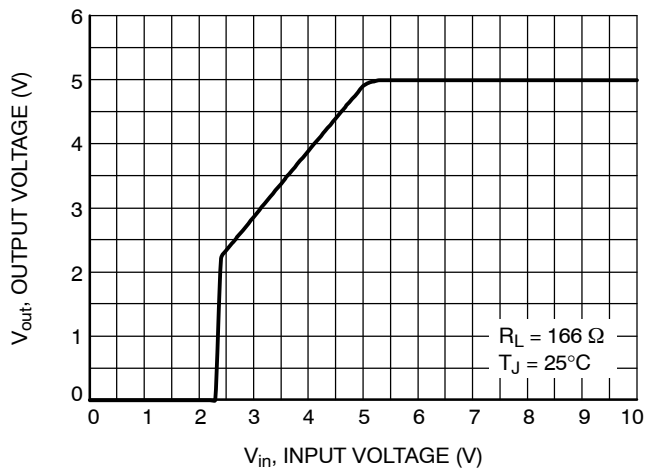


Figure 5. Output Voltage vs. Input Voltage

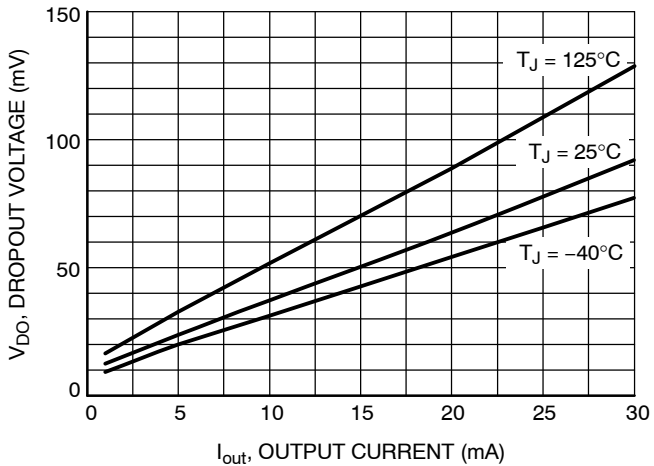


Figure 6. Dropout Voltage vs. Output Current

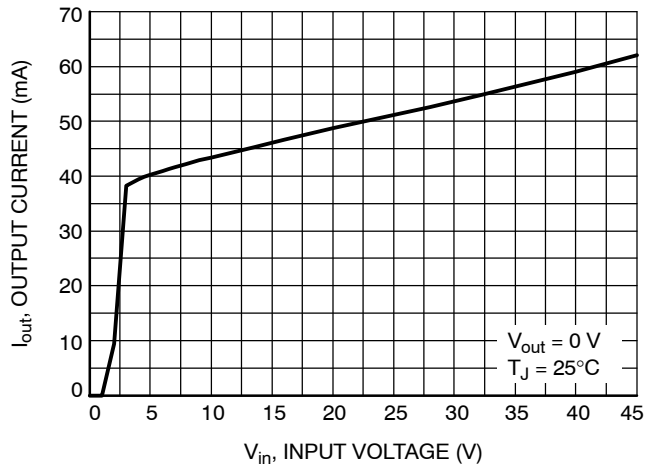


Figure 7. Maximum Output Current vs. Input Voltage

TYPICAL CHARACTERISTICS - 5.0 V VERSION

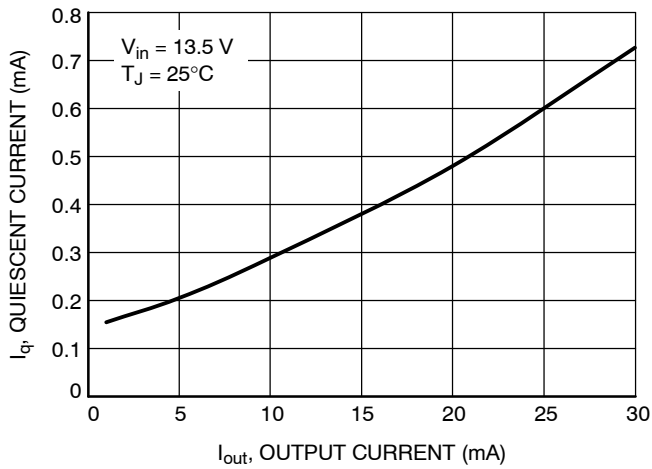


Figure 8. Quiescent Current vs. Output Current (High Load)

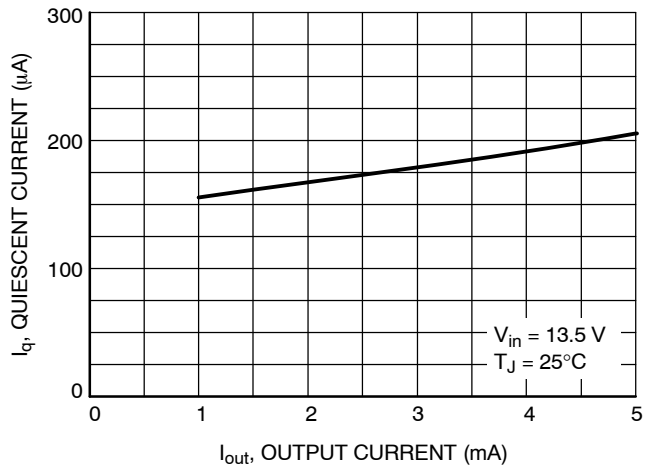


Figure 9. Quiescent Current vs. Output Current (Low Load)

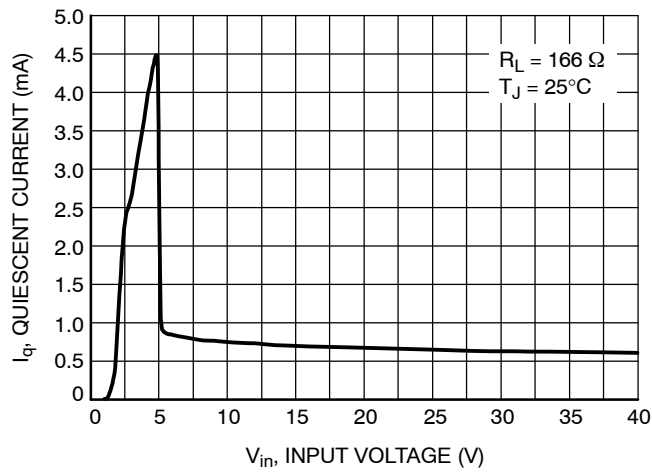


Figure 10. Quiescent Current vs. Input Voltage

TYPICAL CHARACTERISTICS - 3.3 V VERSION

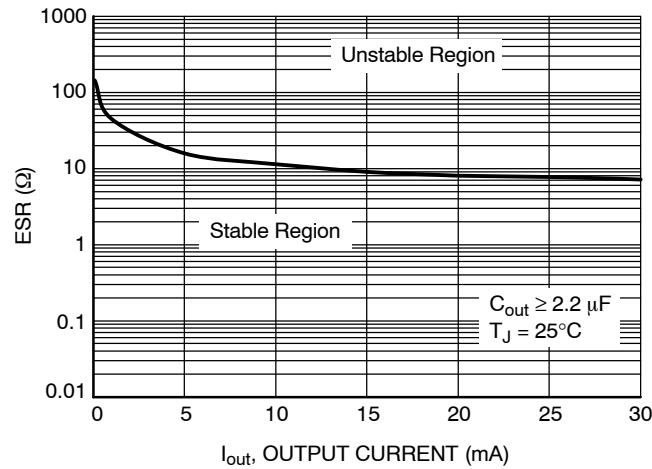


Figure 11. Output Stability with Output Capacitor ESR

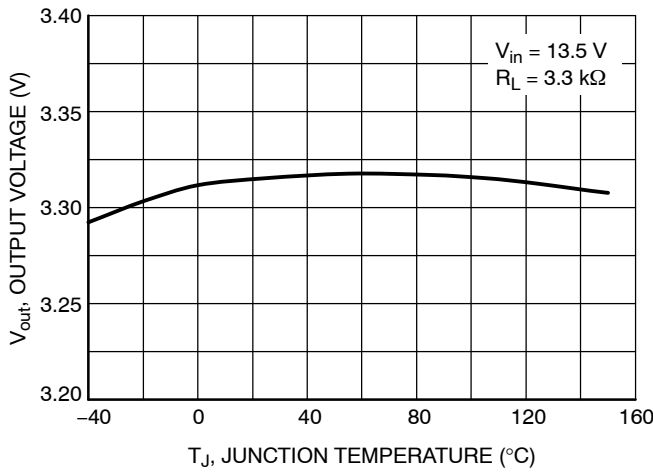


Figure 12. Output Voltage vs. Junction Temperature

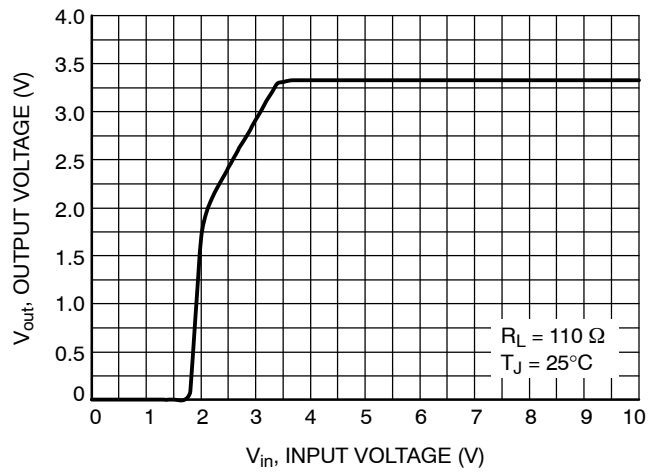


Figure 13. Output Voltage vs. Input Voltage

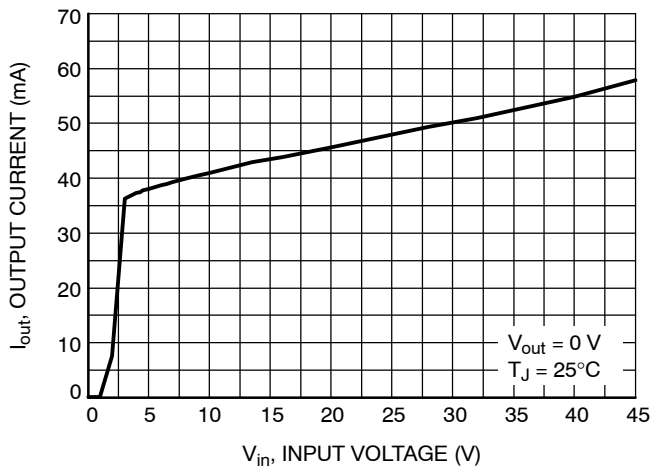


Figure 14. Maximum Output Current vs. Input Voltage

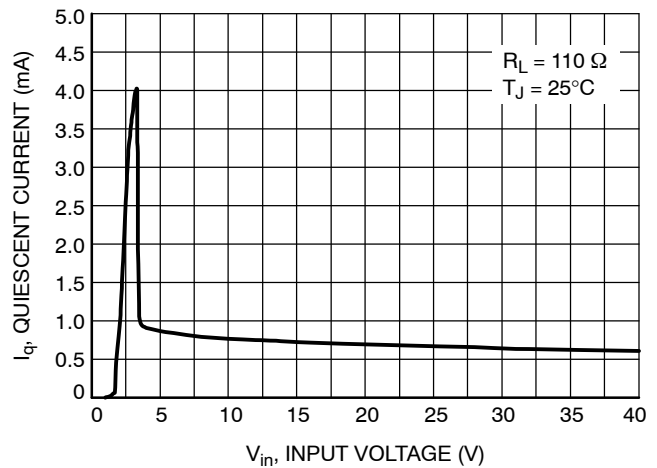
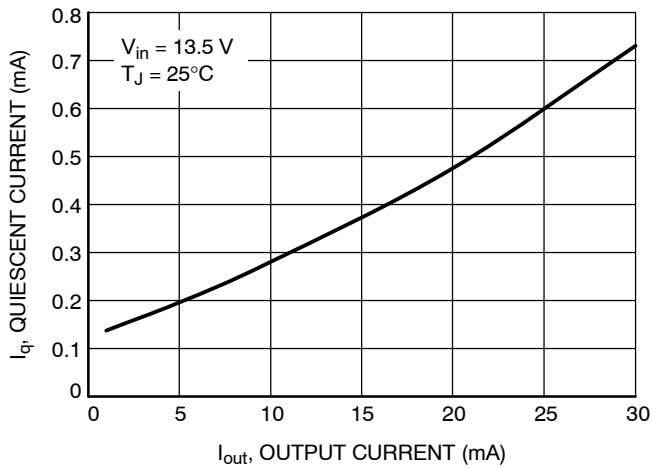


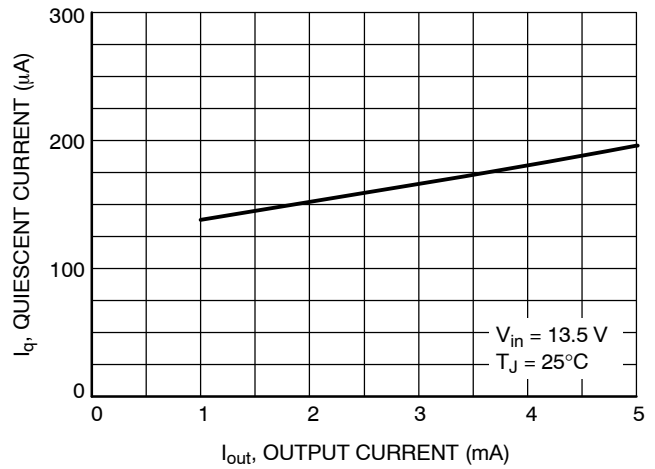
Figure 15. Quiescent Current vs. Input Voltage

# NCV4296-2C

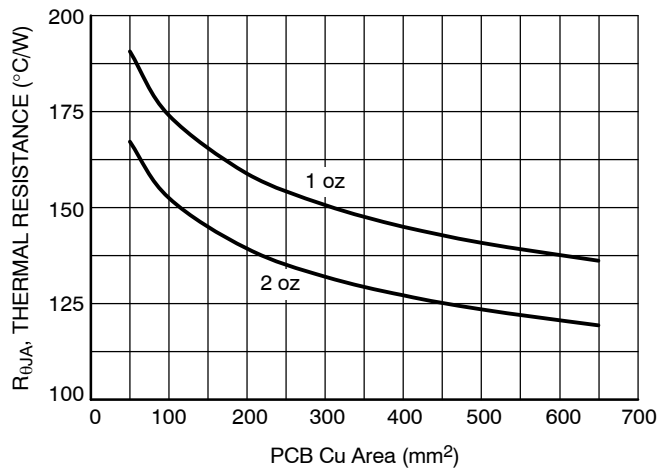
## TYPICAL CHARACTERISTICS – 3.3 V VERSION



**Figure 16. Quiescent Current vs. Output Current (High Load)**



**Figure 17. Quiescent Current vs. Output Current (Low Load)**



**Figure 18.  $R_{\theta JA}$  vs. PCB Cu Area**



## DEFINITIONS

### General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

### Output voltage

The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

### Line Regulation

The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

### Load Regulation

The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

### Dropout Voltage

The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output drops 100 mV below its nominal value. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

### Quiescent and Disable Currents

Quiescent Current ( $I_q$ ) is the difference between the input current (measured through the LDO input pin) and the

output load current. If Inhibit pin is set to LOW the regulator reduces its internal bias and shuts off the output, this term is called the disable current ( $I_{DIS}$ ).

### Current Limit

Current Limit is value of output current by which output voltage drops 100 mV below its nominal value. It means that the device is capable to supply minimum 30 mA.

### PSRR

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

### Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

### Maximum Package Power Dissipation

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

APPLICATIONS INFORMATION

The NCV4296-2C low dropout regulator is self-protected with internal thermal shutdown and internal current limit. Typical characteristics are shown in Figure 3 to Figure 18.

**Input Decoupling (C<sub>in</sub>)**

A ceramic or tantalum 0.1 μF capacitor is recommended and should be connected close to the NCV4296-2C package. Higher capacitance and lower ESR will improve the overall line and load transient response.

**Output Decoupling (C<sub>out</sub>)**

The NCV4296-2C is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. Stability region of ESR vs. Output Current is shown in Figures 3 and 11. The minimum output decoupling value is 2.2 μF and can be augmented to fulfill stringent load transient requirements. The regulator works with ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load transient response.

**Inhibit Operation**

The Inhibit pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet.

**Thermal Considerations**

As power in the NCV4296-2C increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad

configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV4296-2C has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV4296-2C can handle is given by:

$$P_{D(MAX)} = \frac{[T_{J(MAX)} - T_A]}{R_{\theta JA}} \quad (\text{eq. 1})$$

Since T<sub>J</sub> is not recommended to exceed 150°C, then the NCV4296-2C soldered on 645 mm<sup>2</sup>, 1 oz copper area, FR4 can dissipate up to 0.92 W when the ambient temperature (T<sub>A</sub>) is 25°C. See Figure 18 for R<sub>thJA</sub> versus PCB area. The power dissipated by the NCV4296-2C can be calculated from the following equations:

$$P_D \approx V_{in}(I_q @ I_{out}) + I_{out}(V_{in} - V_{out}) \quad (\text{eq. 2})$$

or

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + (V_{out} \times I_{out})}{I_{out} + I_q} \quad (\text{eq. 3})$$

**Hints**

V<sub>in</sub> and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV4296-2C and make traces as short as possible.

**ORDERING INFORMATION**

Device	Marking	Package	Shipping <sup>†</sup>
NCV4296-2CSN50T1G	65V	TSOP-5 (Pb-Free)	3000 / Tape & Reel
NCV4296-2CSN33T1G	63V		

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

## TSOP-5 CASE 483 ISSUE N

DATE 12 AUG 2020



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

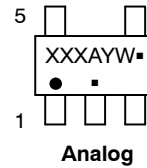
DIM	MILLIMETERS	
	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0°	10°
S	2.50	3.00

### SOLDERING FOOTPRINT\*

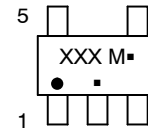


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



Analog



Discrete/Logic

- XXX = Specific Device Code    XXX = Specific Device Code  
 A = Assembly Location        M = Date Code  
 Y = Year                            ■ = Pb-Free Package  
 W = Work Week  
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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