

# 5 V ECL 3-Bit Differential Flip-Flop

## MC10E431

### Description

The MC10E431 is a 3-bit flip-flop with differential clock, data input and data output.

The asynchronous Set and Reset controls are edge-triggered rather than level controlled. This allows the user to rapidly set or reset the flip-flop and then continue clocking at the next clock edge, without the necessity of de-asserting the set/reset signal (as would be the case with a level controlled set/reset).

The E431 is also designed with larger internal swings, an approach intended to minimize the time spent crossing the threshold region and thus reduce the metastability susceptibility window.

The differential input structures are clamped so that the inputs of unused registers can be left open without upsetting the bias network of the device. The clamping action will assert the  $\overline{D}$  and the  $\overline{CLK}$  sides of the inputs. Because of the edge triggered flip-flop nature of the device simultaneously opening both the clock and data inputs will result in an output which reaches an unidentified but valid state. Note that the input clamps only operate when both inputs fall to 2.5 V below  $V_{CC}$ .

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

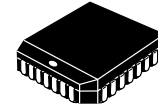
### Features

- Edge-Triggered Asynchronous Set and Reset
- Differential D, CLK and Q;  $V_{BB}$  Reference Available
- 1100 MHz Min. Toggle Frequency
- PECL Mode Operating Range:  $V_{CC} = 4.2$  V to 5.7 V with  $V_{EE} = 0$  V
- NECL Mode Operating Range:  $V_{CC} = 0$  V with  $V_{EE} = -4.2$  V to  $-5.7$  V
- Internal Input 50 k $\Omega$  Pulldown Resistors
- ESD Protection:
  - ◆ > 2 kV Human Body Model
  - ◆ > 200 V Machine Model
  - ◆ > 2 kV Charged Device Model
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity: Level 3 (Pb-Free)  
(For Additional Information, see Application Note [AND8003/D](#))
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 348 Devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



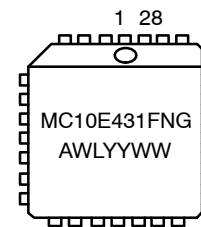
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PLCC-28  
FN SUFFIX  
CASE 776-02

### MARKING DIAGRAM\*



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

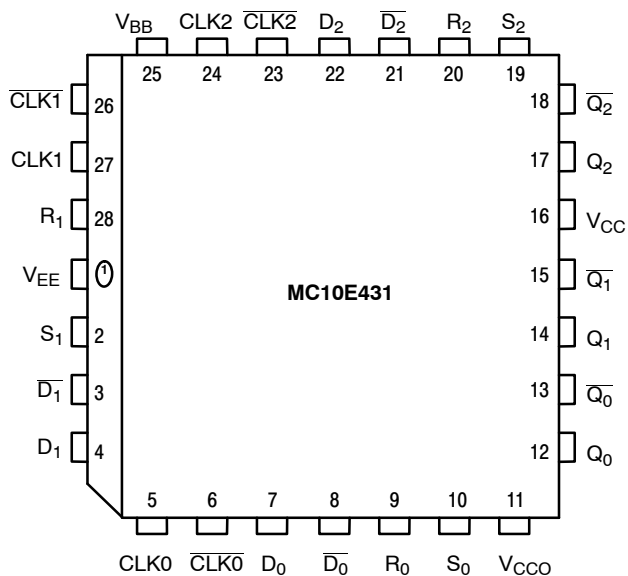
\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

Device	Package	Shipping†
MC10E431FNG	PLCC-28 (Pb-Free)	37 Units / Tube
MC10E431FNR2G	PLCC-28 (Pb-Free)	500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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\* All  $V_{CC}$  and  $V_{CC0}$  pins are tied together on the die.

Warning: All  $V_{CC}$ ,  $V_{CC0}$ , and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Pinout: PLCC-28 (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
$D[0:2], \overline{D}[0:2]$	ECL Differential Data Inputs
$CLK[0:2], \overline{CLK}[0:2]$	ECL Differential Clock
$S[0:2]$	ECL Edge Triggered Set Inputs
$R[0:2]$	ECL Edge Triggered Reset Input
$Q[0:2], \overline{Q}[0:2]$	ECL Differential Data Outputs
$V_{BB}$	Reference Voltage Output
$V_{CC}, V_{CC0}$	Positive Supply
$V_{EE}$	Negative Supply

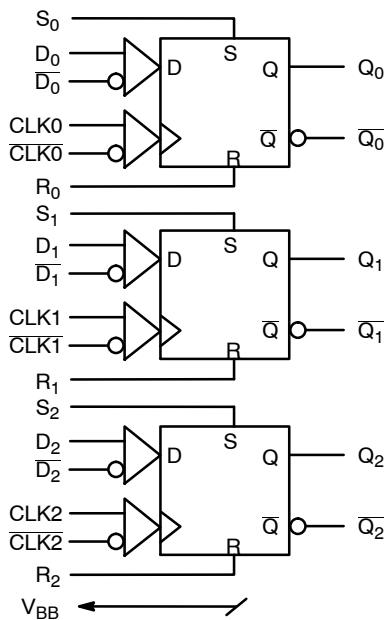


Figure 2. Logic Diagram

Table 2. FUNCTION TABLE

$D_n$	$CLK_n$	$R_n$	$S_n$	$Q_n$
L	Z	L	L	L
H	Z	L	L	H
X	X	Z	L	L
X	X	L	Z	H

Z = Low to high transition

X = Don't Care

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**Table 3. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{CC}$	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		8	V
$V_I$	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 -6	V
$I_{out}$	Output Current	Continuous Surge		50 100	mA
$I_{BB}$	$V_{BB}$ Sink/Source			$\pm 0.5$	mA
$T_A$	Operating Temperature Range			0 to +85	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	PLCC-28 PLCC-28	63.5 43.5	$^{\circ}\text{C}/\text{W}$
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	PLCC-28	22 to 26	$^{\circ}\text{C}/\text{W}$
$T_{sol}$	Wave Solder (Pb-Free)			265	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 4. 10E SERIES PECL DC CHARACTERISTICS** ( $V_{CCx} = 5.0\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  (Note 1))

Symbol	Characteristic	0 $^{\circ}\text{C}$			25 $^{\circ}\text{C}$			85 $^{\circ}\text{C}$			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		110	132		110	132		110	132	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
$V_{OL}$	Output LOW Voltage (Note 2)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
$V_{BB}$	Output Voltage Reference	3.62		3.74	3.65		3.75	3.69		3.81	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	2.7		5.0	2.7		5.0	2.7		5.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $-0.46\text{ V} / +0.06\text{ V}$ .
2. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ .

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**Table 5. 10E SERIES NECL DC CHARACTERISTICS** ( $V_{CCx} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 1))

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		110	132		110	132		110	132	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	-1020	-930	-840	-980	-895	-810	-910	-815	-720	mV
$V_{OL}$	Output LOW Voltage (Note 2)	-1950	-1790	-1630	-1950	-1790	-1630	-1950	-1773	-1595	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1170	-1005	-840	-1130	-970	-810	-1060	-890	-720	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1950	-1715	-1480	-1950	-1715	-1480	-1950	-1698	-1445	mV
$V_{BB}$	Output Voltage Reference	-1.38		-1.27	-1.35		-1.25	-1.31		-1.19	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	-2.3		0.0	-2.3		0.0	-2.3		0.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $-0.46\text{ V} / +0.06\text{ V}$ .
2. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ .

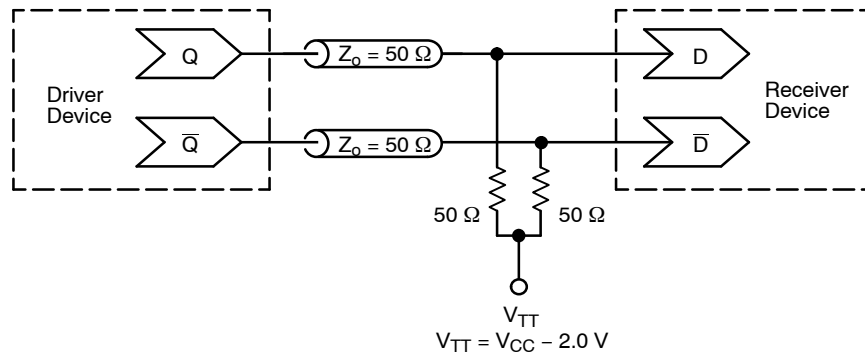
**Table 6. AC CHARACTERISTICS** ( $V_{CCx} = 5.0\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CCx} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{MAX}$	Maximum Toggle Frequency					1.1					GHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay to Output CLK R S	550 500 500	700 725 725	850 975 975	550 550 550	700 725 725	850 925 925	550 550 550	700 725 725	850 925 925	ps
$t_S$	Setup Time D R (Note 2) S (Note 2)	250 1100 1100	0 700 700		200 1000 1000	0 700 700		200 1000 1000	0 700 700		ps
$t_H$	Hold Time D	250	0		200	0		200	0		ps
$t_{PW}$	Minimum Pulse Width CLK	400			400			400			ps
$t_{skew}$	Within-Device Skew (Note 3)		50						50		ps
$t_{JITTER}$	Random Clock Jitter (RMS)		< 1			< 1			< 1		ps
$V_{PP}$	Input Voltage Swing (Differential Configuration)	150		1000	150		1000	150		1000	mV
$t_r/t_f$	Rise/Fall Times (20–80%)	250	450	700				275	450	650	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. 10 Series:  $V_{EE}$  can vary  $-0.46\text{ V} / +0.06\text{ V}$ .
2. These setup times define the minimum time the CLK or SET/RESET input must wait after the assertion of the RESET/SET input to assure the proper operation of the flip-flop.
3. Within-device skew is defined as identical transitions on similar paths through a device.

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**Figure 3. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices)

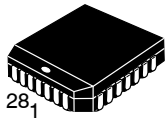
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

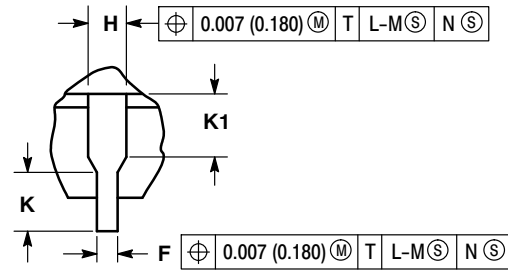
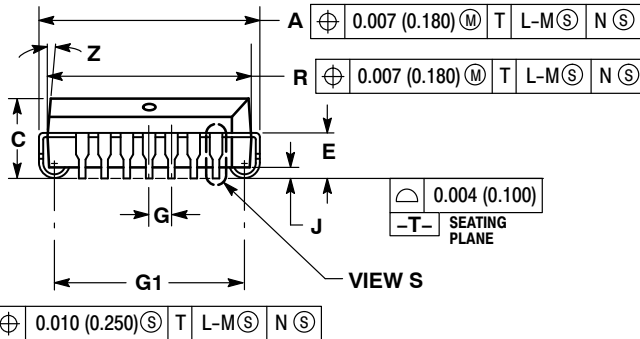
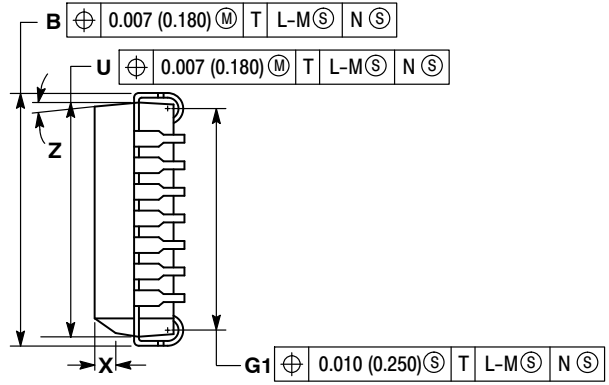
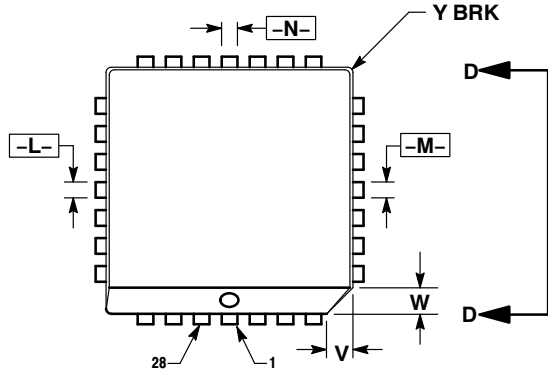
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SCALE 1:1

28 LEAD PLCC  
CASE 776-02  
ISSUE G

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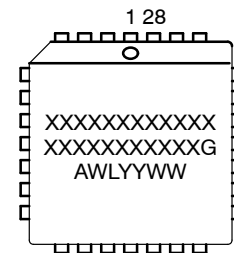


**NOTES:**

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2° 10°		2° 10°	
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

**GENERIC MARKING DIAGRAM\***



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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