

NBSG53A

2.5V/3.3V SiGe Selectable Differential Clock and Data D Flip-Flop/Clock Divider with Reset and OLS*

The NBSG53A is a multi-function differential D flip-flop (DFF) or fixed divide by two (DIV/2) clock generator. This is a part of the GigaComm™ family of high performance Silicon Germanium products. A strappable control pin is provided to select between the two functions. The device is housed in a low profile 4x4 mm 16-pin Flip-Chip BGA (FCBGA) or a 3x3 mm 16 pin QFN package.

The NBSG53A is a device with data, clock, OLS*, reset, and select inputs. Differential inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), LVCMOS/LVTTL, CML, or LVDS. The OLS* input is used to program the peak-to-peak output amplitude between 0 and 800 mV in five discrete steps. The RESET and SELECT inputs are single-ended and can be driven with either LVECL or LVCMOS/LVTTL input levels.

Data is transferred to the outputs on the positive edge of the clock. The differential clock inputs of the NBSG53A allow the device to also be used as a negative edge triggered device.

Features

- Maximum Input Clock Frequency (DFF) > 8 GHz Typical (See Figures 4, 6, 8, 10, and 11)
- Maximum Input Clock Frequency (DIV/2) > 10 GHz Typical (See Figures 5, 7, 9, 10, and 11)
- 210 ps Typical Propagation Delay (OLS = FLOAT)
- 45 ps Typical Rise and Fall Times (OLS = FLOAT)
- DIV/2 Mode (Active with Select Low)
- DFF Mode (Active with Select High)
- Selectable Swing PECL Output with Operating Range: $V_{CC} = 2.375$ V to 3.465 V with $V_{EE} = 0$ V
- Selectable Swing NECL Output with NECL Inputs with Operating Range: $V_{CC} = 0$ V with $V_{EE} = -2.375$ V to -3.465 V
- Selectable Output Level (0 V, 200 mV, 400 mV, 600 mV, or 800 mV Peak-to-Peak Output)
- 50 Ω Internal Input Termination Resistors on all Differential Inputs
- Pb-Free Packages are Available

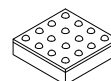
*Output Level Select



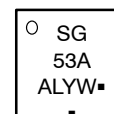
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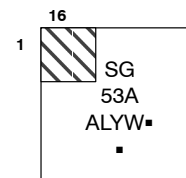
MARKING DIAGRAM*



FCBGA-16
BA SUFFIX
CASE 489



QFN-16
MN SUFFIX
CASE 485G



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.

NBSG53A

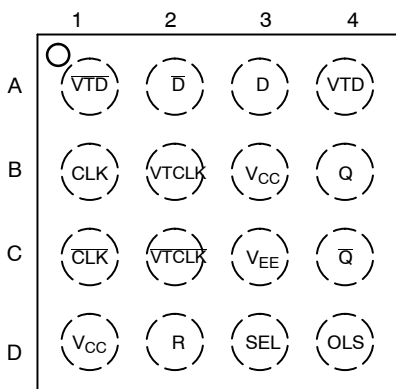


Figure 1. BGA-16 Pinout (Top View)

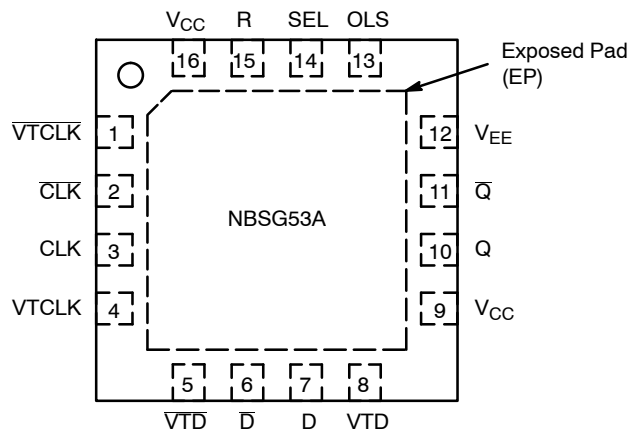


Figure 2. QFN-16 Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin		Name	I/O	Description
BGA	QFN			
C2	1	VTCLK	-	Internal 50 Ω Termination Pin. See Table 4.
C1	2	$\overline{\text{CLK}}$	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Inverted Differential Input.
B1	3	CLK	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Noninverted Differential Input.
B2	4	VTCLK	-	Internal 50 Ω Termination Pin. See Table 4.
A1	5	$\overline{\text{VTD}}$	-	Internal 50 Ω termination pin. See Table 4.
A2	6	$\overline{\text{D}}$	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Inverted Differential Input.
A3	7	D	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Noninverted Differential Input.
A4	8	VTD	-	Internal 50 Ω Termination Pin. See Table 4.
D1,B3	9,16	V _{CC}	-	Positive Supply Voltage
B4	10	Q	RSECL Output	NonInverted Differential Output. Typically Terminated with 50 Ω Resistor to V _{TT} = V _{CC} - 2 V.
C4	11	$\overline{\text{Q}}$	RSECL Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V _{TT} = V _{CC} - 2 V.
C3	12	V _{EE}	-	Negative Supply Voltage
D4	13	OLS*	Input	Input Pin for the Output Level Select (OLS). See Table 2.
D3	14	SEL	LVECL, LVCMOS, LVTTTL Input	Select Logic Input. Internal 75 k Ω to V _{EE} .
D2	15	R	LVECL, LVCMOS, LVTTTL Input	Reset D Flip-Flop. Internal 75 k Ω to V _{EE} .
N/A	-	EP		The Exposed Pad (EP) and the QFN-16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is not electrically connected to the die but may be electrically and thermally connected to V _{EE} on the PC board.

1. All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation. The thermally exposed pad (EP) on package bottom (see case drawing) must be attached to a heat-sinking conduit.
2. In the differential configuration when the input termination pins (VTD, $\overline{\text{VTD}}$, VTCLK, $\overline{\text{VTCLK}}$) are connected to a common termination voltage, and if no signal is applied then the device will be susceptible to self-oscillation.
3. When an output level of 400 mV is desired and V_{CC} - V_{EE} > 3.0 V, 2K Ω resistor should be connected from OLS pin to V_{EE}.

NBSG53A

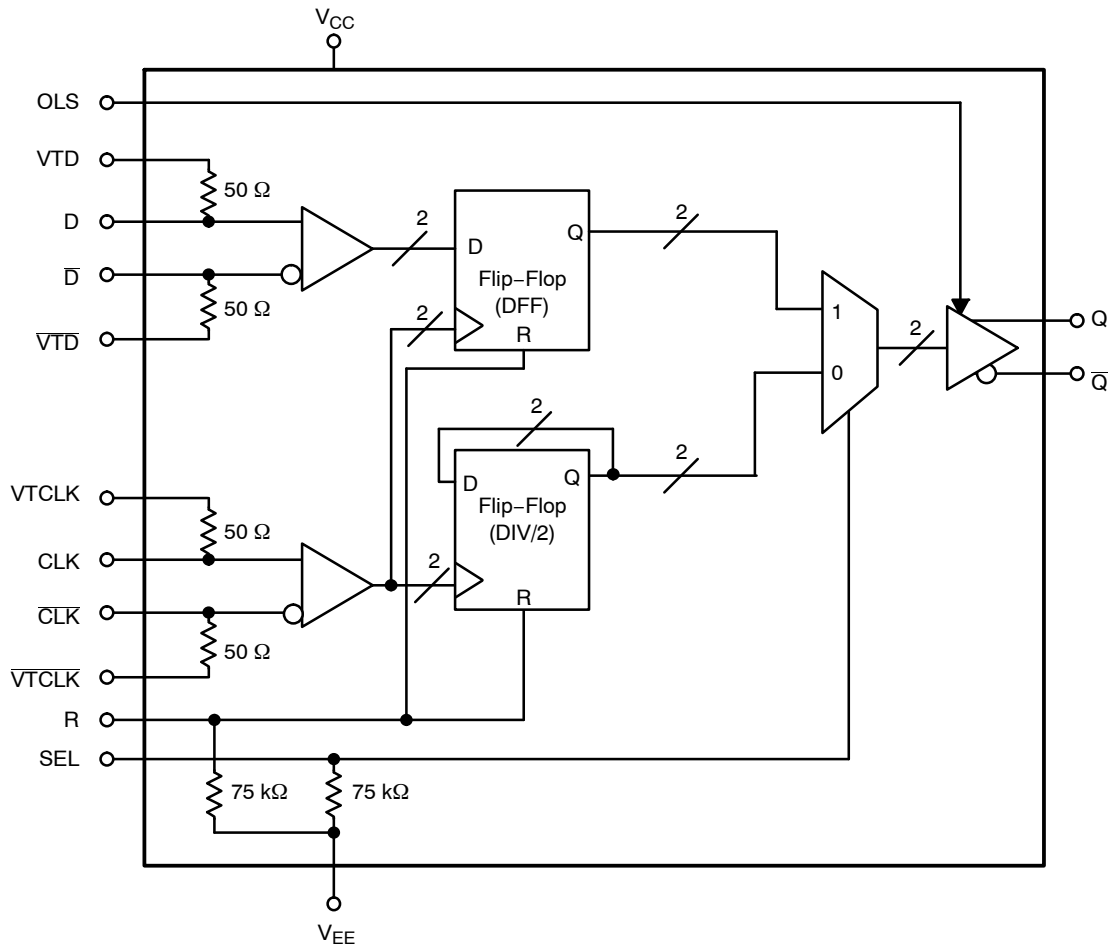


Figure 3. Simplified Logic Diagram

Table 2. OUTPUT LEVEL SELECT (OLS)

OLS	Q/Q̄ VPP	OLS Sensitivity
V _{CC}	800 mV	OLS - 75 mV
V _{CC} - 0.4 V	200 mV	OLS ± 150 mV
V _{CC} - 0.8 V	600 mV	OLS ± 100 mV
V _{CC} - 1.2 V	0	OLS ± 75 mV
V _{EE} (Note 4)	400 mV	OLS + 100 mV
Float	600 mV	N/A

4. When an output level of 400 mV is desired and V_{CC} - V_{EE} > 3.0 V, 2.0 kΩ resistor should be connected from OLS to V_{EE}.

Table 3. TRUTH TABLE

R	SEL	D	CLK	Q	Function
H	x	x	x	L	Reset
L	H	L	Z	L	DFF
L	H	H	Z	H	DFF
L	L	x	Z	Q̄	DIV/2

Z = LOW to HIGH Transition

Table 4. INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTCLK, VTD and VTCLK, VT̄D to V _{CC}
LVDS	Connect VTCLK, VTD and VTCLK, VT̄D Together
AC-COUPLED	Bias VTCLK, VTD and VTCLK, VT̄D Inputs within Common Mode Range (V _{IHCMR})
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTL, LVCMOS	An External Voltage (V _{THR}) should be Applied to the Unused Complementary Differential Input. Nominal V _{THR} is 1.5 V for LVTTL and V _{CC} /2 for LVCMOS Inputs. This Voltage must be within the V _{THR} Specification.

NBSG53A

Table 5. ATTRIBUTES

Characteristics	Value
Positive Operating Voltage Range for V_{CC} ($V_{EE} = 0$ V)	2.375 V to 3.465 V
Negative Operating Voltage Range for V_{EE} ($V_{CC} = 0$ V)	-2.375 V to -3.465 V
Internal Input Pulldown Resistor (R, SEL)	75 k Ω
ESD Protection	Human Body Model Machine Model Charged Device Model
	> 1.5 kV > 50 V > 4 kV
Moisture Sensitivity (Note 5)	FCBGA-16 16-QFN
	Level 3 Level 1
Flammability Rating	UL 94 V-0 @ 0.125 in
Oxygen Index	28 to 34
Transistor Count	482
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

5. For additional information, refer to Application Note AND8003/D.

Table 6. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	$V_{EE} = 0$ V		3.6	V
V_{EE}	Negative Power Supply	$V_{CC} = 0$ V		-3.6	V
V_I	Positive Input Negative Input	$V_{EE} = 0$ V $V_{CC} = 0$ V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	3.6 -3.6	V V
V_{INPP}	Differential Input Voltage $ D - \bar{D} $	$V_{CC} - V_{EE} \geq 2.8$ V $V_{CC} - V_{EE} < 2.8$ V		2.8 $ V_{CC} - V_{EE} $	V V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA mA
I_{OUT}	Output Current	Continuous Surge		25 50	mA mA
T_A	Operating Temperature Range	FCBGA-16 QFN-16		-40 to +70 -40 to +85	$^{\circ}$ C
T_{stg}	Storage Temperature Range			-65 to +150	$^{\circ}$ C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 6)	0 lfpm 500 lfpm 0 lfpm 500 lfpm	FCBGA-16 FCBGA-16 QFN-16 QFN-16	108 86 41.6 35.2	$^{\circ}$ C/W $^{\circ}$ C/W $^{\circ}$ C/W $^{\circ}$ C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	2S2P (Note 6) 2S2P (Note 7)	FCBGA-16 QFN-16	5.0 4.0	$^{\circ}$ C/W $^{\circ}$ C/W
T_{sol}	Wave Solder	Pb Pb-Free	< 3 sec @ 248 $^{\circ}$ C < 3 sec @ 260 $^{\circ}$ C	265 265	$^{\circ}$ C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

6. JEDEC standard 51-6, multilayer board - 2S2P (2 signal, 2 power).

7. JEDEC standard multilayer board - 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

NBSG53A

Table 7. DC CHARACTERISTICS, INPUT WITH PECL OUTPUT $V_{CC} = 2.5\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 8)

Symbol	Characteristic	-40°C			25°C			70°C(BGA)/85°C(QFN)**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current	33	45	57	33	45	57	33	45	57	mA
V_{OH}	Output HIGH Voltage (Note 9)	1460	1510	1560	1490	1540	1590	1515	1565	1615	mV
V_{OL}	Output LOW Voltage (Note 9)										mV
	(OLS = V_{CC})	555	705	855	595	745	895	625	775	925	
	(OLS = $V_{CC} - 0.4\text{ V}$)	1235	1295	1385	1270	1330	1420	1295	1355	1445	
	(OLS = $V_{CC} - 0.8\text{ V}$, OLS = FLOAT)	775	895	1015	810	930	1050	840	960	1080	
	(OLS = $V_{CC} - 1.2\text{ V}$)	1455	1505	1585	1490	1540	1620	1510	1560	1640	
	(OLS = V_{EE})	1005	1095	1215	1040	1130	1250	1065	1155	1275	
V_{OUTPP}	Output Voltage Amplitude										mV
	(OLS = V_{CC})	670	800		660	795		655	790		
	(OLS = $V_{CC} - 0.4\text{ V}$)	125	215		120	210		120	210		
	(OLS = $V_{CC} - 0.8\text{ V}$, OLS = FLOAT)	510	615		505	610		500	605		
	(OLS = $V_{CC} - 1.2\text{ V}$)	0	5		0	0		0	5		
	(OLS = V_{EE})	325	415		320	410		320	410		
V_{IH}	Input HIGH Voltage (Single-Ended) (Notes 11 and 13) CLK, $\overline{\text{CLK}}$, D, $\overline{\text{D}}$	$V_{EE} + 1275$	$V_{CC} - 1000^*$	V_{CC}	$V_{EE} + 1275$	$V_{CC} - 1000^*$	V_{CC}	$V_{EE} + 1275$	$V_{CC} - 1000^*$	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single-Ended) (Notes 12 and 13) CLK, $\overline{\text{CLK}}$, D, $\overline{\text{D}}$	V_{EE}	$V_{CC} - 1400^*$	$V_{IH} - 150$	V_{EE}	$V_{CC} - 1400^*$	$V_{IH} - 150$	V_{EE}	$V_{CC} - 1400^*$	$V_{IH} - 150$	mV
V_{IH}	Input High Voltage (Single-Ended) R, SEL	1290		V_{CC}	1355		V_{CC}	1415		V_{CC}	mV
V_{IL}	Input Low Voltage (Single-Ended) R, SEL	V_{EE}		890	V_{EE}		955	V_{EE}		1015	mV
V_{THR}	Input Threshold Voltage (Single-Ended) (Note 13)	$V_{EE} + 1125$		$V_{CC} - 75$	$V_{EE} + 1125$		$V_{CC} - 75$	$V_{EE} + 1125$		$V_{CC} - 75$	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 10)	1.2		2.5	1.2		2.5	1.2		2.5	V
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH}) R, SEL CLK, $\overline{\text{CLK}}$, D, $\overline{\text{D}}$		35 5	100 50		35 5	100 50		35 5	100 50	μA
I_{IL}	Input LOW Current (@ V_{IL}) R, SEL CLK, $\overline{\text{CLK}}$, D, $\overline{\text{D}}$		20 5	100 50		20 5	100 50		20 5	100 50	μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.125 V to -0.965 V.

9. All outputs loaded with 50 Ω to $V_{CC} - 2.0\text{ V}$.

10. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

11. V_{IH} cannot exceed V_{CC} . $|V_{IH} - V_{THR}| < 2600\text{ mV}$.

12. V_{IL} always $\geq V_{EE}$. $|V_{IL} - V_{THR}| < 2600\text{ mV}$.

13. V_{THR} is the voltage applied to one input when running in single-ended mode.

*Typicals used for testing purposes.

**The device packaged in FCBGA-16 have maximum ambient temperature specification of 70°C and devices packaged in QFN-16 have maximum ambient temperature specification of 85°C.

NBSG53A

Table 8. DC CHARACTERISTICS, INPUT WITH PECL OUTPUT $V_{CC} = 3.3\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 14)

Symbol	Characteristic	-40°C			25°C			70°C(BGA)/85°C(QFN)***			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current	35	47	59	35	47	59	35	47	59	mA
V_{OH}	Output HIGH Voltage (Note 15)	2260	2310	2360	2290	2340	2390	2315	2365	2415	mV
V_{OL}	Output LOW Voltage (Note 15) (OLS = V_{CC}) (OLS = $V_{CC} - 0.4\text{ V}$) (OLS = $V_{CC} - 0.8\text{ V}$, OLS = FLOAT) (OLS = $V_{CC} - 1.2\text{ V}$) **(OLS = V_{EE})	1320 2030 1550 2260 1785	1470 2090 1670 2310 1875	1620 2180 1790 2390 1995	1360 2065 1585 2290 1820	1510 2125 1705 2340 1910	1660 2215 1825 2420 2030	1390 2090 1615 2315 1850	1540 2150 1735 2365 1940	1690 2240 1855 2445 2060	mV
V_{OUTPP}	Output Amplitude Voltage (OLS = V_{CC}) (OLS = $V_{CC} - 0.4\text{ V}$) (OLS = $V_{CC} - 0.8\text{ V}$, OLS = FLOAT) (OLS = $V_{CC} - 1.2\text{ V}$) **(OLS = V_{EE})	705 130 535 0 345	815 220 640 0 435		695 125 530 0 340	805 215 635 0 430		690 125 525 0 335	800 215 630 0 425		mV
V_{IH}	Input HIGH Voltage (Single-Ended) (Notes 17 and 19) CLK, $\overline{\text{CLK}}$, D, $\overline{\text{D}}$	$V_{EE} + 1275$	$V_{CC} - 1000^*$	V_{CC}	$V_{EE} + 1275$	$V_{CC} - 1000^*$	V_{CC}	$V_{EE} + 1275$	$V_{CC} - 1000^*$	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single-Ended) (Notes 18 and 19) CLK, $\overline{\text{CLK}}$, D, $\overline{\text{D}}$	$V_{IH} - 2600$	$V_{CC} - 1400^*$	$V_{IH} - 150$	$V_{IH} - 2600$	$V_{CC} - 1400^*$	$V_{IH} - 150$	$V_{IH} - 2600$	$V_{CC} - 1400^*$	$V_{IH} - 150$	mV
V_{IH}	Input High Voltage (Single-Ended) R, SEL	2090		V_{CC}	2155		V_{CC}	2215		V_{CC}	mV
V_{IL}	Input Low Voltage (Single-Ended) R, SEL	V_{EE}		1690	V_{EE}		1755	V_{EE}		1815	mV
V_{THR}	Input Threshold Voltage (Single-Ended) (Note 19)	$V_{EE} + 1125$		$V_{CC} - 75$	$V_{EE} + 1125$		$V_{CC} - 75$	$V_{EE} + 1125$		$V_{CC} - 75$	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 16)	1.2		3.3	1.2		3.3	1.2		3.3	V
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH}) R, SEL CLK, $\overline{\text{CLK}}$, D, $\overline{\text{D}}$		35 5	100 50		35 5	100 50		35 5	100 50	μA
I_{IL}	Input LOW Current (@ V_{IL}) R, SEL CLK, $\overline{\text{CLK}}$, D, $\overline{\text{D}}$		20 5	100 50		20 5	100 50		20 5	100 50	μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

14. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925 V to -0.165 V.

15. All outputs loaded with 50 Ω to $V_{CC} - 2.0\text{ V}$.

16. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

17. V_{IH} cannot exceed V_{CC} . $|V_{IH} - V_{THR}| < 2600\text{ mV}$.

18. V_{IL} always $\geq V_{EE}$. $|V_{IL} - V_{THR}| < 2600\text{ mV}$.

19. V_{THR} is the voltage applied to one input when running in single-ended mode.

*Typicals used for testing purposes.

**When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0\text{ V}$, a 2 k Ω resistor should be connected from OLS to V_{EE} .

***The device packaged in FCBGA-16 have maximum ambient temperature specification of 70°C and devices packaged in QFN-16 have maximum ambient temperature specification of 85°C.

NBSG53A

Table 9. DC CHARACTERISTICS, NECL INPUT WITH NECL OUTPUT

$V_{CC} = 0\text{ V}$; $V_{EE} = -3.465\text{ V to } -2.375\text{ V}$ (Note 20)

Symbol	Characteristic	-40°C			25°C			70°C(BGA)/85°C(QFN)***			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current	35	47	59	35	47	59	35	47	59	mA
V_{OH}	Output HIGH Voltage (Note 21)	-1040	-990	-940	-1010	-960	-910	-985	-935	-885	mV
V_{OL}	Output LOW Voltage (Note 21) -3.465 V $\leq V_{EE} \leq$ -3.0 V (OLS = V_{CC}) (OLS = $V_{CC} - 0.4\text{ V}$) (OLS = $V_{CC} - 0.8\text{ V}$, OLS = FLOAT) (OLS = $V_{CC} - 1.2\text{ V}$) **(OLS = V_{EE}) -3.0 V < $V_{EE} \leq$ -2.375 V (OLS = V_{CC}) (OLS = $V_{CC} - 0.4\text{ V}$) (OLS = $V_{CC} - 0.8\text{ V}$, OLS = FLOAT) (OLS = $V_{CC} - 1.2\text{ V}$) (OLS = V_{EE})	-1980 -1270 -1750 -1040 -1515 -1945 -1265 -1725 -1045 -1495	-1830 -1210 -1630 -990 -1425 -1795 -1205 -1605 -995 -1405	-1680 -1120 -1510 -910 -1305 -1645 -1115 -1485 -915 -1285	-1940 -1235 -1715 -1010 -1480 -1905 -1230 -1690 -1010 -1460	-1790 -1175 -1595 -960 -1390 -1755 -1170 -1570 -960 -1370	-1640 -1085 -1475 -880 -1270 -1605 -1080 -1450 -880 -1250	-1910 -1210 -1685 -985 -1450 -1875 -1205 -1660 -990 -1435	-1760 -1150 -1565 -935 -1360 -1725 -1145 -1540 -940 -1345	-1610 -1060 -1445 -855 -1240 -1575 -1055 -1420 -860 -1225	mV
V_{OUTPP}	Output Voltage Amplitude -3.465 V $\leq V_{EE} \leq$ -3.0 V (OLS = V_{CC}) (OLS = $V_{CC} - 0.4\text{ V}$) (OLS = $V_{CC} - 0.8\text{ V}$, OLS = FLOAT) (OLS = $V_{CC} - 1.2\text{ V}$) **(OLS = V_{EE}) -3.0 V < $V_{EE} \leq$ -2.375 V (OLS = V_{CC}) (OLS = $V_{CC} - 0.4\text{ V}$) (OLS = $V_{CC} - 0.8\text{ V}$, OLS = FLOAT) (OLS = $V_{CC} - 1.2\text{ V}$) (OLS = V_{EE})	705 130 535 0 345 670 125 510 0 325	815 220 640 0 435 800 215 615 5 415	695 125 530 0 340 660 120 505 0 320	805 215 635 0 430 795 210 610 0 410	690 125 525 0 335 655 120 500 0 320	800 215 630 0 425 790 210 605 5 410				mV
V_{IH}	Input HIGH Voltage (Single-Ended) (Notes 23 and 25) CLK, $\overline{\text{CLK}}$, D, $\overline{\text{D}}$	$V_{EE} + 1275$	$V_{CC} - 1000^*$	V_{CC}	$V_{EE} + 1275$	$V_{CC} - 1000^*$	V_{CC}	$V_{EE} + 1275$	$V_{CC} - 1000^*$	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single-Ended) (Notes 24 and 25) CLK, $\overline{\text{CLK}}$, D, $\overline{\text{D}}$	$V_{IH} - 2600$	$V_{CC} - 1400^*$	$V_{IH} - 150$	$V_{IH} - 2600$	$V_{CC} - 1400^*$	$V_{IH} - 150$	$V_{IH} - 2600$	$V_{CC} - 1400^*$	$V_{IH} - 150$	mV
V_{IH}	Input High Voltage (Single-Ended) R, SEL	-1210		V_{CC}	-1145		V_{CC}	-1085		V_{CC}	mV
V_{IL}	Input Low Voltage (Single-Ended) R, SEL	V_{EE}		-1610	V_{EE}		-1545	V_{EE}		-1485	mV
V_{THR}	Input Threshold Voltage (Single-Ended) (Note 25)	$V_{EE} + 1125$		$V_{CC} - 75$	$V_{EE} + 1125$		$V_{CC} - 75$	$V_{EE} + 1125$		$V_{CC} - 75$	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

20. Input and output parameters vary 1:1 with V_{CC} .

21. All outputs loaded with 50 Ω to $V_{CC} - 2.0\text{ V}$.

22. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

23. V_{IH} cannot exceed V_{CC} . $|V_{IH} - V_{THR}| < 2600\text{ mV}$.

24. V_{IL} always $\geq V_{EE}$. $|V_{IL} - V_{THR}| < 2600\text{ mV}$.

25. V_{THR} is the voltage applied to one input when running in single-ended mode.

*Typicals used for testing purposes.

**When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0\text{ V}$, a 2 k Ω resistor should be connected from OLS to V_{EE} .

***The device packaged in FCBGA-16 have maximum ambient temperature specification of 70°C and devices packaged in QFN-16 have maximum ambient temperature specification of 85°C.

NBSG53A

Table 9. DC CHARACTERISTICS, NECL INPUT WITH NECL OUTPUT

$V_{CC} = 0\text{ V}$; $V_{EE} = -3.465\text{ V}$ to -2.375 V (Note 20) (continued)

Symbol	Characteristic	-40°C			25°C			70°C(BGA)/85°C(QFN)***			Unit		
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 22)	$V_{EE} + 1.2$			0.0	$V_{EE} + 1.2$			0.0	$V_{EE} + 1.2$		0.0	V
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55		Ω	
I_{IH}	Input HIGH Current (@ V_{IH}) R, SEL CLK, $\overline{\text{CLK}}$, D, $\overline{\text{D}}$		35 5	100 50		35 5	100 50		35 5	100 50		μA	
I_{IL}	Input LOW Current (@ V_{IL}) R, SEL CLK, $\overline{\text{CLK}}$, D, $\overline{\text{D}}$		20 5	100 50		20 5	100 50		20 5	100 50		μA	
I_{OLS}	OLS Input Current (See Figure 12) (OLS = V_{CC}) (OLS = $V_{CC} - 0.4\text{ V}$) (OLS = $V_{CC} - 0.8\text{ V}$, OLS = FLOAT) (OLS = $V_{CC} - 1.2\text{ V}$) $-3.465\text{ V} \leq V_{EE} \leq -3.0\text{ V}$ *(OLS = V_{EE}) $-3.0\text{ V} < V_{EE} \leq -2.375\text{ V}$ (OLS = V_{EE})		300 100 5 -300 -1500 -1000	900 300 100 -100 -600 -400		300 100 5 -300 -1500 -1000	900 300 100 -100 -600 -400		300 100 5 -300 -1500 -1000	900 300 100 -100 -600 -400		μA	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

20. Input and output parameters vary 1:1 with V_{CC} .

21. All outputs loaded with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

22. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

23. V_{IH} cannot exceed V_{CC} . $|V_{IH} - V_{THR}| < 2600\text{ mV}$.

24. V_{IL} always $\geq V_{EE}$. $|V_{IL} - V_{THR}| < 2600\text{ mV}$.

25. V_{THR} is the voltage applied to one input when running in single-ended mode.

*Typicals used for testing purposes.

**When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0\text{ V}$, a $2\text{ k}\Omega$ resistor should be connected from OLS to V_{EE} .

***The device packaged in FCBGA-16 have maximum ambient temperature specification of 70°C and devices packaged in QFN-16 have maximum ambient temperature specification of 85°C .

NBSG53A

Table 10. AC CHARACTERISTICS for FCBGA-16

$V_{CC} = 0\text{ V}$; $V_{EE} = -3.465\text{ V to } -2.375\text{ V}$ or $V_{CC} = 2.375\text{ V to } 3.465\text{ V}$; $V_{EE} = 0\text{ V}$

Symbol	Characteristic	-40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{max}	Maximum Frequency (See Figures 4, 6, 8, 10, and 11) DFF		8			8			8		GHz
	(See Figures 5, 7, 9, 10, and 11) (Note 26) DIV/2		10			10			10		
t _{PLH} , t _{PHL}	Propagation Delay to Output Differential CLK→Q, Q̄ (OLS = V _{CC}) (OLS = V _{CC} - 0.4 V) (OLS = V _{CC} - 0.8 V, OLS = FLOAT) **(OLS = V _{EE})	160	210	260	160	215	270	165	220	275	ps
		150	200	250	155	205	255	160	210	260	
		155	205	255	160	210	260	160	215	270	
		155	205	255	160	210	260	160	215	270	
	SEL→Q, Q̄ (OLS = V _{CC}) (OLS = V _{CC} - 0.4 V) (OLS = V _{CC} - 0.8 V, OLS = FLOAT) **(OLS = V _{EE})	165	220	275	170	225	280	170	225	280	
		160	210	260	160	210	260	160	210	260	
		160	215	270	165	220	275	165	220	275	
		160	210	260	160	215	270	165	220	275	
	R→Q, Q̄ (OLS = V _{CC}) DIV/2 (OLS = V _{CC}) DFF (OLS = V _{CC} - 0.4 V) DIV/2 (OLS = V _{CC} - 0.4 V) DFF (OLS = V _{CC} - 0.8 V, OLS = FLOAT) DIV/2 (OLS = V _{CC} - 0.8 V, OLS = FLOAT) DFF **(OLS = V _{EE}) DIV/2 **(OLS = V _{EE}) DFF	220	295	370	225	300	375	225	300	375	
		200	270	340	205	275	345	205	275	345	
		215	285	355	220	290	360	220	290	360	
		195	260	325	200	265	330	200	265	330	
220		290	360	220	295	370	220	295	370		
200		265	330	200	270	340	200	270	340		
215		285	355	220	290	360	220	290	360		
195		260	325	200	265	330	200	265	330		
t _{SKEW}	Duty Cycle Skew (Notes 27 and 29) DFF		5	20		5	20		5	20	ps
t _{JITTER}	RMS Random Clock Jitter f _{in} ≤ 8 GHz (See Figures 4 and 6) (Note 26)		0.5	1.5		0.5	1.5		0.5	1.5	ps
	Peak-to-Peak Data Dependent Jitter f _{in} = 8 Gb/s					TBD					
V _{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 28)	75		2600	75		2600	75		2600	mV
t _r t _f	Output Rise/Fall Times (20% - 80%) @ 1 GHz Q, Q̄ (OLS = V _{CC}) (OLS = V _{CC} - 0.4 V) (OLS = V _{CC} - 0.8 V, OLS = FLOAT) **(OLS = V _{EE})	30	50	65	30	50	65	30	50	65	ps
		20	40	60	20	40	60	20	40	60	
		25	45	65	25	45	65	25	45	65	
		25	45	65	25	45	65	25	45	65	
t _s	Setup Time D→CLK	30	14		30	10		30	13		ps
t _h	Hold Time D→CLK	25	12		25	7		25	9		ps
t _{rr}	Reset Recovery DFF, DIV/2	40	9		40	12		40	10		ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

26. Measured using a 500 mV source, 50% duty cycle clock source. Repetitive 1010 input data pattern. All outputs loaded with 50 Ω to V_{CC} - 2.0 V. Input edge rates is 40 ps (20% - 80%).

27. See Figure 14. t_{SKEW} = |t_{PLH} - t_{PHL}| for a nominal 50% differential clock input waveform.

28. V_{INPP} (MAX) cannot exceed V_{CC} - V_{EE} (Applicable only when V_{CC} - V_{EE} < 2600 mV).

29. See Figure 10. Duty Cycle % vs. Frequency.

**When an output level of 400 mV is desired and V_{CC} - V_{EE} > 3.0 V, a 2 kΩ resistor should be connected from OLS to V_{EE}.

NBSG53A

Table 11. AC CHARACTERISTICS for QFN-16

$V_{CC} = 0\text{ V}$; $V_{EE} = -3.465\text{ V to } -2.375\text{ V}$ or $V_{CC} = 2.375\text{ V to } 3.465\text{ V}$; $V_{EE} = 0\text{ V}$

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (See Figures 4, 6, 8, 10, and 11) DFF (See Figures 5, 7, 9, 10, and 11) (Note 30) DIV/2		8			8			8		GHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential (Note 34) CLK→Q, \bar{Q} SEL→Q, \bar{Q} R→Q, \bar{Q} D _{IN} /2 DFF	150 160 215 195	215 190 280 270	285 280 375 345	150 160 215 195	215 190 280 270	285 280 375 345	150 160 215 195	215 190 280 270	285 280 375 345	ps
t_{SKEW}	Duty Cycle Skew (Notes 31 and 33) DFF		5	20		5	20		5	20	ps
t_{JITTER}	RMS Random Clock Jitter $f_{in} \leq 8\text{ GHz}$ (See Figures 4 and 6) (Note 30) Peak-to-Peak Data Dependent Jitter $f_{in} = 8\text{ Gb/s}$		0.5	1		0.5	1		0.5	1	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 32)	75		2600	75		2600	75		2600	mV
t_r , t_f	Output Rise/Fall Times (20% – 80%) @ 1 GHz Q, \bar{Q} (OLS = V_{CC}) (OLS = $V_{CC} - 0.4\text{ V}$) (OLS = $V_{CC} - 0.8\text{ V}$, OLS = FLOAT) **(OLS = V_{EE})	28 15 25 20	40 40 35 35	65 65 65 65	28 15 25 20	40 40 35 35	65 65 65 65	28 15 25 20	40 40 35 35	65 65 65 65	ps
t_s	Setup Time D→CLK	30	14		30	10		30	13		ps
t_h	Hold Time D→CLK	25	12		25	7		25	0		ps
t_{rr}	Reset Recovery DFF, DIV/2	40	9		40	12		40	10		ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

30. Measured using a 500 mV source, 50% duty cycle clock source. Repetitive 1010 input data pattern. All outputs loaded with 50 Ω to $V_{CC} - 2.0\text{ V}$. Input edge rates is 40 ps (20% – 80%).

31. See Figure 14. $t_{SKEW} = |t_{PLH} - t_{PHL}|$ for a nominal 50% differential clock input waveform.

32. V_{INPP} (MAX) cannot exceed $V_{CC} - V_{EE}$ (Applicable only when $V_{CC} - V_{EE} < 2600\text{ mV}$).

33. See Figure 10. Duty Cycle % vs. Frequency.

34. For all OLS Configuration.

**When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0\text{ V}$, a 2 kΩ resistor should be connected from OLS to V_{EE} .

***The device packaged in FCBGA-16 have maximum ambient temperature specification of 70°C and devices packaged in QFN-16 have maximum ambient temperature specification of 85°C.

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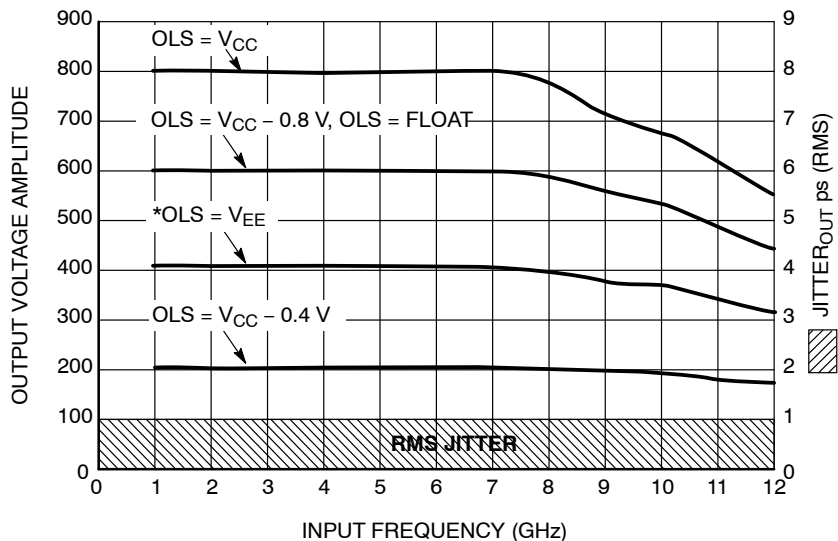


Figure 4. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) for DFF Mode ($V_{CC} - V_{EE} = 3.3\text{ V}$ @ 25°C ; Repetitive 1010 Input Data Pattern)

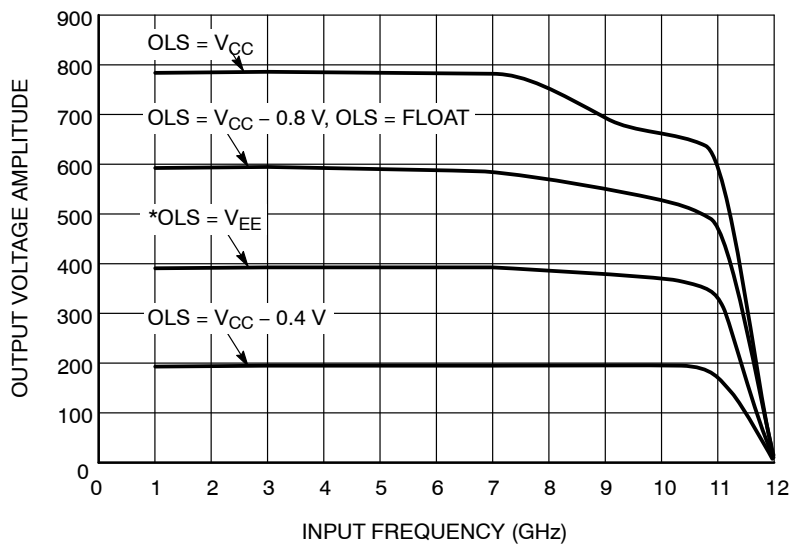


Figure 5. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) for DIV/2 Mode ($V_{CC} - V_{EE} = 3.3\text{ V}$ @ 25°C)

*When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0\text{ V}$, a $2\text{ k}\Omega$ resistor should be connected from OLS to V_{EE} .

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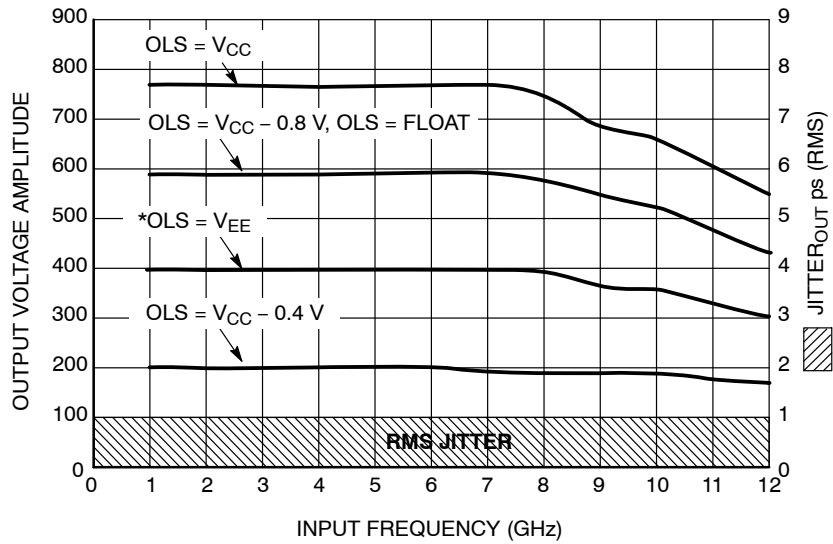


Figure 6. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) for DFF Mode ($V_{CC} - V_{EE} = 2.5\text{ V}$ @ 25°C ; Repetitive 1010 Input Data Pattern)

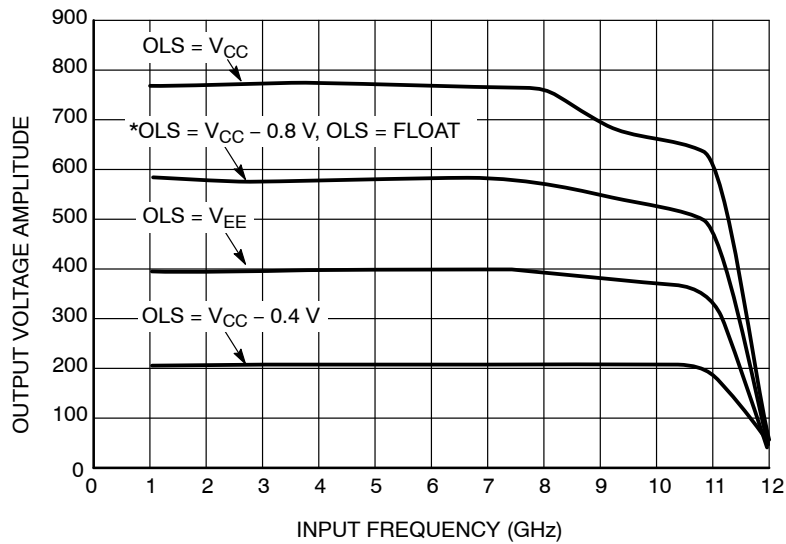


Figure 7. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) for DIV/2 Mode ($V_{CC} - V_{EE} = 2.5\text{ V}$ @ 25°C)

*When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0\text{ V}$, a 2 k Ω resistor should be connected from OLS to V_{EE} .

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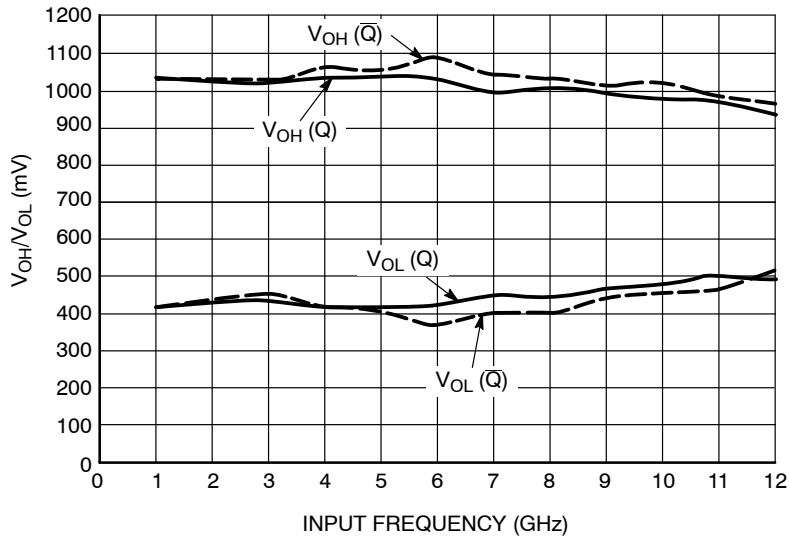


Figure 8. V_{OH}/V_{OL} (Q/Q) vs. Input Frequency (f_{in}) for DFF Mode ($V_{CC} - V_{EE} = 3.3\text{ V}$ @ 25°C and $OLS = V_{CC} - 0.8\text{ V}$, $OLS = \text{FLOAT}$)

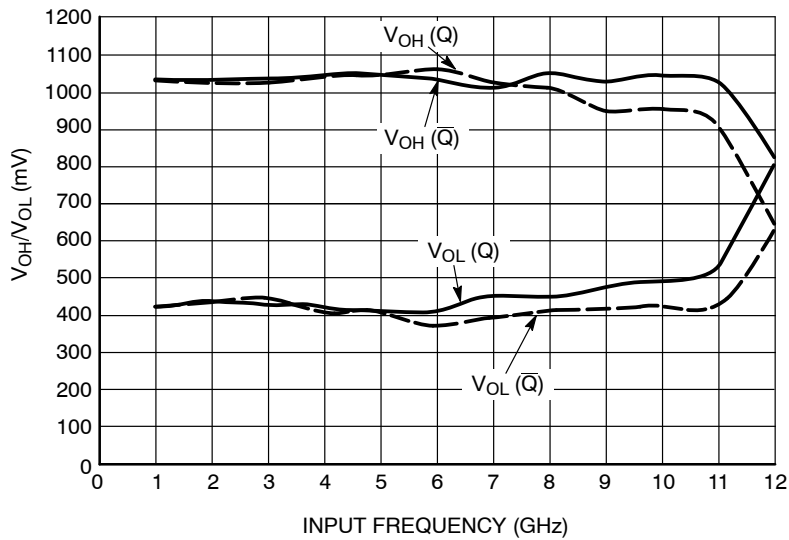


Figure 9. V_{OH}/V_{OL} (Q/Q) vs. Input Frequency (f_{in}) for DIV/2 Mode ($V_{CC} - V_{EE} = 3.3\text{ V}$ @ 25°C and $OLS = V_{CC} - 0.8\text{ V}$, $OLS = \text{FLOAT}$)

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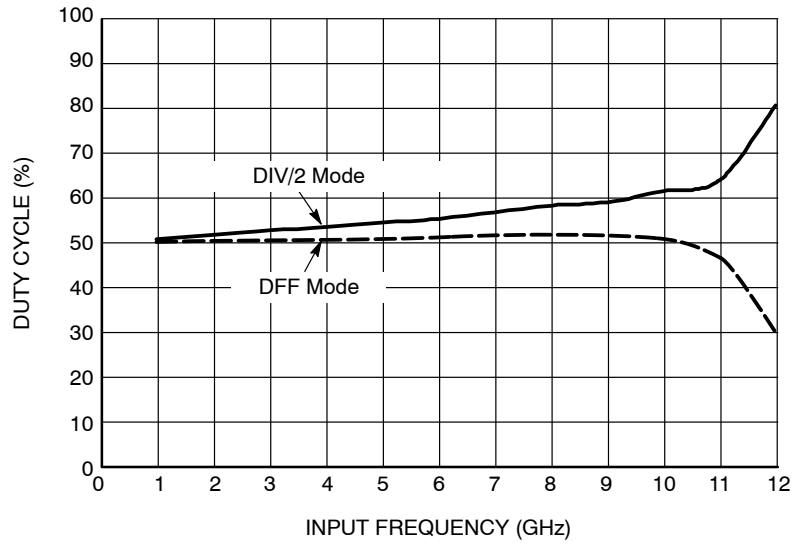


Figure 10. Duty Cycle % vs. Input Frequency (f_{in})
($V_{CC} - V_{EE} = 3.3 \text{ V @ } 25^{\circ}\text{C}$)

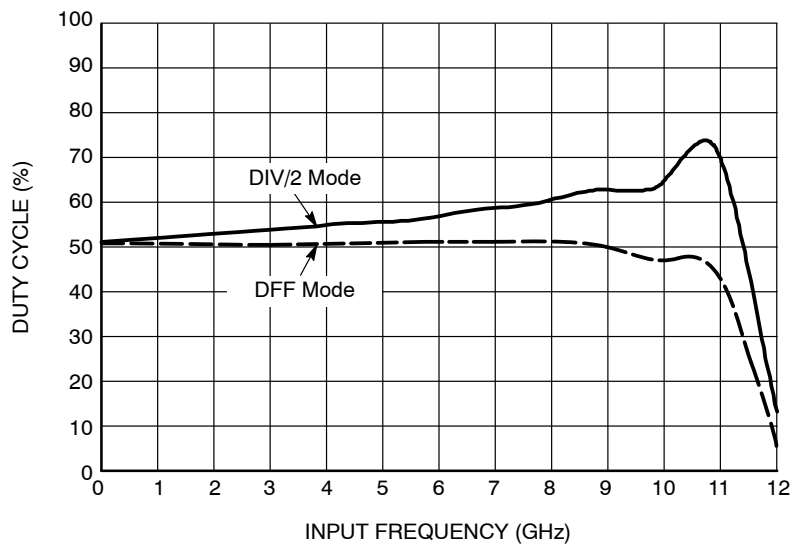


Figure 11. Duty Cycle % vs. Input Frequency (f_{in})
($V_{CC} - V_{EE} = 2.5 \text{ V @ } 70^{\circ}\text{C}$)

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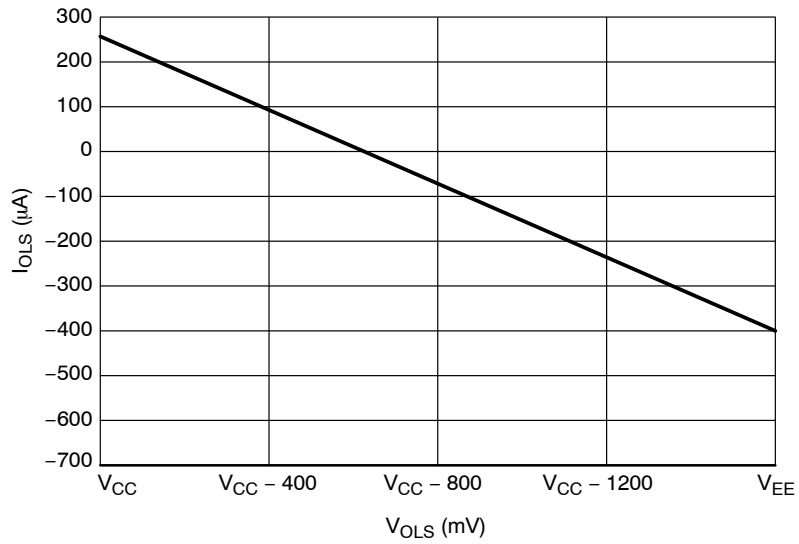


Figure 12. Typical OLS Input Current vs. OLS Input Voltage
 $(V_{CC} - V_{EE} = 3.3 \text{ V @ } 25^\circ\text{C})$

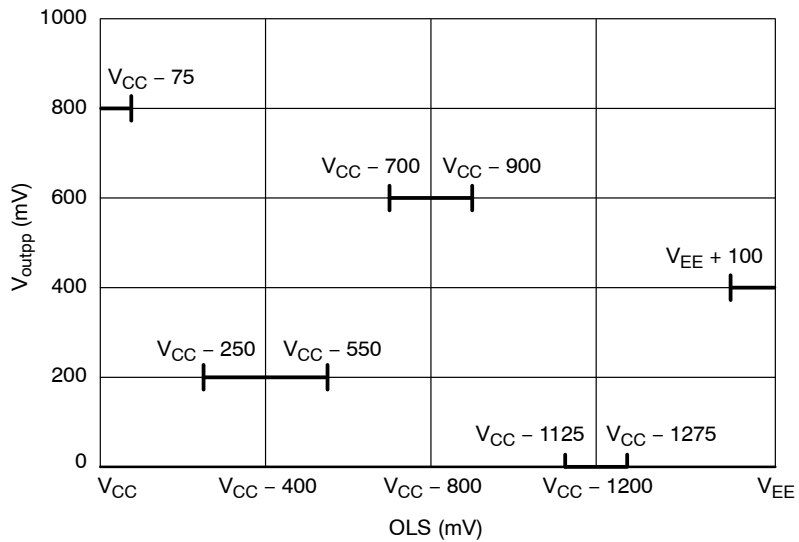


Figure 13. OLS Operating Area

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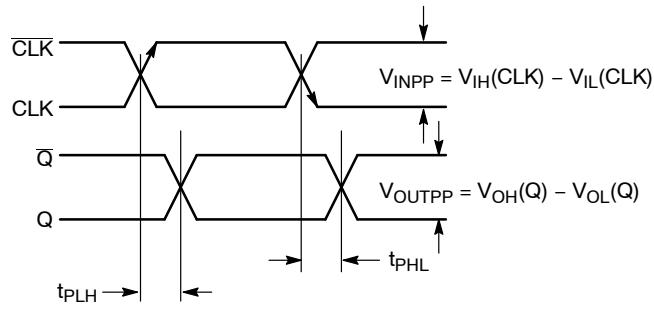


Figure 14. AC Reference Measurement

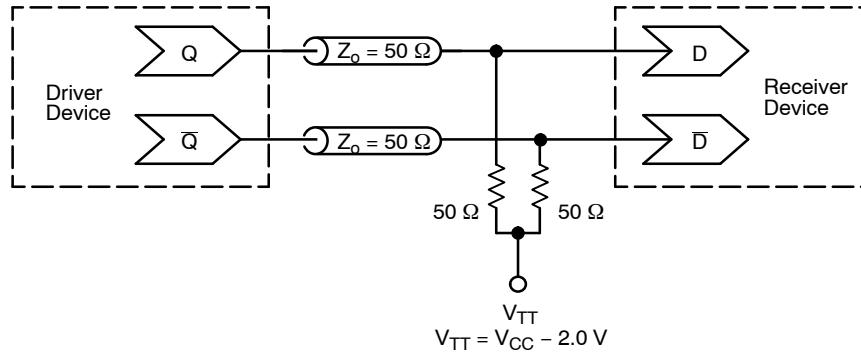


Figure 15. Typical Termination for Output Driver and Device Evaluation
(Refer to Application Note AND8020/D – Termination of ECL Logic Devices)

ORDERING INFORMATION

Device	Package Type	Shipping [†]
NBSG53ABAHTBG	FCBGA-16 (Pb-Free)	100 / Tape & Reel
NBSG53ABA	FCBGA-16, 4x4 mm	100 Units / Tray (Contact Sales Representative)
NBSG53ABAR2	FCBGA-16, 4x4 mm	100 / Tape & Reel (Contact Sales Representative)
NBSG53AMN	QFN-16, 3x3 mm	123 Units / Rail
NBSG53AMNG	QFN-16, 3x3 mm (Pb-Free)	123 Units / Rail
NBSG53AMNR2	QFN-16, 3x3 mm	3000 / Tape & Reel
NBSG53AMNR2G	QFN-16, 3x3 mm (Pb-Free)	3000 / Tape & Reel
NBSG53AMNHTBG	QFN-16 (Pb-Free)	100 / Tape & Reel

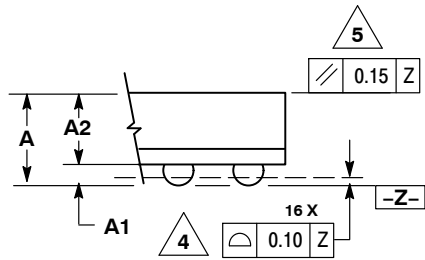
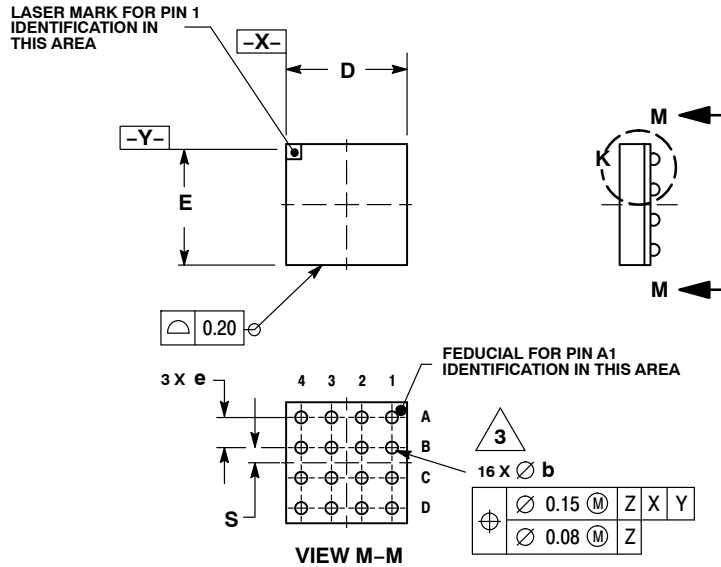
Board	Description
NBSG53ABAEVB	NBSG53ABA Evaluation Board

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NBSG53A

PACKAGE DIMENSIONS

**FCBGA-16
BA SUFFIX**
PLASTIC 4 X 4 (mm) BGA FLIP CHIP PACKAGE
CASE 489-01
ISSUE O



DETAIL K
ROTATED 90° CLOCKWISE

NOTES:

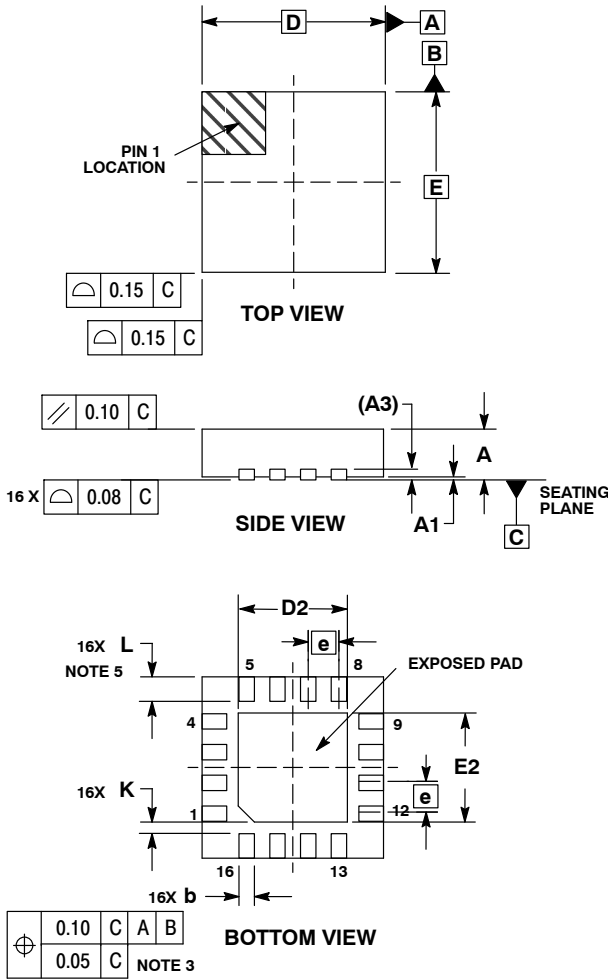
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

MILLIMETERS		
DIM	MIN	MAX
A	1.40	MAX
A1	0.25	0.35
A2	1.20	REF
b	0.30	0.50
D	4.00	BSC
E	4.00	BSC
e	1.00	BSC
S	0.50	BSC

NBSG53A

PACKAGE DIMENSIONS

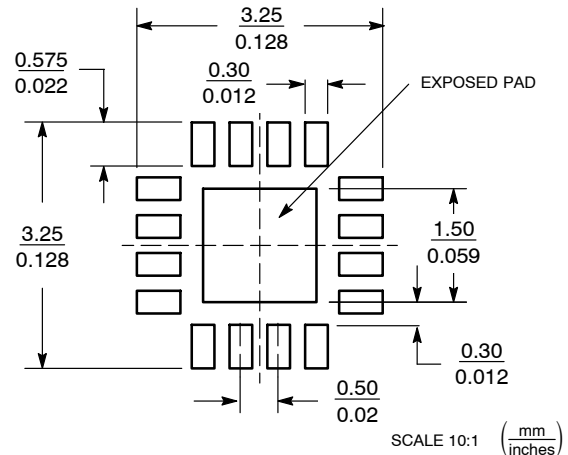
16 PIN QFN
CASE 485G-01
ISSUE C



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
 5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.18 TYP	
L	0.30	0.50

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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