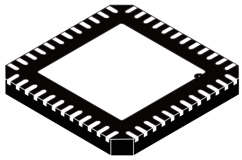
L6208Q

DMOS driver for bipolar stepper motor

Datasheet - production data



VFQFPN48
(7 x 7 mm)

Features

- Operating supply voltage from 8 to 52 V
- 5.6 A output peak current
- $R_{DS(on)}$ 0.3 Ω typ. value at T_j = 25 °C
- Operating frequency up to 100 kHz
- Non-dissipative overcurrent protection
- Dual independent constant t_{OFF} PWM current controllers
- Fast/slow decay synchronous rectification
- Fast decay quasi-synchronous rectification
- Decoding logic for stepper motor full and half step drive
- Cross conduction protection
- Thermal shutdown
- Undervoltage lockout
- Integrated fast freewheeling diodes

Application

- Bipolar stepper motor

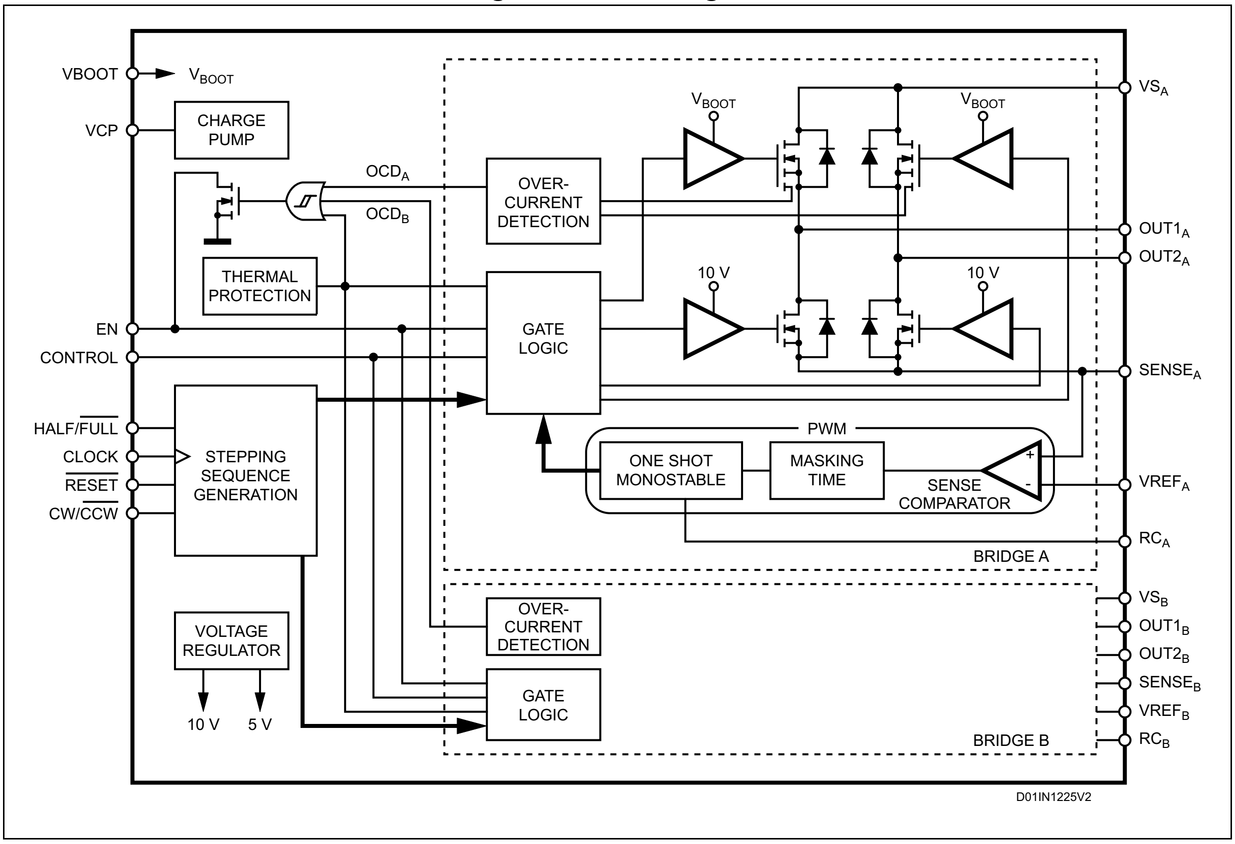
Description

The L6208Q device is a DMOS fully integrated stepper motor driver with non-dissipative overcurrent protection, realized in BCDmultipower technology, which combines isolated DMOS power transistors with CMOS and bipolar circuits on the same chip. The device includes all the circuitry needed to drive a two-phase bipolar stepper motor including: a dual DMOS full bridge, the constant OFF time PWM current controller that performs the chopping regulation, and the phase sequence generator that generates the stepping sequence. Available in a VFQFPN48 7 x 7 mm package, the L6208Q features a non-dissipative overcurrent protection on the high-side Power MOSFETs and thermal shutdown.

Contents

1 Block diagram

Figure 1. Block diagram



2 Electrical data

2.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
V_S	Supply voltage	$V_{SA} = V_{SB} = V_S$	60	V
V_{OD}	Differential voltage between VS_A, $OUT1_A$, $OUT2_A$, $SENSE_A$ and VS_B, $OUT1_B$, $OUT2_B$, $SENSE_B$	$V_{SA} = V_{SB} = V_S = 60$ V; $VSENSE_A = VSENSE_B =$ GND	60	V
V_{BOOT}	Bootstrap peak voltage	$V_{SA} = V_{SB} = V_S$	$V_S + 10$	V
V_{IN},V_{EN}	Input and enable voltage range	-	-0.3 to +7	V
V_{REFA}, V_{REFB}	Voltage range at pins V_{REFA} and V_{REFB}	-	-0.3 to +7	V
V_{RCA}, V_{RCB}	Voltage range at pins RC_A and RC_B	-	-0.3 to +7	V
V_{SENSEA}, V_{SENSEB}	Voltage range at pins $SENSE_A$ and $SENSE_B$	-	-1 to +4	V
$I_{S(peak)}$	Pulsed supply current (for each VS pin), internally limited by the overcurrent protection	$V_{SA} = V_{SB} = V_S$; $t_{PULSE} < 1$ ms	7.1	A
I_S	RMS supply current (for each VS pin)	$VS_A = VS_B = V_S$	2.5	A
T_{stg}, T_{OP}	Storage and operating temperature range	-	-40 to 150	°C

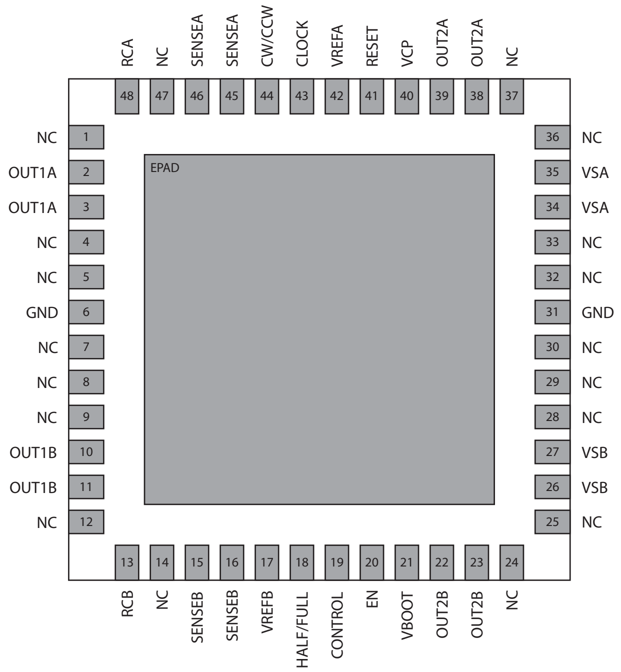
2.2 Recommended operating conditions

Table 2. Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Max.	Unit
V_S	Supply voltage	$V_{SA} = V_{SB} = V_S$	8	52	V
V_{OD}	Differential voltage between VS_A, $OUT1_A$, $OUT2_A$, $SENSE_A$ and VS_B, $OUT1_B$, $OUT2_B$, $SENSE_B$	$V_{SA} = V_{SB} = V_S$; $V_{SENSEA} = V_{SENSEB}$	-	52	V
V_{REFA}, V_{REFB}	Voltage range at pins V_{REFA} and V_{REFB}	-	-0.1	5	V
V_{SENSEA}, V_{SENSEB}	Voltage range at pins $SENSE_A$ and $SENSE_B$	Pulsed $t_W < t_{rr}$	-6	6	V
		DC	-1	1	V
I_{OUT}	RMS output current	-	-	2.5	A
T_j	Operating junction temperature	-	-25	+125	°C
f_{sw}	Switching frequency	-	-a	100	kHz

3 Pin connection

Figure 2.Pin connection (top view)



Note: The exposed PAD must be connected to GND pin.

Table 3. Pin description

Pin	Name	Type	Function
43	CLOCK	Logic input	Step clock input. The state machine makes one step on each rising edge.
44	CW/CCW	Logic input	Selects the direction of the rotation. HIGH logic level sets clockwise direction, whereas low logic level sets counterclockwise direction. If not used, it must be connected to GND or +5 V.
45, 46	$SENSE_A$	Power supply	Bridge A source pin. This pin must be connected to power ground through a sensing power resistor.
48	RC_A	RC pin	RC network pin. A parallel RC network connected between this pin and ground sets the current controller OFF time of bridge A.
2, 3	$OUT1_A$	Power output	Bridge A output 1.
6, 31	GND	GND	Ground terminals. In PowerDIP24 and SO24 packages, these pins are also used for heat dissipation towards the PCB. On PowerSO36 package the slug is connected to these pins.
10, 11	$OUT1_B$	Power output	Bridge B output 1.
13	RC_B	RC pin	RC network pin. A parallel RC network connected between this pin and ground sets the current controller OFF time of bridge B.

Table 3. Pin description (continued)

Pin	Name	Type	Function
15, 16	$SENSE_B$	Power supply	Bridge B source pin. This pin must be connected to power ground through a sensing power resistor.
17	$VREF_B$	Analog input	Bridge B current controller reference voltage. Do not leave this pin open or connected to GND.
18	HALF/ FULL	Logic input	Step mode selector. High logic level sets half step mode, low logic level sets full step mode. If not used, it must be connected to GND or +5 V.
19	CONTROL	Logic input	Decay mode selector. High logic level sets slow decay mode. Low logic level sets fast decay mode. If not used, it must be connected to GND or +5 V.
20	EN	Logic input[(1)]	Chip enable. Low logic level switches off all power MOSFETs of both bridge A and bridge B. This pin is also connected to the collector of the overcurrent and thermal protection to implement overcurrent protection. If not used, it must be connected to +5 V through a resistor.
21	VBOOT	Supply voltage	Bootstrap voltage needed for driving the upper power MOSFETs of both bridge A and bridge B.
22, 23	$OUT2_B$	Power output	Bridge B output 2.
34, 35	VS_A	Power supply	Bridge A power supply voltage. It must be connected to the supply voltage together with pin VS_B.
26, 27	VS_B	Power supply	Bridge B power supply voltage. It must be connected to the supply voltage together with pin VS_A.
38, 39	$OUT2_A$	Power output	Bridge A output 2.
40	VCP	Output	Charge pump oscillator output.
41	RESET	Logic input	Reset pin. Low logic level restores the home state (state 1) on the phase sequence generator state machine. If not used, it must be connected to +5 V.
42	$VREF_A$	Analog input	Bridge A current controller reference voltage. Do not leave this pin open or connected to GND.

1. Also connected at the output drain of the overcurrent and thermal protection MOSFET. Therefore, it must be driven putting in series a resistor with a value in the range of 2.2 kΩ - 180 kΩ, recommended 100 kΩ.

4 Electrical characteristics

V_S = 48 V, T_A = 25 °C, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{Sth(ON)}$	Turn-on threshold	-	6.6	7	7.4	V
$V_{Sth(OFF)}$	Turn-off threshold	-	5.6	6	6.4	V
I_S	Quiescent supply current	All bridges OFF; T_j = -25 °C to 125 °C(1)	-	5	10	mA
$T_{j(OFF)}$	Thermal shutdown temperature	-	-	165	-	°C
Output DMOS transistors						
$R_{DS(ON)}$	High-side switch ON resistance	T_j = 25 °C	-	0.34	0.4	Ω
		T_j = 125 °C(1)	-	0.53	0.59	
	Low-side switch ON resistance	T_j = 25 °C	-	0.28	0.34	
		T_j = 125 °C(1)	-	0.47	0.53	
I_{DSS}	Leakage current	EN = low; OUT = V_S	-	-	2	mA
		EN = low; OUT = GND	-0.15	-	-	mA
Source drain diodes						
V_{SD}	Forward ON voltage	I_{SD} = 2.5 A, EN = low	-	1.15	1.3	V
t_{rr}	Reverse recovery time	I_f = 2.5 A	-	300	-	ns
t_{fr}	Forward recovery time	-	-	200	-	ns
Logic input (EN, CONTROL, HALF/FULL, CLOCK, RESET, CW/CCW)						
V_{IL}	Low level logic input voltage	-	-0.3	-	0.8	V
V_{IH}	High level logic input voltage	-	2	-	7	V
I_{IL}	Low level logic input current	GND logic input voltage	-10	-		µA
I_{IH}	High level logic input current	7 V logic input voltage	-	-	10	µA
$V_{th(ON)}$	Turn-on input threshold	-	-	1.8	2.0	V
$V_{th(OFF)}$	Turn-off input threshold	-	0.8	1.3	-	V
$V_{th(HYS)}$	Input threshold hysteresis	-	0.25	0.5	-	V
Switching characteristics						
$t_{D(on)EN}$	Enable to out turn ON delay time(2)	I_{LOAD} = 2.5 A, resistive load	100	250	400	ns
$t_{D(off)EN}$	Enable to out turn OFF delay time(2)	I_{LOAD} = 2.5 A, resistive load	300	550	800	ns
t_{RISE}	Output rise time(2)	I_{LOAD} = 2.5 A, resistive load	40	-	250	ns
t_{FALL}	Output fall time(2)	I_{LOAD} = 2.5 A, resistive load	40	-	250	ns
t_{DCLK}	Clock to output delay time(3)	I_{LOAD} = 2.5 A, resistive load	-	2	-	µs

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{CLK(min)L}$	Minimum clock time(4)	-	-	-	1	µs
$t_{CLK(min)H}$	Minimum clock time(4)	-	-	-	1	µs
f_{CLK}	Clock frequency	-	-	-	100	kHz
$t_{S(MIN)}$	Minimum setup time(5)	-	-	-	1	µs
$t_{H(MIN)}$	Minimum hold time(5)	-	-	-	1	µs
$t_{R(MIN)}$	Minimum reset time(5)	-	-	-	1	µs
$t_{RCLK(MIN)}$	Minimum reset to clock delay time(5)	-	-	-	1	µs
t_{DT}	Deadtime protection	-	0.5	1	-	µs
f_{CP}	Charge pump frequency	T_j = -25 °C to 125 °C(7)	-	0.6	1	MHz
t_{DT}	Deadtime protection	-	0.5	1	-	µs
f_{CP}	Charge pump frequency	-25 °C < T_j < 125 °C	-	0.6	1	MHz
PWM comparator and monostable						
I_{RCA}, I_{RCB}	Source current at pins RCA and RCB	$V_{RCA} = V_{RCB}$ = 2.5 V	3.5	5.5	-	mA
V_{offset}	Offset voltage on sense comparator	V_{REFA}, V_{REFB} = 0.5 V	-	±5	-	mV
t_{PROP}	Turn OFF propagation delay(6)	-	-	500	-	ns
t_{BLANK}	Internal blanking time on SENSE pins	-	-	1	-	µs
$t_{ON(MIN)}$	Minimum ON time	-	-	1.5	2	µs
t_{OFF}	PWM recirculation time	R_{OFF} = 20 kΩ; C_{OFF} = 1 nF	-	13	-	µs
		R_{OFF} = 100 kΩ; C_{OFF} = 1 nF	-	61	-	µs
I_{BIAS}	Input bias current at pins $VREF_A$ and $VREF_B$	-	-	-	10	µA
Overcurrent detection						
I_{sover}	Input supply overcurrent detection threshold	-25 °C < T_j < 125 °C	4	5.6	7.1	A
R_{OPDR}	Open drain ON resistance	I = 4 mA	-	40	60	Ω
$t_{OCD(ON)}$	OCD turn-on delay time (7)	I = 4 mA; C_{EN} < 100 pF	-	200	-	ns
$t_{OCD(OFF)}$	OCD turn-off delay time (7)	I = 4 mA; C_{EN} < 100 pF	-	100	-	ns

1. Tested at 25 °C in a restricted range and guaranteed by characterization.
2. See *Figure 3*.
3. See *Figure 4*.
4. See *Figure 5*.
5. See *Figure 6*.
6. Measured applying a voltage of 1 V to pin SENSE and a voltage drop from 2 V to 0 V to pin V_{REF}.
7. See *Figure 7*.

Figure 3. Switching characteristic definition

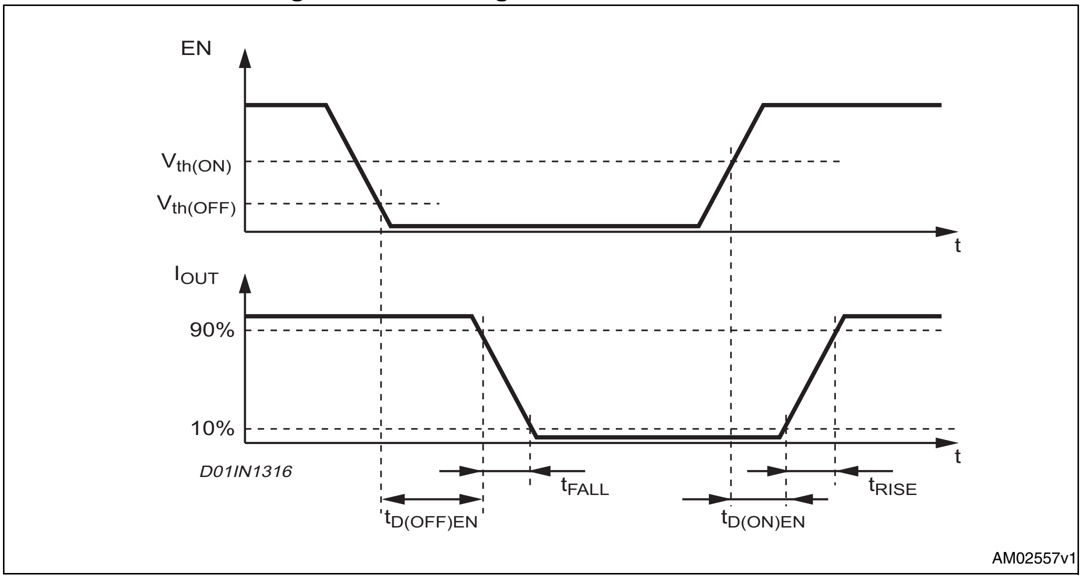


Figure 4. Clock to output delay time

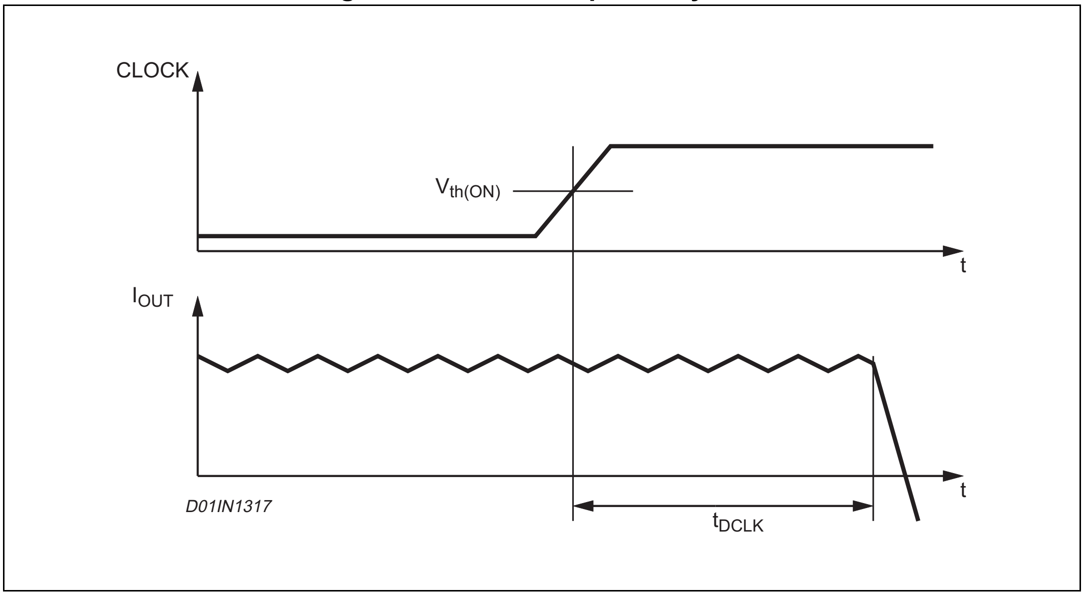


Figure 5. Minimum timing definition; clock input

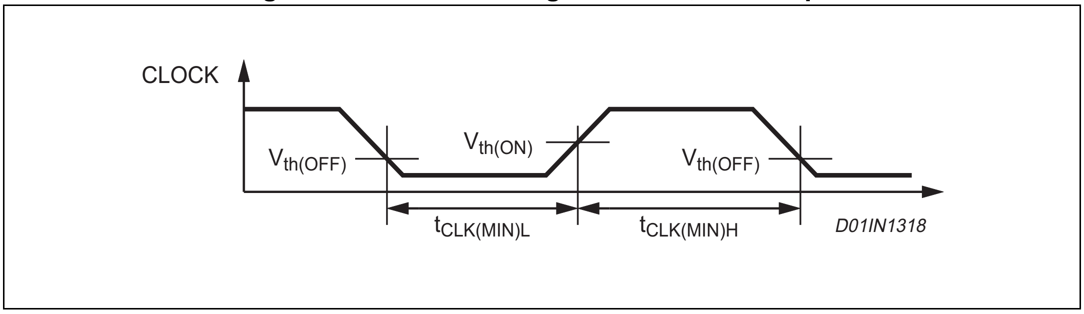


Figure 6. Minimum timing definition; logic inputs

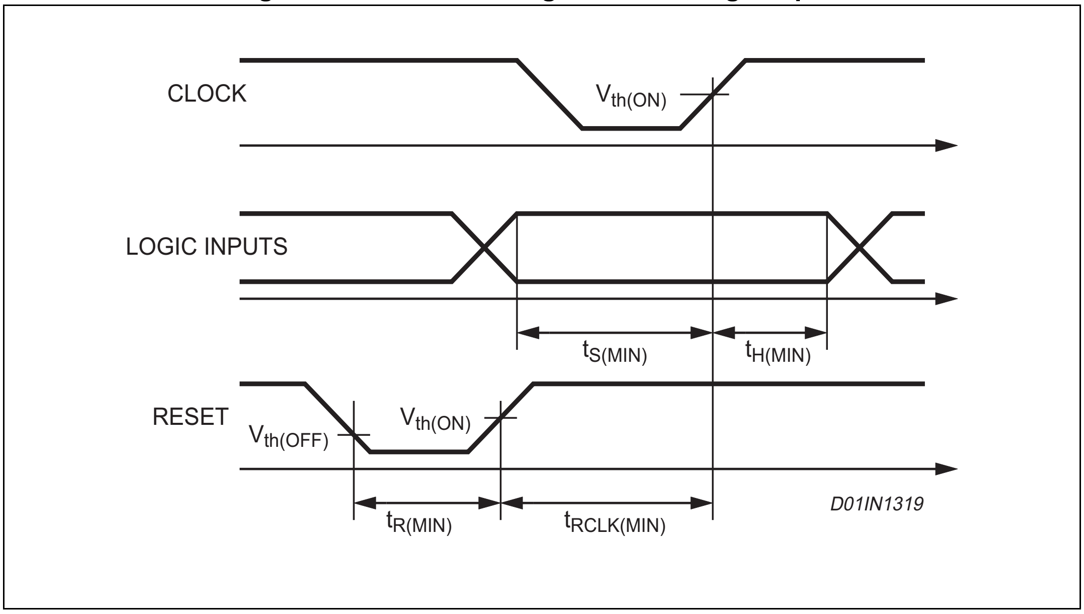
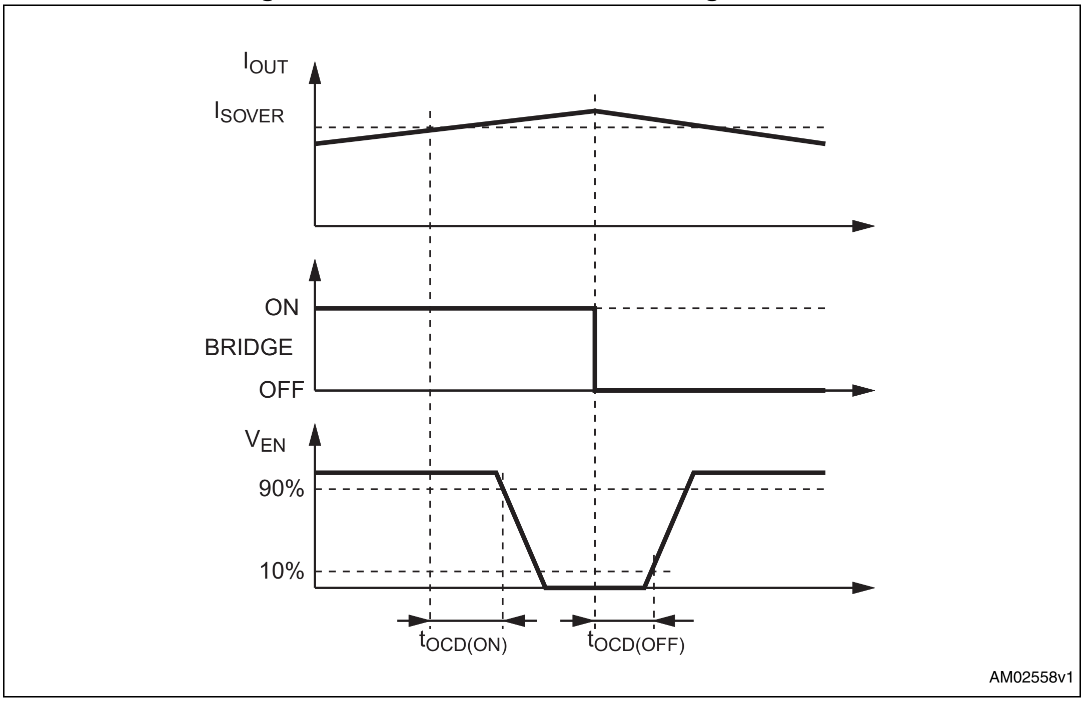


Figure 7. Overcurrent detection timing definition



5 Circuit description

5.1 Power stages and charge pump

The L6208Q device integrates two independent power MOSFET full bridges, each power MOSFET has an $R_{DS(ON)}$ = 0.3 Ω (typical value at 25 °C) with intrinsic fast freewheeling diode. Cross conduction protection is implemented by using a deadtime (t_{DT} = 1 µs typical value) set by internal timing circuit between the turn-off and turn-on of two power MOSFETs in one leg of a bridge.

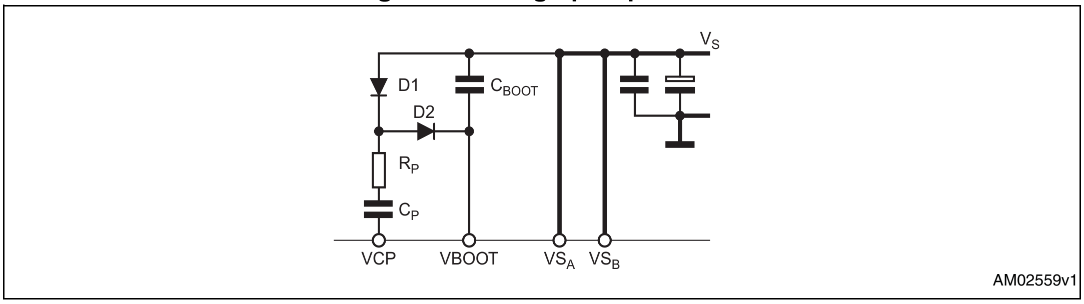
Pins VS_A and VS_B must be connected together to the supply voltage (V_S).

Using an N-channel power MOSFET for the upper transistors in the bridge requires a gate drive voltage above the power supply voltage. The bootstrapped supply (V_{BOOT}) is obtained through an internal oscillator and a few external components to realize a charge pump circuit, as shown in *Figure 8*. The oscillator output (pin VCP) is a square wave at 600 kHz (typically) with 10 V amplitude. Recommended values/part numbers for the charge pump circuit are shown in *Table 5*.

Table 5. Charge pump external component values

Component	Value
C_{BOOT}	220 nF
C_P	10 nF
R_P	100 Ω
D1	1N4148
D2	1N4148

Figure 8. Charge pump circuit



5.2 Logic inputs

Pins CONTROL, HALF/FULL, CLOCK, RESET and CW/CCW are TTL/CMOS and µC compatible logic inputs. The internal structure is shown in *Figure 9*. Typical values for turn-on and turn-off thresholds are respectively $V_{th(ON)}$ = 1.8 V and $V_{th(OFF)}$ = 1.3 V.

Pin EN (Enable) has identical input structure with the exception that the drain of the overcurrent and thermal protection MOSFET is also connected to this pin. Due to this connection, some care must be taken in driving this pin. The EN input may be driven in one of two configurations, as shown in *Figure 10* or *11*. If driven by an open drain (collector) structure, a pull-up resistor R_{EN} and a capacitor C_{EN} are connected, as shown in *Figure 10*. If the driver is a standard push-pull structure, the resistor R_{EN} and the capacitor C_{EN} are connected, as shown in *Figure 11*. The resistor R_{EN} should be chosen in the range from 2.2 kΩ to 180 kΩ. Recommended values for R_{EN} and C_{EN} are respectively 100 kΩ and 5.6 nF. More information on selecting the values is found in *Section 5.9*.

Figure 9. Logic inputs internal structure

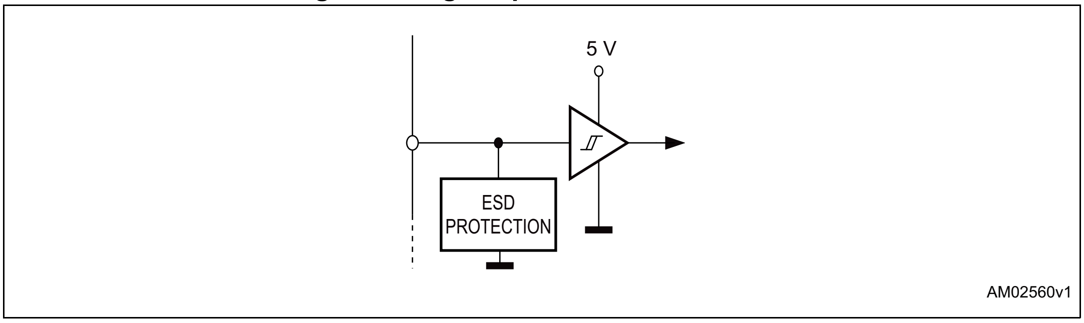


Figure 10. EN pins open collector driving

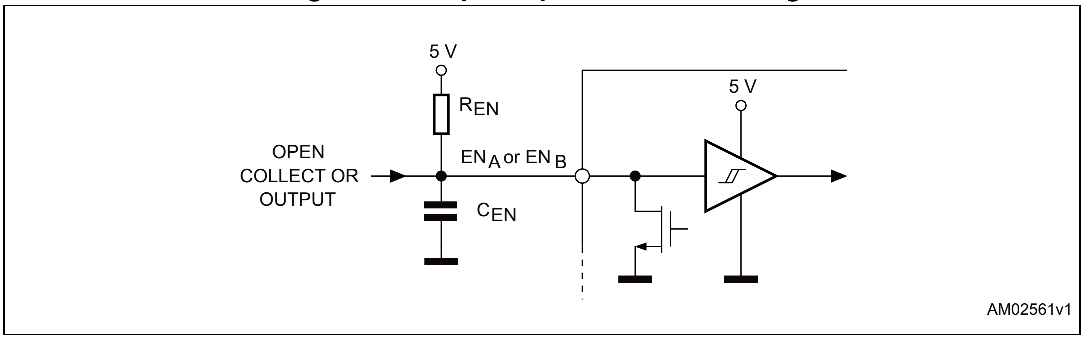
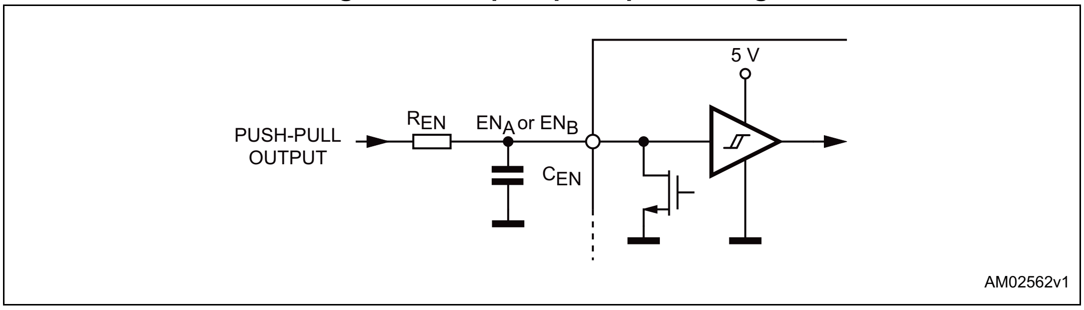


Figure 11. EN pins push-pull driving



5.3 PWM current control

The L6208Q device includes a constant OFF time PWM current controller for each of the two bridges. The current control circuit senses the bridge current by sensing the voltage drop across an external sense resistor connected between the source of the two lower power MOSFET transistors and ground, as shown in *Figure 12.* As the current in the load builds up, the voltage across the sense resistor increases proportionally. When the voltage drop across the sense resistor becomes greater than the voltage at the reference input ($VREF_A$ or $VREF_B$), the sense comparator triggers the monostable switching the low-side MOSFET off. The low-side MOSFET remains off for the time set by the monostable and the motor current recirculates in the upper path. When the monostable times out, the bridge again turns on. As the internal deadtime, used to prevent cross conduction in the bridge, delays the turn-on of the power MOSFET, the effective OFF time is the sum of the monostable time plus the deadtime.

Figure 12. PWM current controller simplified schematic

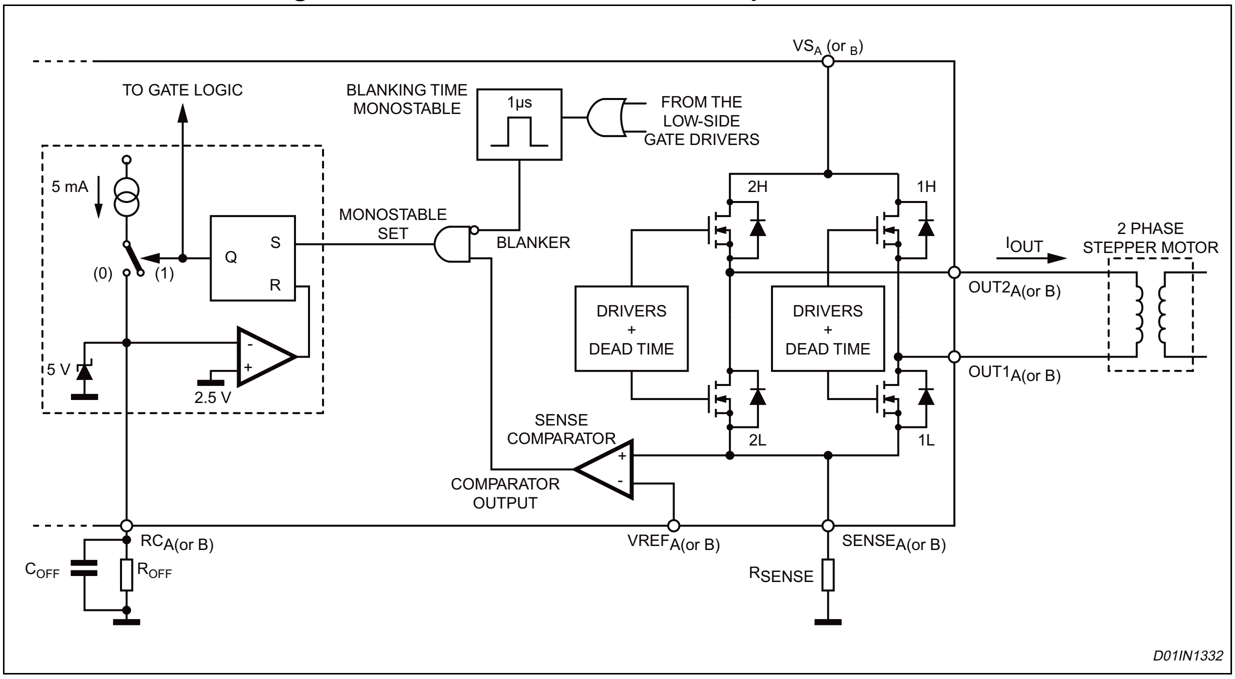


Figure 13 shows the typical operating waveforms of the output current, the voltage drop across the sensing resistor, the RC pin voltage and the status of the bridge. More details regarding the Synchronous Rectification and the output stage configuration are included in *Section 5.4*.

Immediately after the low-side Power MOSFET turns on, a high peak current flows through the sensing resistor due to the reverse recovery of the freewheeling diodes. The L6208Q device provides a 1 µs blanking time t_{BLANK} that inhibits the comparator output so that this current spike cannot prematurely re-trigger the monostable.

Figure 13. Output current regulation waveforms

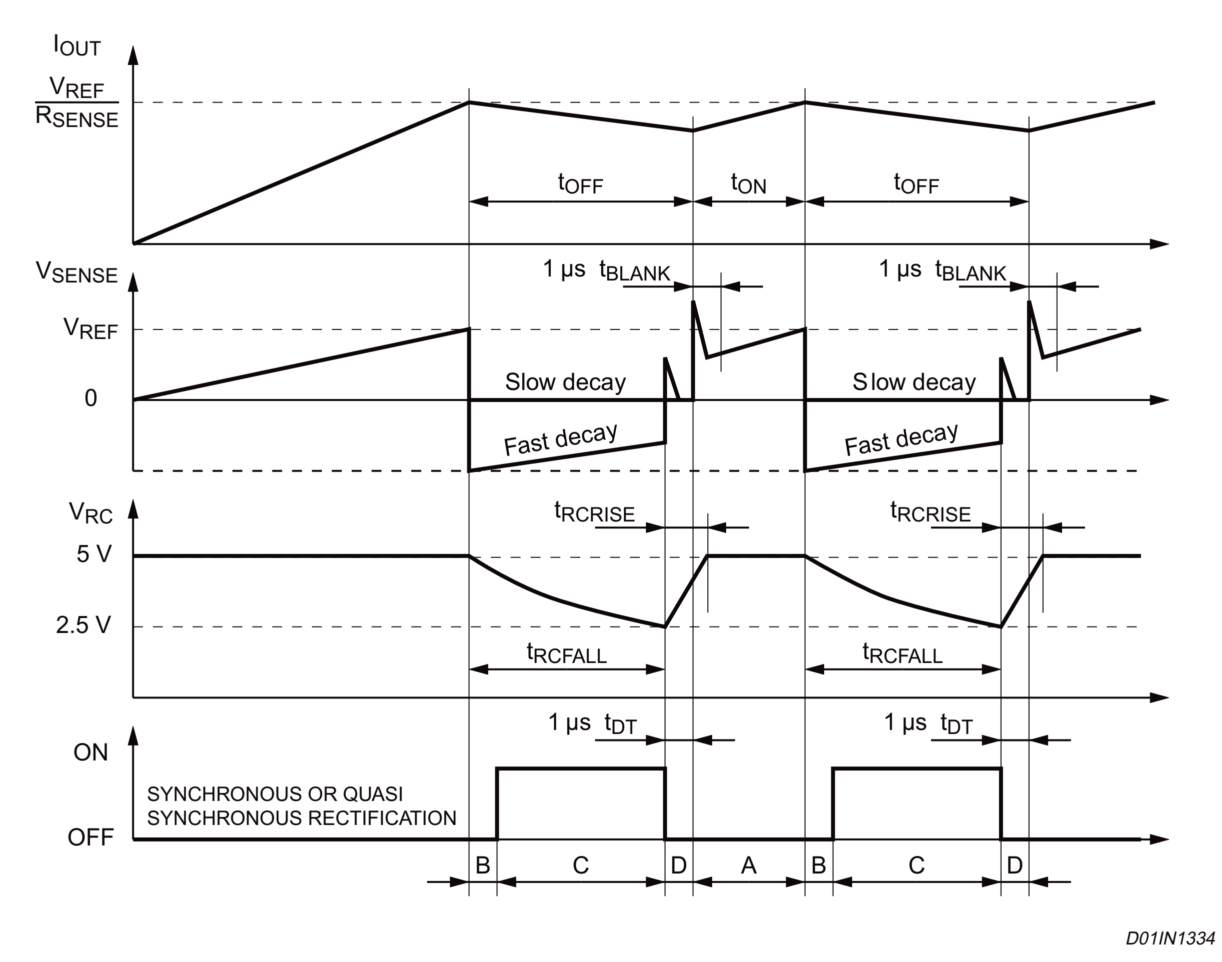


Figure 14 shows the magnitude of the OFF time t_{OFF} versus C_{OFF} and R_{OFF} values. It can be approximately calculated from *Equation 1* and *Equation 2*:

Equation 1

$$t_{RCFALL} = 0.6 \cdot R_{OFF} \cdot C_{OFF}$$

$$t_{OFF} = t_{RCFALL} + t_{DT} = 0.6 \cdot R_{OFF} \cdot C_{OFF} + t_{DT}$$

where R_{OFF} and C_{OFF} are the external component values and t_{DT} is the internally generated deadtime with:

Equation 2

$$20\ k\Omega \le R_{OFF} \le 100\ k\Omega$$

$$0.47\ nF \le C_{OFF} \le 100\ nF$$

$$t_{DT} = 1\ \mu s\ \text{(typical value)}$$

therefore:

Equation 3

$$t_{OFF(MIN)} = 6.6\ \mu s$$

$$t_{OFF(MAX)} = 6\ ms$$

These values allow a sufficient range of t_{OFF} to implement the drive circuit for most motors.

The capacitor value chosen for C_{OFF} also affects the rise time t_{RCRISE} of the voltage at the pin R_{COFF}. The rise time t_{RCRISE} is only an issue if the capacitor is not completely charged before the next time the monostable is triggered. Therefore, the ON time t_{ON}, which depends on motors and supply parameters, must be bigger than t_{RCRISE} to allow a good current regulation by the PWM stage. Furthermore, the ON time t_{ON} can not be smaller than the minimum ON time $t_{ON(MIN)}$.

Equation 4

$$\begin{cases} t_{ON} > t_{ON(MIN)} \\ t_{ON} > t_{RCRISE} - t_{DT} \end{cases} = 1.5\mu s(typ)$$

$$t_{RCRISE} = 600 \cdot C_{OFF}$$

Figure 15 shows the lower limit for the ON time t_{ON} for having a good PWM current regulation capacity. It should be mentioned that t_{ON} is always bigger than $t_{ON(MIN)}$ because the device imposes this condition, but it can be smaller than t_{RCRISE} - t_{DT}. In this last case the device continues to work but the OFF time t_{OFF} is not more constant.

Therefore, a small C_{OFF} value gives more flexibility to the applications (allows smaller ON time and, therefore, higher switching frequency), but, the smaller the value for C_{OFF}, the more influential the noises on the circuit performance.

Figure 14. t_{OFF} vs. C_{OFF} and R_{OFF}

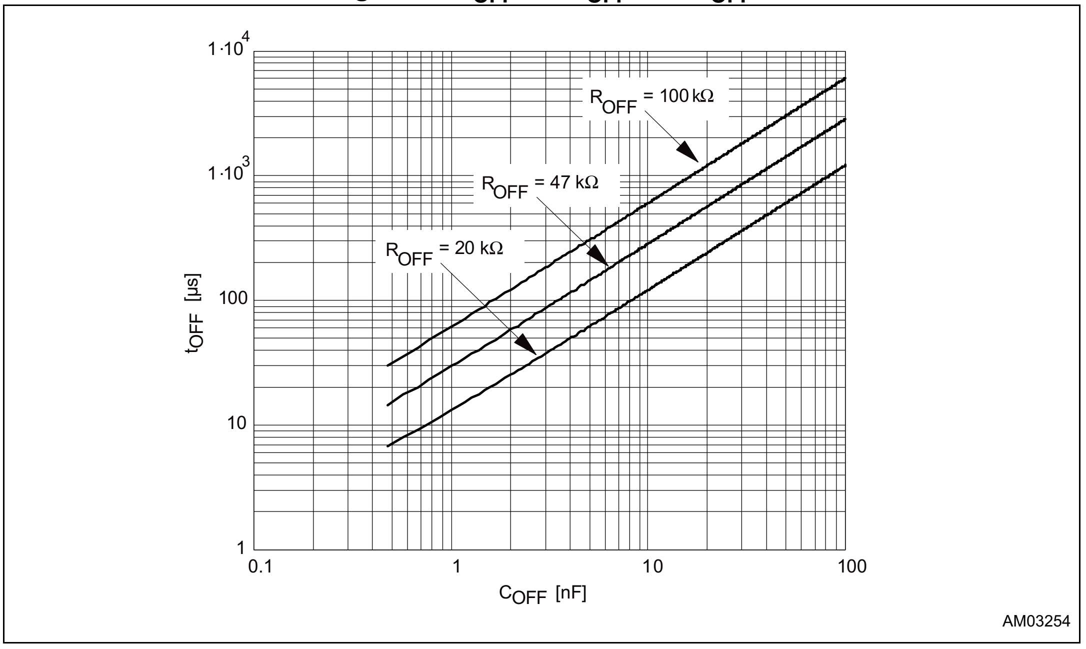
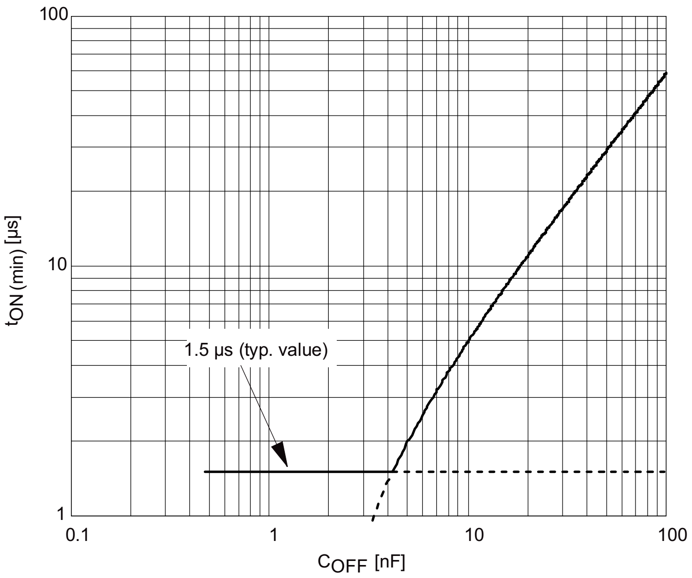


Figure 15. Area where t_{ON} can vary maintaining the PWM regulation



5.4 Decay mode

The CONTROL input is used to select the behavior of the bridge during the OFF time. When the CONTROL pin is low, the fast decay mode is selected and both transistors in the bridge are switched off during the OFF time. When the CONTROL pin is high, the slow decay mode is selected and only the low-side transistor of the bridge is switched off during the OFF time. *Figure 16* shows the operation of the bridge in fast decay mode. At the start of the OFF time, both of the power MOSFETs are switched off and the current recirculates through the two opposite freewheeling diodes. The current decays with a high di/dt since the voltage across the coil is essentially the power supply voltage. After the deadtime, the lower power MOSFET in parallel with the conducting diode is turned on in synchronous rectification mode. In applications where the motor current is low, it is possible that the current may decay completely to zero during the OFF time. At this point, if both of the power MOSFETs were operating in the synchronous rectification mode, it would then be possible for the current to build in the opposite direction. To prevent this only the lower power MOSFET is operated in synchronous rectification mode. This operation is called quasi-synchronous rectification mode. When the monostable times out, the power MOSFETs are turned on again after some delay set by the deadtime to prevent cross conduction.

Figure 17 shows the operation of the bridge in slow decay mode. At the start of the OFF time, the lower power MOSFET is switched off and the current recirculates around the upper half of the bridge. Since the voltage across the coil is low, the current decays slowly. After the deadtime the upper power MOSFET is operated in the synchronous rectification mode. When the monostable times out, the lower power MOSFET is turned on again after some delay set by the deadtime to prevent cross conduction.

Figure 16. Fast decay mode output stage configurations

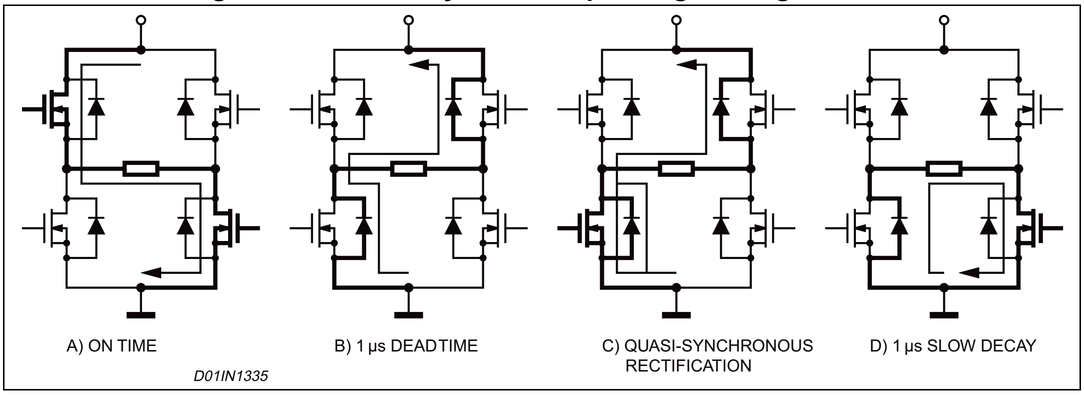
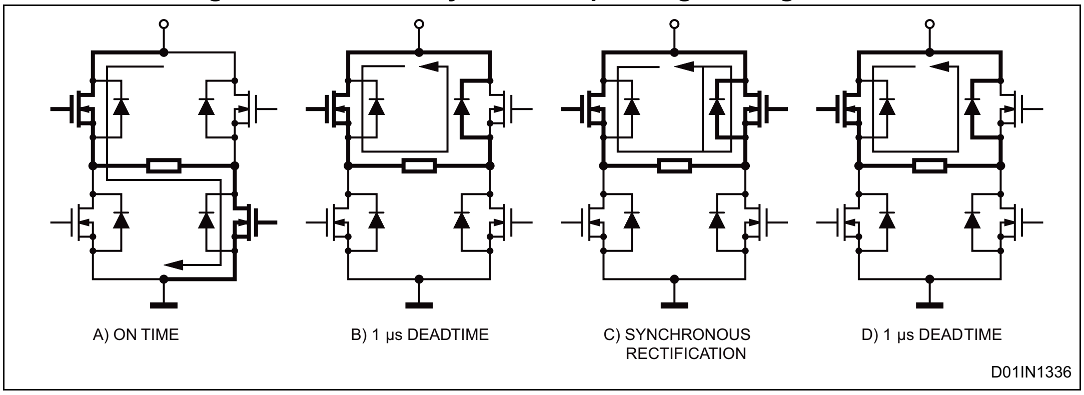


Figure 17. Slow decay mode output stage configurations



5.5 Stepping sequence generation

The phase sequence generator is a state machine that provides the phase and enable inputs for the two bridges to drive a stepper motor in either full step or half step. Two full step modes are possible, the normal drive mode where both phases are energized at each step and the wave drive mode where only one phase is energized at a time. The drive mode is selected by the HALF/FULL input and the current state of the sequence generator, as described below. A rising edge of the CLOCK input advances the state machine to the next state. The direction of rotation is set by the CW/CCW input. The RESET input resets the state machine to state.

5.6 Half step mode

A HIGH logic level on the HALF/FULL input selects half step mode. *Figure 18* shows the motor current waveforms and the state diagram for the phase sequencer generator. At startup or after a RESET the phase sequencer is at state 1. After each clock pulse the state changes following the sequence 1, 2, 3, 4, 5, 6, 7, 8, etc. if CW/CCW is high (clockwise movement) or 1, 8, 7, 6, 5, 4, 3, 2, etc. if CW/CCW is low (counterclockwise movement).

5.7 Normal drive mode (full step two-phase-on)

A low level on the HALF/FULL input selects the full step mode. When the low level is applied, when the state machine is at an ODD numbered state, normal drive mode is selected. *Figure 19* shows the motor current waveform state diagram for the state machine of the phase sequencer generator. Normal drive mode can easily be selected by holding the HALF/FULL input low and applying a RESET. At startup or after a RESET the state machine is in state 1. While, when the HALF/FULL input is kept low, the state changes following the sequence 1, 3, 5, 7, etc. if CW/CCW is high (clockwise movement) or 1, 7, 5, 3, etc. if CW/CCW is low (counterclockwise movement).

5.8 Wave drive mode (full step one-phase-on)

A low level on the pin HALF/FULL input selects the full step mode. When the low level is applied, when the state machine is at an EVEN numbered state, the wave drive mode is selected. *Figure 20* shows the motor current waveform and the state diagram for the state machine of the phase sequence generator. To enter wave drive mode the state machine must be in an EVEN numbered state. The most direct method to select the wave drive mode is to first apply a RESET, then while keeping the HALF/FULL input high, apply one pulse to the clock input, then take the HALF/FULL input low. This sequence first forces the state machine to state 1. The clock pulse, with the HALF/FULL input high, advances the state machine from state 1 to either state 2 or 8 depending on the CW/CCW input. Starting from this point, each clock pulse (rising edge) advances the state machine following the sequence 2, 4, 6, 8, etc. if CW/CCW is high (clockwise movement) or 8, 6, 4, 2, etc. if CW/ CCW is low (counterclockwise movement).

Figure 18. Half step mode

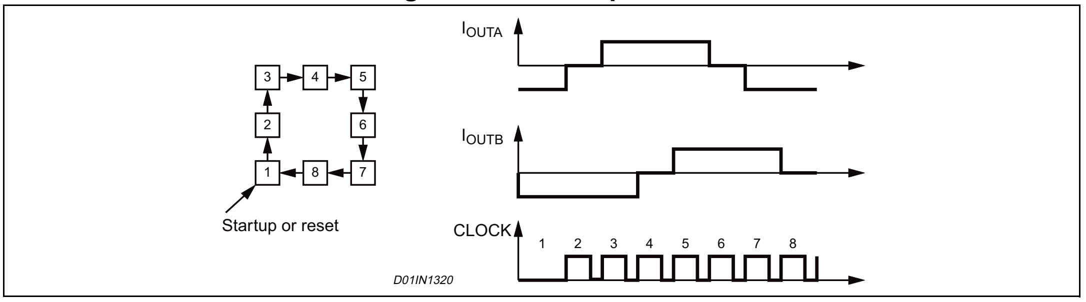


Figure 19. Normal drive mode

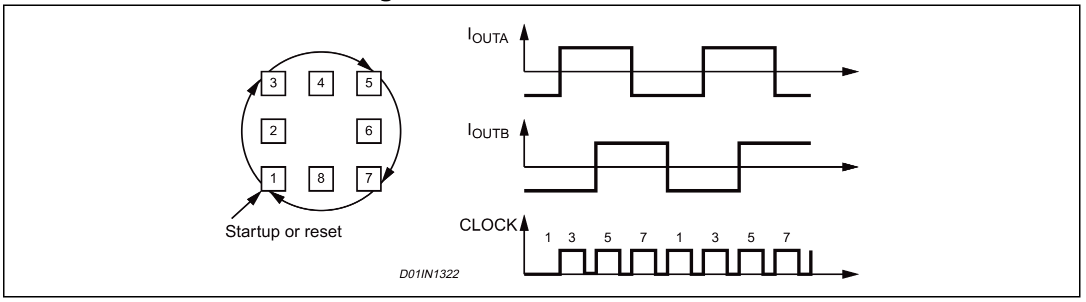
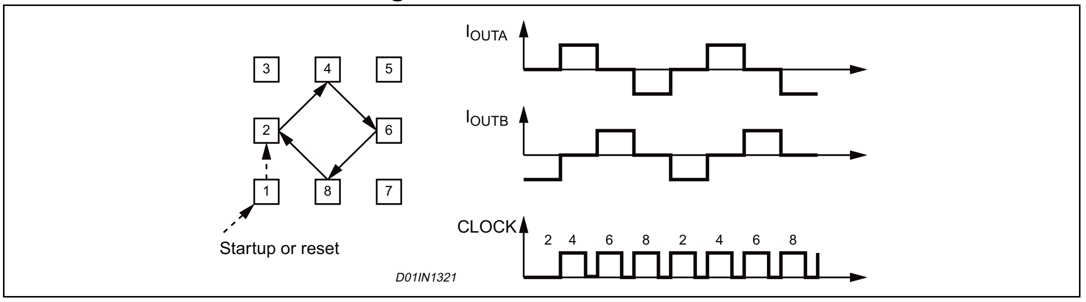


Figure 20. Wave drive mode



5.9 Non-dissipative overcurrent detection and protection

The L6208Q device integrates an overcurrent detection circuit (OCD). With this internal overcurrent detection, the external current sense resistor normally used and its associated power dissipation are eliminated. *Figure 21* shows a simplified schematic of the overcurrent detection circuit.

To implement overcurrent detection, a sensing element that delivers a small but precise fraction of the output current is implemented with each high-side power MOSFET. Since this current is a small fraction of the output current, there is very little additional power dissipation. This current is compared with an internal reference current I_{REF}. When the output current reaches the detection threshold (typically 5.6 A), the OCD comparator signals a fault condition. When a fault condition is detected, the EN pin is pulled below the turn-off threshold (1.3 V typical) by an internal open drain MOSFET with a pull-down capability of 4 mA. By using an external R-C on the EN pin, the OFF time before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs.

Figure 21. Overcurrent protection simplified schematic

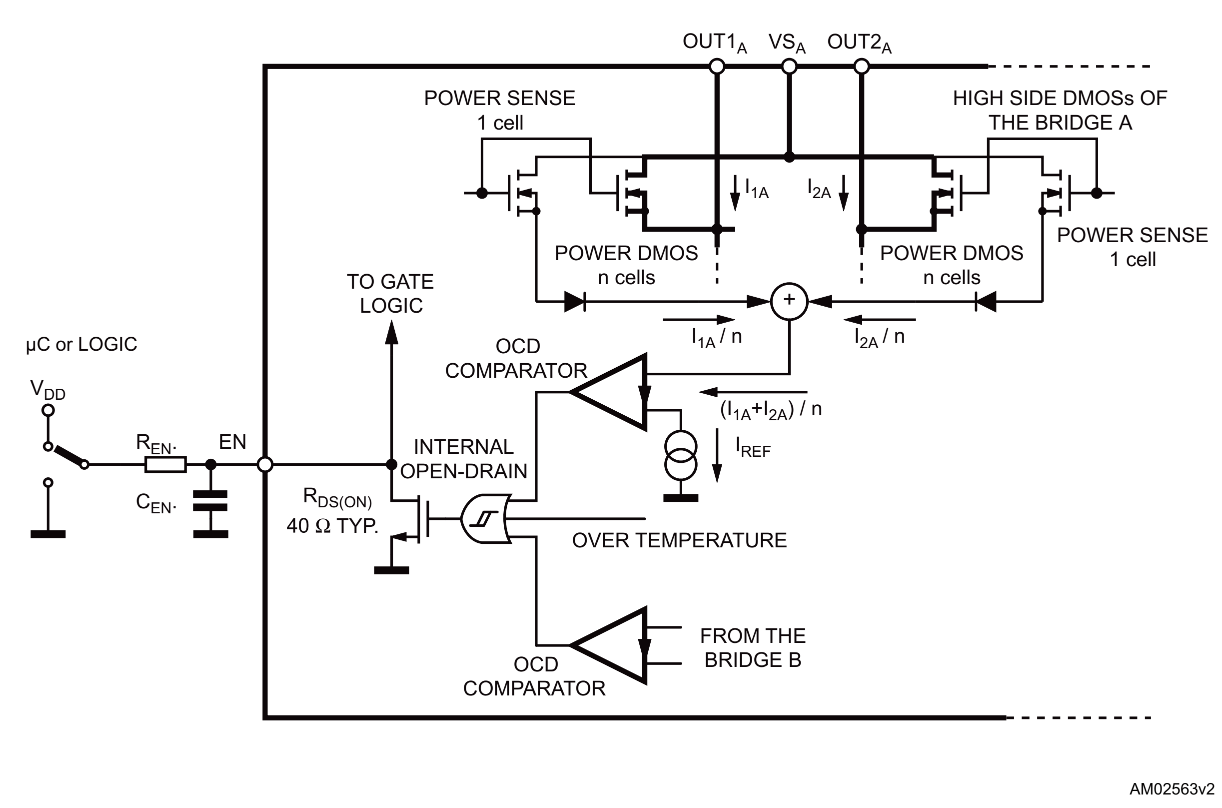


Figure 22 shows the overcurrent detection operation. The disable time $t_{DISABLE}$ before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs. It is affected by both C_{EN} and R_{EN} values and its magnitude is reported in *Figure 23*. The delay time t_{DELAY} before turning off the bridge when an overcurrent has been detected depends only on C_{EN} value. Its magnitude is reported in *Figure 24*.

C_{EN} is also used for providing immunity to pin EN against fast transient noises. Therefore the value of C_{EN} should be chosen as big as possible according to the maximum tolerable delay time and the R_{EN} value should be chosen according to the desired disable time.

The resistor R_{EN} should be chosen in the range from 2.2 kΩ to 180 kΩ. Recommended values for R_{EN} and C_{EN} are respectively 100 kΩ and 5.6 nF which allow to obtain 200 µs disable time.

Figure 22. Overcurrent protection waveforms

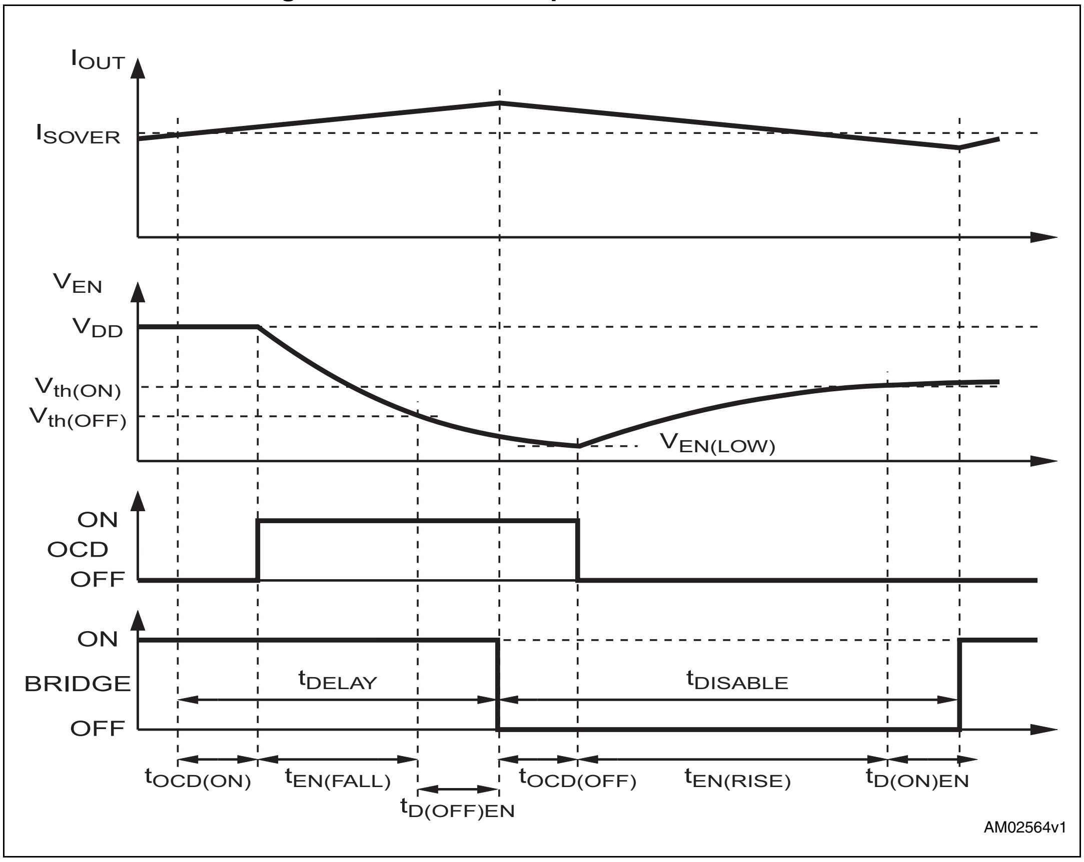


Figure 23. $t_{DISABLE}$ vs. C_{EN} and R_{EN} (V_{DD} = 5 V)

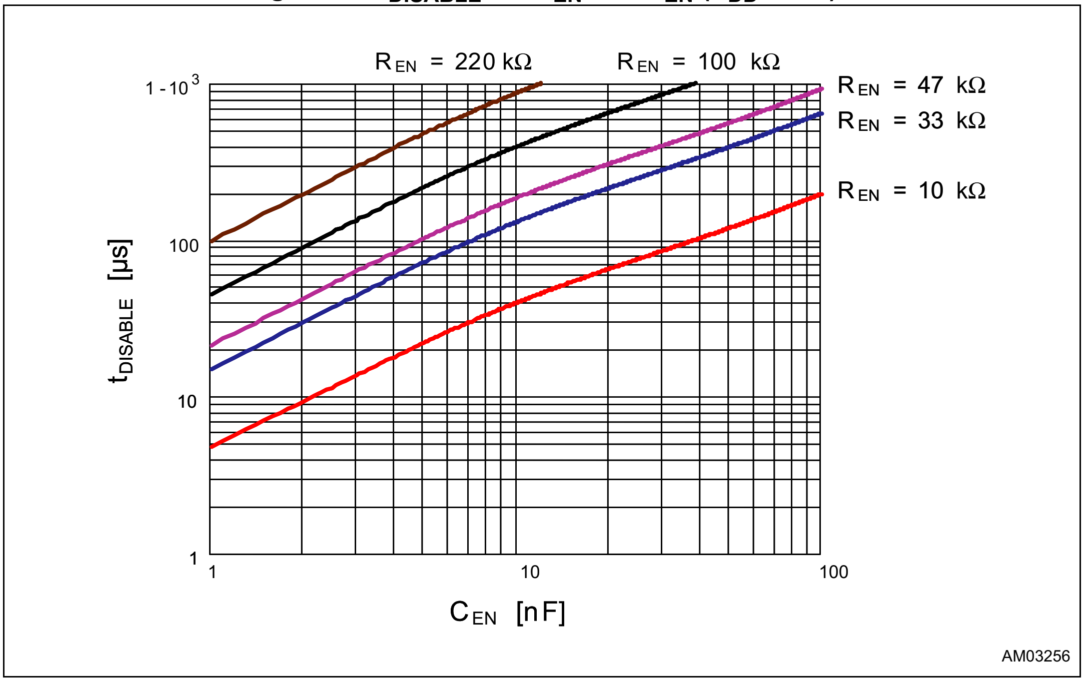
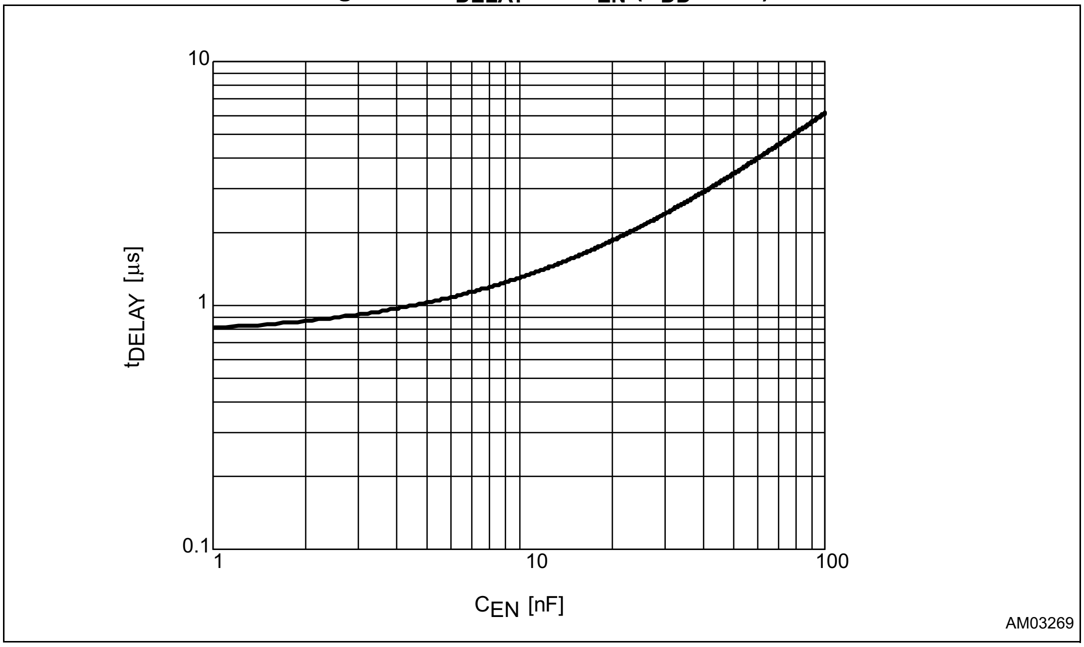


Figure 24. t_{DELAY} vs. C_{EN} (V_{DD} = 5 V)



5.10 Thermal protection

In addition to the overcurrent detection, the L6208Q device integrates a thermal protection to prevent device destruction in the case of junction over temperature. It works sensing the die temperature by means of a sensitive element integrated in the die. The device switches off when the junction temperature reaches 165 °C (typ. value) with 15 °C hysteresis (typ. value).

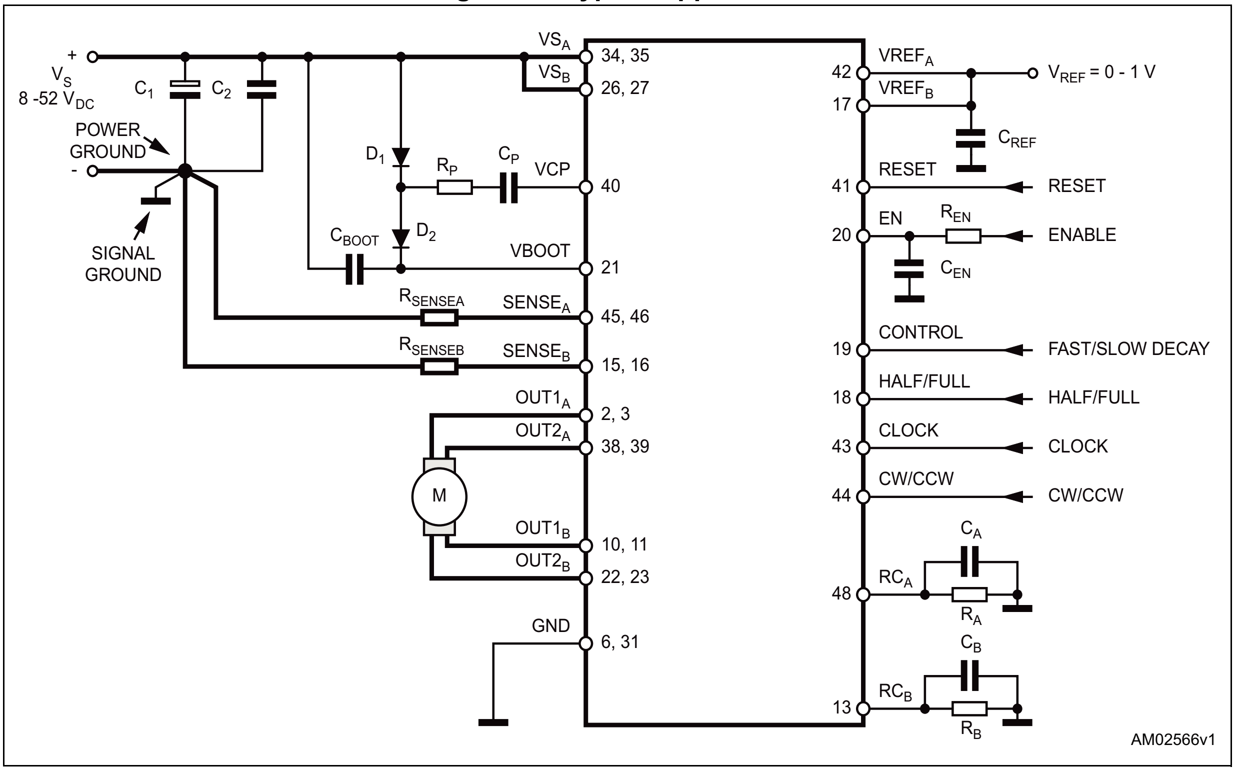
6 Application information

A typical application using the L6208Q device is shown in *Figure 25*. Typical component values for the application are shown in *Table 6*. A high quality ceramic capacitor in the range of 100 to 200 nF should be placed between the power pins (VS_A and VS_B) and ground near the L6208Q to improve the high frequency filtering on the power supply and reduce high frequency transients generated by the switching. The capacitors connected from the EN input to ground set the shutdown time when an overcurrent is detected (see *Section 5.9 on page 20*). The two current sensing inputs ($SENSE_A$ and $SENSE_B$) should be connected to the sensing resistors with a trace length as short as possible in the layout. The sense resistors should be non-inductive resistors to minimize the di/dt transients across the resistor. To increase noise immunity, unused logic pins (except EN) are best connected to 5 V (high logic level) or GND (low logic level) (see *Section 3 on page 6*). It is recommended to keep power ground and signal ground separate on the PCB.

Table 6. Component values for typical application

Component	Value
C_1	100 µF
C_2	100 nF
C_A	1 nF
C_B	1 nF
C_{BOOT}	220 nF
C_P	10 nF
C_{ENB}	5.6 nF
C_{REF}	68 nF
D_1	1N4148
D_2	1N4148
R_A	39 kΩ
R_B	39 kΩ
R_{EN}	100 kΩ
R_P	100 Ω
R_{SENSEA}	0.3 Ω
R_{SENSEB}	0.3 Ω

Figure 25. Typical application



Note: To reduce the IC thermal resistance, therefore improving the dissipation path, the NC pins can be connected to GND.

7 Output current capability and IC power dissipation

Figure 26, *27*, *28* and *29* show the approximate relation between the output current and the IC power dissipation using PWM current control driving a two-phase stepper motor, for different driving sequences:

- HALF STEP mode (*Figure 26*) in which, alternately, one phase / two phases are energized.
- NORMAL DRIVE (FULL STEP TWO-PHASE-ON) mode (*Figure 27*) in which two phases are energized during each step.
- WAVE DRIVE (FULL STEP ONE-PHASE-ON) mode (*Figure 28*) in which only one phase is energized at each step.
- MICROSTEPPING mode (*Figure 29*), in which the current follows a sinewave profile, provided through the Vref pins.

For a given output current and driving sequence the power dissipated by the IC can be easily evaluated, in order to establish which package should be used and how large the onboard copper dissipating area must be to guarantee a safe operating junction temperature (125 °C maximum).

Figure 26. IC power dissipation vs. output current in half step mode

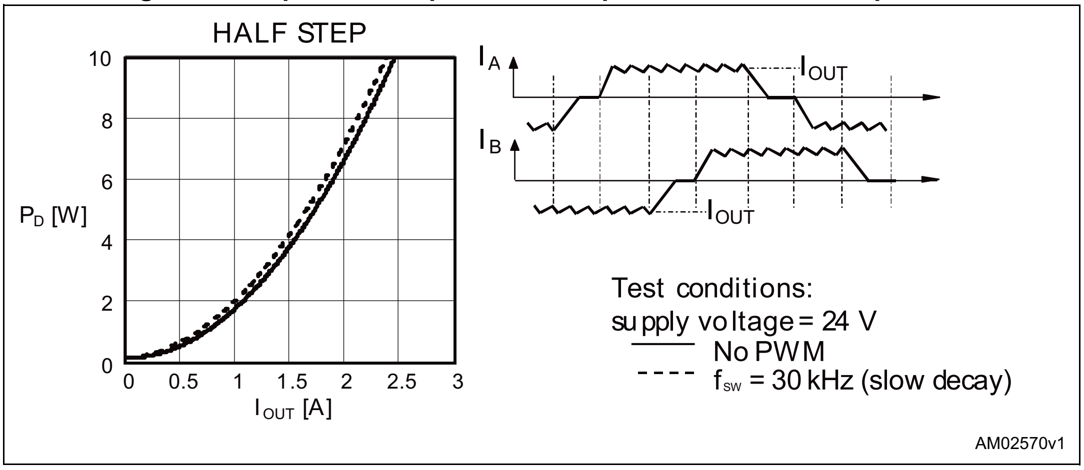


Figure 27. IC power dissipation vs. output current in normal mode (full step two-phase-on)

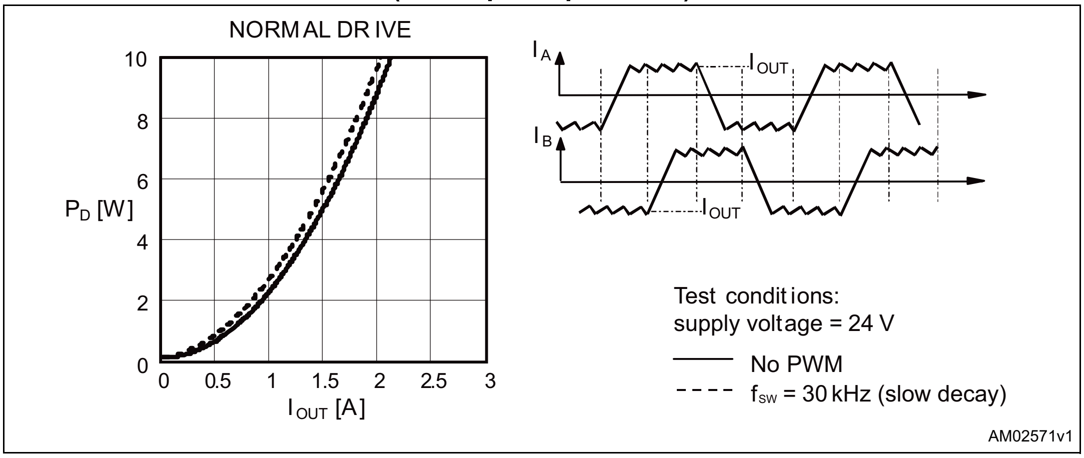


Figure 28. IC power dissipation vs. output current in wave mode (full step one-phase-on)

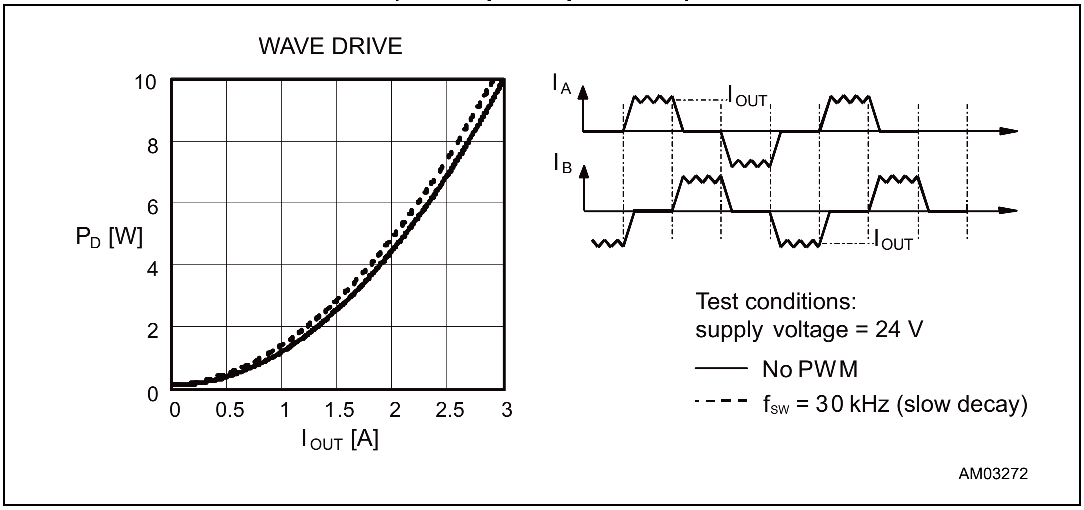
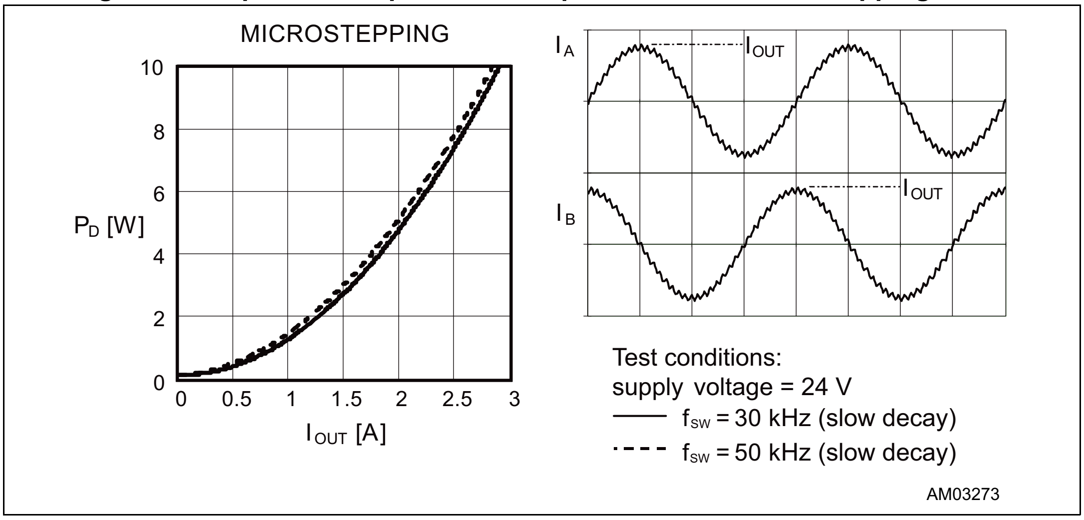


Figure 29. IC power dissipation vs. output current in micro stepping mode



8 Thermal management

In most applications the power dissipation in the IC is the main factor that sets the maximum current that can be delivered by the device in a safe operating condition. Therefore, it must be considered very carefully. Besides the available space on the PCB, the right package should be chosen considering the power dissipation. Heat sinking can be achieved using copper on the PCB with proper area and thickness.

Table 7. Thermal data

Symbol	Parameter	Package	Typ.	Unit
R_{thJA}	Thermal resistance junction-ambient	VFQFPN48(1)	17	°C/W

1. VFQFPN48 mounted on the EVAL6208Q rev 1 board (see EVAL6208Q databrief): four-layer FR4 PCB with a dissipating copper surface of about 45 cm^2 on each layer and 25 via holes below the IC.

9 Electrical characteristic curves

Figure 30. Typical quiescent current vs. supply voltage

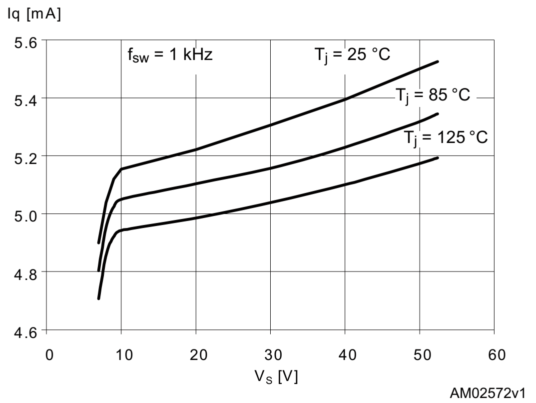


Figure 31. Typical high-side $R_{DS(on)}$ vs. supply voltage

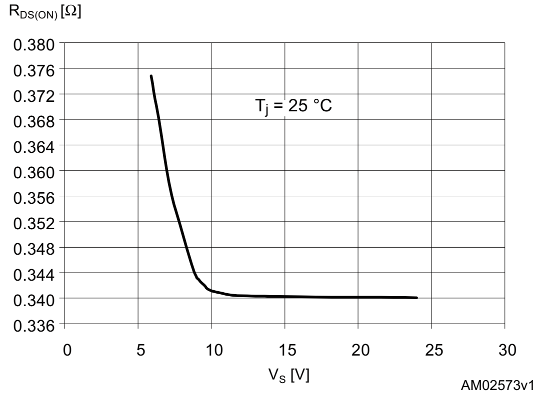


Figure 32. Normalized typical quiescent current vs. switching frequency

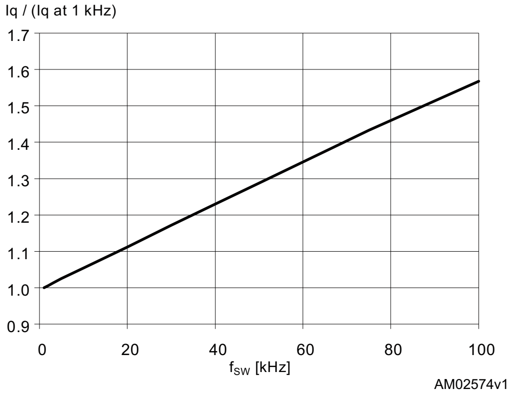


Figure 33. Normalized $R_{DS(on)}$ vs.junction temperature (typical value)

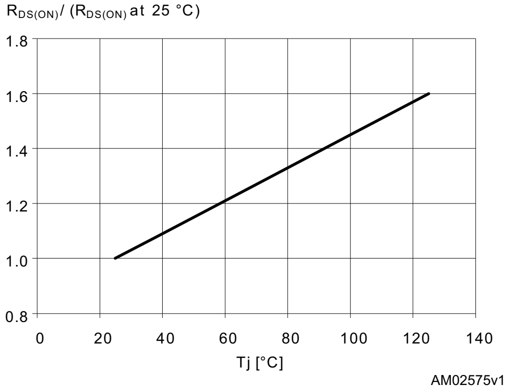


Figure 34. Typical low-side $R_{DS(on)}$ vs. supply voltage

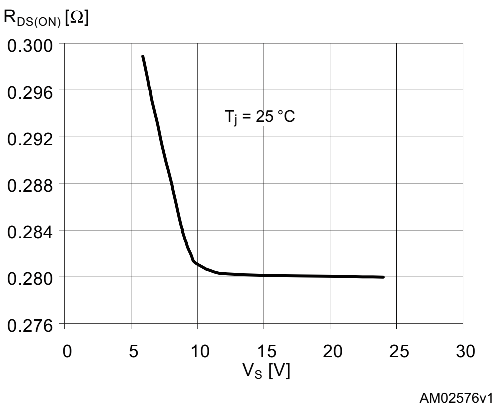
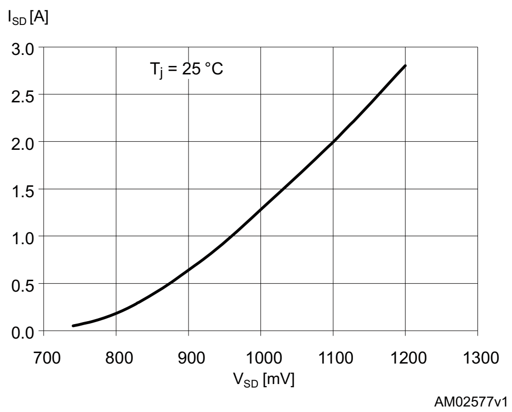


Figure 35. Typical drain-source diode forward ON characteristic



10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

10.1 VFQFPN48 (7 x 7 x 1.0 mm) package information

Figure 36. VFQFPN48 (7 x 7 x 1.0 mm) package outline

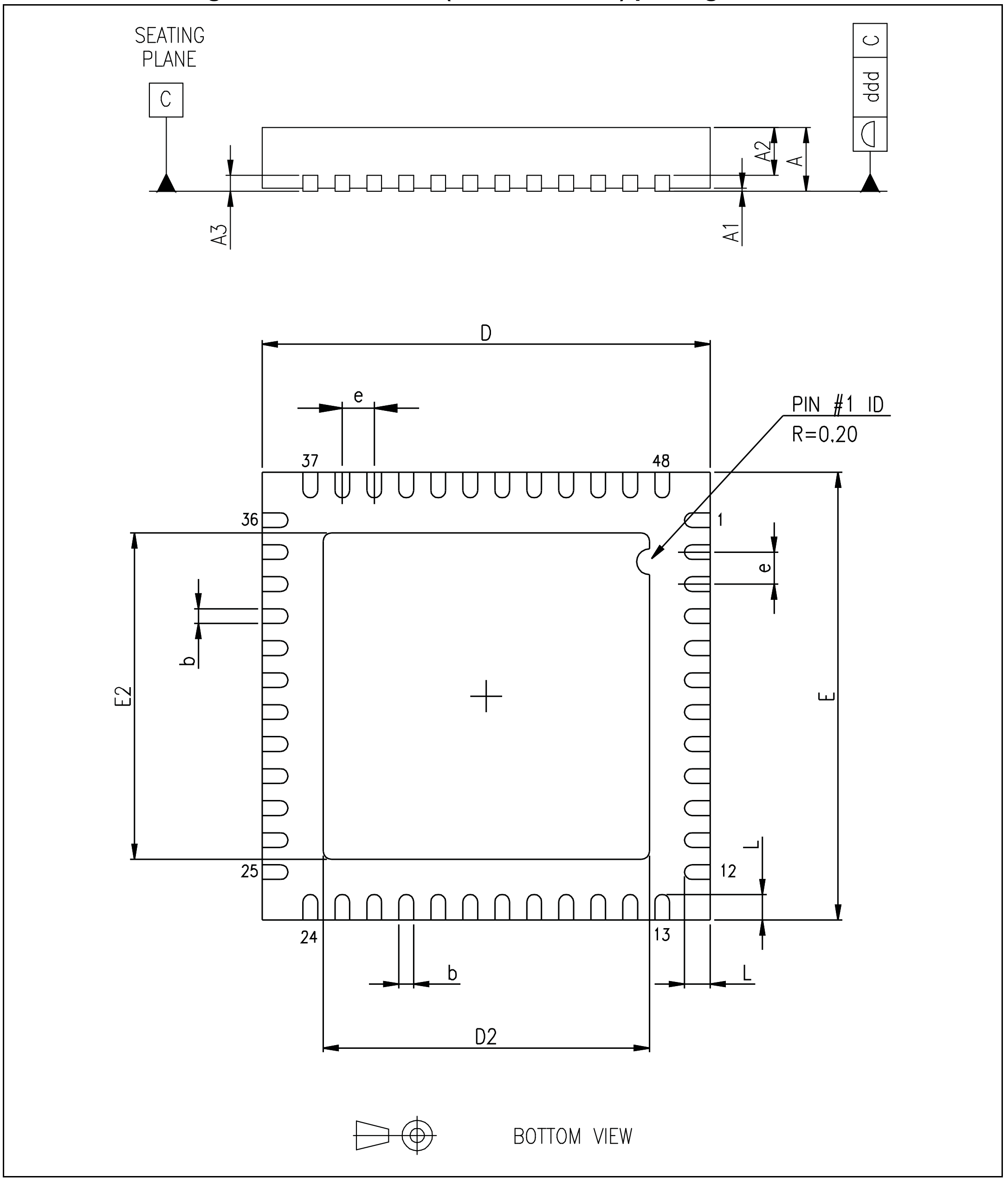


Table 8. VFQFPN48 (7 x 7 x 1.0 mm) package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	-	0.02	0.05
A2	-	0.65	1.00
A3	-	0.25	-
b	0.18	0.23	0.30
D	6.85	7.00	7.15
D2	4.95	5.10	5.25
E	6.85	7.00	7.15
E2	4.95	5.10	5.25
e	0.45	0.50	0.55
L	0.30	0.40	0.50
ddd	-	0.08	-

11 Order codes

Table 9. Ordering information

Order codes	Package	Packaging
L6208Q	VFQFPN48 7 x 7 x 1.0 mm	Tray
L6208QTR		Tape and reel

12 Revision history

Table 10. Document revision history

Date	Revision	Changes
29-Jul-2011	1	First release
28-Nov-2011	2	Document moved from preliminary to final datasheet
12-Jun-2013	3	Unified package name to “VFQFPN48” in the whole document. *Figure 1* moved to page 3, added *Section 1: Block diagram*. Corrected headings in *Table 1* and *Table 2* (replaced “Parameter” by “Test condition”). Corrected unit in *Table 6* (row C_1). Added titles to *Equation 1* to *Equation 4* and cross-references in *Section 5.3: PWM current control*. Added *Table 7: Thermal data* in *Section 8: Thermal management*. Updated *Section 10: Package information* (modified titles, reversed order of *Figure 36* and *Table 8*). Unified “C_{EN}”, “t_{DT}”, “t_{ON}”,“t_{OFF}”, “C_{OFF}”, “R_{OFF}”, “$V_{th(ON)}$”, “$V_{th(OFF)}$”(subscript, lower/upper case) in the whole document. Minor corrections throughout document.
13-Mar-2017	4	Updated *Figure 1 on page 4* (replaced by new figure). Minor modifications throughout document.