Precision Low Power Single-Supply JFET Amplifiers

Data Sheet

AD8625/AD8626/AD8627

FEATURES

- SC70 package
- Very low I_B: 1 pA max
- Single-supply operation: 5 V to 26 V
- Dual-supply operation: ±2.5 V to ±13 V
- Rail-to-rail output
- Low supply current: 630 µA/amp typ
- Low offset voltage: 500 µV max
- Unity gain stable
- No phase reversal

APPLICATIONS

- Photodiode amplifiers
- ATEs
- Line-powered/battery-powered instrumentation
- Industrial controls
- Automotive sensors
- Precision filters
- Audio

PIN CONFIGURATIONS

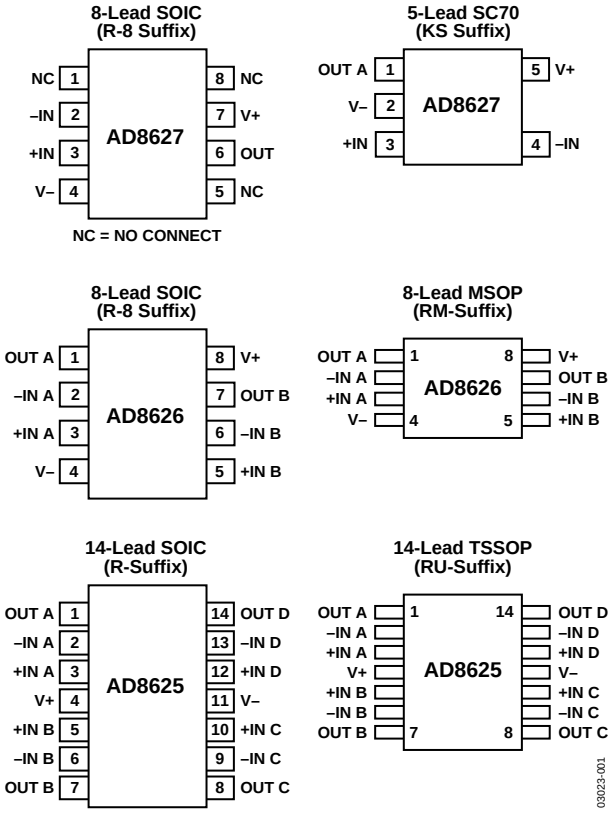

Figure 1.

GENERAL DESCRIPTION

The AD862x is a precision JFET input amplifier. It features true single-supply operation, low power consumption, and rail-to-rail output. The outputs remain stable with capacitive loads of over 500 pF; the supply current is less than 630 µA/amp. Applications for the AD862x include photodiode transimpedance amplification, ATE reference level drivers, battery management, both line powered and portable instrumentation, and remote sensor signal conditioning, which includes automotive sensors.

The AD862x's ability to swing nearly rail-to-rail at the input and rail-to-rail at the output enables it to be used to buffer CMOS DACs, ASICs, and other wide output swing devices in single-supply systems.

The 5 MHz bandwidth and low offset are ideal for precision filters.

The AD862x is fully specified over the industrial temperature range. (−40°C to +85°C). The AD8627 is available in both 5-lead SC70 and 8-lead SOIC surface-mount packages (SC70 packaged parts are available in tape and reel only). The AD8626 is available in MSOP and SOIC packages, while the AD8625 is available in TSSOP and SOIC packages.

Rev. F
Document Feedback

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12/10—Rev. D to Rev. E

Removed Table Summary Conditions Above Table 3 ... 5
Updated Outline Dimensions ... 18

3/09—Rev. C to Rev. D

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11/04—Rev. B to Rev. C

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

@V_S = 5 V, V_{CM} = 1.5 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.05	0.5	mV
		−40°C < T_A < +85°C			1.2	mV
Input Bias Current	I_B			0.25	1	pA
		−40°C < T_A < +85°C			60	pA
Input Offset Current	I_{OS}				0.5	pA
		−40°C < T_A < +85°C			25	pA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.5 V	66	87		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.5 V to 4.5 V	100	230		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +85°C		2.5		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}		4.92			V
		I_L = 2 mA, −40°C < T_A < +85°C	4.90			V
Output Voltage Low	V_{OL}				0.075	V
		I_L = 2 mA, −40°C < T_A < +85°C			0.08	V
Output Current	I_{OUT}			±10		mA
POWER SUPPLY						
Power-Supply Rejection Ratio	PSRR	V_S = 5 V to 26 V	80	104		dB
Supply Current/Amplifier	I_{SY}			630	785	µA
		−40°C < T_A < +85°C			800	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR			5		V/µs
Gain Bandwidth Product	GBP			5		MHz
Phase Margin	$Ø_M$			60		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		1.9		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		17.5		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.4		fA/√Hz
Channel Separation	C_s	f = 1 kHz		104		dB

@V_S = ±13 V; V_{CM} = 0 V; T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.35	0.75	mV
		−40°C < T_A < +85°C			1.35	mV
Input Bias Current	I_B			0.25	1	pA
		−40°C < T_A < +85°C			60	pA
Input Offset Current	I_{OS}				0.5	pA
		−40°C < T_A < +85°C			25	pA
Input Voltage Range			−13		+11	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −13 V to +10 V	76	105		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = −11 V to +11 V	150	310		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +85°C		2.5		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}		+12.92			V
	V_{OH}	I_L = 2 mA, −40°C < T_A < +85°C	+12.91			V
Output Voltage Low	V_{OL}				−12.92	V
	V_{OL}	I_L = 2 mA, −40°C < T_A < +85°C			−12.91	V
Output Current	I_{OUT}			±15		mA
POWER SUPPLY						
Power-Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±13 V	80	104		dB
Supply Current/Amplifier	I_{SY}			710	850	µA
		−40°C < T_A < +85°C			900	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR			5		V/µs
Gain Bandwidth Product	GBP			5		MHz
Phase Margin	$Ø_M$			60		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		16		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.5		fA/√Hz
Channel Separation	C_s	f = 1 kHz		105		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Ratings
Supply Voltage	27 V
Input Voltage	V_{S-} to V_{S+}
Differential Input Voltage	± Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range, R Package	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range, R Package	−65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

θ_{JA} is specified for worst-case conditions when devices are soldered in circuit boards for surface-mount packages.

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
5-Lead SC70 (KS)	376	126	°C/W
8-Lead MSOP (RM)	210	45	°C/W
8-Lead SOIC (R)	158	43	°C/W
14-Lead SOIC (R)	120	36	°C/W
14-Lead TSSOP (RU)	180	35	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

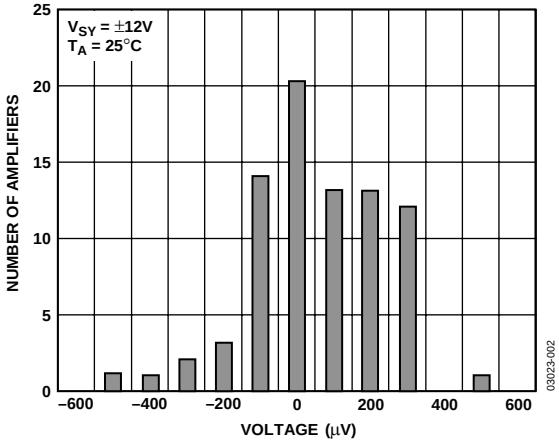


Figure 2. Input Offset Voltage

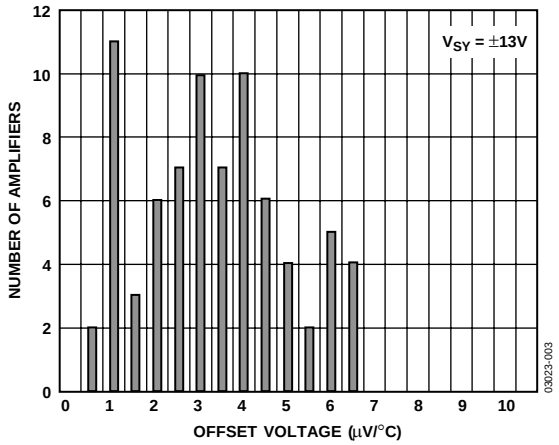


Figure 3. Offset Voltage Drift

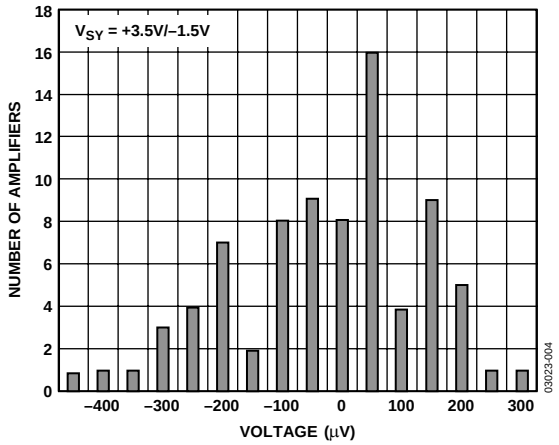


Figure 4. Input Offset Voltage

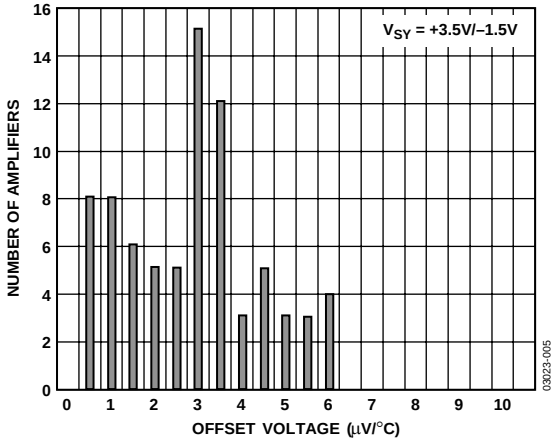


Figure 5. Offset Voltage Drift

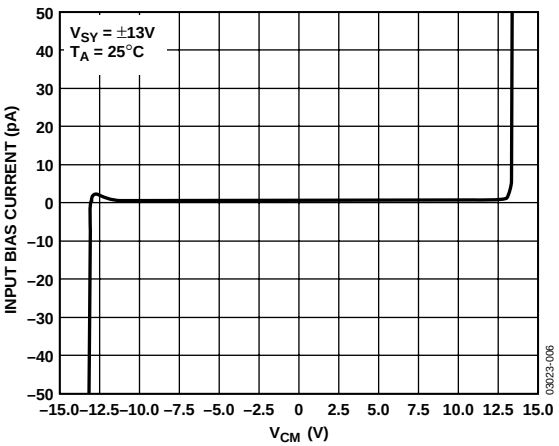


Figure 6. Input Bias Current vs. V_{CM}

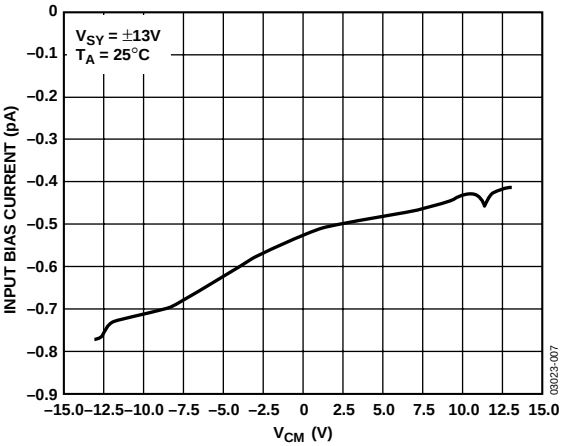


Figure 7. Input Bias Current vs. V_{CM}

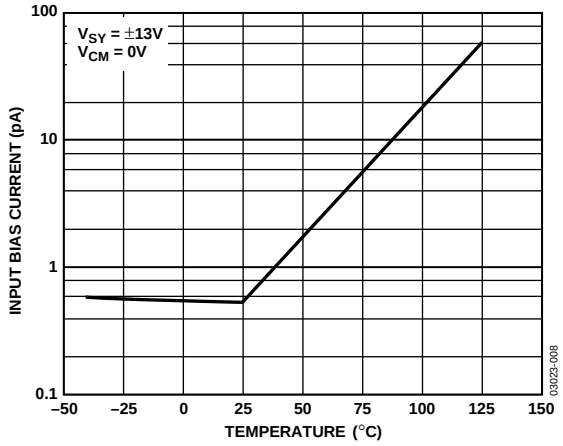


Figure 8. Input Bias Current vs. Temperature

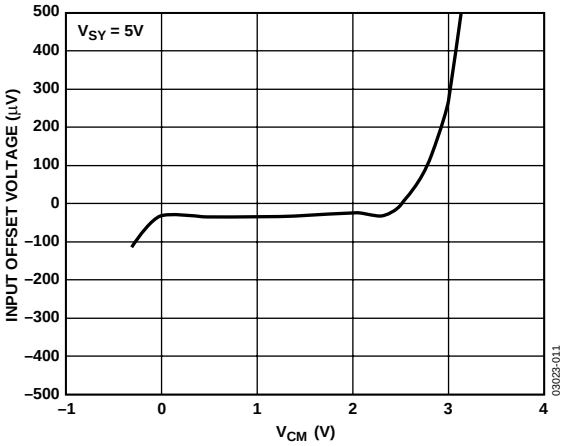


Figure 11. Input Offset Voltage vs. V_{CM}

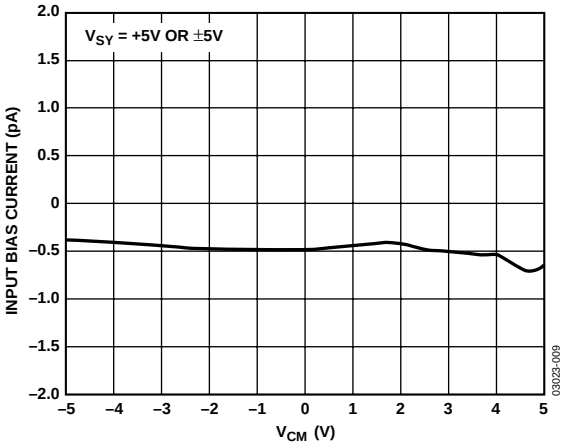


Figure 9. Input Bias Current vs. V_{CM}

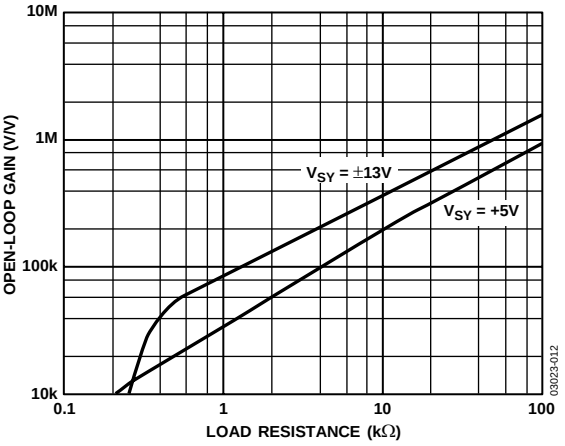


Figure 12. Open-Loop Gain vs. Load Resistance

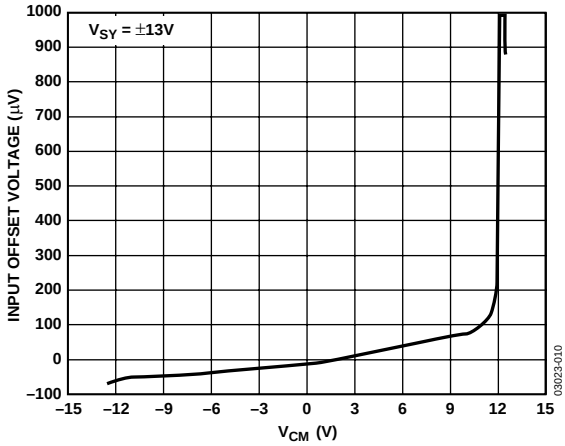


Figure 10. Input Offset Voltage vs. V_{CM}

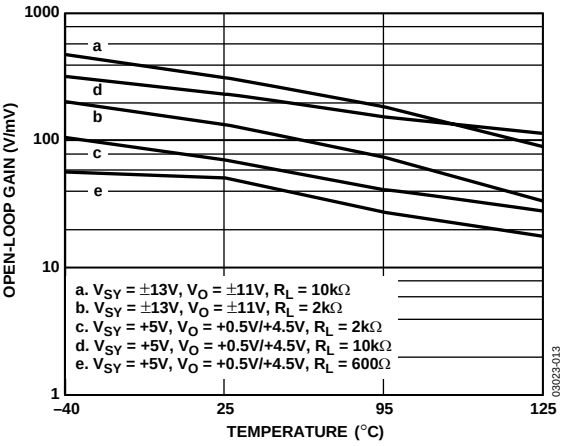


Figure 13. Open-Loop Gain vs. Temperature

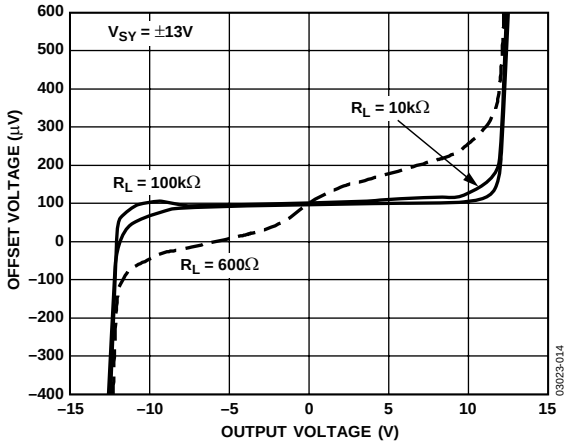


Figure 14. Input Error Voltage vs. Output Voltage for Resistive Loads

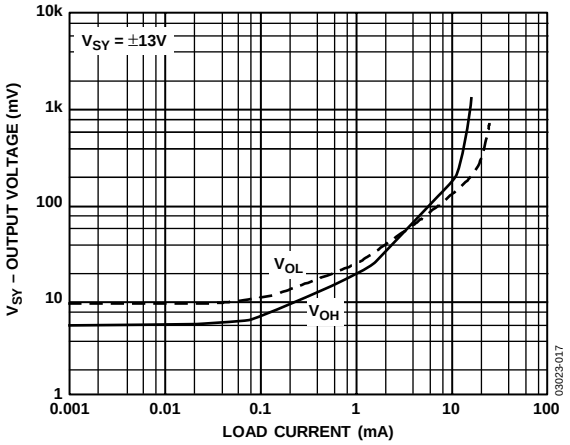


Figure 17. Output Saturation Voltage vs. Load Current

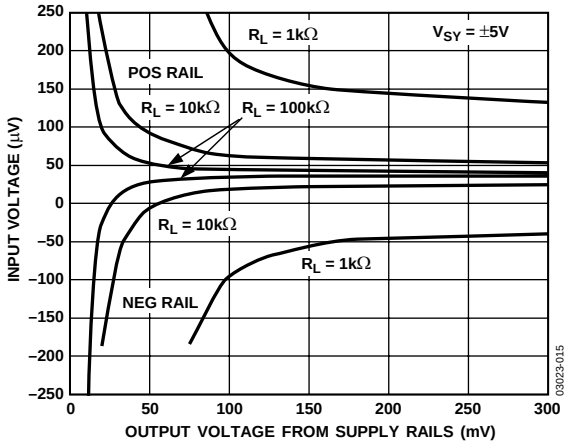


Figure 15. Input Error Voltage vs. Output Voltage within 300 mV of Supply Rails

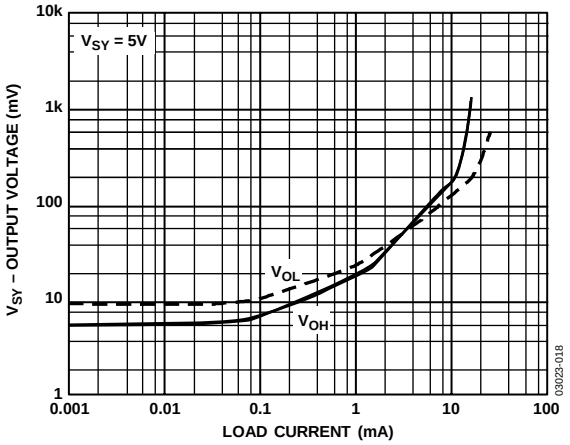


Figure 18. Output Saturation Voltage vs. Load Current

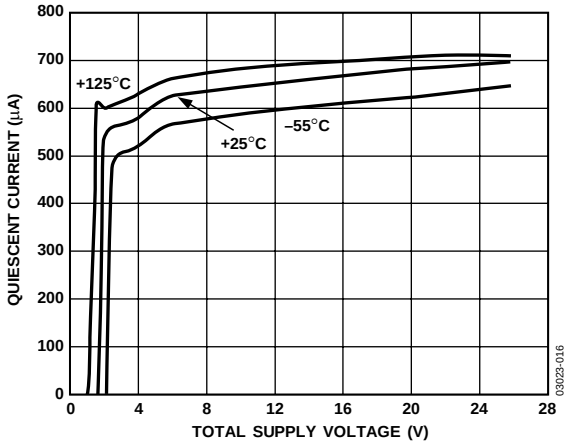


Figure 16. Quiescent Current vs. Supply Voltage at Different Temperatures

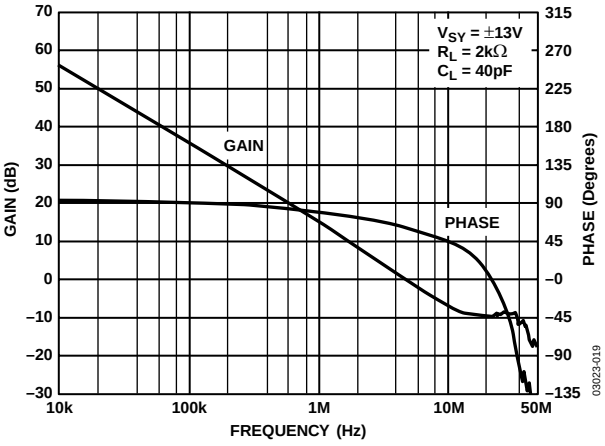


Figure 19. Open-Loop Gain and Phase Margin vs. Frequency

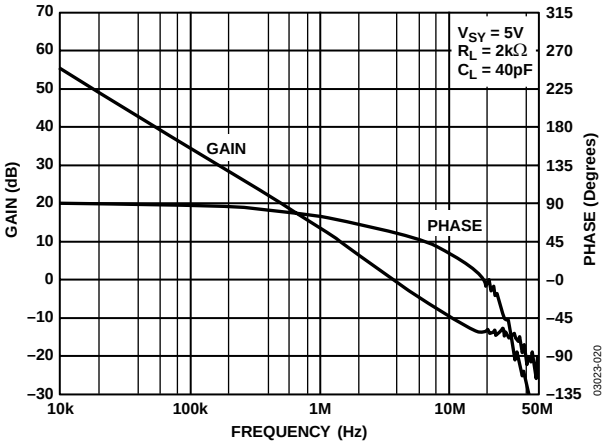


Figure 20. Open-Loop Gain and Phase Margin vs. Frequency

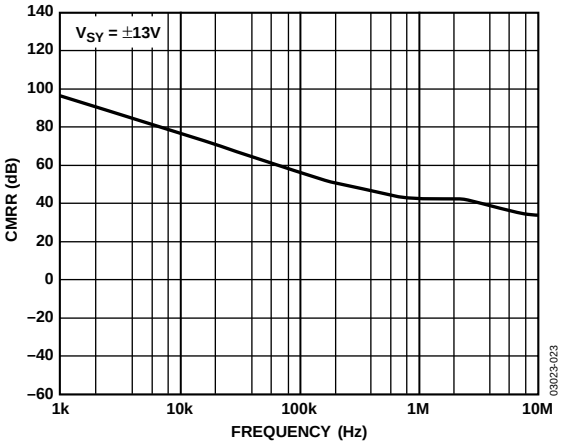


Figure 23. CMRR vs. Frequency

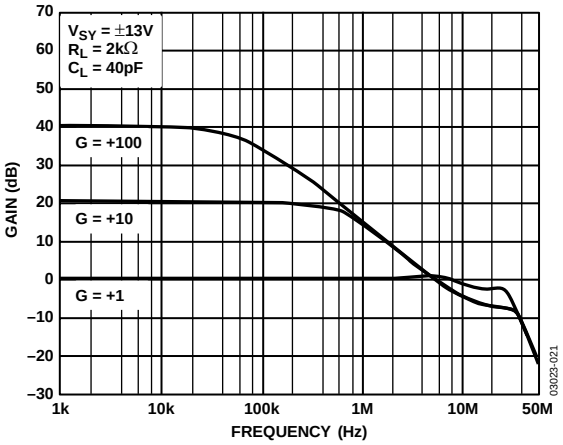


Figure 21. Closed-Loop Gain vs. Frequency

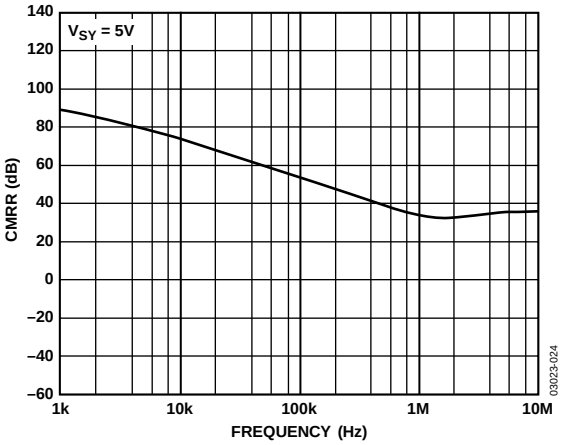


Figure 24. CMRR vs. Frequency

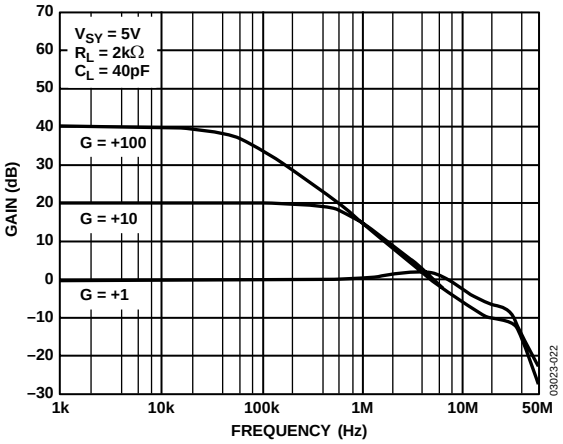


Figure 22. Closed-Loop Gain vs. Frequency

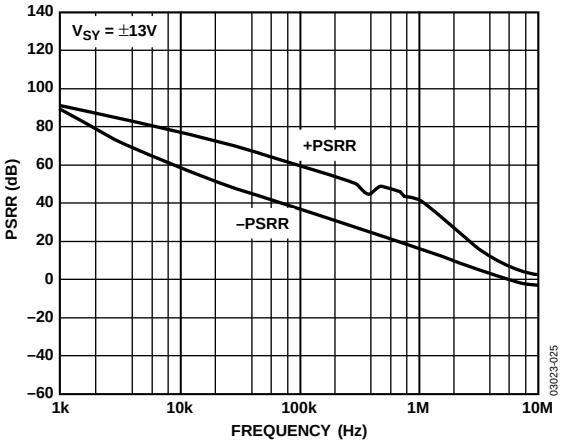


Figure 25. PSRR vs. Frequency

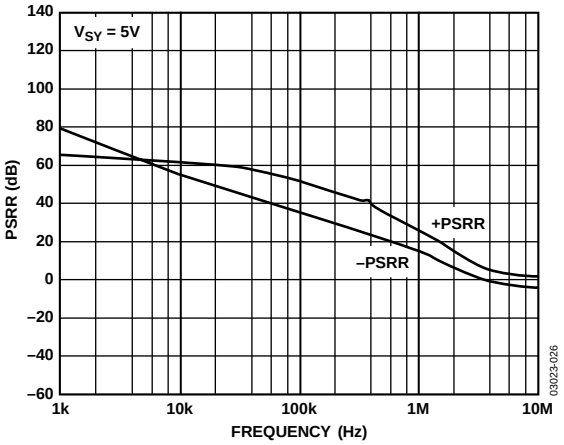


Figure 26. PSRR vs. Frequency

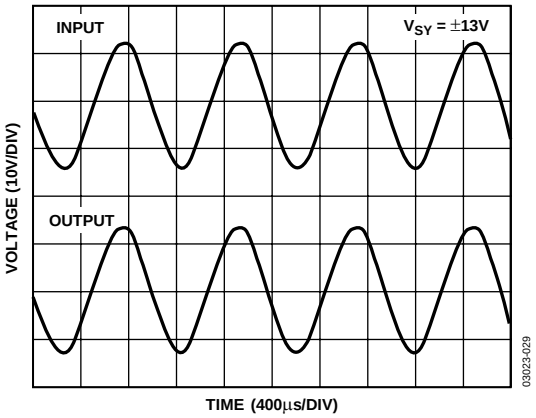


Figure 29. No Phase Reversal

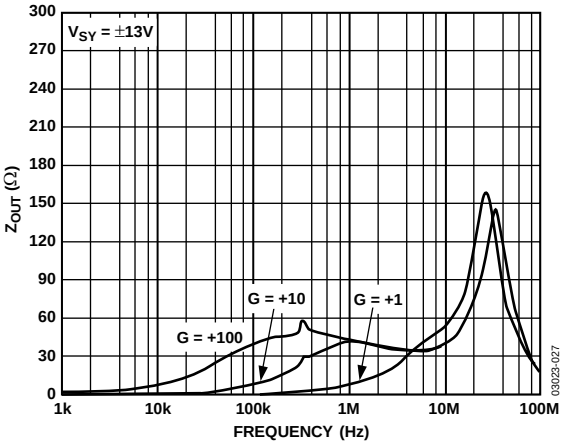


Figure 27. Output Impedance vs. Frequency

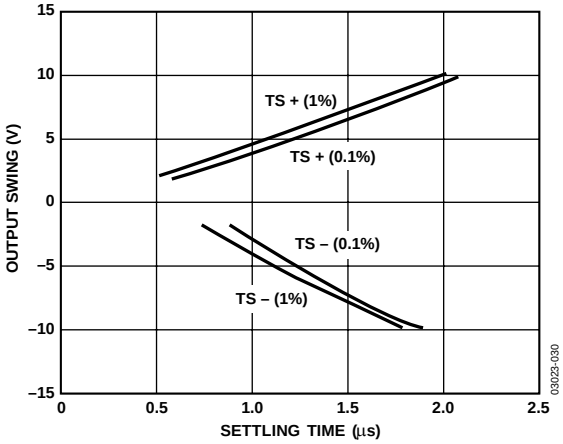


Figure 30. Output Swing and Error vs. Settling Time

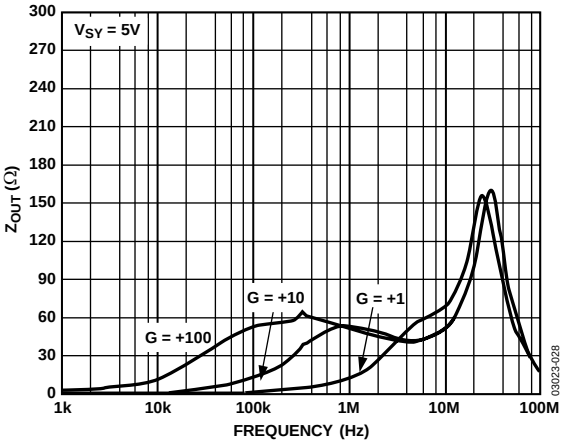


Figure 28. Output Impedance vs. Frequency

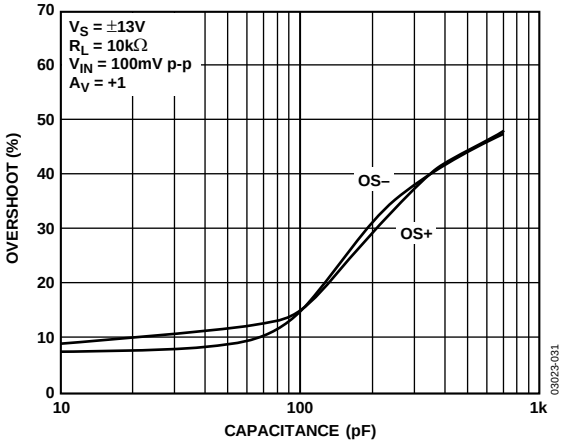


Figure 31. Small-Signal Overshoot vs. Load Capacitance

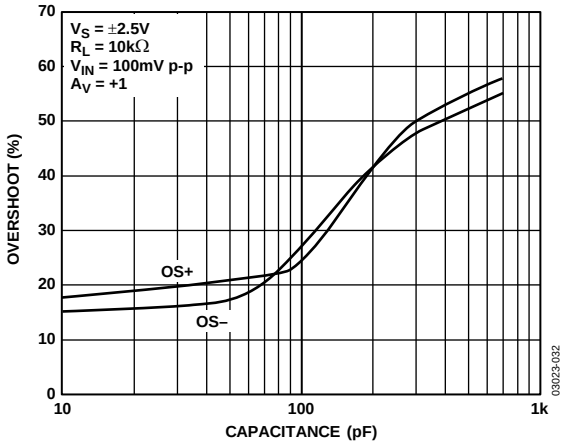


Figure 32. Small-Signal Overshoot vs. Load Capacitance

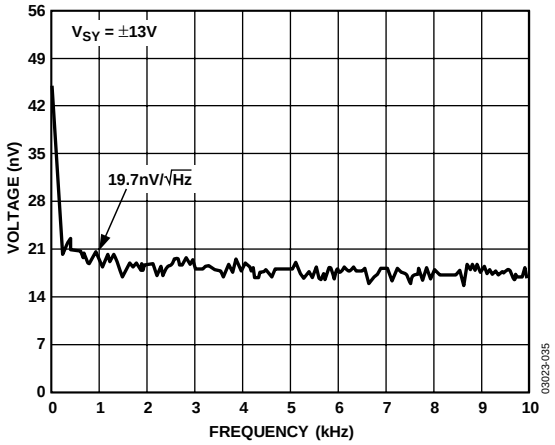


Figure 35. Voltage Noise Density

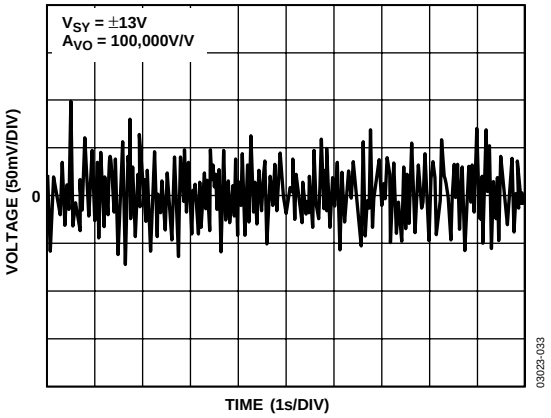


Figure 33. 0.1 Hz to 10 Hz Noise

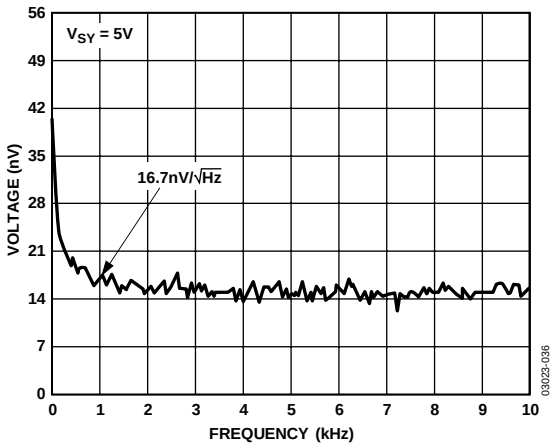


Figure 36. Voltage Noise Density

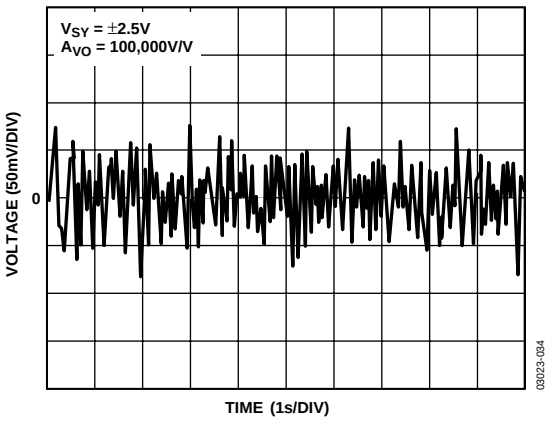


Figure 34. 0.1 Hz to 10 Hz Noise

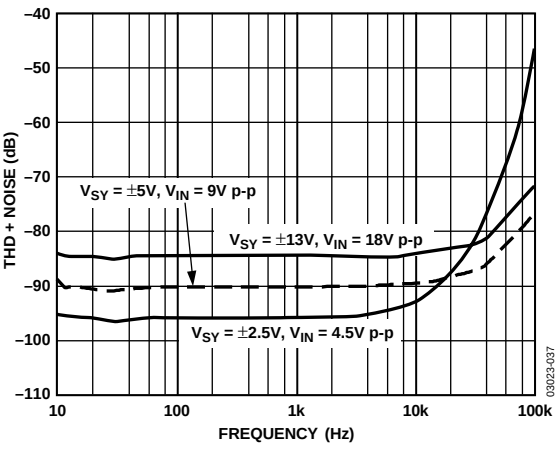


Figure 37. Total Harmonic Distortion + Noise vs. Frequency

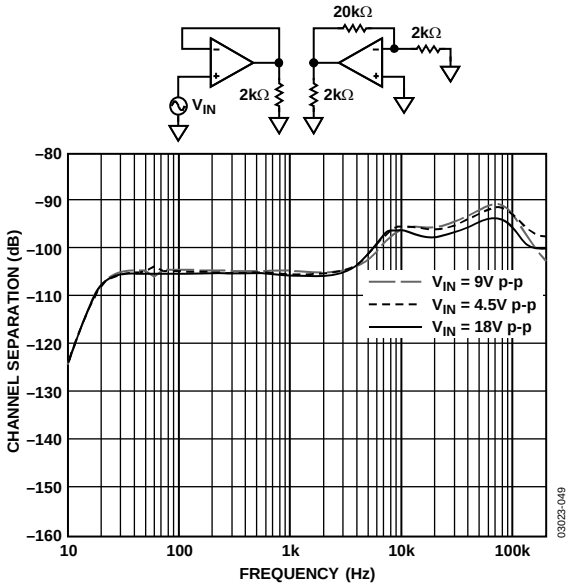


Figure 38. Channel Separation

APPLICATIONS INFORMATION

The AD862x is one of the smallest and most economical JFETs offered. It has true single-supply capability and has an input voltage range that extends below the negative rail, allowing the part to accommodate input signals below ground. The rail-to-rail output of the AD862x provides the maximum dynamic range in many applications. To provide a low offset, low noise, high impedance input stage, the AD862x uses n-channel JFETs. The input common-mode voltage extends from 0.2 V below $-V_S$ to 2 V below $+V_S$. Driving the input of the amplifier, configured in the unity gain buffer, closer than 2 V to the positive rail causes an increase in common-mode voltage error, as illustrated in Figure 15, and a loss of amplifier bandwidth. This loss of bandwidth causes the rounding of the output waveforms shown in Figure 39 and Figure 40, which have inputs that are 1 V and 0 V from $+V_S$, respectively.

The AD862x does not experience phase reversal with input signals close to the positive rail, as shown in Figure 29. For input voltages greater than $+V_{SY}$, a resistor in series with the AD862x's noninverting input prevents phase reversal at the expense of greater input voltage noise. This current-limiting resistor should also be used if there is a possibility of the input voltage exceeding the positive supply by more than 300 mV, or if an input voltage is applied to the AD862x when $\pm V_{SY} = 0$. Either of these conditions damages the amplifier if the condition exists for more than 10 seconds. A 10 kΩ resistor allows the amplifier to withstand up to 10 V of continuous overvoltage, while increasing the input voltage noise by a negligible amount.

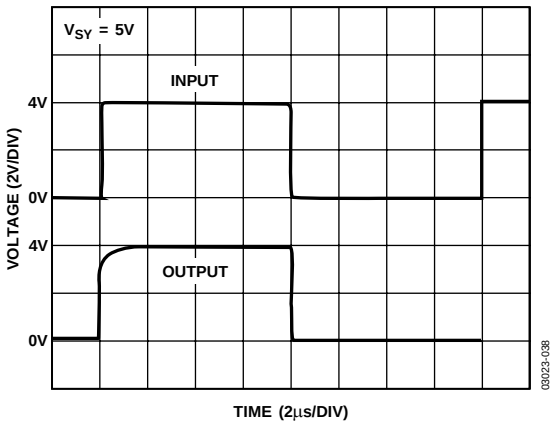


Figure 39. Unity Gain Follower Response to 0 V to 4 V Step

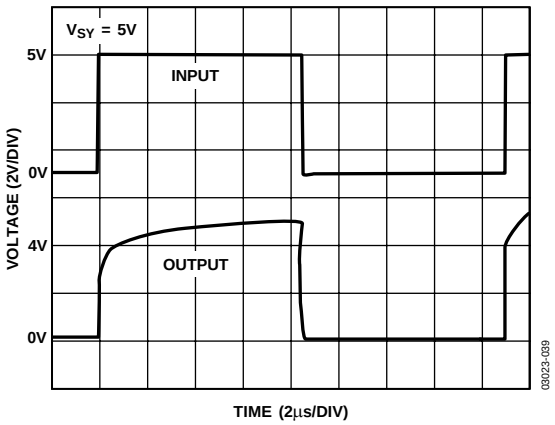


Figure 40. Unity Gain Follower Response to 0 V to 5 V Step

The AD862x can safely withstand input voltages 15 V below V_{SY} if the total voltage between the positive supply and the input terminal is less than 26 V. Figure 41 through Figure 43 show the AD862x in different configurations accommodating signals close to the negative rail. The amplifier input stage typically maintains picoamp-level input currents across that input voltage range.

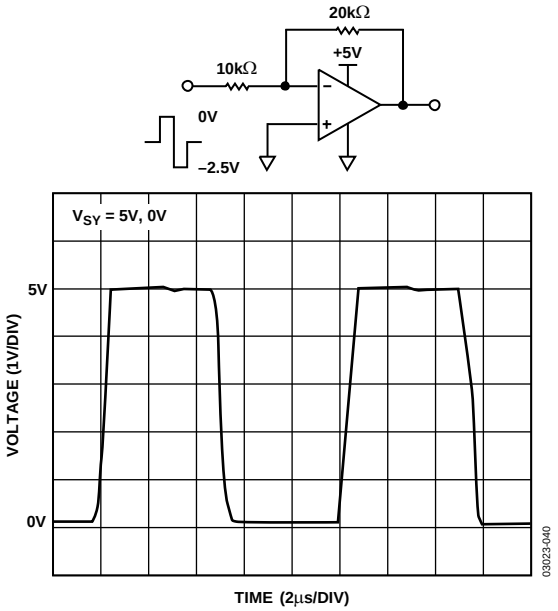


Figure 41. Gain-of-Two Inverter Response to 2.5 V Step, Centered 1.25 V below Ground

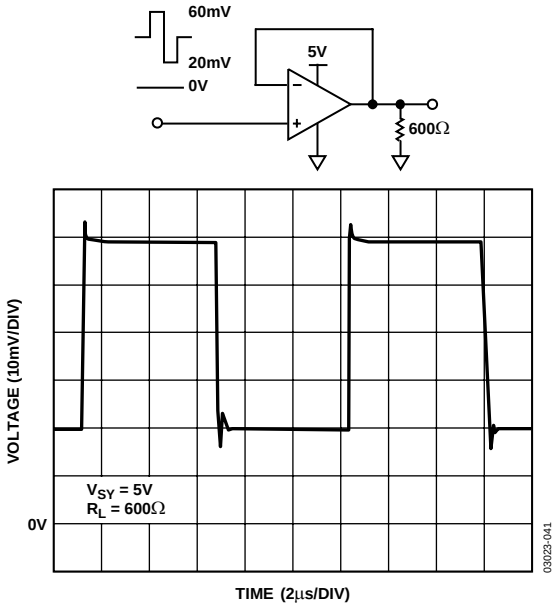


Figure 42. Unity Gain Follower Response to 40 mV Step, Centered 40 mV above Ground

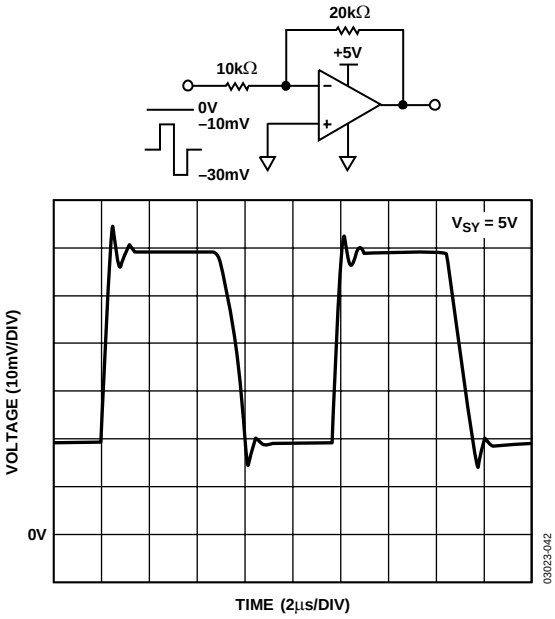


Figure 43. Gain-of-Two Inverter Response to 20 mV Step, Centered 20 mV below Ground

The AD862x is designed for 16 nV/√Hz wideband input voltage noise and maintains low noise performance to low frequencies, as shown in Figure 35. This noise performance, along with the AD862x's low input current and current noise, means that the AD862x contributes negligible noise for applications with large source resistances.

The AD862x has a unique bipolar rail-to-rail output stage that swings within 5 mV of the rail when up to 2 mA of current is drawn. At larger loads, the drop-out voltage increases, as shown in Figure 17 and Figure 18. The AD862x's wide bandwidth and fast slew rate allows it to be used with faster signals than older single-supply JFETs. Figure 44 shows the response of the AD862x, configured in unity gain, to a V_{IN} of 20 V p-p at 50 kHz. The full-power bandwidth (FPBW) of the part is close to 100 kHz.

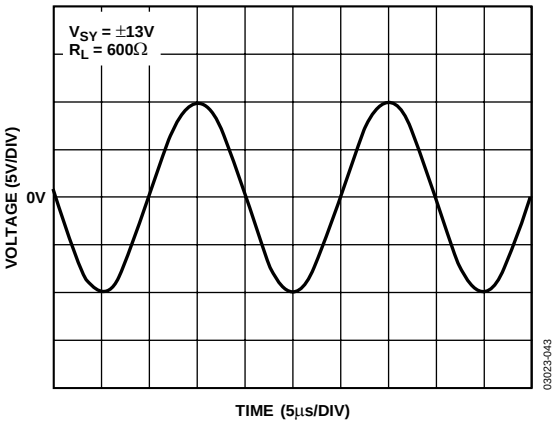


Figure 44. Unity Gain Follower Response to 20 V, 50 kHz Input Signal

MINIMIZING INPUT CURRENT

The AD862x is guaranteed to 1 pA maximum input current with a ±13 V supply voltage at room temperature. Careful attention to how the amplifier is used maintains or possibly betters this performance. The amplifier's operating temperature should be kept as low as possible. Like other JFET input amplifiers, the AD862x's input current doubles for every 10°C rise in junction temperature, as illustrated in Figure 8. On-chip power dissipation raises the device operating temperature, causing an increase in input current. Reducing supply voltage to cut power dissipation reduces the AD862x's input current. Heavy output loads can also increase chip temperature; maintaining a minimum load resistance of 1 kΩ is recommended.

The AD862x is designed for mounting on PC boards. Maintaining picoampere resolution in those environments requires a lot of care. Both the board and the amplifier's package have finite resistance. Voltage differences between the input pins and other pins, as well as PC board metal traces may cause parasitic currents larger than the AD862x's input current, unless special precautions are taken. To ensure the best result, refer to the ADI website for proper board layout seminar materials. Two common methods of minimizing parasitic leakages that should be used are guarding of the input lines and maintaining adequate insulation resistance.

Contaminants, such as solder flux on the board's surface and the amplifier's package, can greatly reduce the insulation resistance between the input pin and traces with supply or signal voltages. Both the package and the board must be kept clean and dry.

PHOTODIODE PREAMPLIFIER APPLICATION

The low input current and offset voltage levels of the AD862x, together with its low voltage noise, make this amplifier an excellent choice for preamplifiers used in sensitive photodiode applications. In a typical photovoltaic preamp circuit, shown in Figure 45, the output of the amplifier is equal to

$$V_{OUT} = -ID(R_f) = -R_p(P)R_f$$

where:
ID = photodiode signal current (A).
R_p = photodiode sensitivity (A/W).
R_f = value of the feedback resistor, in Ω.
P = light power incident to photodiode surface, in W.

The amplifier's input current, I_B, contributes an output voltage error proportional to the value of the feedback resistor. The offset voltage error, V_{OS}, causes a small current error due to the photodiode's finite shunt resistance, R_D.

The resulting output voltage error, V_E, is equal to

$$V_E = \left(1 + \frac{R_f}{R_D}\right)V_{OS} + R_f(I_B)$$

A shunt resistance on the order of 100 MΩ is typical for a small photodiode. Resistance R_D is a junction resistance that typically drops by a factor of two for every 10°C rise in temperature. In the AD862x, both the offset voltage and drift are low, which helps minimize these errors. With I_B values of 1 pA and V_{OS} of 50 mV, V_E for Figure 45 is very negligible. Also, the circuit in Figure 45 results in an SNR value of 95 dB for a signal bandwidth of 30 kHz.

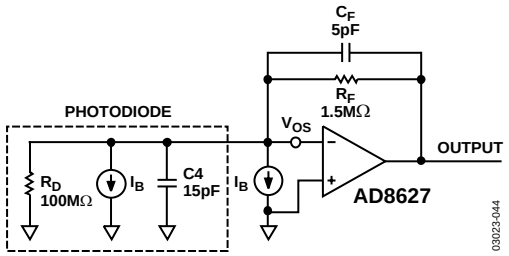


Figure 45. A Photodiode Model Showing DC Error

OUTPUT AMPLIFIER FOR DACs

Many system designers use amplifiers as buffers on the output of amplifiers to increase the DAC's output driving capability. The high resolution current output DACs need high precision amplifiers on their output as current-to-voltage converters (I/V). Additionally, many DACs operate with a single supply of 5 V. In a single-supply application, selection of a suitable op amp may be more difficult because the output swing of the amplifier does not usually include the negative rail, in this case AGND. This can result in some degradation of the DAC's specified performance, unless the application does not use codes near zero. The selected op amp needs to have very low offset voltage—for a 14-bit DAC, the DAC LSB is 300 μV with a 5 V reference—to eliminate the need for output offset trims. Input bias current should also be very low because the bias current multiplied by the DAC output impedance (about 10 kΩ in some cases) adds to the zero-code error. Rail-to-rail input and output performance is desired. For fast settling, the slew rate of the op amp should not impede the settling time of the DAC. Output impedance of the DAC is constant and code independent, but in order to minimize gain errors, the input impedance of the output amplifier should be as high as possible. The AD862x, with a very high input impedance, I_B of 1 pA, and a fast slew rate, is an ideal amplifier for these types of applications. A typical configuration with a popular DAC is shown in Figure 46. In these situations, the amplifier adds another time constant to the system, increasing the settling time of the output. The AD862x, with 5 MHz of BW, helps in achieving a faster effective settling time of the combined DAC and amplifier.

In applications with full 4-quadrant multiplying capability or a bipolar output swing, the circuit in Figure 47 can be used. In this circuit, the first and second amplifiers provide a total gain of 2, which increases the output voltage span to 20 V. Biasing the external amplifier with a 10 V offset from the reference voltage results in a full 4-quadrant multiplying circuit.

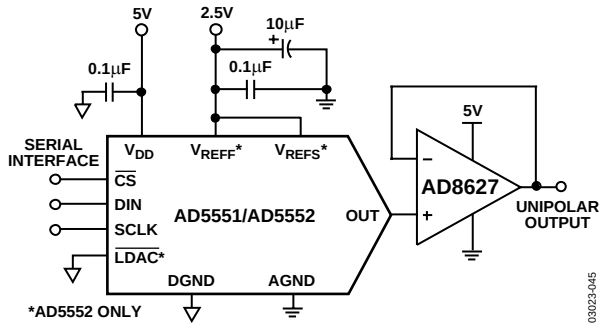


Figure 46. Unipolar Output

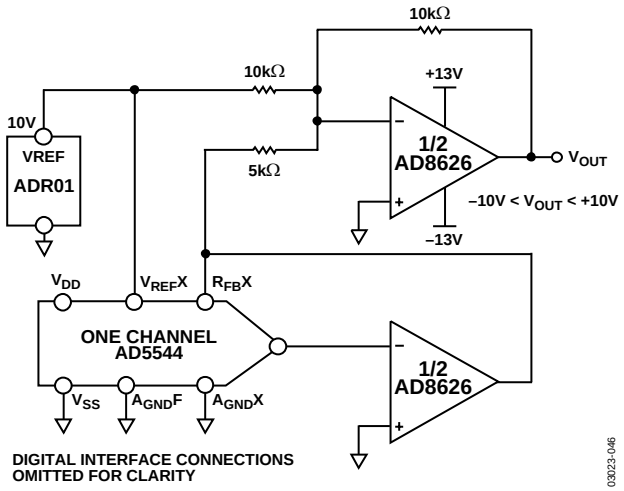


Figure 47. 4-Quadrant Multiplying Application Circuit

EIGHT-POLE SALLEN KEY LOW-PASS FILTER

The AD862x's high input impedance and dc precision make it a great selection for active filters. Due to the very low bias current of the AD862x, high value resistors can be used to construct low frequency filters. The AD862x's picoamp-level input currents contribute minimal dc errors. Figure 49 shows an example of a 10 Hz, 8-pole Sallen Key filter constructed using the AD862x. Different numbers of the AD862x can be used depending on the desired response, which is shown in Figure 48. The high value used for R1 minimizes interaction with signal source resistance. Pole placement in this version of the filter minimizes the Q associated with the lower pole section of the filter. This eliminates any peaking of the noise contribution of resistors in the preceding sections, minimizing the inherent output voltage noise of the filter.

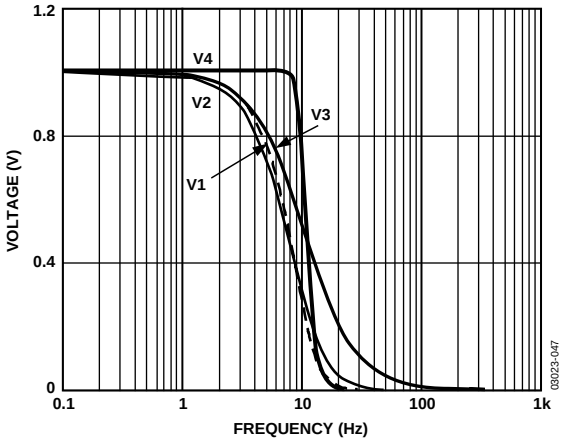


Figure 48. Frequency Response Output at Different Stages of the Low-Pass Filter

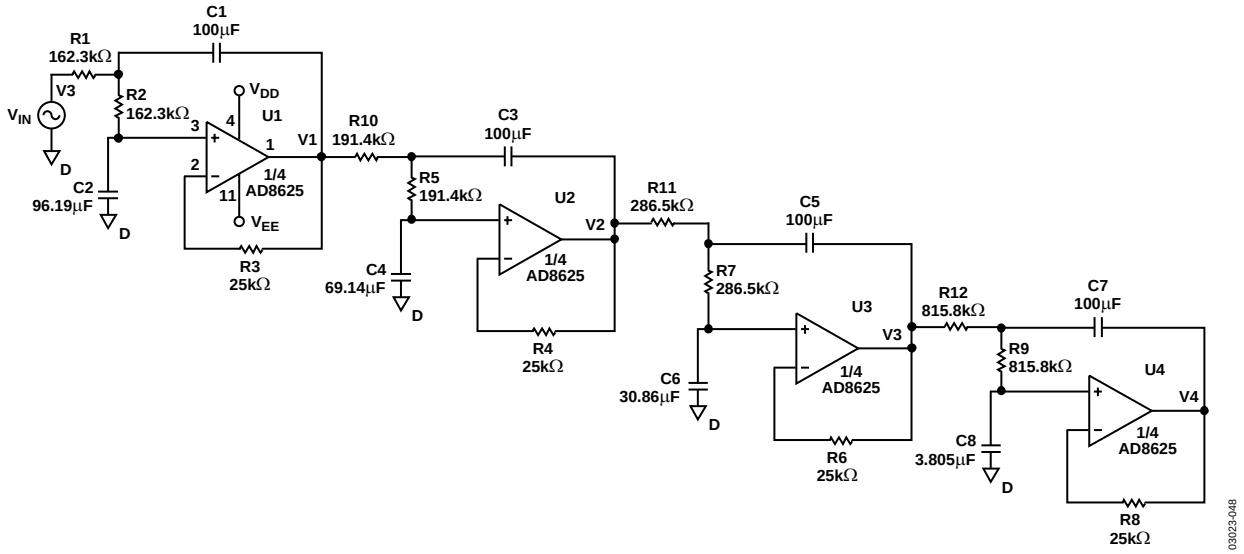
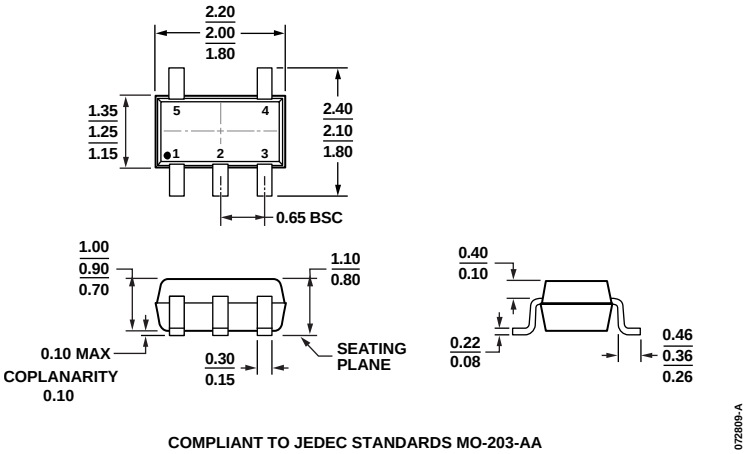


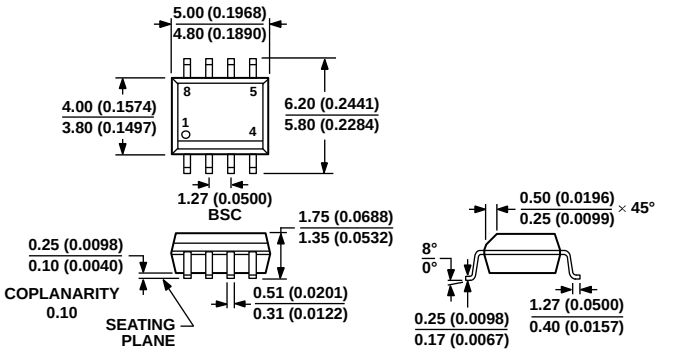
Figure 49. 10 Hz, 8-Pole Sallen Key Low-Pass Filter

OUTLINE DIMENSIONS



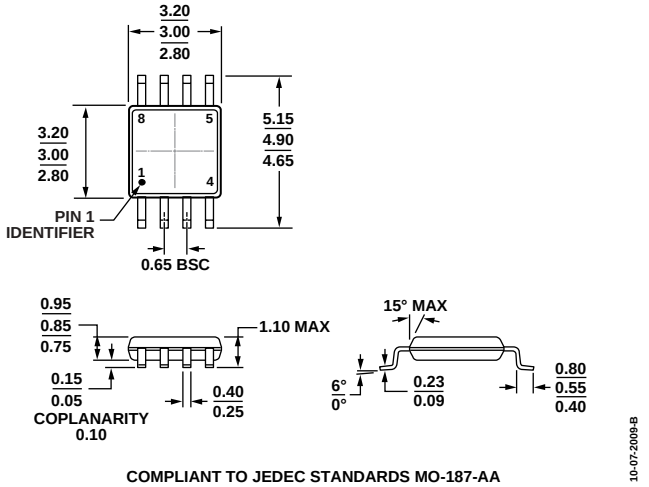
COMPLIANT TO JEDEC STANDARDS MO-203-AA

Figure 50. 5-Lead Plastic Surface-Mount Package [SC70]
(KS-5)
Dimensions shown in millimeters



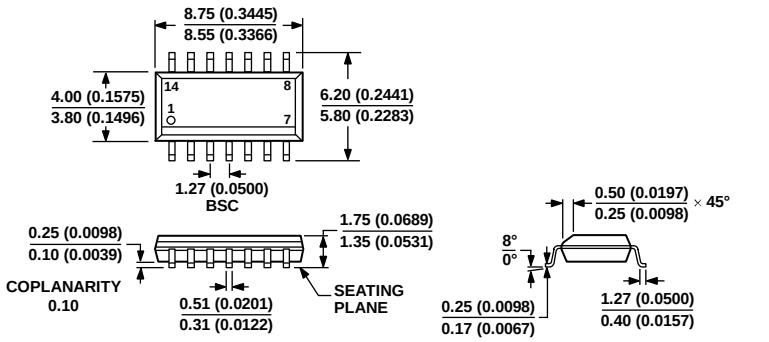
COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 51. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)



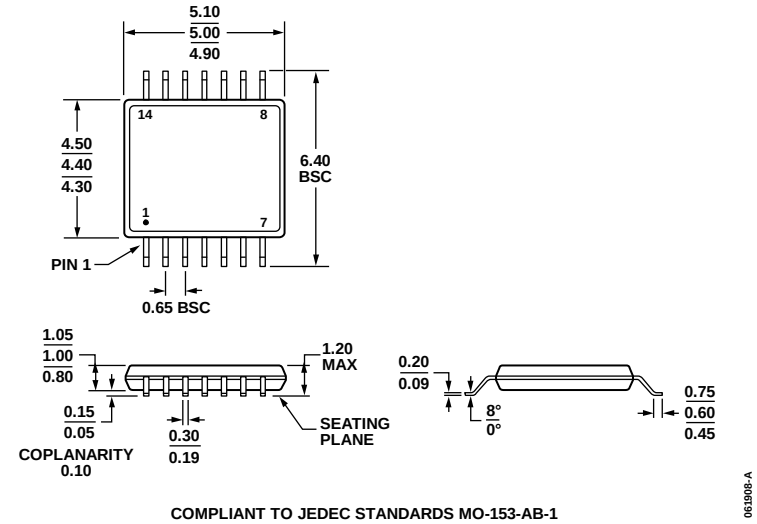
COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 52. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 53. 14-Lead Standard Small Outline Package [SOIC_N]
(R-14)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 54. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option	Branding
AD8625ARUZ	–40°C to +85°C	14-Lead TSSOP	RU-14	
AD8625ARUZ-REEL	–40°C to +85°C	14-Lead TSSOP	RU-14	
AD8625ARZ	–40°C to +85°C	14-Lead SOIC_N	R-14	
AD8625ARZ-REEL	–40°C to +85°C	14-Lead SOIC_N	R-14	
AD8625ARZ-REEL7	–40°C to +85°C	14-Lead SOIC_N	R-14	
AD8626ARMZ-REEL	–40°C to +85°C	8-Lead MSOP	RM-8	BJA
AD8626ARMZ	–40°C to +85°C	8-Lead MSOP	RM-8	BJA
AD8626ARZ	–40°C to +85°C	8-Lead SOIC_N	R-8	
AD8626ARZ-REEL	–40°C to +85°C	8-Lead SOIC_N	R-8	
AD8626ARZ-REEL7	–40°C to +85°C	8-Lead SOIC_N	R-8	
AD8627AKSZ-REEL	–40°C to +85°C	5-Lead SC70	KS-5	B9B
AD8627AKSZ-REEL7	–40°C to +85°C	5-Lead SC70	KS-5	B9B
AD8627AKSZ-R2	–40°C to +85°C	5-Lead SC70	KS-5	B9B
AD8627ARZ	–40°C to +85°C	8-Lead SOIC_N	R-8	
AD8627ARZ-REEL	–40°C to +85°C	8-Lead SOIC_N	R-8	
AD8627ARZ-REEL7	–40°C to +85°C	8-Lead SOIC_N	R-8	

[1] Z = RoHS Compliant Part; # denotes product may be top or bottom marked.
[2] For the AD8627AKS models, pre-0542 parts were branded with B9A without #.