

Vishay Siliconix

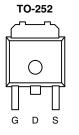
RoHS

COMPLIANT

HALOGEN

P-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	R _{DS(on)} (Ω) Max.	I _D (A)	Q _g (Typ.)	
- 40	0.0162 at V _{GS} = - 10 V	- 36	67	
- 40	0.0230 at V _{GS} = - 4.5 V	- 24	07	



Top View

Ordering Information: SUD45P04-16P-GE3 (Lead (Pb)-free and Halogen-free)

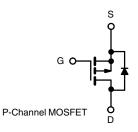
Drain Connected to Tab

FEATURES

- Halogen-free According to IEC 61249-2-21
 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_{α} and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- Power Switch
- · Load Switch in High Current Applications
- DC/DC Converters



ABSOLUTE MAXIMUM RATINGS	(T _C = 25 °C, unless ot	herwise noted)		
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	- 40	v
Gate-Source Voltage		V _{GS}	± 20	v
Continuous Drain Current (T 150 °C)	T _C = 25 °C	1-	- 36	
Continuous Drain Current (T _J = 150 °C)	T _C = 70 °C	I _D	- 29	٨
Pulsed Drain Current (t = 300 μs)		I _{DM}	- 100	- A
Avalanche Current		I _{AS}	- 32	
Single Avalanche Energy ^a	L = 0.1 mH	E _{AS}	51	mJ
Maximum Power Dissipation ^a	T _C = 25 °C	P	41.7 ^b	
	T _A = 25 °C ^c	– P _D –	2.1	— W
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Junction-to-Ambient (PCB Mount) ^c	R _{thJA}	60	°C/W	
Junction-to-Case (Drain)	R _{thJC}	3	°C/W	

Notes:

a. Duty cycle \leq 1 %.

b. See SOA curve for voltage derating.

c. When mounted on 1" square PCB (FR-4 material).

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	$V_{DS} = 0 V, I_{D} = -250 \mu A$	- 40			V 2.5
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -250 \ \mu A$	- 1		- 2.5	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 250	nA
		$V_{DS} = -40 \text{ V}, V_{GS} = 0 \text{ V}$			- 1	
Zero Gate Voltage Drain Current	I _{DSS}	V_{DS} = - 40 V, V_{GS} = 0 V, T_{J} = 125 °C			- 50	μΑ
		$V_{DS} = -40 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 150 ^{\circ}\text{C}$			- 250	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le$ - 10 V, V_{GS} = - 10 V	- 50			Α
	D	V _{GS} = - 10 V, I _D = - 14 A		0.0135	0.0162	Ω
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 12 A		0.0190	0.0230	
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 20 V, I _D = - 14 A		40		S
Dynamic ^b	•					
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = - 20 V, f = 1 MHz		2765		pF
Output Capacitance	C _{oss}			330		
Reverse Transfer Capacitance	C _{rss}			280		
Total Gate Charge ^c	Qg			67	100	
Gate-Source Charge ^c	Q _{gs}	$V_{DS} = -20 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -14 \text{ A}$		13.5		nC
Gate-Drain Charge ^c	Q _{gd}			14		
Gate Resistance	Rg	f = 1 MHz	0.5	2.5	5	Ω
Turn-On Delay Time ^c	t _{d(on)}			10	20	
Rise Time ^c	t _r	V_{DD} = - 20 V, R_L = 2 Ω		11	20	
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong$ - 10 A, V_{GEN} = - 10 V, R_g = 1 Ω		42	63	ns
Fall Time ^c	t _f			12	20	
Drain-Source Body Diode Ratings an	nd Characteri	stics T _C = 25 °C ^b				
Continuous Current	۱ _S				- 36	
Pulsed Current	I _{SM}				- 100	A
Forward Voltage ^a	V _{SD}	I _F = - 10 A, V _{GS} = 0 V		- 0.8	- 1.5	V
Reverse Recovery Time	t _{rr}			38	57	ns
Peak Reverse Recovery Current	I _{RM(REC)}	I _F = - 10 A, dI/dt = 100 A/μs		2.3	3.5	А
Reverse Recovery Charge	Q _{rr}	1 1		40	60	nC

Notes:

a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

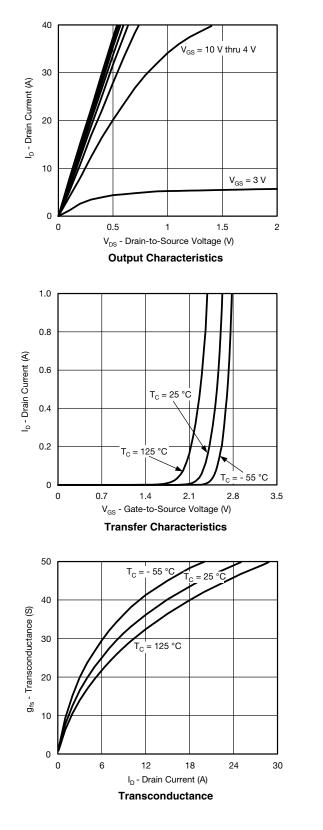
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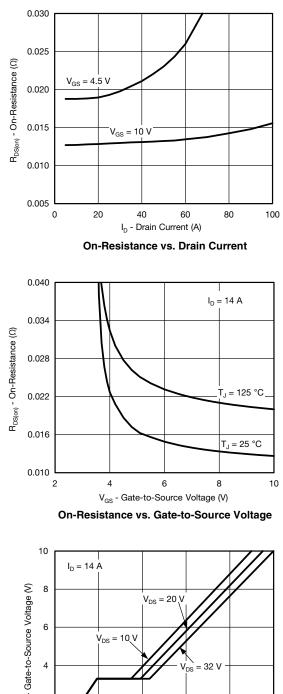
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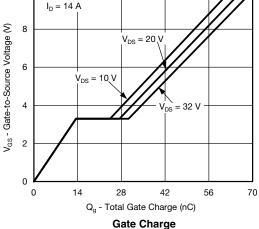


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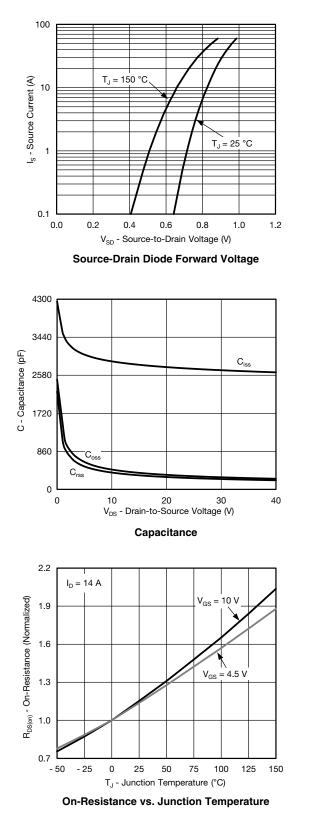
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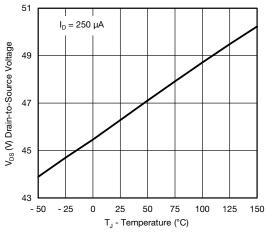


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

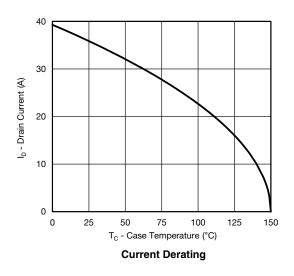


2.3 I_D = 250 μA 2.0 V_{GS(th)} (V) 1.7 1.4 1.1 - 50 - 25 100 150 0 25 50 75 125 T_J - Temperature (°C)

Threshold Voltage



Drain Source Breakdown vs. Junction Temperature



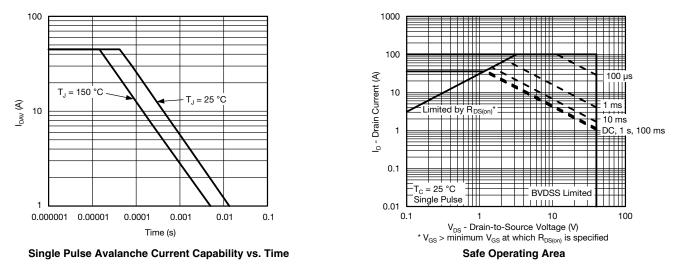
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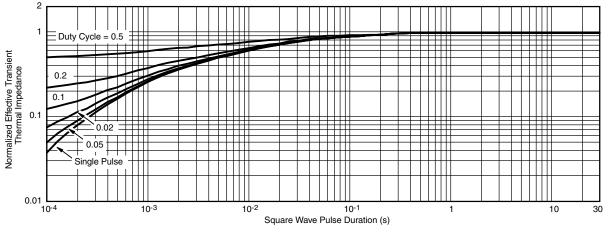
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





Normalized Thermal Transient Impedance, Junction-to-Case

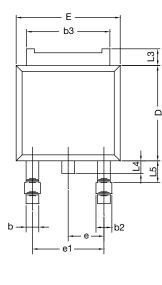
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63372.

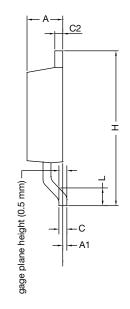
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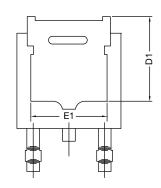


TO-252AA Case Outline

VERSION 1: FACILITY CODE = Y







	MILLIMETERS		
DIM.	MIN.	MAX.	
А	2.18	2.38	
A1	-	0.127	
b	0.64	0.88	
b2	0.76	1.14	
b3	4.95	5.46	
С	0.46	0.61	
C2	0.46	0.89	
D	5.97	6.22	
D1	4.10	-	
E	6.35	6.73	
E1	4.32	-	
Н	9.40	10.41	
е	2.28 BSC		
e1	4.56 BSC		
L	1.40	1.78	
L3	0.89	1.27	
L4	-	1.02	
L5	1.01	1.52	

Note

• Dimension L3 is for reference only



VERSION 2: FACILITY CODE = N



	MILLIMETERS		
DIM.	MIN.	MAX.	
А	2.18	2.39	
A1	-	0.13	
b	0.65	0.89	
b1	0.64	0.79	
b2	0.76	1.13	
b3	4.95	5.46	
с	0.46	0.61	
c1	0.41	0.56	
c2	0.46	0.60	
D	5.97	6.22	
D1	5.21	-	
E	6.35	6.73	
E1	4.32	-	
e	2.29 BSC		
Н	9.94	10.34	

	MILLIMETERS		
DIM.	MIN.	MAX.	
L	1.50	1.78	
L1	2.74 ref.		
L2	0.51 BSC		
L3	0.89	1.27	
L4	-	1.02	
L5	1.14	1.49	
L6	0.65	0.85	
θ	0°	10°	
θ1	0° 15°		
θ2	25°	35°	

Notes

Dimensioning and tolerance confirm to ASME Y14.5M-1994

All dimensions are in millimeters. Angles are in degrees

Heat sink side flash is max. 0.8 mm

Radius on terminal is optional •

ECN: E19-0649-Rev. Q, 16-Dec-2019 DWG: 5347

Revision: 16-Dec-2019

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RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads Dimensions in Inches/(mm)

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