This version (26 Jun 2014 16:43) was ***approved*** by JasonC, Connor.kang, Keiichi.Okuji.
The Previously approved version (06 Feb 2014 23:24) is available.

DPG3

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The DPG3, or Data Pattern Generator 3, is a device designed to support the evaluation of Analog Devices' High-Speed Digital-to-Analog Converters (DAC). The device is connected to a PC over USB, and allows a user to download a data vector into the DPG3, which is then played out to an attached DAC evaluation board at full speed.

Please note: *Analog Devices' pattern generators and high-speed DAC evaluation boards are designed and sold solely to support an efficient and thorough means by which to evaluate Analog Devices high speed DACs in a lab environment for a wide range of end applications. Any application or use of the pattern generators and/or high-speed DAC evaluation boards, other than specified above, will not be supported.*

This page describes the hardware of DPG3. The device can be driven from many different software applications. For more information on the software, please see the High-Speed DAC Software Suite documentation.

For information on the DPG2, the predecessor to the DPG3, please see the DPG2 page.

Ordering Code

The part number for the DPG3 is AD-DPG3.

To order an DPG3, please visit the DPG3 Ordering Page

Hardware Specifications

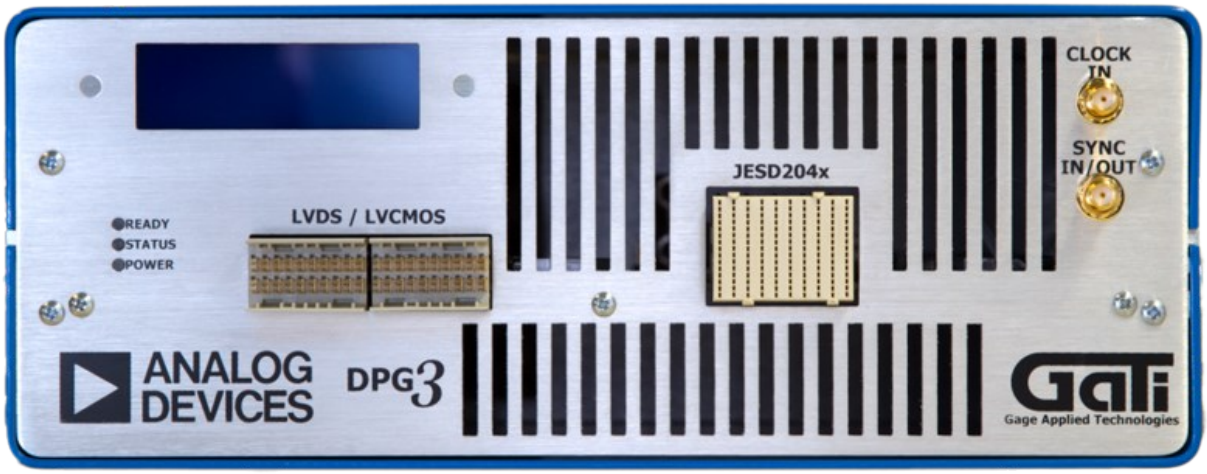
Please note that not all hardware options and specifications are supported with any particular evaluation board or software package. Specifications are subject to change without notice.

- Converter Interfaces
  - CMOS Interface
    - 32-bits (shared with the P lines of the LVDS bus)
    - Up to 250Mbps per bit(SDR)
    - Same connector and pinout as DPG2
  - LVDS Interface
    - 32-bits (P lines shared with CMOS interface)
    - Up to 1.6Gbps per bit (800MHz DDR)
    - Same connector and pinout as DPG2
  - High-Speed Serial Interface *(For JESD204 Converters)*
    - 16 Tx lanes
    - Up to 8.5Gbps per lane
- Memory
  - Dual DDR3 SO-DIMM

- Maximum pattern length of 134M samples (*limited to 30M samples in most 3'rd party software*)

- PC Interface
  - USB 2.0 “B” connector
- Clocking
  - On-connector clock input for all interfaces
  - Optional external clock input via front-panel SMA jack for CMOS and LVDS interfaces
- Trigger
  - SMA jack for trigger input or output
- Specified for operation at 25ºC only

Some PCs with USB 3.0 *SuperSpeed* ports have been unable to communicate reliably with the DPG3. On these PCs, the standard USB 2.0 ports (without the SS logo) should be used with the DPG3.



Output Data

The vector length must be at least 64 points per channel, and the vector length must be divisible by 64 for proper operation.

Clocking

The clocking system varies between the traditional CMOS/LVDS interfaces and the newer high-speed serial interface. In all cases, the DPG needs to be provided with a clock. It cannot generate a data clock internally.

CMOS/LVDS

Most evaluation boards will supply a clock to the DPG over the CMOS/LVDS connector. In all cases, this clock is LVDS, even if the rest of the interface is CMOS. A clock will be provided with the data that is synchronous to the data (source synchronous), which will match the format of the data.

ly via the SMA jack on the front of the unit. In this case, the clock's amplitude must be +4dBm. This

method is not recommended for general use. To enable the external clock operation, click the *Advanced/Debug* button in DPGDownloader, and select *Front panel SMA jack* as the Clock Source in the Clock section.

High-Speed Serial

The high-speed serial transceivers inside the DPG3 require a reference clock in order to be able to lock on to the embedded clock inside the serial data stream. This clock must be provided over the connector to the evaluation board.

External Trigger

The SMA jack on the front of the unit for the trigger can be used either as an input or as an output trigger. To enable the trigger, click *Advanced/Debug* in DPGDownloader, and check the *Enable Trigger* box in the Trigger section.

Input Trigger

When set as an input, the unit will start playback when the trigger is asserted (raised from low to high).

The input high threshold is 2.0V, and the input low threshold is 0.8V, allowing it to be directly interfaced with 3.3V logic signals.

Output Trigger

When set as an output, the trigger will pulse when the playback is running at the beginning of the vector. Therefore, it will pulse every time the vector is looped when in Loop mode, or only once if the unit is in Count mode.

Connector Pinouts

The DGP3 has two separate connector systems for interfacing with evaluation boards. One, for CMOS and LVDS interface DACs, is backwards compatible with the DPG2. The second connector is new to the DPG3, and supports high-speed serial, power, and communications.

CMOS/LVDS Pinout

The CMOS/LVDS connection on DPG2 and DPG3 uses two AMP/Tyco 1469169-1 connectors, placed side-by-side, with 139.2mil spacing between the centers of the innermost pins on both connectors. The mating connector on the evaluation board side is two AMP/Tyco 1469028-1. Note that both connectors are always required.

Left Side Connector

The left connector when looking at the connection on the DPG from the evaluation board side (J17 on the DPG2, J8 on the DPG3)

Pin	Name	Description
A1	CLK_DCOA_P	Data Clock Out from the DUT, into the DPG. Positive side of differential signal.(required)
B1	CLK_DCOA_N	Data Clock Out from the DUT, into the DPG. Negative side of differential signal.(required)
A2	CLK_TXI_O_P	Data Clock output from DPG, synchronous with “I” data. Positive side of differential signal.
B2	CLK_TXI_O_N	Data Clock output from DPG, synchronous with “I” data. Negative side of differential signal.
A3	TXI_DATA_P15	“I” channel data bit 15.
B3	TXI_DATA_N15	“I” channel data bit 15, negative side in LVDS mode. Not used in CMOS mode.
A4	TXI_DATA_P14	“I” channel data bit 14.
B4	TXI_DATA_N14	“I” channel data bit 14, negative side in LVDS mode. Not used in CMOS mode.
A5	TXI_DATA_P13	“I” channel data bit 13.
B5	TXI_DATA_N13	“I” channel data bit 13, negative side in LVDS mode. Not used in CMOS mode.
A6	TXI_DATA_P12	“I” channel data bit 12.
B6	TXI_DATA_N12	“I” channel data bit 12, negative side in LVDS mode. Not used in CMOS mode.
A7	TXI_DATA_P11	“I” channel data bit 11.
B7	TXI_DATA_N11	“I” channel data bit 11, negative side in LVDS mode. Not used in CMOS mode.
A8	TXI_DATA_P10	“I” channel data bit 10.
B8	TXI_DATA_N10	“I” channel data bit 10, negative side in LVDS mode. Not used in CMOS mode.

Pin	Name	Description
A9	TXI_DATA_P9	“I” channel data bit 9.
B9	TXI_DATA_N9	“I” channel data bit 9, negative side in LVDS mode. Not used in CMOS mode.
A10	TXI_DATA_P8	“I” channel data bit 8.
B10	TXI_DATA_N8	“I” channel data bit 8, negative side in LVDS mode. Not used in CMOS mode.
BG1	GROUND	Digital Ground
BG2	GROUND	Digital Ground
BG3	GROUND	Digital Ground
BG4	GROUND	Digital Ground
BG5	GROUND	Digital Ground
BG6	GROUND	Digital Ground
BG7	GROUND	Digital Ground
BG8	GROUND	Digital Ground
BG9	GROUND	Digital Ground
BG10	GROUND	Digital Ground
C1	N/C	No Connect (DPG2) / “Q” channel bi-directional, low-speed LVDS 1, positive side (DPG3)
D1	N/C	No Connect (DPG2) / “Q” channel bi-directional, low-speed LVDS 1, negative side (DPG3)
C2	N/C	No Connect (DPG2) / “Q” channel bi-directional, low-speed LVDS 0, positive side (DPG3)
D2	N/C	No Connect (DPG2) / “Q” channel bi-directional, low-speed LVDS 0, negative side (DPG3)
C3	TXQ_DATA_P15	“Q” channel data bit 15.
D3	TXQ_DATA_N15	“Q” channel data bit 15, negative side in LVDS mode. Not used in CMOS mode.
C4	TXQ_DATA_P14	“Q” channel data bit 14.
D4	TXQ_DATA_N14	“Q” channel data bit 14, negative side in LVDS mode. Not used in CMOS mode.
C5	TXQ_DATA_P13	“Q” channel data bit 13.
D5	TXQ_DATA_N13	“Q” channel data bit 13, negative side in LVDS mode. Not used in CMOS mode.
C6	TXQ_DATA_P12	“Q” channel data bit 12.
D6	TXQ_DATA_N12	“Q” channel data bit 12, negative side in LVDS mode. Not used in CMOS mode.
C7	TXQ_DATA_P11	“Q” channel data bit 11.
D7	TXQ_DATA_N11	“Q” channel data bit 11, negative side in LVDS mode. Not used in CMOS mode.
C8	TXQ_DATA_P10	“Q” channel data bit 10.
D8	TXQ_DATA_N10	“Q” channel data bit 10, negative side in LVDS mode. Not used in CMOS mode.
C9	TXQ_DATA_P9	“Q” channel data bit 9.
D9	TXQ_DATA_N9	“Q” channel data bit 9, negative side in LVDS mode. Not used in CMOS mode.
C10	TXQ_DATA_P8	“Q” channel data bit 8.
D10	TXQ_DATA_N8	“Q” channel data bit 8, negative side in LVDS mode. Not used in CMOS mode.
DG1	GROUND	Digital Ground
DG2	GROUND	Digital Ground
DG3	GROUND	Digital Ground
DG4	GROUND	Digital Ground

Pin	Name	Description
DG5	GROUND	Digital Ground
DG6	GROUND	Digital Ground
DG7	GROUND	Digital Ground
DG8	GROUND	Digital Ground
DG9	GROUND	Digital Ground
DG10	GROUND	Digital Ground

Right Side Connector

The right connector when looking at the connection on the DPG from the evaluation board side (J18 on the DPG2, J10 on the DPG3)

Pin	Name	Description
A1	TXI_DATA_P7	“I” channel data bit 7.
B1	TXI_DATA_N7	“I” channel data bit 7, negative side in LVDS mode. Not used in CMOS mode.
A2	TXI_DATA_P6	“I” channel data bit 6.
B2	TXI_DATA_N6	“I” channel data bit 6, negative side in LVDS mode. Not used in CMOS mode.
A3	TXI_DATA_P5	“I” channel data bit 5.
B3	TXI_DATA_N5	“I” channel data bit 5, negative side in LVDS mode. Not used in CMOS mode.
A4	TXI_DATA_P4	“I” channel data bit 4.
B4	TXI_DATA_N4	“I” channel data bit 4, negative side in LVDS mode. Not used in CMOS mode.
A5	TXI_DATA_P3	“I” channel data bit 3.
B5	TXI_DATA_N3	“I” channel data bit 3, negative side in LVDS mode. Not used in CMOS mode.
A6	TXI_DATA_P2	“I” channel data bit 2.
B6	TXI_DATA_N2	“I” channel data bit 2, negative side in LVDS mode. Not used in CMOS mode.
A7	TXI_DATA_P1	“I” channel data bit 1.
B7	TXI_DATA_N1	“I” channel data bit 1, negative side in LVDS mode. Not used in CMOS mode.
A8	TXI_DATA_P0	“I” channel data bit 0.
B8	TXI_DATA_N0	“I” channel data bit 0, negative side in LVDS mode. Not used in CMOS mode.
A9	N/C	No Connect (DPG2) / “I” channel bi-directional, low-speed LVDS 1, positive side (DPG3)
B9	N/C	No Connect (DPG2) / “I” channel bi-directional, low-speed LVDS 1, negativeside (DPG3)
A10	N/C	No Connect (DPG2) / “I” channel bi-directional, low-speed LVDS 0, positive side (DPG3)
B10	N/C	No Connect (DPG2) / “I” channel bi-directional, low-speed LVDS 0, negative side (DPG3)
BG1	GROUND	Digital Ground
BG2	GROUND	Digital Ground
BG3	GROUND	Digital Ground
BG4	GROUND	Digital Ground
BG5	GROUND	Digital Ground
BG6	GROUND	Digital Ground
BG7	GROUND	Digital Ground
BG8	GROUND	Digital Ground
BG9	GROUND	Digital Ground

Pin	Name	Description
BG10	GROUND	Digital Ground
C1	TXQ_DATA_P7	“Q” channel data bit 7.
D1	TXQ_DATA_N7	“Q” channel data bit 7, negative side in LVDS mode. Not used in CMOS mode.
C2	TXQ_DATA_P6	“Q” channel data bit 6.
D2	TXQ_DATA_N6	“Q” channel data bit 6, negative side in LVDS mode. Not used in CMOS mode.
C3	TXQ_DATA_P5	“Q” channel data bit 5.
D3	TXQ_DATA_N5	“Q” channel data bit 5, negative side in LVDS mode. Not used in CMOS mode.
C4	TXQ_DATA_P4	“Q” channel data bit 4.
D4	TXQ_DATA_N4	“Q” channel data bit 4, negative side in LVDS mode. Not used in CMOS mode.
C5	TXQ_DATA_P3	“Q” channel data bit 3.
D5	TXQ_DATA_N3	“Q” channel data bit 3, negative side in LVDS mode. Not used in CMOS mode.
C6	TXQ_DATA_P2	“Q” channel data bit 2.
D6	TXQ_DATA_N2	“Q” channel data bit 2, negative side in LVDS mode. Not used in CMOS mode.
C7	TXQ_DATA_P1	“Q” channel data bit 1.
D7	TXQ_DATA_N1	“Q” channel data bit 1, negative side in LVDS mode. Not used in CMOS mode.
C8	TXQ_DATA_P0	“Q” channel data bit 0.
D8	TXQ_DATA_N0	“Q” channel data bit 0, negative side in LVDS mode. Not used in CMOS mode.
C9	CLK_TXQ_O_P	Data Clock output from DPG, synchronous with “Q” data. Positive side of differential signal.
D9	CLK_TXQ_O_N	Data Clock output from DPG, synchronous with “Q” data. Negative side of differential signal.
C10	CLK_DCOB_P	Data Clock Out from the DUT, into the DPG. Positive side of differential signal. Must be phase and frequency locked with CLK_DCOA. (required for DPG2)
D10	CLK_DCOB_N	Data Clock Out from the DUT, into the DPG. Negative side of differential signal. Must be phase and frequency locked with CLK_DCOA. (required for DPG2)
DG1	GROUND	Digital Ground
DG2	GROUND	Digital Ground
DG3	GROUND	Digital Ground
DG4	GROUND	Digital Ground
DG5	GROUND	Digital Ground
DG6	GROUND	Digital Ground
DG7	GROUND	Digital Ground
DG8	GROUND	Digital Ground
DG9	GROUND	Digital Ground
DG10	GROUND	Digital Ground

High-Speed Serial Connector

The second connector system on the DPG3 uses an FCi AirMax connector, part number 10057041-101LF. The mating connector used on the evaluation board is part number 10037324-101LF.

Pin	Name	Description
A1	SCL	I2C Clock for communicating with evaluation board
		ıicating with evaluation board

Pin	Name	Description
C1	GROUND	Digital Ground
D1	ALIGN_TX_N	SYSREF clock input for Tx
E1	ALIGN_TX_P	SYSREF clock input for Tx
F1	GROUND	Digital Ground
G1	FRAME_TX_N	Device clock input for Tx
H1	FRAME_TX_P	Device clock input for Tx
I1	GROUND	Digital Ground
J1	TXSYNC2_N	SYNC input for Tx (secondary)
K1	TXSYNC2_P	SYNC input for Tx (secondary)
L1	GROUND	Digital Ground
M1	TXSYNC1_N	SYNC input for Tx
N1	TXSYNC1_P	SYNC input for Tx
O1	GROUND	Digital Ground
A2	GPIO3	General-Purpose I/O 3
B2	PWR_SENSE	Pulled up to 3.3V on the evaluation board to allow the DPG3 to detect when a board is powered
C2	BRD_DETECT	Tied to ground on the evaluation board to allow the DPG3 to detect a connected board
D2	GROUND	Digital Ground
E2	RX13_N	Receive SERDES Lane (into FPGA) 13*
F2	RX13_P	Receive SERDES Lane (into FPGA) 13*
G2	GROUND	Digital Ground
H2	TX9_N	Transmit SERDES Lane (from FPGA) 9
I2	TX9_P	Transmit SERDES Lane (from FPGA) 9
J2	GROUND	Digital Ground
K2	RX5_N	Receive SERDES Lane (into FPGA) 5*
L2	RX5_P	Receive SERDES Lane (into FPGA) 5*
M2	GROUND	Digital Ground
N2	TX1_N	Transmit SERDES Lane (from FPGA) 1
O2	TX1_P	Transmit SERDES Lane (from FPGA) 1
A3	GROUND	Power Ground
B3	+6V0	+6V Power
C3	GROUND	Digital Ground
D3	RX14_N	Receive SERDES Lane (into FPGA) 14*
E3	RX14_P	Receive SERDES Lane (into FPGA) 14*
F3	GROUND	Digital Ground
G3	TX10_N	Transmit SERDES Lane (from FPGA) 10
H3	TX10_P	Transmit SERDES Lane (from FPGA) 10
I3	GROUND	Digital Ground
J3	RX6_N	Receive SERDES Lane (into FPGA) 6*

Pin	Name	Description
K3	RX6_P	Receive SERDES Lane (into FPGA) 6*
L3	GROUND	Digital Ground
M3	TX2_N	Transmit SERDES Lane (from FPGA) 2
N3	TX2_P	Transmit SERDES Lane (from FPGA) 2
O3	GROUND	Digital Ground
A4	+6V0	+6V Power
B4	GROUND	Power Ground
C4	+6V0	+6V Power
D4	GROUND	Digital Ground
E4	RX15_N	Receive SERDES Lane (into FPGA) 15*
F4	RX15_P	Receive SERDES Lane (into FPGA) 15*
G4	GROUND	Digital Ground
H4	TX11_N	Transmit SERDES Lane (from FPGA) 11
I4	TX11_P	Transmit SERDES Lane (from FPGA) 11
J4	GROUND	Digital Ground
K4	RX7_N	Receive SERDES Lane (into FPGA) 7*
L4	RX7_P	Receive SERDES Lane (into FPGA) 7*
M4	GROUND	Digital Ground
N4	TX3_N	Transmit SERDES Lane (from FPGA) 3
O4	TX3_P	Transmit SERDES Lane (from FPGA) 3
A5	GROUND	Power Ground
B5	+6V0	+6V Power
C5	GROUND	Digital Ground
D5	RX16_N	Receive SERDES Lane (into FPGA) 16*
E5	RX16_P	Receive SERDES Lane (into FPGA) 16*
F5	GROUND	Digital Ground
G5	TX12_N	Transmit SERDES Lane (from FPGA) 12
H5	TX12_P	Transmit SERDES Lane (from FPGA) 12
I5	GROUND	Digital Ground
J5	RX8_N	Receive SERDES Lane (into FPGA) 8*
K5	RX8_P	Receive SERDES Lane (into FPGA) 8*
L5	GROUND	Digital Ground
M5	TX4_N	Transmit SERDES Lane (from FPGA) 4
N5	TX4_P	Transmit SERDES Lane (from FPGA) 4
O5	GROUND	Digital Ground
A6	+6V0	+6V Power
B6	GROUND	Power Ground
C6	+6V0	+6V Power

Pin	Name	Description
D6	GROUND	Digital Ground
E6	TX13_N	Transmit SERDES Lane (from FPGA) 13
F6	TX13_P	Transmit SERDES Lane (from FPGA) 13
G6	GROUND	Digital Ground
H6	RX9_N	Receive SERDES Lane (into FPGA) 9*
I6	RX9_P	Receive SERDES Lane (into FPGA) 9*
J6	GROUND	Digital Ground
K6	TX5_N	Transmit SERDES Lane (from FPGA) 5
L6	TX5_P	Transmit SERDES Lane (from FPGA) 5
M6	GROUND	Digital Ground
N6	RX1_N	Receive SERDES Lane (into FPGA) 1*
O6	RX1_P	Receive SERDES Lane (into FPGA) 1*
A7	CS3	SPI Chip Select 3†
B7	CS6	SPI Chip Select 6†
C7	GROUND	Digital Ground
D7	TX14_N	Transmit SERDES Lane (from FPGA) 14
E7	TX14_P	Transmit SERDES Lane (from FPGA) 14
F7	GROUND	Digital Ground
G7	RX10_N	Receive SERDES Lane (into FPGA) 10*
H7	RX10_P	Receive SERDES Lane (into FPGA) 10*
I7	GROUND	Digital Ground
J7	TX6_N	Transmit SERDES Lane (from FPGA) 6
K7	TX6_P	Transmit SERDES Lane (from FPGA) 6
L7	GROUND	Digital Ground
M7	RX2_N	Receive SERDES Lane (into FPGA) 2*
N7	RX2_P	Receive SERDES Lane (into FPGA) 2*
O7	GROUND	Digital Ground
A8	CS2	SPI Chip Select 2†
B8	CS5	SPI Chip Select 5†
C8	CS7	SPI Chip Select 7†
D8	GROUND	Digital Ground
E8	TX15_N	Transmit SERDES Lane (from FPGA) 15
F8	TX15_P	Transmit SERDES Lane (from FPGA) 15
G8	GROUND	Digital Ground
H8	RX11_N	Receive SERDES Lane (into FPGA) 11*
I8	RX11_P	Receive SERDES Lane (into FPGA) 11*
J8	GROUND	Digital Ground
K8	TX7_N	Transmit SERDES Lane (from FPGA) 7

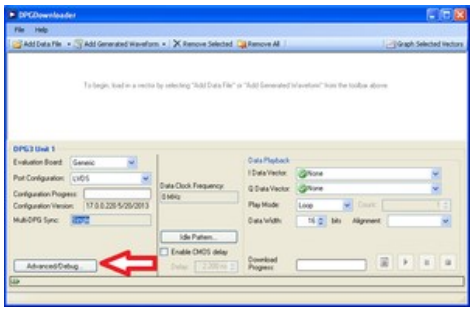
Pin	Name	Description
L8	TX7_P	Transmit SERDES Lane (from FPGA) 7
M8	GROUND	Digital Ground
N8	RX3_N	Receive SERDES Lane (into FPGA) 3*
O8	RX3_P	Receive SERDES Lane (into FPGA) 3*
A9	CS1	SPI Chip Select 1†
B9	CS4	SPI Chip Select 4†
C9	GROUND	Digital Ground
D9	TX16_N	Transmit SERDES Lane (from FPGA) 16
E9	TX16_P	Transmit SERDES Lane (from FPGA) 16
F9	GROUND	Digital Ground
G9	RX12_N	Receive SERDES Lane (into FPGA) 12*
H9	RX12_P	Receive SERDES Lane (into FPGA) 12*
I9	GROUND	Digital Ground
J9	TX8_N	Transmit SERDES Lane (from FPGA) 8
K9	TX8_P	Transmit SERDES Lane (from FPGA) 8
L9	GROUND	Digital Ground
M9	RX4_N	Receive SERDES Lane (into FPGA) 4*
N9	RX4_P	Receive SERDES Lane (into FPGA) 4*
O9	GROUND	Digital Ground
A10	MISO	SPI Master-In, Slave-Out Data†
B10	MOSI	SPI Master-Out, Slave-In Data†
C10	SCLK	SPI Clock†
D10	GROUND	Digital Ground
E10	ALIGN_RX_N	SYSREF clock input for Rx*
F10	ALIGN_RX_P	SYSREF clock input for Rx*
G10	GROUND	Digital Ground
H10	FRAME_RX_N	Device clock input for Rx*
I10	FRAME_RX_P	Device clock input for Rx*
J10	GROUND	Digital Ground
K10	RXSYNC2_N	SYNC input for Rx (secondary)*
L10	RXSYNC2_P	SYNC input for Rx (secondary)*
M10	GROUND	Digital Ground
N10	RXSYNC1_N	SYNC input for Rx*
O10	RXSYNC1_P	SYNC input for Rx*

** The RX SERDES lines are not enabled, and can not be used with JESD204 ADCs*

† The SPI lines are not enabled. Communication with parts on the evaluation board is performed over the I2C link, and converted into SPI on the evaluation board

Firmware Update

The firmware of the DPG3 can be updated when new features or fixes are available. To update the firmware, click the *Advanced/Debug* button in DPGDownloader. Click the *Update* button in the Firmware section, and select the new firmware file. Do not interrupt the firmware update process. The unit may become inoperable if the update process is interrupted.



Legacy CMOS Evaluation Boards

Some legacy evaluation boards for DACs with a CMOS data interface use a ribbon cable to connect to a pattern generator, instead of connecting directly. To use these boards on a DPG3, an adapter board is required. Please contact DPG Support to request this adapter board.

Support

Please contact DPG Support with any additional questions regarding the DPG or DAC Software Suite.