Nine-Output 3.3 V Buffer

Features

- One-input to nine-output buffer/driver

- Supports two DIMMs or four SO-DIMMs with one additional output for feedback to an external or chipset phase-locked loop (PLL)

- Low power consumption for mobile applications
  - Less than 32 mA at 66.6 MHz with unloaded outputs

- 1-ns input-output delay

- Buffers all frequencies from 2 MHz to 133.33 MHz

- Output-output skew less than 250 ps

- Multiple V_{DD} and V_{SS} pins for noise and electromagnetic interference (EMI) reduction

- Space-saving 16-pin 150-mil small-outline integrated circuit (SOIC) package

- 3.3-V operation

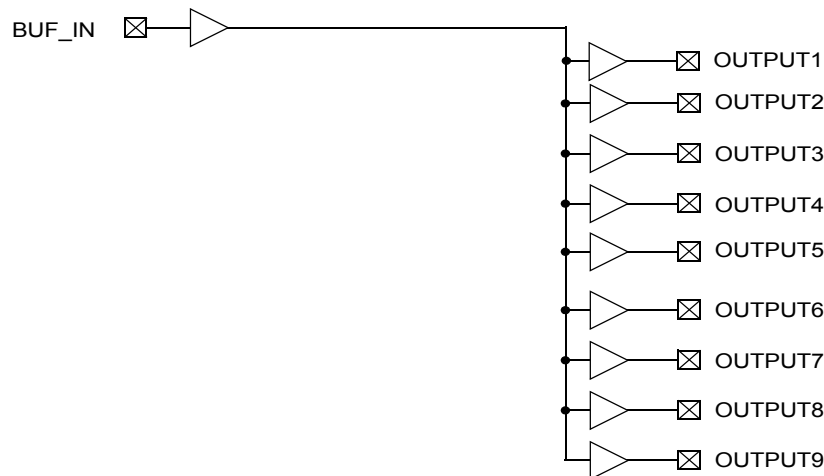- Industrial temperature available

Functional Description

The CY2309NZ is a low-cost buffer designed to distribute high-speed clocks in mobile PC systems and desktop PC systems with SDRAM support. The part has nine outputs, eight of which can be used to drive two DIMMs or four SO-DIMMs, and the remaining can be used for external feedback to a PLL. The device operates at 3.3 V and outputs can run up to 133.33 MHz.

The CY2309NZ is designed for low EMI and power optimization. It has multiple V_{SS} and V_{DD} pins for noise optimization and consumes less than 32 mA at 66.6 MHz, making it ideal for the low-power requirements of mobile systems. It is available in an ultra-compact 150-mil 16-pin SOIC package.

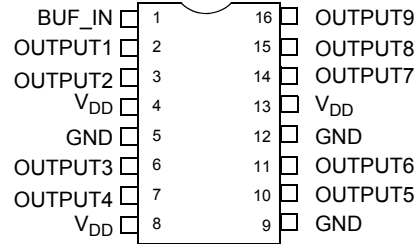For a complete list of related documentation, click here.

Logic Block Diagram

Contents

Pinout

Figure 1. 16-pin SOIC pinout (Top View)

```
            BUF_IN  ☐ 1        16 ☐  OUTPUT9
           OUTPUT1  ☐ 2        15 ☐  OUTPUT8
           OUTPUT2  ☐ 3        14 ☐  OUTPUT7
               VDD  ☐ 4        13 ☐  VDD
               GND  ☐ 5        12 ☐  GND
           OUTPUT3  ☐ 6        11 ☐  OUTPUT6
           OUTPUT4  ☐ 7        10 ☐  OUTPUT5
               VDD  ☐ 8         9 ☐  GND
```

Pin Descriptions

Pin	Signal	Description
4, 8, 13	V_{DD}	3.3-V digital voltage supply
5, 9, 12	GND	Ground
1	BUF_IN	Input clock
2, 3, 6, 7, 10, 11, 14, 15, 16	OUTPUT [1:9]	Outputs

Maximum Ratings

Supply voltage to ground potential ....–0.5 V to +7.0 V

DC input voltage ....–0.5 V to 7.0 V

Storage temperature .... –65 °C to +150 °C

Junction temperature .... 150 °C

Static discharge voltage
(per MIL-STD-883, Method 3015) ....>2,000 V

Operating Conditions

For commercial and industrial temperature devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage	3.0	3.6	V
T_A	(Ambient operating temperature) commercial	0	70	°C
	(Ambient operating temperature) industrial	–40	85	°C
C_L	Load capacitance, Fout < 100 MHz	–	30	pF
	Load capacitance, 100 MHz < Fout < 133.33 MHz	–	15	pF
C_{IN}	Input capacitance	–	7	pF
BUF_IN, OUTPUT [1:9]	Operating frequency	2	133.33	MHz
t_{PU}	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics

For commercial and industrial temperature devices

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW voltage [1]		–	0.8	V
V_{IH}	Input HIGH voltage [1]		2.0	–	V
I_{IL}	Input LOW current	$V_{IN} = 0$ V	–	50.0	μA
I_{IH}	Input HIGH current	$V_{IN} = V_{DD}$	–	100.0	μA
V_{OL}	Output LOW voltage [2]	$I_{OL} = 8$ mA	–	0.4	V
V_{OH}	Output HIGH voltage [2]	$I_{OH} = –8$ mA	2.4	–	V
I_{DD}	Supply current	Unloaded outputs at 66.66 MHz	–	32	mA

Thermal Resistance

Parameter [3]	Description	Test Conditions	16-pin SOIC	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	111	°C/W
θ_{JC}	Thermal resistance (junction to case)		60	°C/W

Notes
1. BUF_IN input has a threshold voltage of V_{DD}/2.
2. Parameter is guaranteed by design and characterization. It is not 100% tested in production.
3. These parameters are guaranteed by design and are not tested.

Switching Characteristics

For commercial and industrial temperature devices [4]

Parameter	Description	Condition	Min	Typ	Max	Unit
	Duty cycle[5] = $t_2 \div t_1$	Measured at 1.4 V	40.0	50.0	60.0	%
t_3	Rise time[5]	Measured between 0.8 V and 2.0 V	–	–	1.50	ns
t_4	Fall time[5]	Measured between 0.8 V and 2.0 V	–	–	1.50	ns
t_5	Output to output skew[5]	All outputs equally loaded	–	–	250	ps
t_6	Propagation delay, BUF_IN Rising edge to Output Rising edge[5]	Measured at $V_{DD}/2$	1	5	9.2	ns

Notes
4. All parameters specified with loaded outputs.
5. Parameter is guaranteed by design and characterization. It is not 100% tested in production.

Switching Waveforms

Figure 2. Duty Cycle Timing
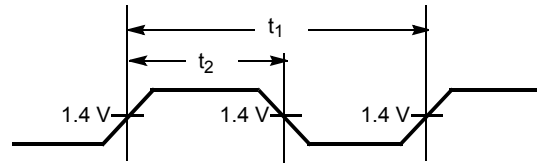
Figure 3. All Outputs Rise/Fall Time
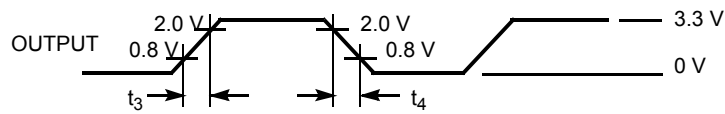
Figure 4. Output-Output Skew
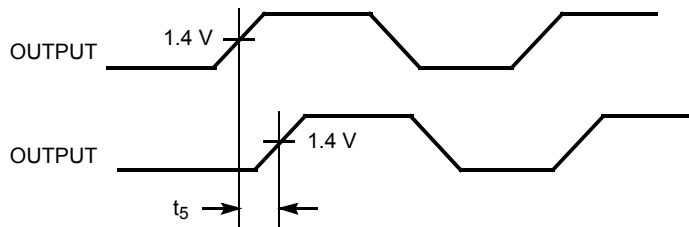
Figure 5. Input-Output Propagation Delay
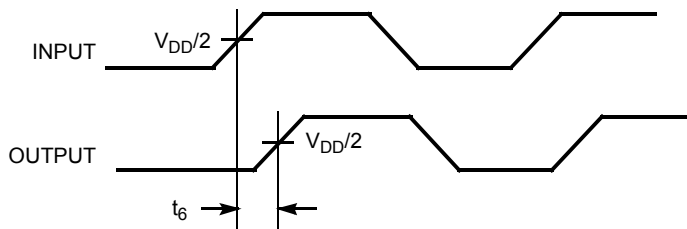
Test Circuits

Figure 6. Test Circuits
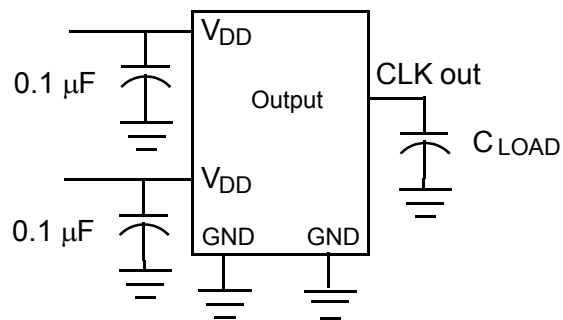
Ordering Information

Ordering Code	Package Type	Operating Range
Pb-free		
CY2309NZSXC-1H	16-pin SOIC (150 Mils)	Commercial
CY2309NZSXC-1HT	16-pin SOIC (150 Mils) – Tape and Reel	Commercial
CY2309NZSXI-1H	16-pin SOIC (150 Mils)	Industrial
CY2309NZSXI-1HT	16-pin SOIC (150 Mils) – Tape and Reel	Industrial

Ordering Code Definitions

CY 2309 NZ S X X - 1H X

X = blank or T
blank = Tube; T = Tape and Reel

High Output Drive Strength

Temperature Grade: X = C or I
C = Commercial; I = Industrial

Pb-free

Package Type:
S = 16-pin SOIC

Non Zero Delay Buffer

Base Part Number

Company ID: CY = Cypress
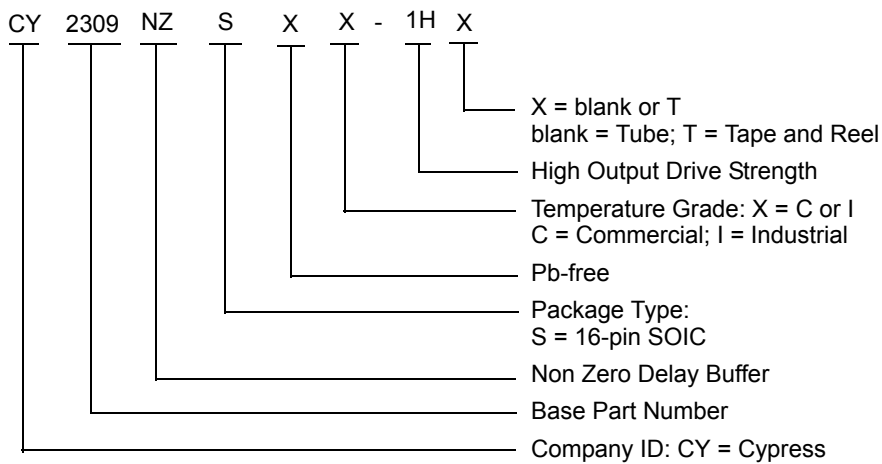
Package Diagram

Figure 7. 16-pin SOIC (150 Mils) S16.15/SZ16.15 Package Outline, 51-85068
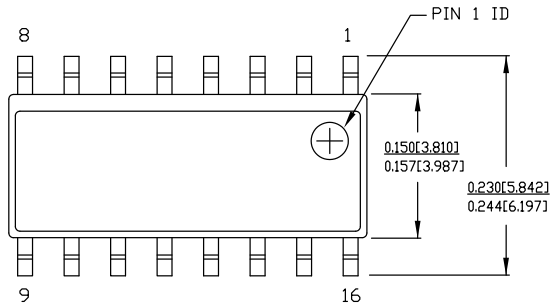
NOTE:

1. DIMENSIONS IN INCHES[MM] MAX.

2. REFERENCE JEDEC MS-012

3. PACKAGE WEIGHT : refer to PMDD spec. 001-04308

PART #	
S16.15	STANDARD PKG.
SZ16.15	LEAD FREE PKG.
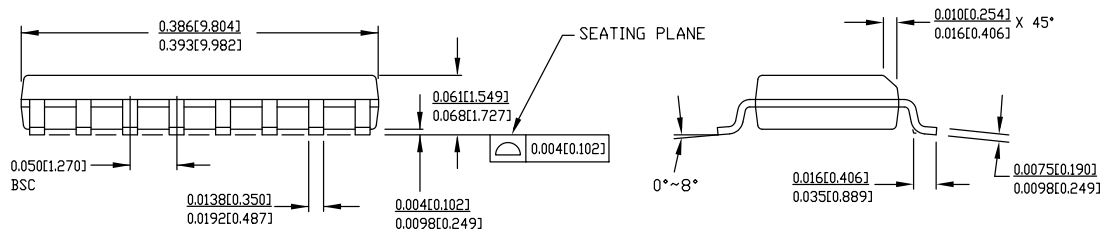
51-85068 *E

Acronyms

Acronym	Description
EMI	Electromagnetic Interference
PLL	Phase-Locked Loop
SOIC	Small-Outline Integrated Circuit

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
MHz	megahertz
μA	microampere
mA	milliampere
ms	millisecond
mV	millivolt
ns	nanosecond
pF	picofarad
V	volt

Document History Page

Document Title: CY2309NZ, Nine-Output 3.3 V Buffer				
Document Number: 38-07182				

Rev.	ECN	Orig. of Change	Submission Date	Description of Change
**	111858	DSG	12/09/01	Change from Spec number: 38-00709 to 38-07182
*A	121834	RBI	12/14/02	Power-up requirements added to Operating Conditions Information
*B	130563	SDR	10/23/03	Added industrial operating temperature to operating conditions
*C	212991	RGL / GGK	03/30/04	Updated the propagation delay T_6 spec to 9.2 ns in the Switching Characteristics table
*D	270149	RGL	10/04/04	Added Lead-free devices Replaced 8.7 ns Input/Output Delay to 1 ns Input/Output Delaying the features section
*E	2568533	AESA	09/23/08	Changed "SDRAM [1:9]" to "OUTPUT [1:9]" in Operating Conditions table. Removed part number CY2309NZSI-1H and CY2309NZSI-1HT. Added Note "Not recommended for new designs." Updated to new template.
*F	2904715	CXQ	04/05/10	Updated Ordering Information: Removed parts CY2309NZSC-1H, CY2309NZSC-1HT. Updated Package Diagram.
*G	3082147	CXQ	11/10/2010	Updated Maximum Ratings: Changed the following from: "DC Input Voltage (Except REF) .... –0.5 V to VDD + 0.5 V" "DC Input Voltage REF ....–0.5 V to 7.0 V" to: "DC Input Voltage ....–0.5 V to 7.0 V" Updated footnotes Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated to new template.
*H	4201460	CINM	11/25/2013	Updated Package Diagram: spec 51-85068 – Changed revision from *C to *E. Updated to new template. Completing Sunset Review.
*I	4578443	TAVA	11/25/2014	Updated Functional Description: Added "For a complete list of related documentation, click here." at the end.
*J	4715451	XHT	04/10/2015	Updated Operating Conditions: Updated minimum value of BUF_IN, OUTPUT [1:9] parameter as 5 MHz.
*K	4743611	TAVA	04/27/2015	Updated Operating Conditions: Changed minimum value of BUF_IN, OUTPUT [1:9] parameter from 5 MHz to 2 MHz. Updated to new template.
*L	5260404	PSR	05/05/2016	Added Thermal Resistance. Updated to new template.
*M	5553717	TAVA	12/14/2016	Updated to new template. Completing Sunset Review.

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Document Number: 38-07182 Rev. *M   Revised December 14, 2016   Page 11 of 11