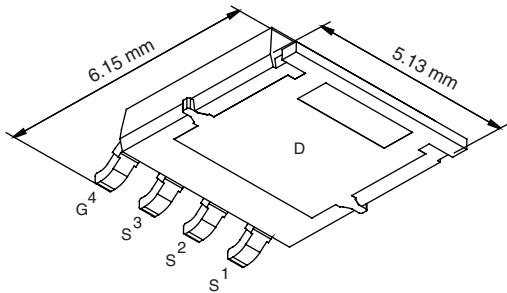




## N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a, g</sup>	Q <sub>g</sub> (Typ.)
30	0.0022 at V <sub>GS</sub> = 10 V	60	40.6 nC
	0.0026 at V <sub>GS</sub> = 4.5 V	60	

PowerPAK® SO-8L Single



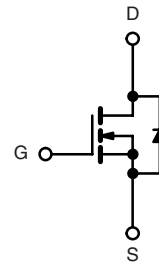
### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R<sub>g</sub> Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC


**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**

### APPLICATIONS

- POL
- VRM
- DC/DC Converters
- High Current Switching



N-Channel MOSFET

Ordering Information: SiJ458DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	30	V	
Gate-Source Voltage	V <sub>GS</sub>	± 20		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	A	
		T <sub>C</sub> = 70 °C		
		T <sub>A</sub> = 25 °C		
		T <sub>A</sub> = 70 °C		
Pulsed Drain Current	I <sub>DM</sub>	80	A	
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C		
		T <sub>A</sub> = 25 °C		
Single Pulse Avalanche Current	I <sub>AS</sub>	40	mJ	
Single Pulse Avalanche Energy	E <sub>AS</sub>	80		
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	W	
		T <sub>C</sub> = 70 °C		
		T <sub>A</sub> = 25 °C		
		T <sub>A</sub> = 70 °C		
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260		

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>b, f</sup>	R <sub>thJA</sub>	20	25	°C/W	
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	1.3	1.8		

Notes:

- Based on T<sub>C</sub> = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile ([www.vishay.com/ppg?73257](http://www.vishay.com/ppg?73257)). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 65 °C/W.
- Package limited.



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		32		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-6.7		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0		2.5	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.0018	0.0022	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$		0.0021	0.0026	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$		100		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		4810		pF
Output Capacitance	$C_{oss}$			892		
Reverse Transfer Capacitance	$C_{rss}$			444		
Total Gate Charge	$Q_g$	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		81	122	nC
		$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		40.6	61	
Gate-Source Charge	$Q_{gs}$			10.8		
Gate-Drain Charge	$Q_{gd}$		13.5			
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	0.4	1.1	2.2	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		16	30	ns
Rise Time	$t_r$			10	20	
Turn-Off Delay Time	$t_{d(off)}$			43	80	
Fall Time	$t_f$			9	18	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		38	75	
Rise Time	$t_r$			44	80	
Turn-Off Delay Time	$t_{d(off)}$			49	90	
Fall Time	$t_f$			24	45	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			60	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				80	
Body Diode Voltage	$V_{SD}$	$I_S = 4\text{ A}$		0.7	1.1	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		35	70	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			32	64	nC
Reverse Recovery Fall Time	$t_a$			17		ns
Reverse Recovery Rise Time	$t_b$			18		

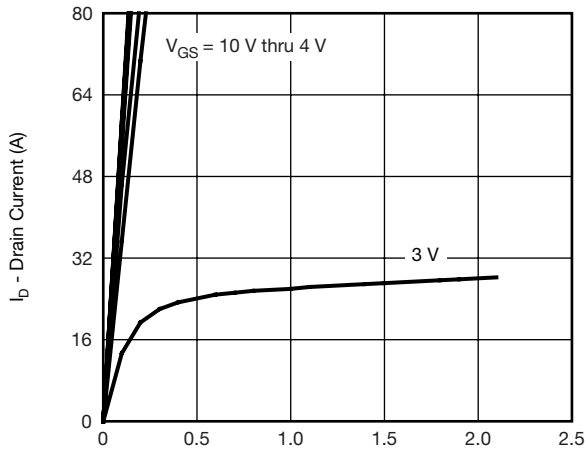
Notes:

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 b. Guaranteed by design, not subject to production testing.

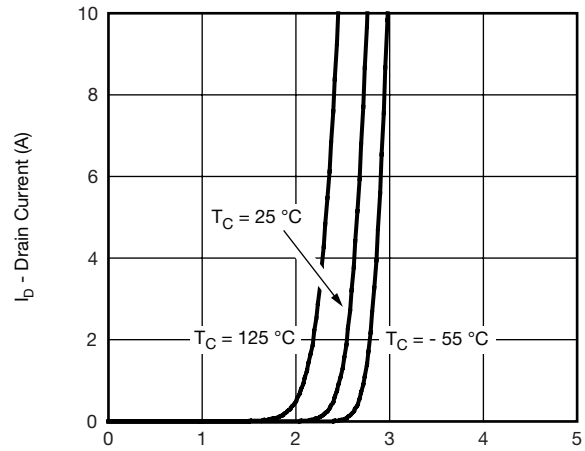
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



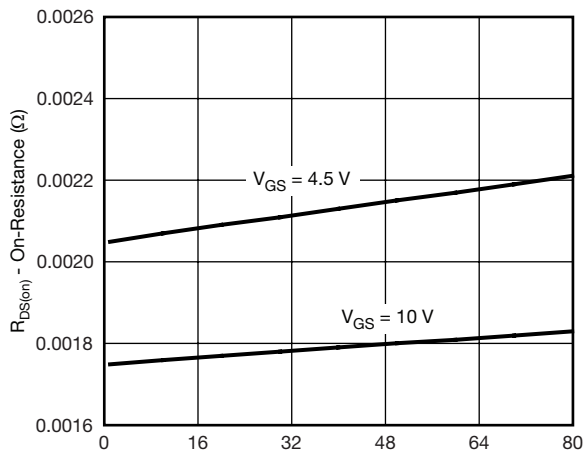
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



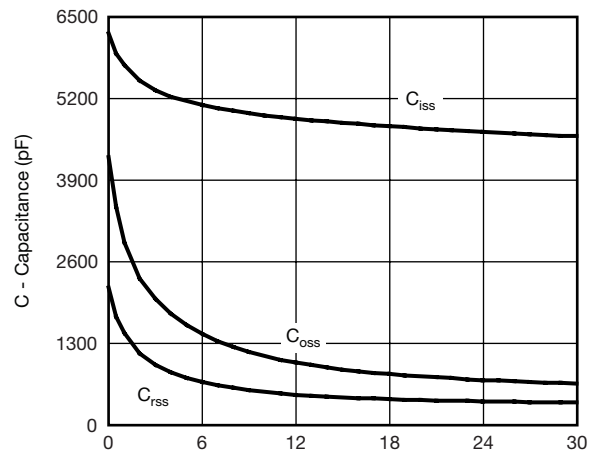
$V_{DS}$  - Drain-to-Source Voltage (V)  
**Output Characteristics**



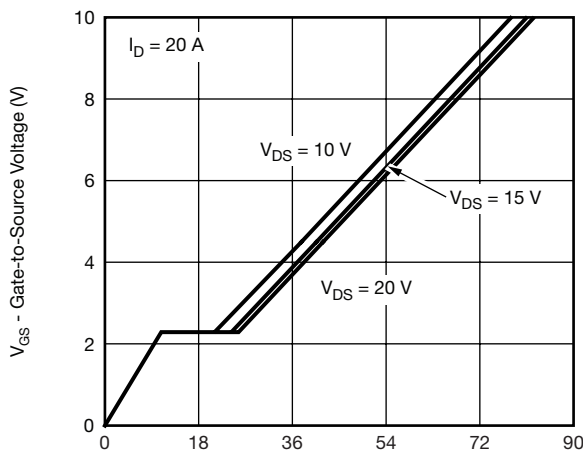
$V_{GS}$  - Gate-to-Source Voltage (V)  
**Transfer Characteristics**



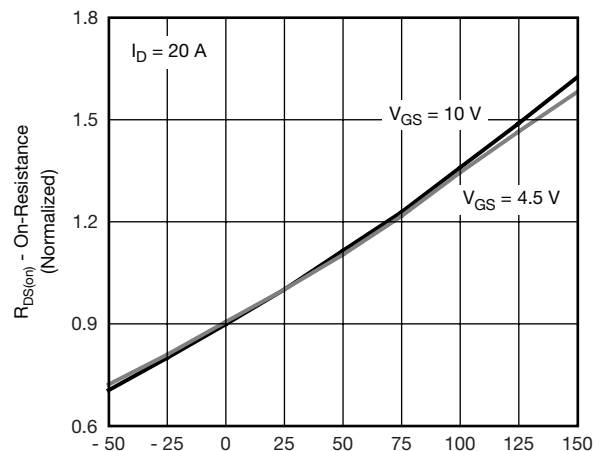
$I_D$  - Drain Current (A)  
**On-Resistance vs. Drain Current and Gate Voltage**



$V_{DS}$  - Drain-to-Source Voltage (V)  
**Capacitance**



$Q_g$  - Total Gate Charge  
**Gate Charge**



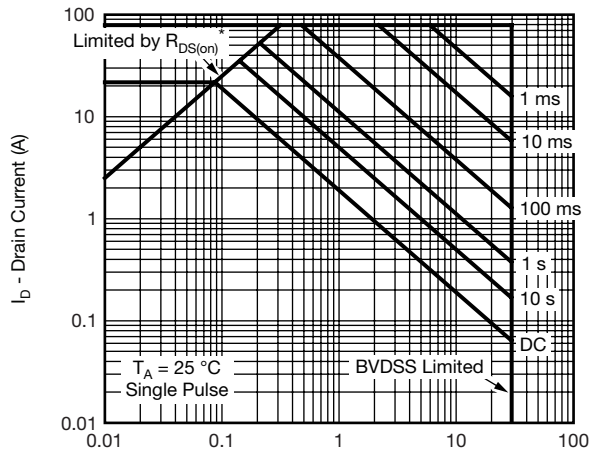
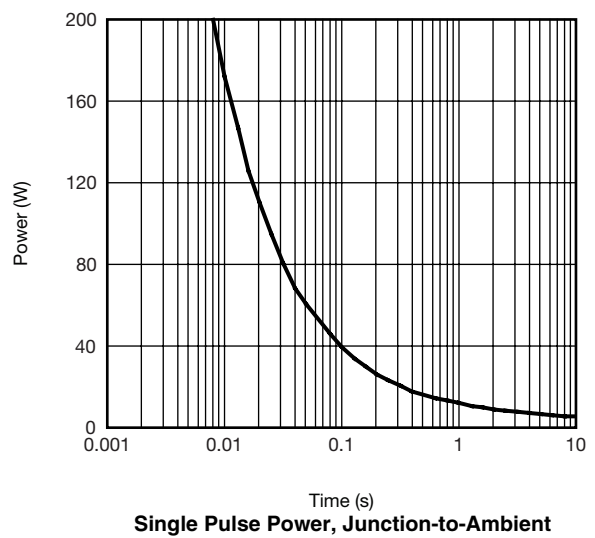
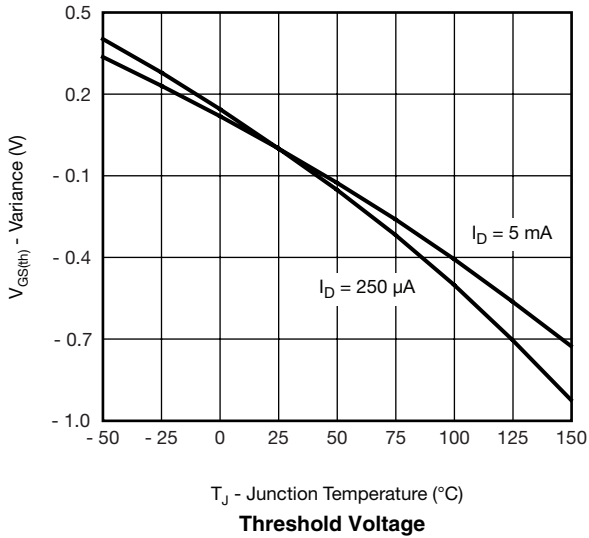
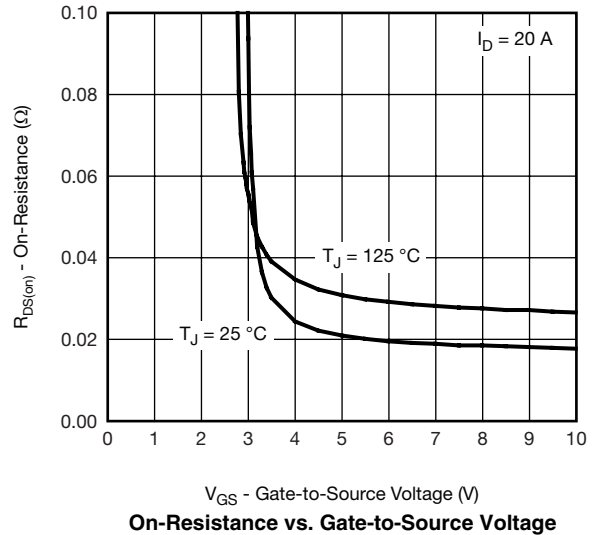
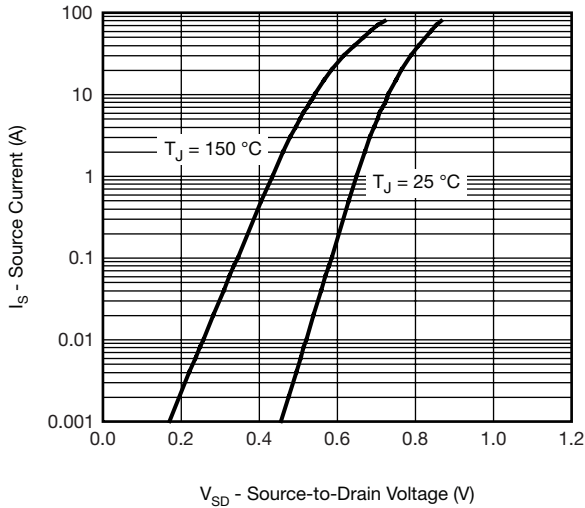
$T_J$  - Junction Temperature ( $^\circ\text{C}$ )  
**On-Resistance vs. Junction Temperature**

# SiJ458DP

Vishay Siliconix



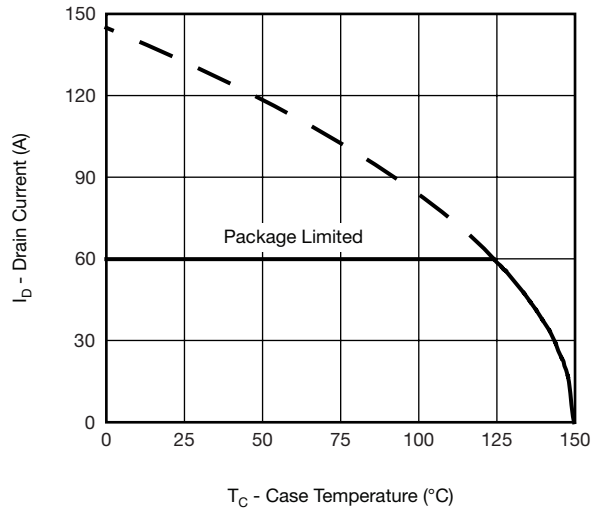
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



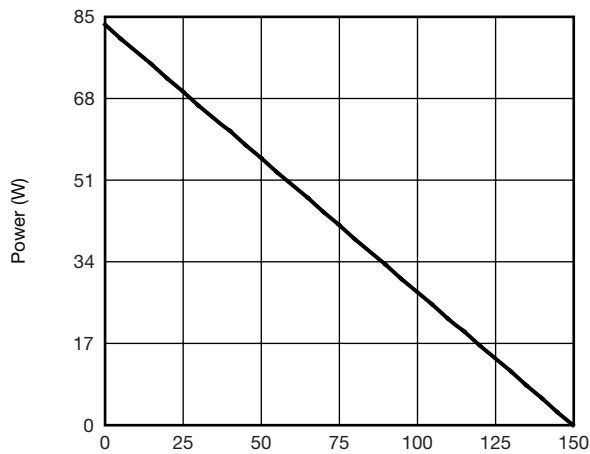
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



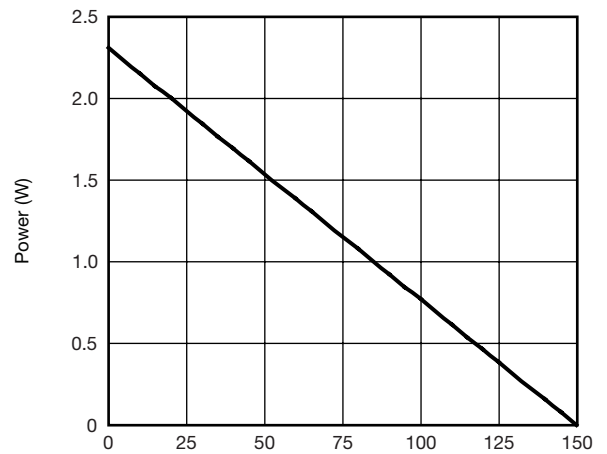
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**Current Derating\***



$T_C$  - Case Temperature (°C)  
**Power, Junction-to-Case**



$T_A$  - Ambient Temperature (°C)  
**Power, Junction-to-Ambient**

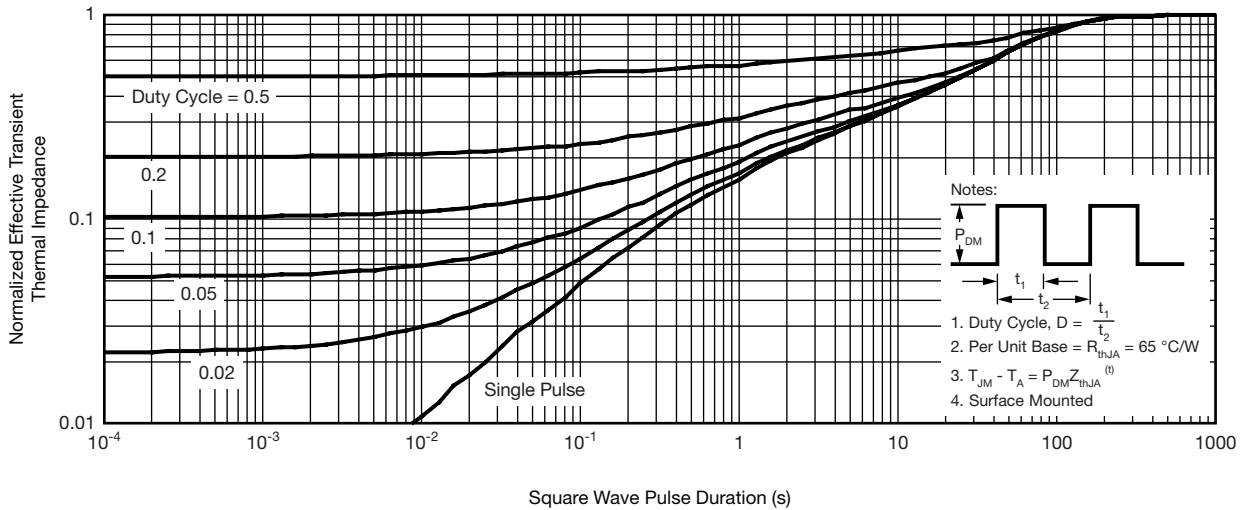
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

# SiJ458DP

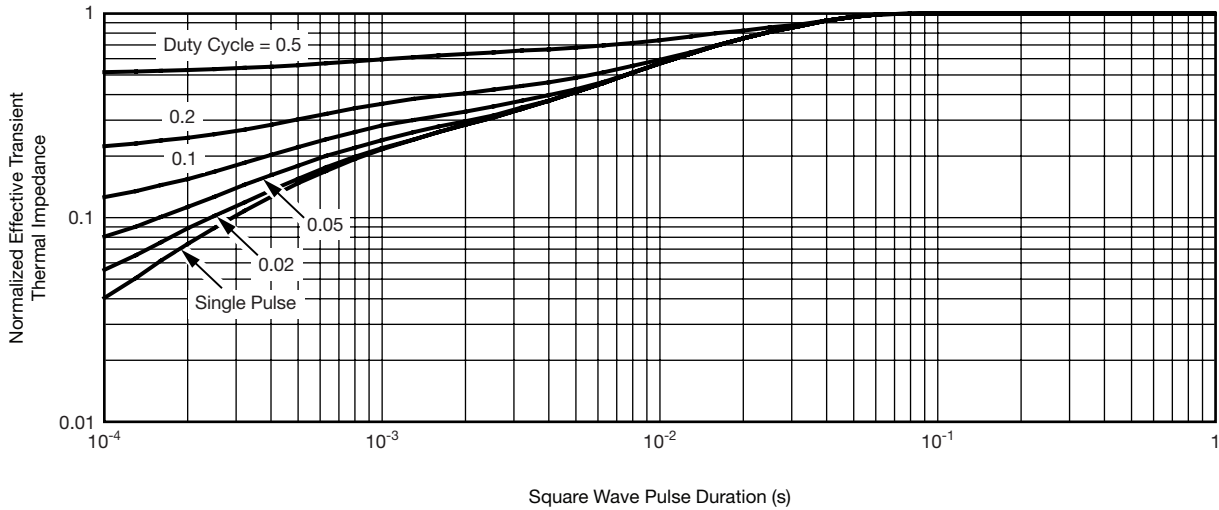
Vishay Siliconix



## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

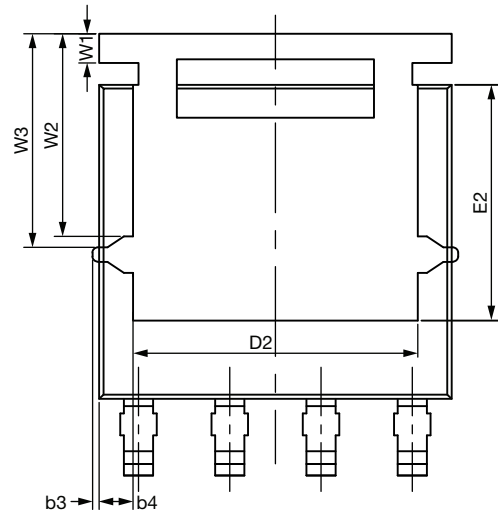
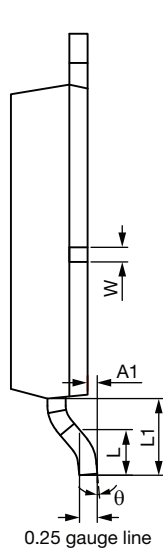
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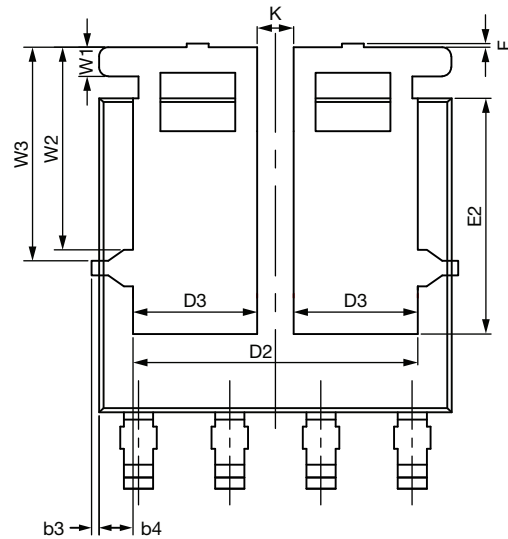
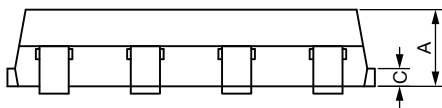
# PowerPAK® SO-8L Case Outline for Non-AI Parts



Topside view



Backside view (single)



Backside view (dual)



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.094			0.004		
b4	0.47			0.019		
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	3.18	3.28	3.38	0.125	0.129	0.133
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.51			0.020		
W	0.23			0.009		
W1	0.41			0.016		
W2	2.82			0.111		
W3	2.96			0.117		
θ	0°	-	10°	0°	-	10°
ECN: T16-0221-Rev. D, 16-May-16 DWG: 5976						

**Note**

- Millimeters will gover





## RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE



Recommended Minimum Pads  
Dimensions in mm (inches)



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