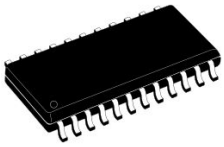
L6229

Datasheet

DMOS driver for 3-phase brushless DC motor

Power S036



SO24

(20 + 2 + 2)

Features

- Operating supply voltage from 8 to 52 V
- 2.8 A output peak current (1.4 A DC)
- $R_{DS(ON)}$ 0.73 Ω typ. value at T_j = 25 °C
- Operating frequency up to 100 kHz
- Non-dissipative overcurrent detection and protection
- Diagnostic output
- Constant t_{OFF} PWM current controller
- Slow decay synchronous rectification
- 60° and 120° Hall effect decoding logic
- Brake function
- Tachometer output for speed loop
- Cross conduction protection
- Thermal shutdown
- Undervoltage lockout
- Integrated fast free wheeling diodes

Application

- Factory automation end-points
- Home appliances
- Small pumps
- ATMs

Product status link
L6229

Product summary		
Order code	**Package**	**Packing**
L6229D	SO-24	Tube
L6229DTR	SO-24	Tape and reel
L6229PD	PowerSO36	Tube
L6229PDTR	PowerSO36	Tape and reel

Product label
SUSTAINABLE TECHNOLOGY

Description

The L6229 is a DMOS fully integrated 3-phase motor driver with overcurrent protection.

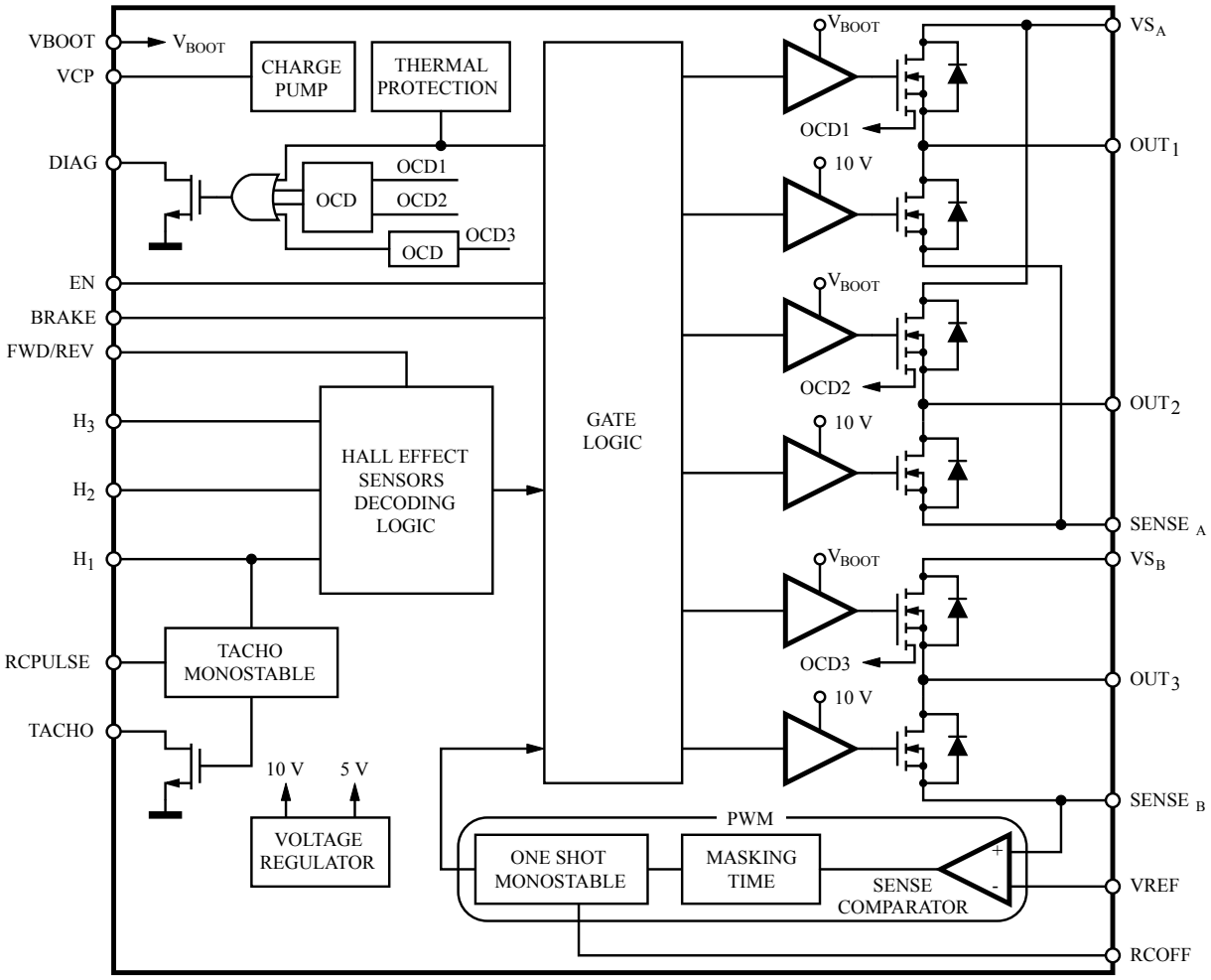
Realized in BCD technology, the device combines isolated DMOS power transistors with CMOS and bipolar circuits on the same chip.

The device includes all the circuitry needed to drive a 3-phase BLDC motor including: a 3-phase DMOS bridge, a constant off time PWM current controller and the decoding logic for single ended Hall sensors that generates the required sequence for the power stage.

Available in Power SO36 and SO24 (20 + 2 + 2) packages, the L6229 features a non-dissipative overcurrent protection on the high-side power MOSFET and thermal shutdown.

1 Block diagram

Figure 1. **Block diagram**



2 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Test conditions	Value	Unit
V_S	Supply voltage	$V_{SA} = V_{SB} = V_S$	60	V
V_{OD}	Differential voltage between: VS_A, OUT_1, OUT_2, $SENSE_A$ and VS_B, OUT_3, $SENSE_B$	$V_{SA} = V_{SB} = V_S = 60$ V; $V_{SENSEA} = V_{SENSEB}$ = GND	60	V
V_{BOOT}	Bootstrap peak voltage	$V_{SA} = V_{SB} = V_S$	V_S + 10	V
V_{IN}, V_{EN}	Logic inputs voltage range	-	-0.3 to 7	V
V_{REF}	Voltage range at pin VREF	-	-0.3 to 7	V
V_{RCOFF}	Voltage range at pin RCOFF	-	-0.3 to 7	V
$V_{RCPULSE}$	Voltage range at pin RCPULSE	-	-0.3 to 7	V
V_{SENSE}	Voltage range at pins $SENSE_A$ and $SENSE_B$	-	-1 to 4	V
$I_{S(peak)}$	Pulsed supply current (for each VS_A and VS_B pin)	$V_{SA} = V_{SB} = V_S$; t_{PULSE} < 1 ms	3.55	A
I_S	DC supply current (for each VS_A and VS_B pin)	$V_{SA} = V_{SB} = V_S$	1.4	A
T_{stg}, T_{OP}	Storage and operating temperature range	-	-40 to 150	°C

3 Recommended operating condition

Table 2. Recommended operating condition

Symbol	Parameter	Test conditions	Min.	Max.	Unit
V_S	Supply voltage	$V_{SA} = V_{SB} = V_S$	8	52	V
V_{OD}	Differential voltage between: VS_A, OUT_1, OUT_2, $SENSE_A$ and VS_B, OUT_3, $SENSE_B$	$V_{SA} = V_{SB} = V_S$; $V_{SENSEA} = V_{SENSEB}$	-	52	V
V_{REF}	Voltage range at pin VREF	-	-0.1	5	V
V_{SENSE}	Voltage range at pins $SENSE_A$ and $SENSE_B$	(pulsed $t_W < t_{rr}$) (DC)	-6 -1	6 1	V
I_{OUT}	DC output current	$V_{SA} = V_{SB} = V_S$	-	1.4	A
f_{SW}	Switching frequency	-	-	100	kHz

4 Thermal data

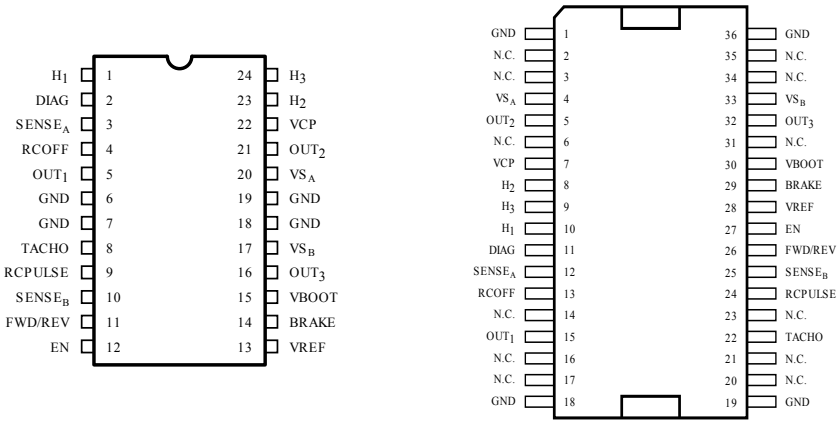
Table 3. **Thermal data**

Symbol	Description	SO24	PowerSO36	Unit
$R_{th(j\text{-}pins)}$	Maximum thermal resistance junction pins	15	-	°C/W
$R_{th(j\text{-}case)}$	Maximum thermalresistance junction case	-	2	°C/W
$R_{th(j\text{-}amb)1}$	Maximum thermal resistance junction ambient (1)	55	-	°C/W
$R_{th(j\text{-}amb)1}$	Maximum thermal resistance junction ambient (2)	-	36	°C/W
$R_{th(j\text{-}amb)1}$	Maximum thermal resistance junction ambient (3)	-	16	°C/W
$R_{th(j\text{-}amb)2}$	Maximum thermal resistance junction ambient (4)	78	63	°C/W

1. *Mounted on a multilayer FR4 PCB with a dissipating copper surface on the bottom side of 6 cm^2 (with a thickness of 35 µm).*
2. *Mounted on a multilayer FR4 PCB with a dissipating copper surface on the top side of 6 cm^2 (with a thickness of 35 µm).*
3. *Mounted on a multilayer FR4 PCB with a dissipating copper surface on the top side of 6 cm^2 (with a thickness of 35 µm), 16 via holes and a ground layer.*
4. *Mounted on a multilayer FR4 PCB without any heat-sinking surface on the board.*

5 Pin connections

Figure 2. **Pin connections (top view)**



SO24 **PowerSO36** (1)

1. *The slug is internally connected to pins 1, 18, 19 and 36 (GND pins).*

Table 4. **Pin functions**

Package		Pin name	Type	Function
SO24	PowerSO36			
Pin no.	Pin no.			
1	10	H_1	Sensor input	Single ended Hall effect sensor input 1.
2	11	DIAG	Open drain output	Overcurrent detection and thermal protection pin. An internal open drain transistor pulls to GND when an overcurrent on one of the high-side MOSFET is detected or during thermal protection.
3	12	$SENSE_A$	Power supply	Half-bridge 1 and half-bridge 2 source pin. This pin must be connected together with pin $SENSE_B$ to power ground through a sensing power resistor.
4	13	RCOFF	RC pin	RC network pin. A parallel RC network connected between this pin and ground sets the current controller OFF-time.
5	15	OUT_1	Power output	Output 1
6, 7, 18, 19	1, 18, 19, 36	GND	GND	Ground terminals. On SO24 package, these pins are also used for heat dissipation toward the PCB. On PowerSO36 package the slug is connected on these pins.
8	22	TACHO	Open drain output	Frequency-to-voltage open drain output. Every pulse from pin H_1 is shaped as a fixed and adjustable length pulse.
9	24	RCPULSE	RC pin	RC network pin. A parallel RC network connected between this pin and ground sets the duration of the monostable pulse used for the frequency-to-voltage converter.
10	25	$SENSE_B$	Power supply	Half-bridge 3 source pin. This pin must be connected together with pin $SENSE_A$ to power ground through a sensing power resistor. At this pin also the inverting input of the sense comparator is connected.
11	26	FWD/REV	Logic input	Selects the direction of the rotation. HIGH logic level sets forward operation, whereas LOW logic level sets reverse operation. If not used, it has to be connected to GND or +5 V.

Package		Pin name	Type	Function
SO24	PowerSO36			
Pin no.	Pin no.			
12	27	EN	Logic input	Chip enable. LOW logic level switches OFF all power MOSFET. If not used, it has to be connected to +5 V.
13	28	VREF	Logic input	Current controller reference voltage. Do not leave this pin open or connect to GND.
14	29	BRAKE	Logic input	Brake input pin. LOW logic level switches ON all high- side power MOSFET, implementing the brake function. If not used, it has to be connected to +5 V.
15	30	VBOOT	Supply voltage	Bootstrap voltage needed for driving the upper power MOSFETs.
16	32	OUT_3	Power output	Output 3.
17	33	VS_B	Power supply	Half-bridge 3 power supply voltage. It must be connected to the supply voltage together with pin VS_A.
20	4	VSA	Power supply	Half-bridge 1 and half-bridge 2 power supply voltage. It must be connected to the supply voltage together with pin VS_B.
21	5	OUT_2	Power output	Output 2.
22	7	VCP	Output	Charge pump oscillator output.
23	8	H_2	Sensor input	Single ended Hall effect sensor input 2.
24	9	H_3	Sensor input	Single ended Hall effect sensor input 3.

6 Electrical characteristics

Table 5. Electrical characteristics

Test conditions: V_S = 48 V, T_{amb} = 25 °C , unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{Sth(ON)}$	Turn ON threshold	-	5.8	6.3	6.8	V
$V_{Sth(OFF)}$	Turn OFF threshold	-	5	5.5	6	V
I_S	Quiescent supply current	All bridges OFF; T_J = -25 to 125 °C (1)	-	5	10	mA
$T_{J(OFF)}$	Thermal shutdown temperature	-	-	165	-	°C
Output DMOS transistors						
$R_{DS(ON)}$	High-side + low-side switch ON resistance	T_J = 25 °C	-	1.47	1.69	Ω
		T_J = 125 °C(2)	-	2.35	2.70	Ω
I_{DSS}	Leakage current	EN = low; OUT = V_{CC}	-	-	2	mA
		EN = low; OUT = GND	-0.3	-	-	mA
Source drain diodes						
V_{SD}	Forward ON voltage	I_{SD} = 1.4 A, EN = low	-	1.15	1.3	V
t_{rr}	Reverse recovery time	I_f = 1.4 A	-	300	-	ns
t_{fr}	Forward recovery time	-	-	200	-	ns
Logic input (H1, H2, H3, EN, FWD/REV, BRAKE)						
V_{IL}	Low level logic input voltage	-	-0.3	-	0.8	V
V_{IH}	High level logic input voltage	-	2	-	7	V
I_{IL}	Low level logic input current	GND logic input voltage	-10	-	-	µA
I_{IH}	High level logic input current	7V logic input voltage	-	-	10	µA
$V_{th(ON)}$	Turn-ON input threshold	-	-	1.8	2.0	V
$V_{th(OFF)}$	Turn-OFF input threshold	-	0.8	1.3	-	V
V_{thHYS}	Input thresholds hysteresis	-	0.25	0.5	-	V
Switching characteristics						
$t_{D(on)EN}$	Enable to out turn-ON delay time(2)	I_{LOAD} = 1.4 A, resistive load	500	650	800	ns
$t_{D(off)EN}$	Enable to out turn-OFF delay time(2)	I_{LOAD} = 1.4 A, resistive load	500	-	1000	ns
$t_{D(on)IN}$	Other logic inputs to output turn-ON delay time	I_{LOAD} = 1.4 A, resistive load	-	1.6	-	µs
$t_{D(off)IN}$	Other logic inputs to out turn-OFF delay time	I_{LOAD} = 1.4 A, resistive load	-	800	-	ns
t_{RISE}	Outputrise time (2)	I_{LOAD} = 1.4 A, resistive load	40	-	250	ns
t_{FALL}	Outputfall time (2)	I_{LOAD} = 1.4 A, resistive load	40	-	250	ns
t_{DT}	Deadtime	-	0.5	1	-	µs
f_{CP}	Charge pump frequency	T_J = -25 to 125 °C(1)	-	0.6	1	MHz
PWM comparator and monostable						
I_{RCOFF}	Source current at pin RC_{OFF}	V_{RCOFF} = 2.5 V	3.5	5.5	-	mA
V_{OFFSET}	Offset voltage on sense comparator	V_{ref} = 0.5 V	-	±5	-	mV

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{prop}	Turn OFF propagation delay(3)	V_{ref} = 0.5 V	-	500	-	ns
t_{blank}	Internal blanking time on sense comparator	-	-	1	-	µs
$t_{ON(min)}$	Minimum on time	-	-	2.5	3	µs
t_{OFF}	PWM recirculation time	R_{OFF} = 20 kΩ; C_{OFF} = 1 nF	-	13	-	µs
		R_{OFF} = 100 kΩ; C_{OFF} = 1 nF	-	61	-	µs
I_{BIAS}	Input bias current at pin VREF	-	-	-	10	µA
TACHO monostable						
$I_{RCPULSE}$	Source current at pin RCPULSE	$V_{RCPULSE}$ = 2.5 V	3.5	5.5	-	mA
t_{PULSE}	Monostable of time	R_{PUL} = 20 kΩ; C_{PUL} = 1 nF	-	12	-	ms
		R_{PUL} = 100 kΩ; C_{PUL} = 1 nF	-	60	-	ms
R_{TACHO}	Open drain ON resistance	-	-	40	60	Ω
Overcurrent detection and protection						
I_{SOVER}	Supply overcurrent protection threshold	T_J = -25 to 125 °C(1)	2	2.8	3.55	A
R_{OPDR}	Open drain ON resistance	I_{DIAG} = 4 mA	-	40	60	Ω
I_{OH}	OCD high level leakage current	V_{DIAG} = 5 V	-	1	-	µA
$t_{OCD(ON)}$	OCD turn-ON delay time(4)	I_{DIAG} = 4mA; C_{DIAG} < 100 pF	-	200	-	ns
$t_{OCD(OFF)}$	OCD turn-OFF delay time(4)	I_{DIAG} = 4mA; C_{DIAG} < 100 pF	-	100	-	ns

1. *Tested at 25 °C in a restricted range and guaranteed by characterization.*
2. *See Figure 3: Switching characteristic definition.*
3. *Measured applying a voltage of 1 V to pin SENSE and a voltage drop from 2 V to 0 V to pin VREF.*
4. *See Figure 4: Overcurrent detection timing definition.*

Figure 3. Switching characteristic definition

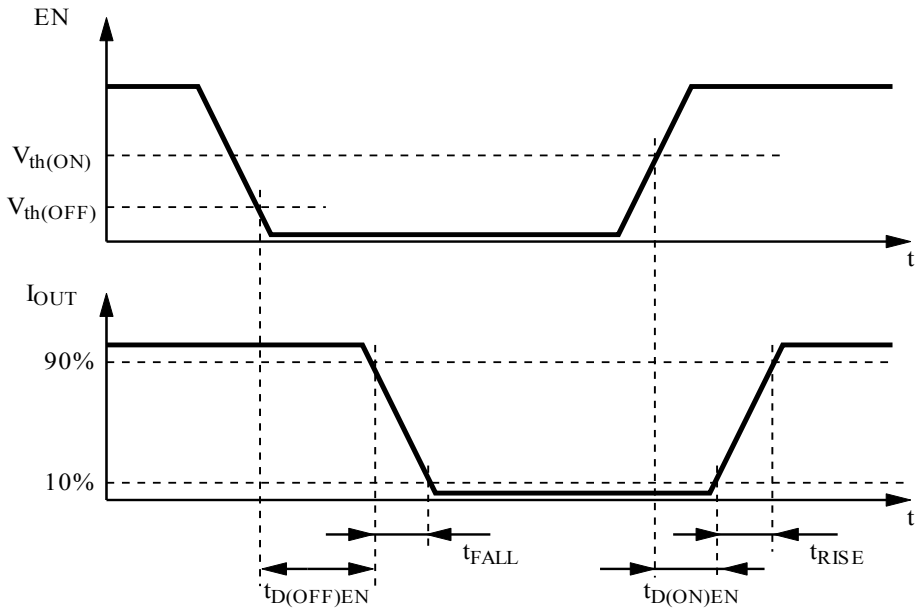
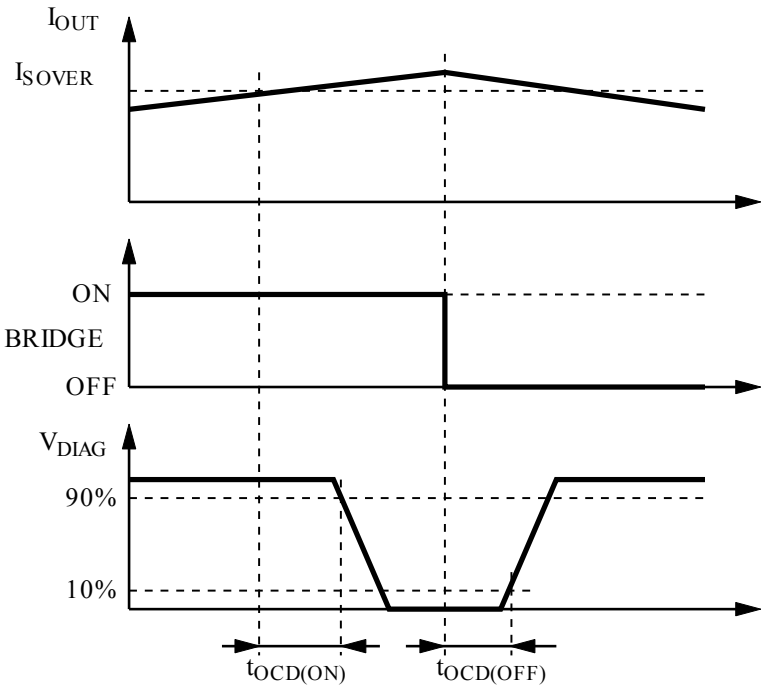


Figure 4. **Overcurrent detection timing definition**



7 Circuit description

7.1 Power stages and charge pump

The L6229 device integrates a 3-phase bridge, which consists of 6 power MOSFETs connected as shown in Block diagram . Each power MOS has an $R_{DS(ON)}$ = 0.73 Ω (typical value at 25 °C) with intrinsic fast free-wheeling diode. Switching patterns are generated by the PWM current controller and the Hall effect sensor decoding logic (see Section 8 PWM current control and Section 10 Decoding logic). Cross conduction protection is implemented by using a deadtime (t_{DT} = 1 µs typical value) set by internal timing circuit between the turn off and turn on of two power MOSFETs in one leg of a bridge.

Pins VS_A and VS_B must be connected together to the supply voltage (V_S).

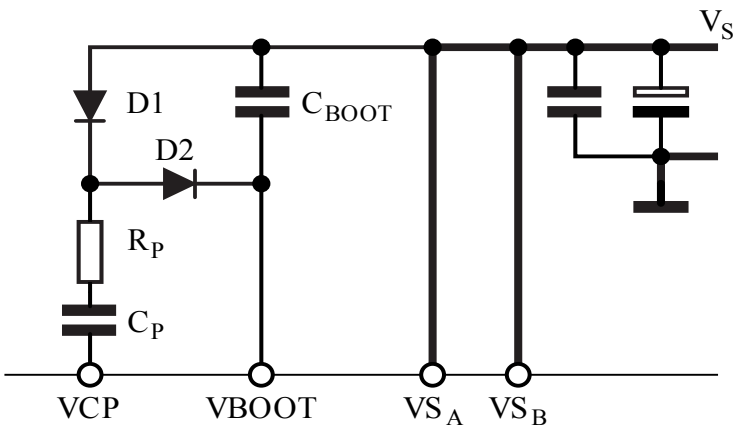
Using N-channel power MOS for the upper transistors in the bridge requires a gate drive voltage above the power supply voltage.

The bootstrapped supply (V_{BOOT}) is obtained through an internal oscillator and few external components to realize a charge pump circuit as shown in Figure 5. The oscillator output (pin VCP) is a square wave at 600 kHz (typically) with 10 V amplitude. Recommended values/part numbers for the charge pump circuit are shown in Table 6.

Table 6. Charge pump external component values

Component	Value
C_{BOOT}	220 nF
C_P	10 nF
R_P	100 Ω
D_1	1N4148
D_2	1N4148

Figure 5. Charge pump circuit



7.2 Logic inputs

Pins FWD/REV, BRAKE, EN, H_1, H_2 and H_3 are TTL/CMOS compatible logic inputs. The internal structure is shown in Figure 6. Typical value for turn-ON and turn-OFF thresholds are respectively $V_{th(ON)}$ = 1.8 V and $V_{th(OFF)}$ = 1.3 V.

Pin EN (enable) may be used to implement overcurrent and thermal protection by connecting it to the open collector DIAG output. If the protection and an external disable function are both desired, the appropriate connection must be implemented. When the external signal is from an open collector output, the circuit in Figure 7 can be used.

For external circuits that are push-pull outputs the circuit in Figure 8 could be used. The resistor R_{EN} should be chosen in the range from 2.2 kΩ to 180 kΩ.

Recommended values for R_{EN} and C_{EN} are respectively 100 kΩ and 5.6 nF. More information for selecting the values can be found Section 12 Non-dissipative overcurrent detection and protection.

Figure 6. Logic input internal structure

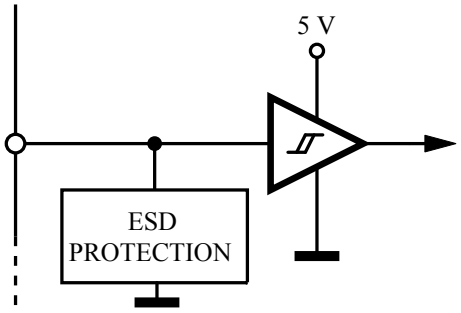


Figure 7. Pin EN open collector driving

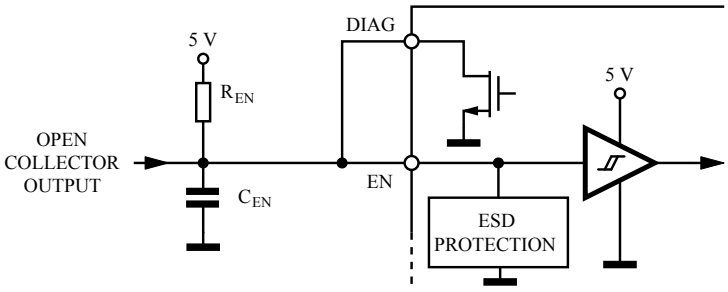
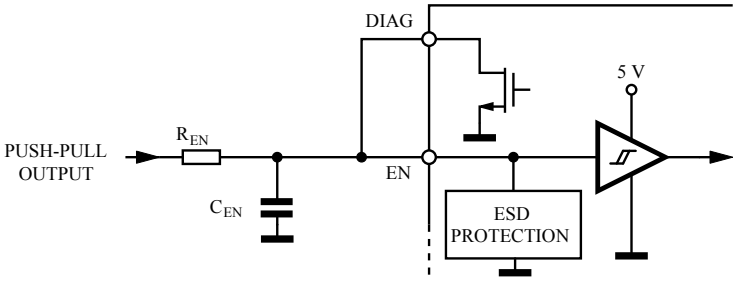


Figure 8. Pin EN push-pull driving



8 PWM current control

The L6229 device includes a constant off time PWM current controller. The current control circuit senses the bridge current by sensing the voltage drop across an external sense resistor connected between the source of the three lower power MOS transistors and ground, as shown in Figure 9. As the current in the motor increases the voltage across the sense resistor increases proportionally. When the voltage drop across the sense resistor becomes greater than the voltage at the reference input pin VREF the sense comparator triggers the monostable switching the bridge off. The power MOS remains off for the time set by the monostable and the motor current recirculates around the upper half of the bridge in slow decay mode as described in Section 9 Slow decay mode. When the monostable times out, the bridge will again turn on. Since the internal deadtime, used to prevent cross conduction in the bridge, delays the turn on of the power MOS, the effective off time t_{OFF} is the sum of the monostable time plus the deadtime.

Figure 10 shows the typical operating waveforms of the output current, the voltage drop across the sensing resistor, the pin RC voltage and the status of the bridge. More details regarding the synchronous rectification and the output stage configuration are included in Section 9 Slow decay mode.

Immediately after the power MOS turns on, a high peak current flows through the sense resistor due to the reverse recovery of the freewheeling diodes. The L6229 device provides a 1 µs blanking time t_{BLANK} that inhibits the comparator output so that the current spike cannot prematurely retrigger the monostable.

Figure 9. PWM current controller simplified schematic

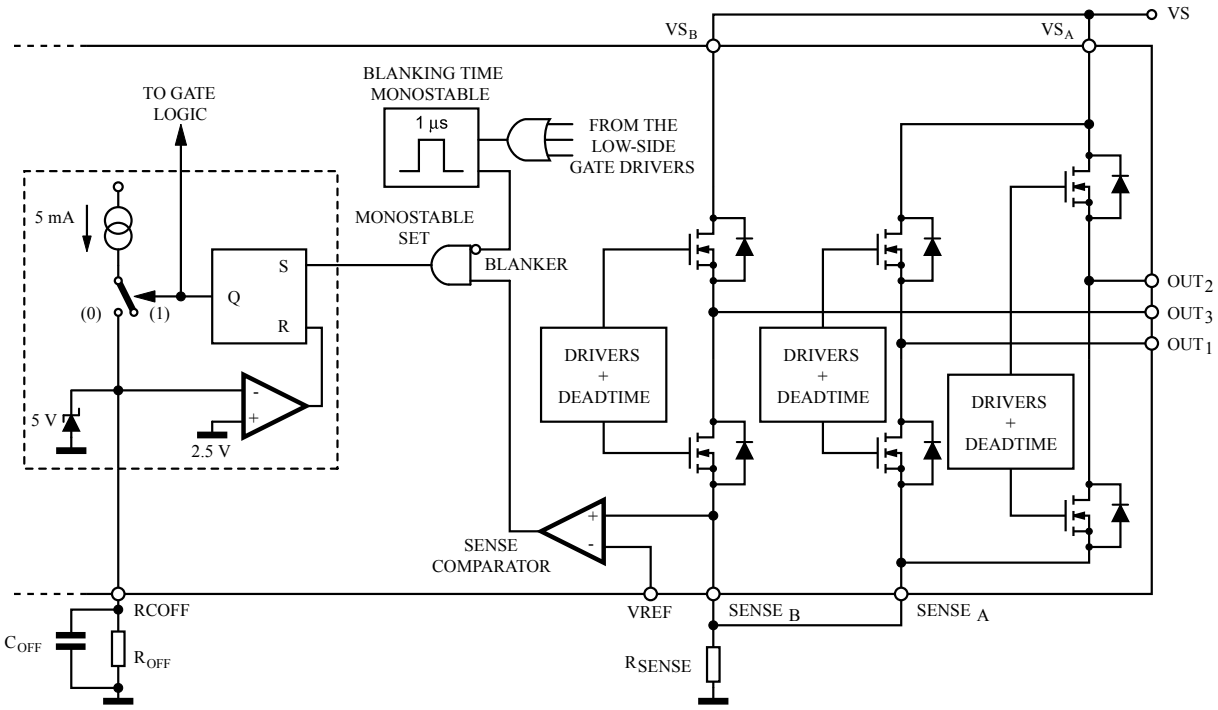


Figure 10. **Output current regulation waveforms**

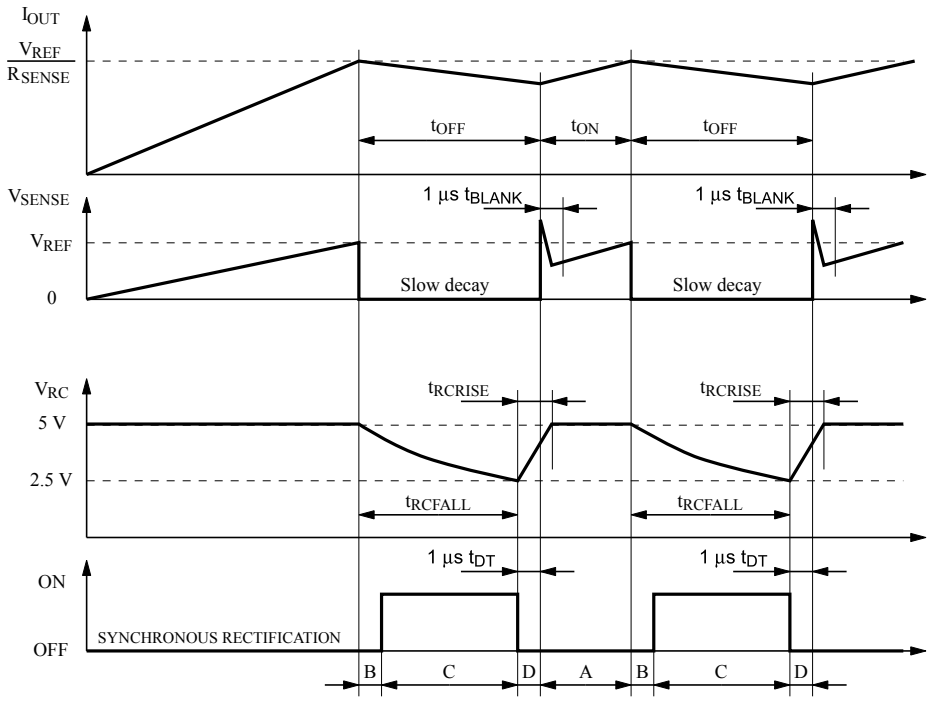


Figure 11 shows the magnitude of the off time t_{OFF} versus C_{OFF} and R_{OFF} values. It can be approximately calculated from the equations:

$$t_{RCFALL} = 0.6 \cdot R_{OFF} \cdot C_{OFF} \quad (1)$$

$$t_{OFF} = t_{RCFALL} + t_{DT} = 0.6 \cdot R_{OFF} \cdot C_{OFF} + t_{DT}$$

where R_{OFF} and C_{OFF} are the external component values and t_{DT} is the internally generated deadtime with:

$$20k\Omega \leq R_{OFF} \leq 100\ k\Omega \quad (2)$$

$$0.47\ nF \leq C_{OFF} \leq 100\ nF$$

$$t_{DT} = 1\mu s \quad (tipical\ \ value)$$

Therefore:

$$t_{OFF\ \ (MIN)} = 6.6\ \mu s \quad (3)$$

$$t_{OFF\ \ (MAX)} = 6\ ms$$

These values allow a sufficient range of t_{OFF} to implement the drive circuit for most motors.

The capacitor value chosen for C_{OFF} also affects the rise time t_{RCRISE} of the voltage at the pin RCOFF. The rise time t_{RCRISE} will only be an issue if the capacitor is not completely charged before the next time the monostable is triggered. Therefore, the on time t_{ON}, which depends by motors and supply parameters, has to be bigger than t_{RCRISE} for allowing a good current regulation by the PWM stage. Furthermore, the on time t_{ON} cannot be smaller than the minimum on time $t_{ON(MIN)}$.

$$\begin{cases} t_{ON} > t_{ON(MIN)} = 2.5\mu s \quad (typ.value) \\ t_{ON} > t_{RCRISE} - t_{DT} \end{cases} \quad (4)$$

$$t_{RCRISE} = 600 \cdot C_{OFF}$$

Figure 12 shows the lower limit for the on time t_{ON} for having a good PWM current regulation capacity. It has to be said that t_{ON} is always bigger than $t_{ON(MIN)}$ because the device imposes this condition, but it can be smaller than t_{RCRISE} - t_{DT}. In this last case the device continues to work but the off time t_{OFF} is not more constant.

So, small C_{OFF} value gives more flexibility for the applications (allows smaller on time and, therefore, higher switching frequency), but, the smaller is the value for C_{OFF}, the more influential will be the noises on the circuit performance.

Figure 11. t_{OFF} versus C_{OFF} and R_{OFF}

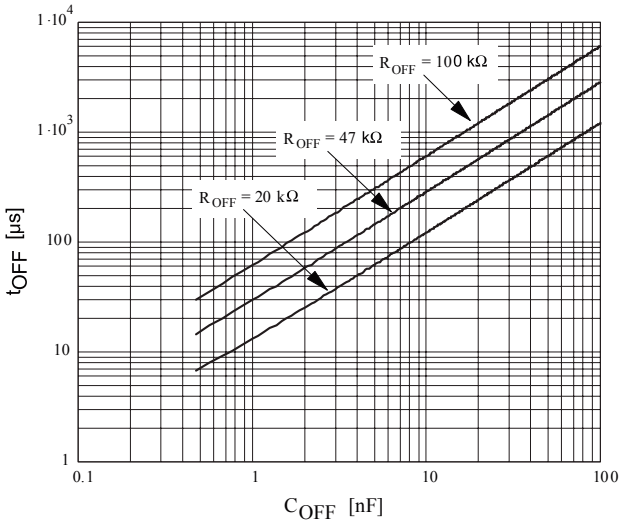
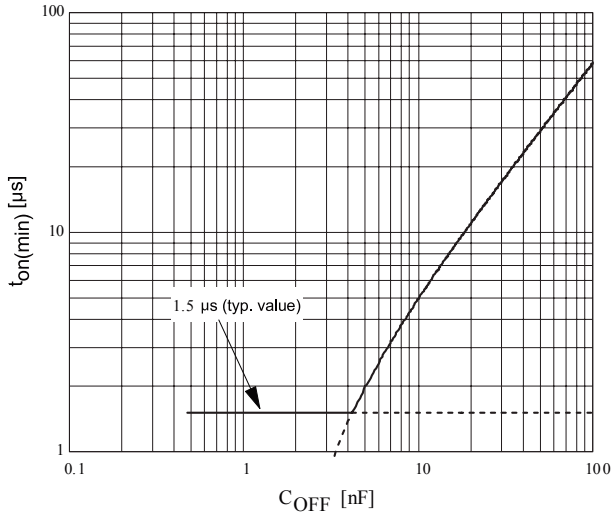


Figure 12. Area where t_{ON} can vary maintaining the PWM regulation

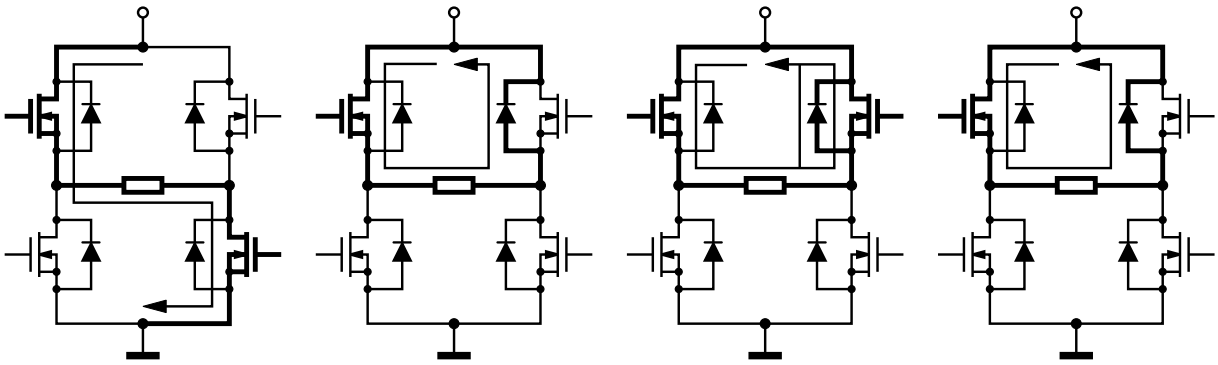


9 Slow decay mode

Figure 13 shows the operation of the bridge in the slow decay mode during the off time. At any time only two legs of the 3-phase bridge are active, therefore only the two active legs of the bridge are shown in Figure 13 and the third leg will be off.

At the start of the off time, the lower power MOS is switched off and the current recirculates around the upper half of the bridge. Since the voltage across the coil is low, the current decays slowly. After the deadtime the upper power MOS is operated in the synchronous rectification mode reducing the impedance of the freewheeling diode and the related conducting losses. When the monostable times out, upper MOS that was operating the synchronous mode turns off and the lower power MOS is turned on again after some delay set by the deadtime to prevent cross conduction.

Figure 13. Slow decay mode output stage configurations



10 Decoding logic

The decoding logic section is a combinatory logic that provides the appropriate driving of the 3-phase bridge outputs according to the signals coming from the three Hall effetct sensors that detect rotor position in a 3-phase BLDC motor.

This novel combinatory logic discriminates between the actual sensors position for sensors spaced at 60, 120, 240 and 300 electrical degrees. This decoding method allows the implementation of a universal IC without dedicating pins to select the sensor configuration.

There are eight possible input combinations for three sensor inputs. Six combinations are valid for rotor positions with 120 electrical degrees sensor phasing (see Figure 14, positions 1, 2, 3a, 4, 5 and 6a) and six combinations are valid for rotor positions with 60 electrical degrees phasing (see Figure 15, positions 1, 2, 3b, 4, 5 and 6b). Four of them are in common (1, 2, 4 and 5) whereas there are two combinations used only in 120 electrical degrees sensor phasing (3a and 6a) and two combinations used only in 60 electrical degrees sensor phasing (3b and 6b).

The decoder can drive motors with different sensor configuration simply by following Table 7. For any input configuration (H_1, H_2 and H_3) there is one output configuration (OUT_1, OUT_2 and OUT_3). The output configuration 3a is the same as 3b and analogously output configuration 6a is the same as 6b.

The sequence of the Hall codes for 300 electrical degrees phasing is the reverse of 60 and the sequence of the Hall codes for 240 phasing is the reverse of 120. So, by decoding the 60 and the 120 codes it is possible to drive the motor with all the four conventions by changing the direction set.

Table 7. 60 and 120 electrical degree decoding logic in forward direction

Hall 120°	1	2	3a	-	4	5	6a	-
Hall 60°	**1**	**2**	**-**	**3b**	**4**	**5**	**-**	**6b**
H_1	H	H	L	H	L	L	H	L
H_2	L	H	H	H	H	L	L	L
H_3	L	L	L	H	H	H	H	L
OUT_1	Vs	High Z	GND	GND	GND	High Z	Vs	Vs
OUT_2	High Z	Vs	Vs	Vs	High Z	GND	GND	GND
OUT_3	GND	GND	High Z	High Z	Vs	Vs	High Z	High Z
Phasing	1 ⇒ 3	2 ⇒ 3	2 ⇒ 1	2 ⇒ 1	3 ⇒ 1	3 ⇒ 2	1 ⇒ 2	1 ⇒ 2

Figure 14. **120° Hall sensor sequence**

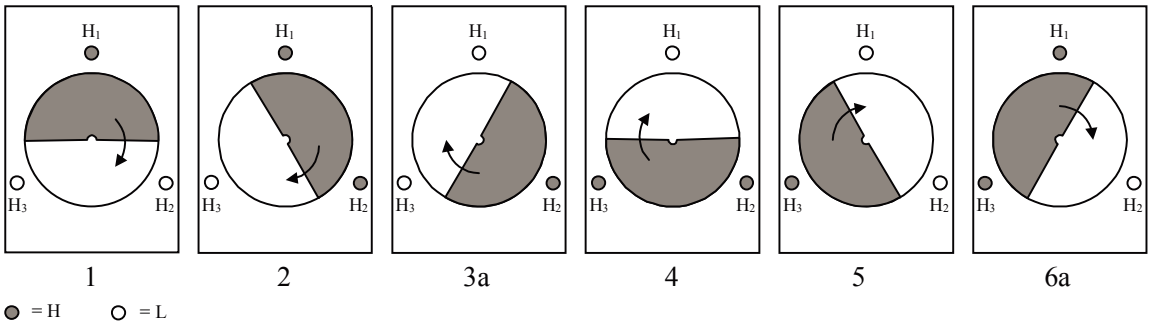
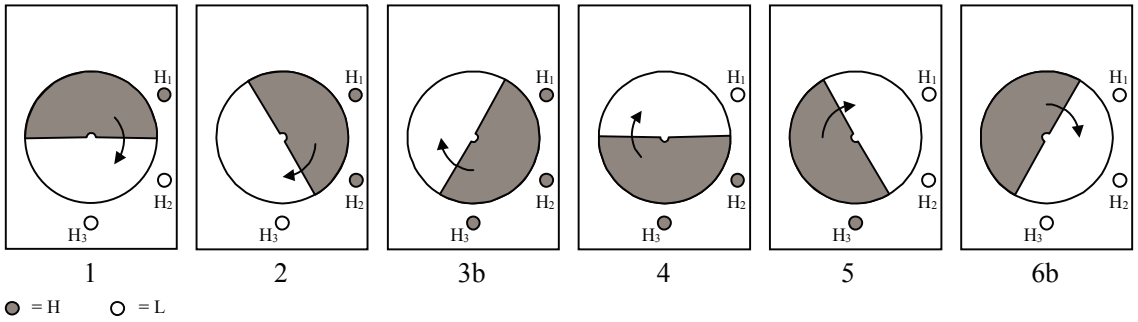


Figure 15. **60° Hall sensor sequence**



11 Tachometer

A tachometer function consists of a monostable, with constant off time (t_{PULSE}), whose input is one Hall effect signal (H_1). It allows developing an easy speed control loop by using an external op amp, as shown in Figure 16. For component values refer to Section 13 Application information.

The monostable output drives an open drain output pin (TACHO). At each rising edge of the Hall effect sensors H_1, the monostable is triggered and the MOSFET connected to pin TACHO is turned off for a constant time t_{PULSE} (see Figure 17). The off time t_{PULSE} can be set using the external RC network (R_{PUL}, C_{PUL}) connected to the pin RCPULSE.

Figure 18 gives the relation between t_{PULSE} and C_{PUL}, R_{PUL}. We have approximately:

$$t_{PULSE} = 0.6 \cdot R_{PUL} \cdot C_{PUL} \quad (5)$$

where C_{PUL} should be chosen in the range from 1 nF to 100 nF and R_{PUL} in the range from 20 kΩ to 100 kΩ.

By connecting the tachometer pin to an external pull-up resistor, the output signal average value V_M is proportional to the frequency of the Hall effect signal and, therefore, to the motor speed. This realizes a simple frequency-to-voltage converter. An op amp, configured as an integrator, filters the signal and compares it with a reference voltage V_{REF}, which sets the speed of the motor.

$$V_M = \frac{t_{PULSE}}{T} \cdot V_{DD} \quad (6)$$

Figure 16. TACHO operation waveforms

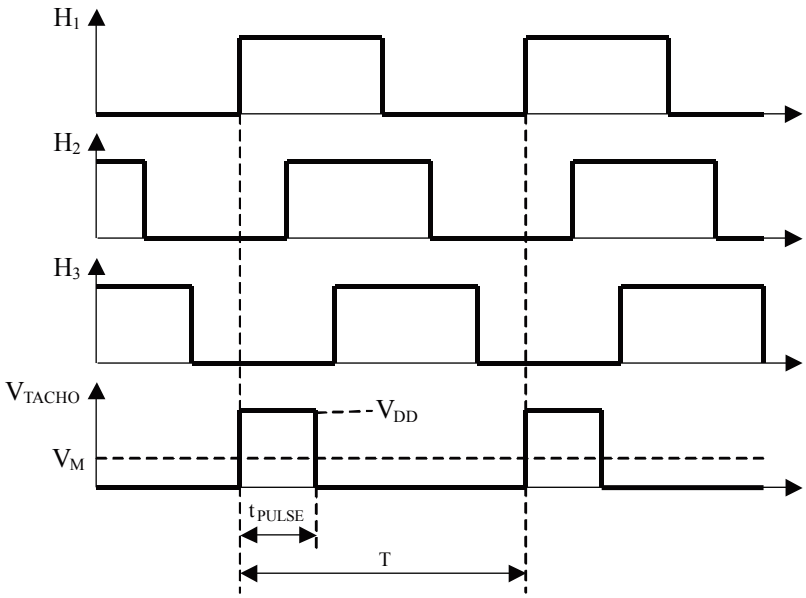


Figure 17. **Tachometer speed control loop**

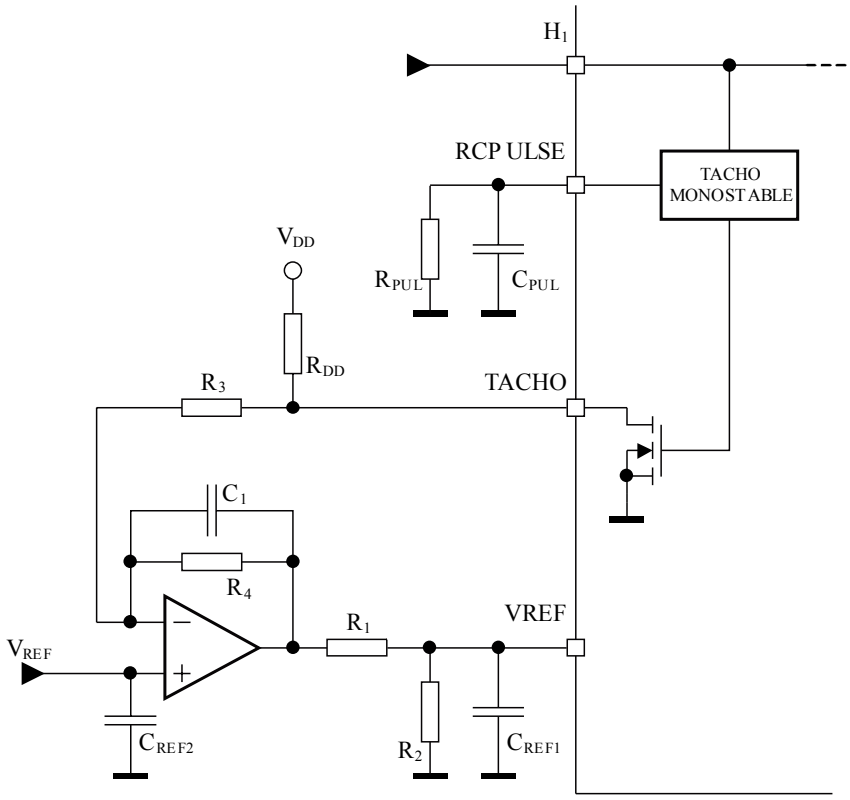
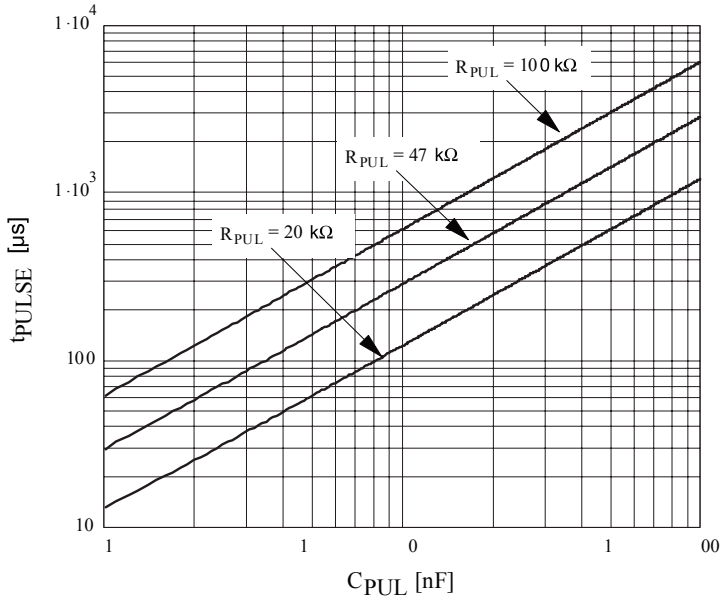


Figure 18. **t_{PULSE} versus C_{PUL} and R_{PUL}**



12 Non-dissipative overcurrent detection and protection

The L6229 device integrates an “Overcurrent Detection” circuit (OCD) for full protection.

This circuit provides output to output and output to ground short-circuit protection as well.

With this internal overcurrent detection, the external current sense resistor normally used and its associated power dissipation are eliminated. Figure 19 shows a simplified schematic for the overcurrent detection circuit.

To implement the overcurrent detection, a sensing element that delivers a small but precise fraction of the output current is implemented with each high-side power MOS. Since this current is a small fraction of the output current there is very little additional power dissipation. This current is compared with an internal reference current I_{REF}. When the output current reaches the detection threshold (typically I_{SOVER} = 2.8 A) the OCD comparator signals a fault condition. When a fault condition is detected, an internal open drain MOS with a pull down capability of 4 mA connected to pin DIAG is turned on.

The pin DIAG can be used to signal the fault condition to a microcontroller or to shut down the 3-phase bridge simply by connecting it to pin EN and adding an external R-C (see R_{EN}, C_{EN}).

Figure 19. Overcurrent protection simplified schematic

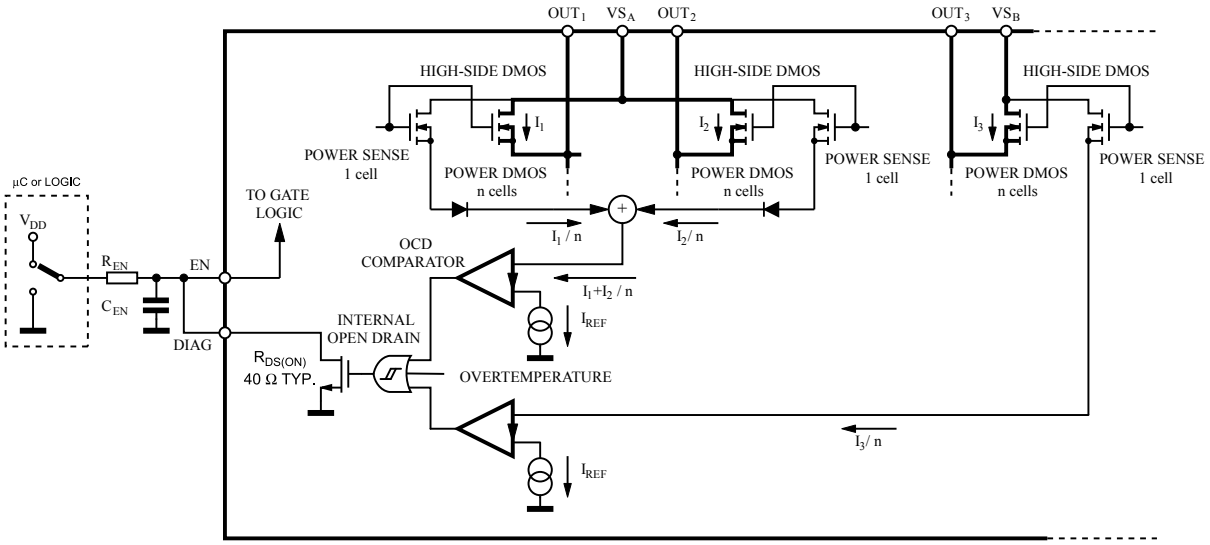


Figure 20 shows the overcurrent detection operation. The disable time $t_{DISABLE}$ before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs. It is affected whether by C_{EN} and R_{EN} values and its magnitude is reported in Figure 21. The delay time t_{DELAY} before turning off the bridge when an overcurrent has been detected depends only by C_{EN} value. Its magnitude is reported in Figure 22.

C_{EN} is also used for providing immunity to pin EN against fast transient noises. Therefore the value of C_{EN} should be chosen as big as possible according to the maximum tolerable delay time and the R_{EN} value should be chosen according to the desired disable time.

The resistor R_{EN} should be chosen in the range from 2.2 kΩ to 180 kΩ. Recommended values for R_{EN} and C_{EN} are respectively 100 kΩ and 5.6 nF that allow obtaining 200 µs disable time.

Figure 20. **Overcurrent protection waveforms**

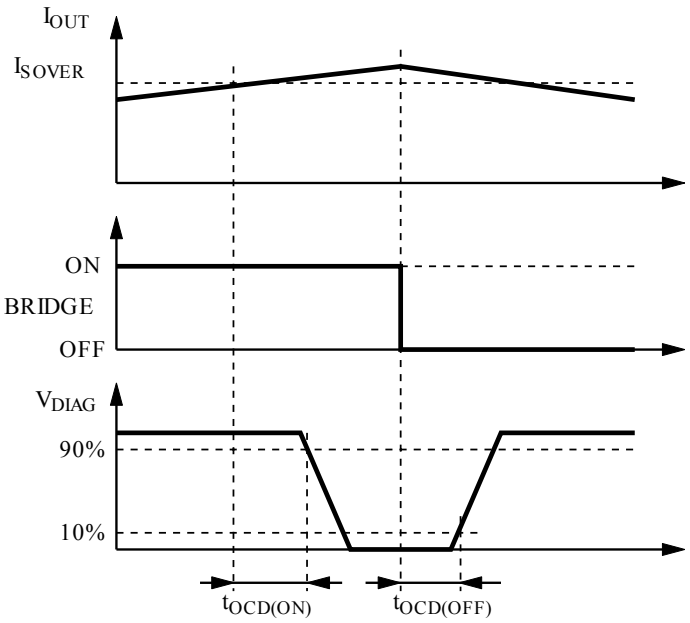


Figure 21. **$t_{DISABLE}$ versus C_{EN} and R_{EN}**

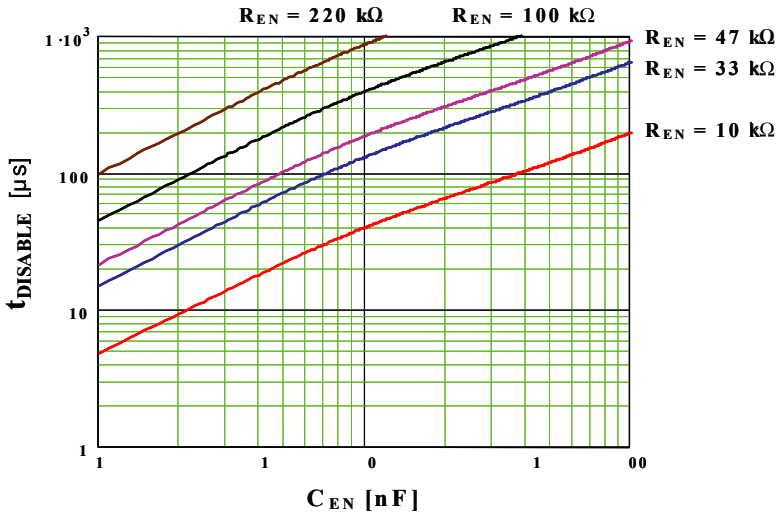
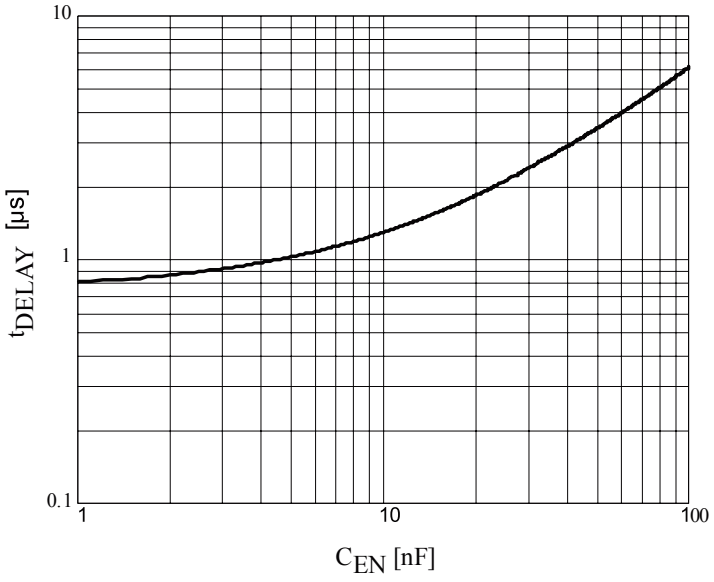


Figure 22. t_{DELAY} versus C_{EN}



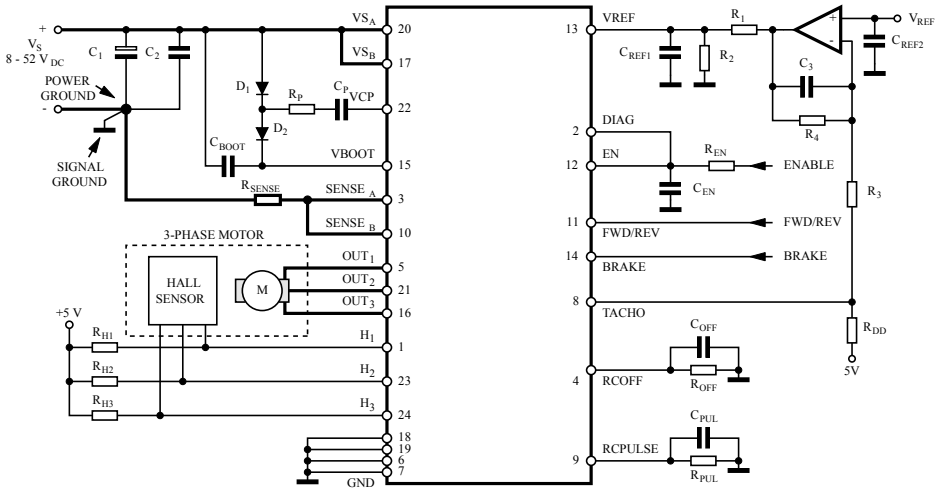
13 Application information

A typical application using the L6229 device is shown in Figure 23. Typical component values for the application are shown in Table 8. A high quality ceramic capacitor (C_2) in the range of 100 nF to 200 nF should be placed between the power pins VS_A and VS_B and ground near the L6229 device to improve the high frequency filtering on the power supply and reduce high frequency transients generated by the switching. The capacitor (C_{EN}) connected from the EN input to ground sets the shutdown time when an overcurrent is detected (see Section 12 Non-dissipative overcurrent detection and protection). The two current sensing inputs ($SENSE_A$ and $SENSE_B$) should be connected to the sensing resistor R_{SENSE} with a trace length as short as possible in the layout. The sense resistor should be non-inductive resistor to minimize the di/dt transients across the resistor. To increase noise immunity, unused logic pins are best connected to 5 V (high logic level) or GND (low logic level) see Table 4. It is recommended to keep power ground and signal ground separated on PCB.

Table 8. Component values for typical application

Component	Value
C_1	100 µF
C_2	100 nF
C_3	220 nF
C_{BOOT}	220 nF
C_{OFF}	1 nF
C_{PUL}	10 nF
C_{REF1}	33 nF
C_{REF2}	100 nF
C_{EN}	5.6 nF
C_P	10 nF
D_1	1N4148
D_2	1N4148
R_1	5.6 kΩ
R_2	1.8 kΩ
R_3	4.7 kΩ
R_4	1 MΩ
R_{DD}	1 kΩ
R_{EN}	100 kΩ
R_P	100 Ω
R_{SENSE}	0.6 Ω
R_{OFF}	33 kΩ
R_{PUL}	47 kΩ
R_{H1}, R_{H2}, R_{H3}	10 Ω

Figure 23. **Typical application**

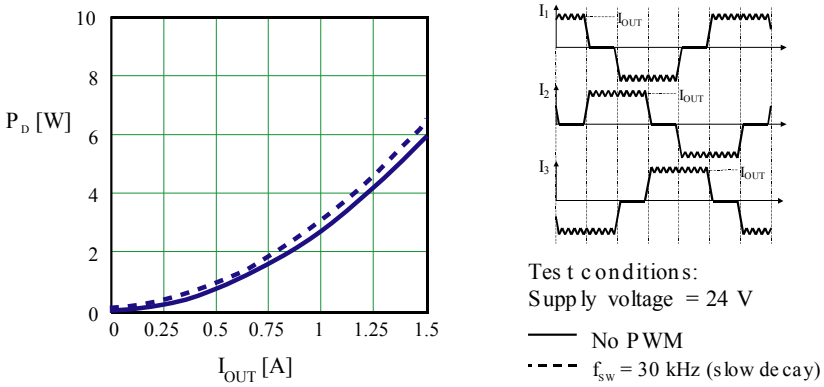


13.1 Output current capability and IC power dissipation

In Figure 24 is shown the approximate relation between the output current and the IC power dissipation using PWM current control.

For a given output current the power dissipated by the IC can be easily evaluated, in order to establish which package should be used and how large must be the on-board copper dissipating area to guarantee a safe operating junction temperature (125 °C maximum).

Figure 24. **IC power dissipation versus output power**



13.2 Thermal management

In most applications the power dissipation in the IC is the main factor that sets the maximum current that can be delivered by the device in a safe operating condition. Selecting the appropriate package and heatsinking configuration for the application is required to maintain the IC within the allowed operating temperature range for the application.

Figure 25 and Figure 26 show the junction to ambient thermal resistance values for the PowerSO36 and SO24 packages.

For instance, using a PowerSO package with a copper slug soldered on a 1.5 mm copper thickness FR4 board with a 6 cm^2 dissipating footprint (copper thickness of 35 µm), the $R_{th(j\text{-}amb)}$ is about 35 °C/W. Figure 26 shows mounting methods for this package. Using a multilayer board with vias to a ground plane, thermal impedance can be reduced down to 15 °C/W.

Figure 25. PowerSO36 junction ambient thermal resistance versus on-board copper area

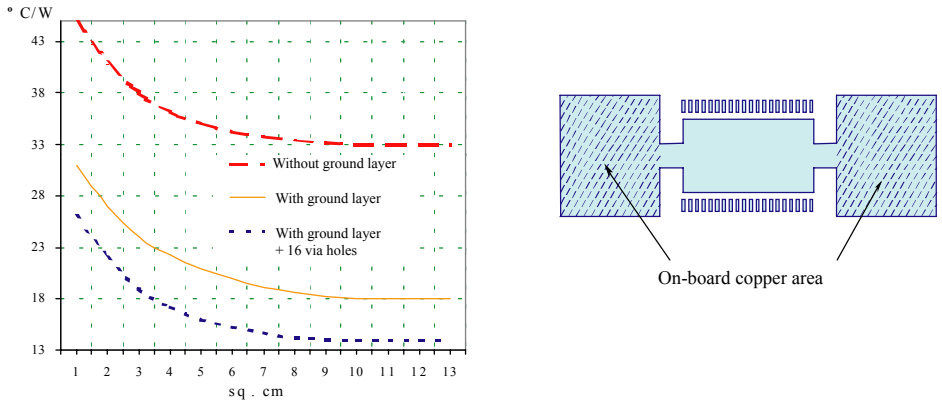


Figure 26. SO24 junction ambient thermal resistance versus on-board copper area

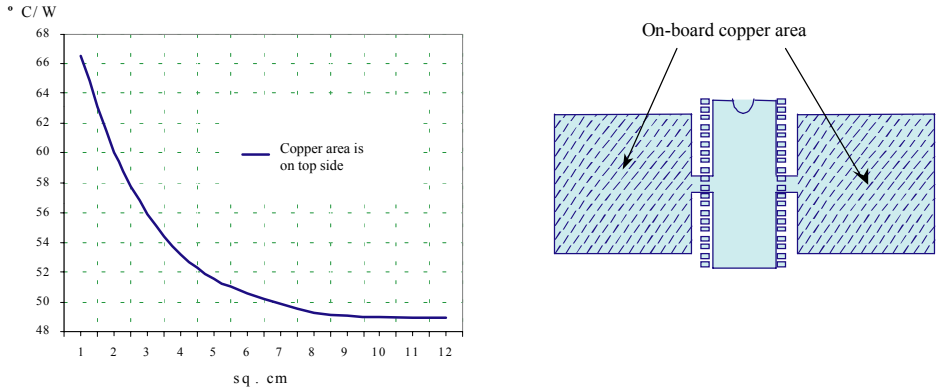
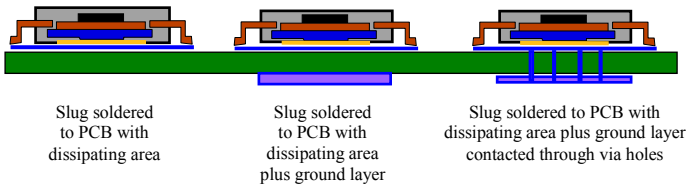


Figure 27. Mounting the PowerSO package



14 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

14.1 PowerSO36 package information

Figure 28. PowerSO36 package outline

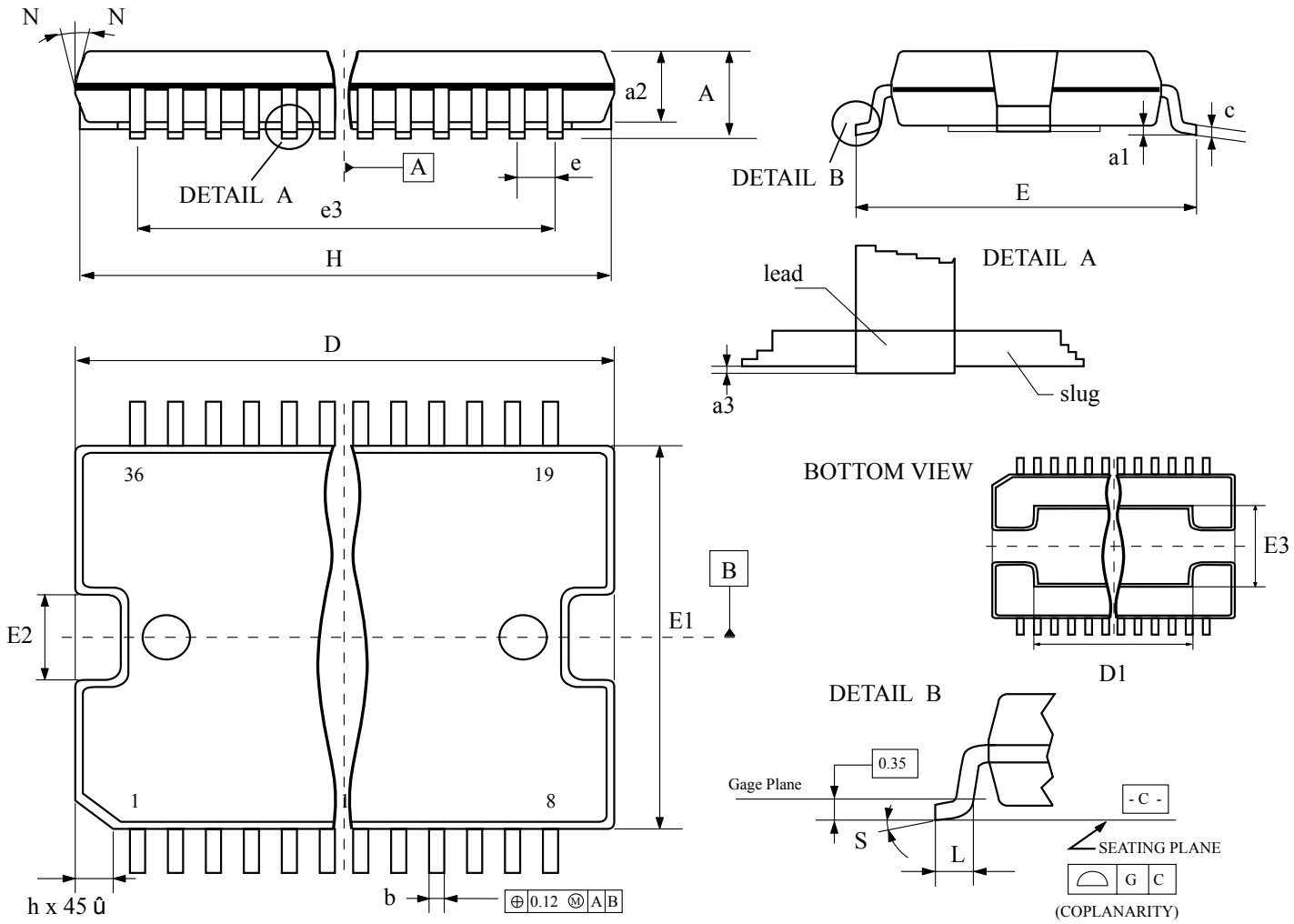


Table 9. **PowerSO36 package mechanical data**

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	3.60	-	-	0.141
a1	0.10	-	0.30	0.004	-	0.012
a2	-	-	3.30		-	0.130
a3	0	-	0.10	0	-	0.004
b	0.22	-	0.38	0.008	-	0.015
c	0.23	-	0.32	0.009	-	0.012
D (1)	15.80	-	16.00	0.622	-	0.630
D1	9.40	-	9.80	0.370	-	0.385
E	13.90	-	14.50	0.547	-	0.570
e	-	0.65	-	-	0.0256	-
e3	-	11.05	-	-	0.435	-
E1 (1)	10.90	-	11.10	0.429	-	0.437
E2	-	-	2.90		-	0.114
E3	5.80	-	6.20	0.228	-	0.244
E4	2.90	-	3.20	0.114	-	0.126
G	0	-	0.10	0	-	0.004
H	15.50	-	15.90	0.610	-	0.626
h	-	-	1.10		-	0.043
L	0.80	-	1.10	0.031	-	0.043
N	10° (max.)					
S	8° (max.)					

1. *"D" and "E1" do not include mold flash or protrusions.*
   - *- Mold flash or protrusions shall not exceed 0.15 mm (0.006 inch)*
   - *- Critical dimensions are "a3", "E" and "G".*

14.2 SO24 package information

Figure 29. **SO24 package outline**

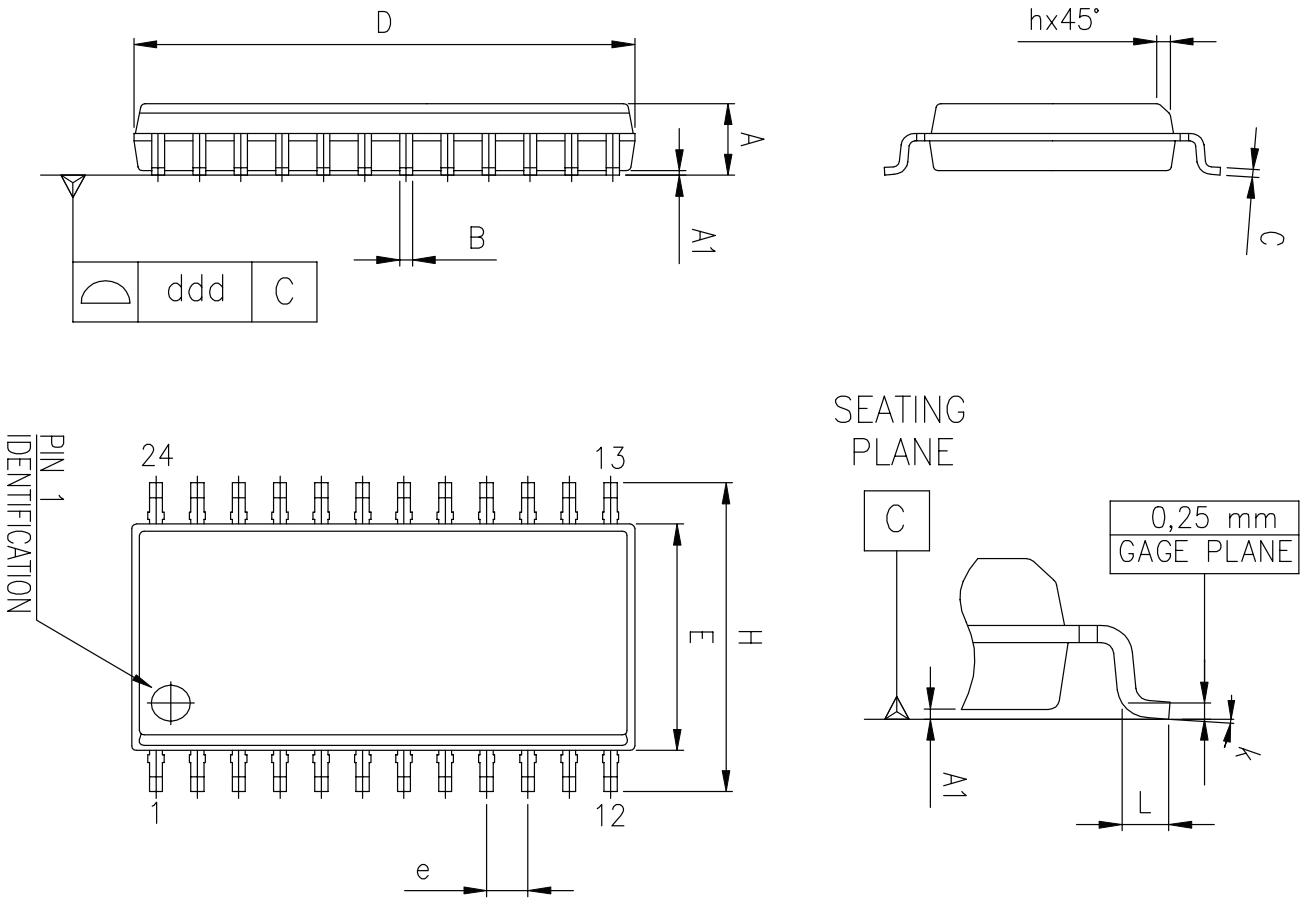


Table 10. **SO24 package mechanical data**

Symbol	Dimensions (mm)			Dimensions (inch)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.35	-	2.65	0.093	-	0.104
A1	0.10	-	0.30	0.004	-	0.012
B	0.33	-	0.51	0.013	-	0.020
C	0.23	-	0.32	0.009	-	0.013
D (1)	15.20	-	15.60	0.598	-	0.614
E	7.40	-	7.60	0.291	-	0.299
e	-	1.27	-	-	0.050	-
H	10.0	-	10.65	0.394	-	0.419
h	0.25	-	0.75	0.010	-	0.030
L	0.40	-	1.27	0.016	-	0.050
k	0°(min.), 8° (max.)					
ddd	-	-	0.10	-	-	0.004

1. *"D" dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.*

Revision hystory

Date	Revision	Changes
1-Sep-2003	1	First issue
1-Jan-2004	2	Migration from ST-Press dms to EDOCS
1-Oct-2004	3	Updated the style graphic form
6-Mar-2014	4	Updated *Section :Features on page 1* (removed section number from*: Features*, minor modifications). Updated *Section : Description on page 1* (removed section number from*:Description*, removed "MultiPower-" from "MultiPower-BCD technology"). Added *Contents on page 2*. Updated *Section 1: Blockdiagramonpage 3*(added section title, renumbered *Figure1:Block diagram*). Added title to *Section 2:Maximum ratingson page 4*. Added title to *Section 3: Pin connections on page 6*, renumbered *Figure 2: Pin connections (top view)*, renumbered note *1*below *Figure 2*. Added title to *Section 4:Electricalcharacteristics onpage 8*, renumbered notes *1* to*4*below *Table 6*, renumbered *Figure 3*and *Figure 4*. Renumbered *Section 5:Circuitdescription onpage 11*, *Section 5.1* and *Section5.2*. Removed "and mC" fromfirst sentence in *Section 5.2*. Added header to *Table7*.Renumbered *Figure 5* to *Figure 8*. Renumbered *Section6:PWMcurrentcontrolonpage 13*. Renumbered *Figure9*to *Figure12*. Numbered *Equation 1* to *Equation 4*. Renumbered *Section 7:Slowdecaymode on page 17*and *Figure 13*. Renumbered *Section 8:Decoding logicon page 18*, *Figure14*and *Figure 15*. Renumbered and renamed *Section 9: Tachometer on page 20*, renumbered *Figure16*to *Figure 18*. Numbered *Equation 5* and *Equation 6*. Renumbered *Section 10:Non-dissipativeovercurrent detectionand protection on page 22*, *Figure 19*to *Figure22*. Renumbered *Section 11:Applicationinformation on page 25*,*Section 11.1* and *Section 11.2*. Added header to *Table 9*. Renumbered *Figure 23* to *Figure 28*. Updated *Section 12: Package information on page 29* (added main title and ECOPACK text. Added titles from *Table 10: PowerSO36 package mechanical data* to*Table 12: SO24 package mechanical data* and from *Figure 29: PowerSO36 package outline* to *Figure 31: SO24 package outline*, reversed order of named tables and figures. Removed 3D figures of packages. Replaced 0.200 by0.020 inch of max. B value in *Table 12*). Added cross-references throughout document. Added section number and title to *Section13:Revisionhistory*. Minor modifications throughout document
4-Oct-2018	5	Removed PowerDIP24 package from the whole document. Removed "Tj" from Table 3 Minor modifications throughout document
4-Nov-2021	6	Added Application section in cover page. Updated order codes, see Product status link / summary in cover page Updated V_S Min. value in Table 2

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