FEATURES

- *Guaranteed max.* 0.5μV/°C Drift
- *Guaranteed max.* 0.6μV pk-pk Noise
- *Guaranteed max.* 2nA Bias Current
- *Guaranteed minimum* 114dB CMRR

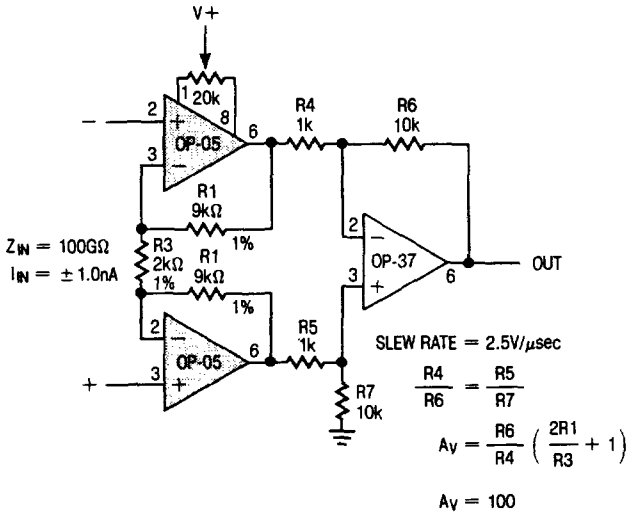
APPLICATIONS

- Strain Gauges
- Thermocouple Amplifiers
- Instrumentation Amplifiers
- Medical Instruments

DESCRIPTION

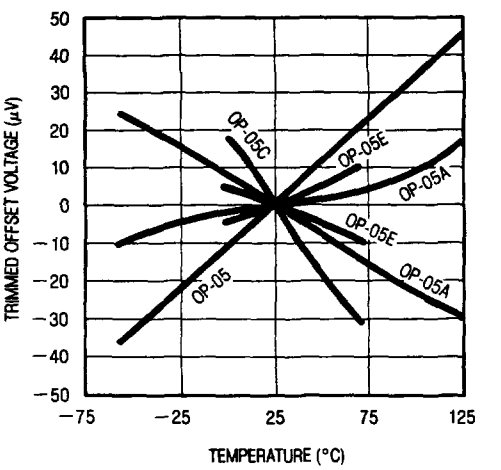
The OP-05 is an internally compensated op-amp which provides excellent input offset voltage, low bias current, very high common mode rejection, and low offset voltage drift with temperature when the input offset voltage is externally trimmed to zero. Direct replacement of similar devices in existing systems can result in significant system performance improvement without redesign. The OP-05 is particularly well suited for instrumentation and low signal level applications where precision and stability over time and temperature are important. Internal frequency compensation enhances the OP-05's versatility for a wide variety of precision op-amp uses. Linear's advanced design, process and test techniques ensure device performance as well as reliability. An instrumentation amplifier application is shown below. For higher performance requirements see the LT1001 single precision op amp and the LT1002 dual matched precision op amp series.

Instrumentation Amplifier



Trimmed Offset Voltage with Temperature of Six Representative Units

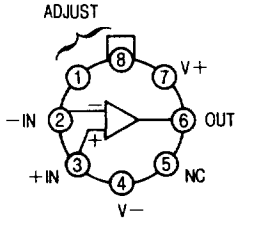
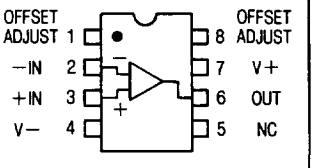
(Offset Trimmed to Zero at 25°C with 20kΩ Pot)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage Equal to Supply Voltage
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range
OP-05/OP-05A ..... −55°C to 125°C
OP-05E/OP-05C ..... 0°C to 70°C
Storage Temperature Range
All Devices ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NO.	OFFSET VOLTAGE MAX
TOP VIEW OFFSET ADJUST  METAL CAN H PACKAGE	OP-05AH OP-05H OP-05EH OP-05CH	0.15mV 0.5mV 0.5mV 1.3mV
TOP VIEW  HERMETIC J8 PACKAGE PLASTIC DIP N8 PACKAGE	OP-05AJ8 OP-05J8 OP-05EJ8 OP-05CJ8 OP-05EN8 OP-05CN8	0.15mV 0.5mV 0.5mV 1.3mV 0.5mV 1.3mV

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-05A MIN	OP-05A TYP	OP-05A MAX	OP-05 MIN	OP-05 TYP	OP-05 MAX	UNITS
V_{OS}	Input Offset Voltage			0.07	0.15		0.2	0.5	mV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Notes 1 and 2)		0.2	1.0		0.2	1.0	µV/Month
I_{OS}	Input Offset Current			0.7	2.0		1.0	2.8	nA
I_B	Input Bias Current			±0.7	±2.0		±1.0	±3.0	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.35	0.6		0.35	0.6	μV_{p-p}
	Input Noise Voltage Density	f_o = 10Hz f_o = 100Hz (Note 2) f_o = 1000Hz		10.3 10.0 9.6	18.0 13.0 11.0		10.3 10.0 9.6	18.0 13.0 11.0	nV/√Hz
i_n	Input Noise Current	0.1Hz to 10Hz (Note 2)		14	30		14	30	pA_{p-p}
	Input Noise Current Density	f_o = 10Hz f_o = 100Hz (Note 2) f_o = 1000Hz		0.32 0.14 0.12	0.80 0.23 0.17		0.32 0.14 0.12	0.80 0.23 0.17	pA/√Hz
R_{in}	Input Resistance Differential Mode	(Note 3)	30	80		20	60		MΩ
	Input Resistance Common Mode			200			200		GΩ
	Input Voltage Range		±13.5	±14.0		±13.5	±14.0		V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±13.5V	114	126		114	126		dB
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±18V	100	108		100	108		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V $R_L \geq 500\Omega$, V_O = ±0.5V V_S = ±3V (Note 3)	300 150	500 500		200 150	500 500		V/mV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.3		0.1	0.3		V/µS
GBW	Closed Loop Bandwidth	A_{VCL} = +1 (Note 2)	0.4	0.6		0.4	0.6		MHz
Z_o	Open Loop Output Impedance	V_O = 0, I_O = 0, f = 10Hz		60			60		Ω
P_d	Power Dissipation	No load V_S = ±3V, No load		90 4	120 6		90 4	120 6	mW
	Offset Adjustment Range	Null Pot = 20kΩ		±4			±4		mV

See Notes on page 2-324

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		OP-05A MIN	OP-05A TYP	OP-05A MAX	OP-05 MIN	OP-05 TYP	OP-05 MAX	UNITS
V_{OS}	Input Offset Voltage		●		0.10	0.24		0.3	0.7	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift Without External Trim With External Trim	 Null Pot = 20kΩ (Note 2)	 ● ●		 0.3 0.2	 0.9 0.5		 0.7 0.3	 2.0 1.0	μV/°C
I_{OS}	Input Offset Current		●		1.0	4.0		1.8	5.6	nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Input Offset Current Drift	(Note 2)	●		5	25		8	50	pA/°C
I_B	Input Bias Current		●		±1.0	±4.0		±2.0	±6.0	nA
$\frac{\Delta I_B}{\Delta Temp}$	Average Input Bias Current Drift	(Note 2)	●		8	25		13	50	pA/°C
	Input Voltage Range		●	±13.0	±13.5		±13.0	±13.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	110	123		110	123		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	94	106		94	106		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$	●	200	400		150	400		V/mV
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.0	±12.6		±12.0	±12.6		V

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-05E MIN	OP-05E TYP	OP-05E MAX	OP-05C MIN	OP-05C TYP	OP-05C MAX	UNITS
V_{OS}	Input Offset Voltage			0.2	0.5		0.3	1.3	mV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Notes 1 and 2)		0.3	1.5		0.4	2.0	μV/Month
I_{OS}	Input Offset Current			1.2	3.8		1.8	6.0	nA
I_B	Input Bias Current			±1.2	±4.0		±1.8	±7.0	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.35	0.6		0.38	0.65	μV_{p-p}
	Input Noise Voltage Density	$f_o = 10Hz$ $f_o = 100Hz$ (Note 2) $f_o = 1000Hz$		10.3 10.0 9.6	18.0 13.0 11.0		10.5 10.2 9.8	20.0 13.5 11.5	$nV/\sqrt{Hz}$
i_n	Input Noise Current	0.1Hz to 10Hz (Note 2)		14	30		15	35	pA_{p-p}
	Input Noise Current Density	$f_o = 10Hz$ $f_o = 100Hz$ (Note 2) $f_o = 1000Hz$		0.32 0.14 0.12	0.80 0.23 0.17		0.35 0.15 0.13	0.90 0.27 0.18	$pA/\sqrt{Hz}$
R_{in}	Input Resistance Differential Mode	(Note 3)	15	50		8	33		MΩ
	Input Resistance Common Mode			160			120		GΩ
	Input Voltage Range		±13.5	±14.0		±13.5	±14.0		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	110	123		100	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	94	106		90	104		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 500\Omega$, $V_O = \pm 0.5V$ $V_S = \pm 3V$ (Note 3)	200 150	500 500		120 100	400 400		V/mV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		±12.0 ±11.5	±13.0 ±12.8 ±12.0		V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.3		0.1	0.3		V/μS
GBW	Closed Loop Bandwidth	$A_{VCL} = +1$ (Note 2)	0.4	0.6		0.4	0.6		MHz
Z_o	Open Loop Output Impedance	$V_O = 0$, $I_O = 0$, $f = 10Hz$		60			60		Ω
P_d	Power Dissipation	No load $V_S = \pm 3V$, No load		90 4	120 6		95 4	150 8	mW
	Offset Adjustment Range	Null Pot = 20kΩ		±4			±4		mW

See Notes on page 2-324

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $0°C \leq T_A \leq 70°C$.

SYMBOL	PARAMETER	CONDITIONS		OP-05E MIN	OP-05E TYP	OP-05E MAX	OP-05C MIN	OP-05C TYP	OP-05C MAX	UNITS
V_{OS}	Input Offset Voltage		●		0.25	0.6		0.35	1.6	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift									
	Without External Trim		●		0.7	2.0		1.3	4.5	μV/°C
	With External Trim	Null Pot = 20kΩ (Note 2)	●		0.2	0.6		0.4	1.5	
I_{OS}	Input Offset Current		●		1.4	5.3		2.0	8.0	nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Input Offset Current Drift	(Note 2)	●		8	35		12	50	pA/°C
I_B	Input Bias Current		●		±1.5	±5.5		±2.2	±9.0	nA
$\frac{\Delta I_B}{\Delta Temp}$	Average Input Bias Current Drift	(Note 2)	●		13	35		18	50	pA/°C
	Input Voltage Range		●	±13.0	±13.5		±13.0	±13.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	107	123		97	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	90	103		86	100		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$	●	180	450		100	400		V/mV
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.0	±12.6		±11.0	±12.6		V

The ● denotes the specifications which apply over the full operating temperature range.

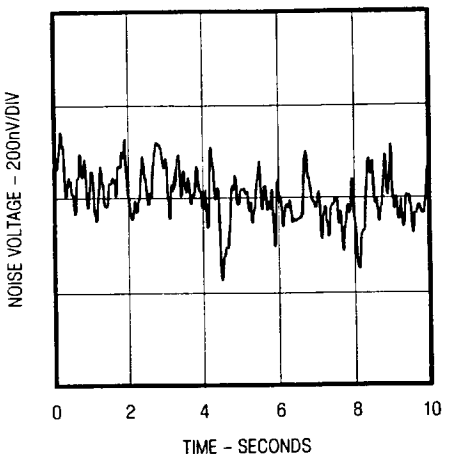
Note 1: Long term offset voltage stability is the average value of offset voltage vs. time plotted over extended periods following 30 days of operation. Values for time under 30 days of operation are typically 2.5μV following the first hour of operation.

Note 2: This parameter is sample tested.

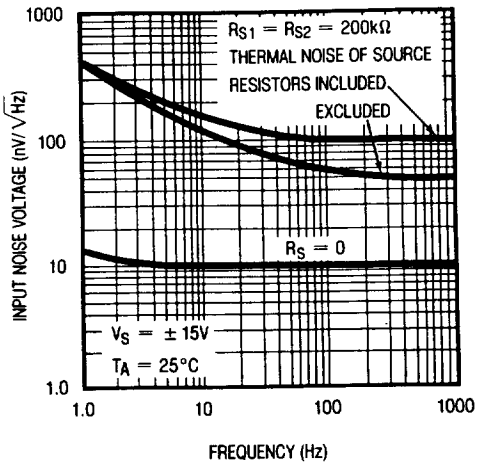
Note 3: This parameter is guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

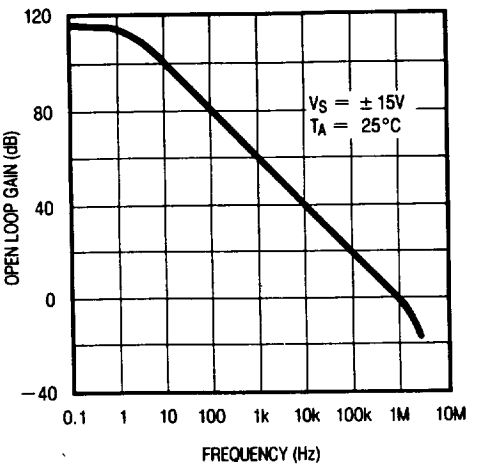
Low Frequency Noise (Closed Loop Gain = 25,000)



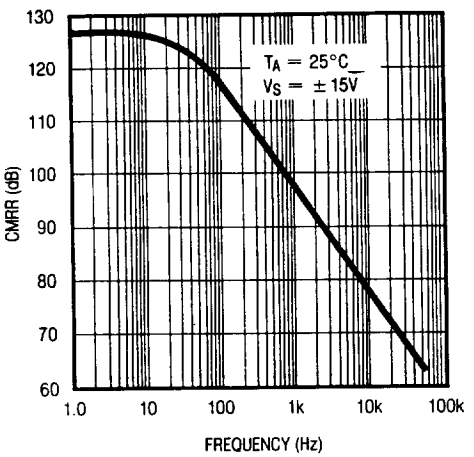
Total Input Noise Voltage vs Frequency



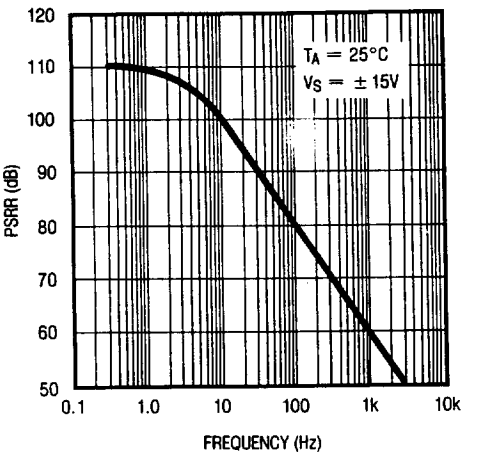
Open-Loop Frequency Response



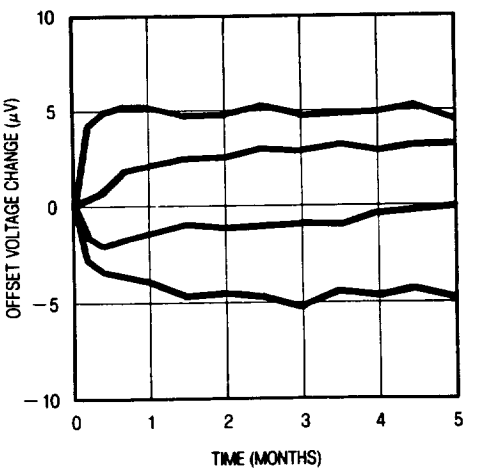
Common Mode Rejection Ratio vs Frequency



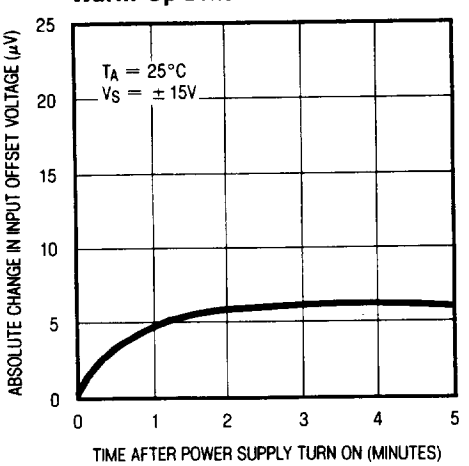
Power Supply Rejection Ratio vs Frequency



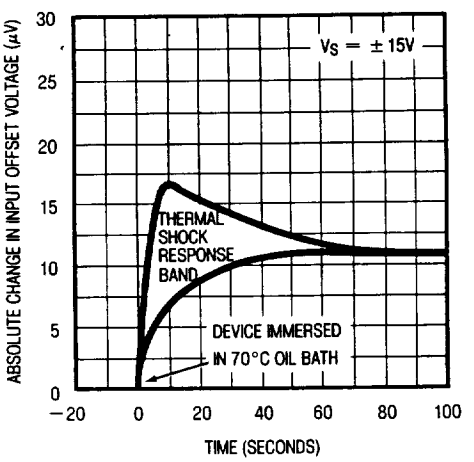
Long Term Stability of Four Representative Units



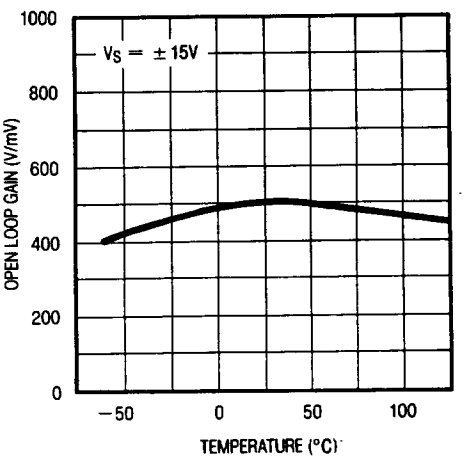
Warm-Up Drift



Offset Voltage Change Due to Thermal Shock



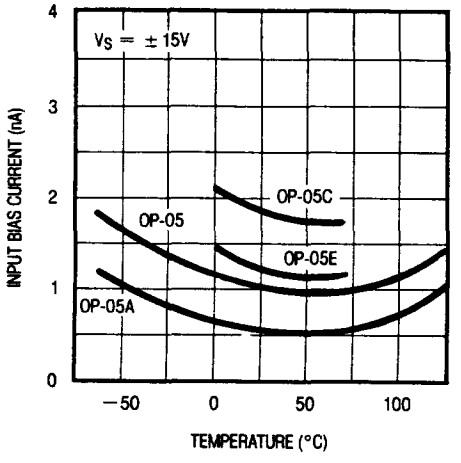
Open-Loop Gain vs Temperature



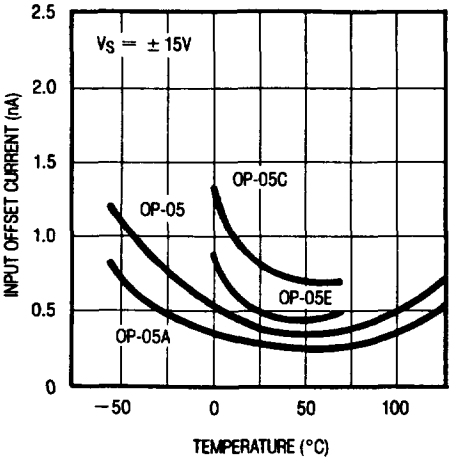
2

TYPICAL PERFORMANCE CHARACTERISTICS

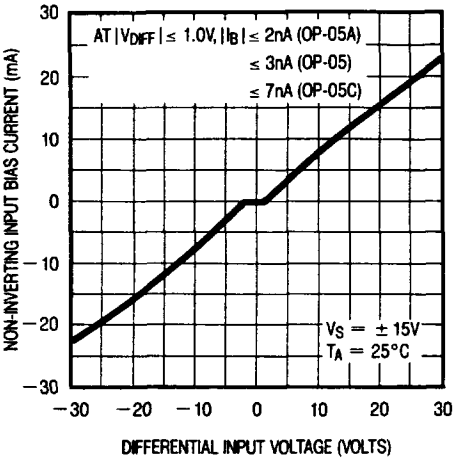
Input Bias Current vs Temperature



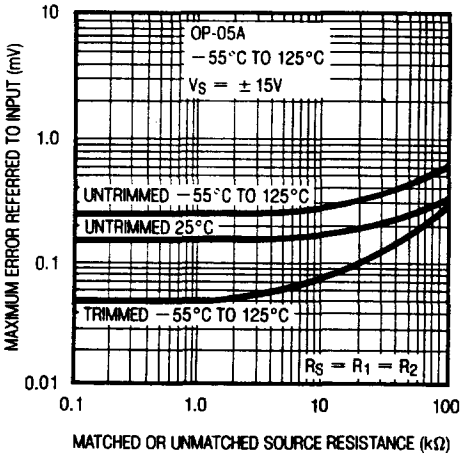
Input Offset Current vs Temperature



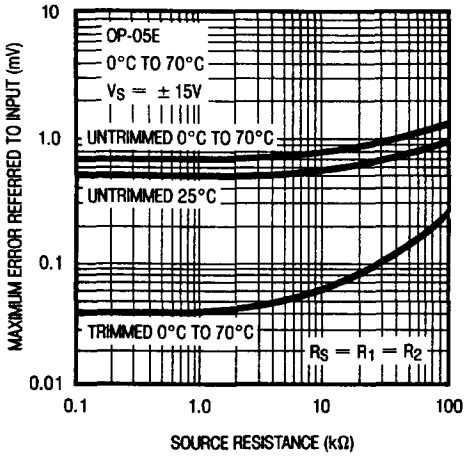
Input Bias Current vs Differential Input Voltage



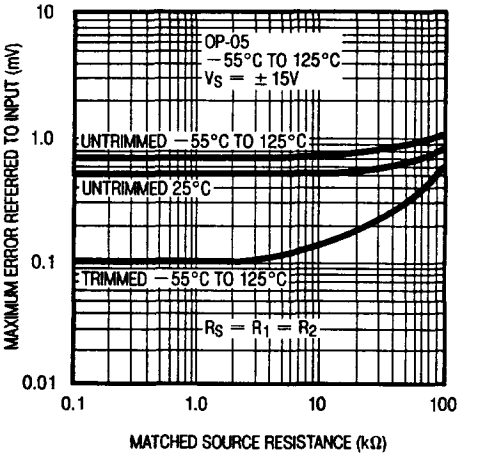
Maximum Error vs Source Resistance



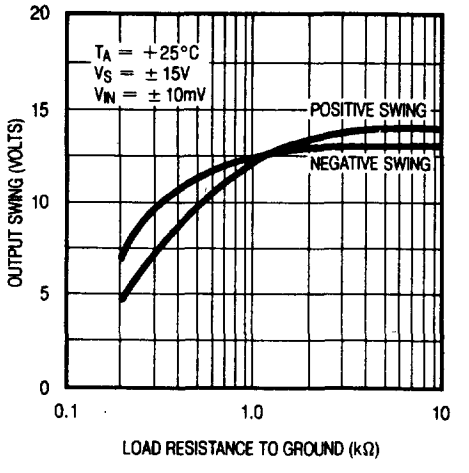
Maximum Error vs Source Resistance



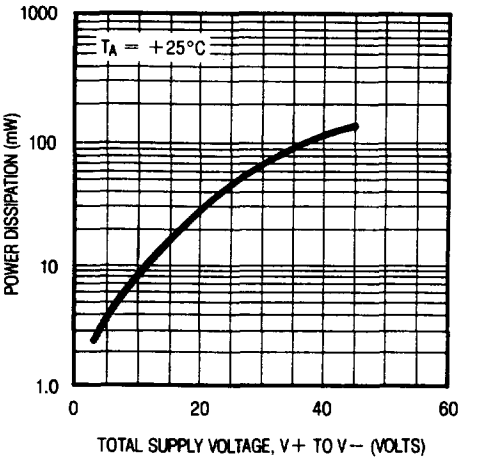
Maximum Error vs Source Resistance



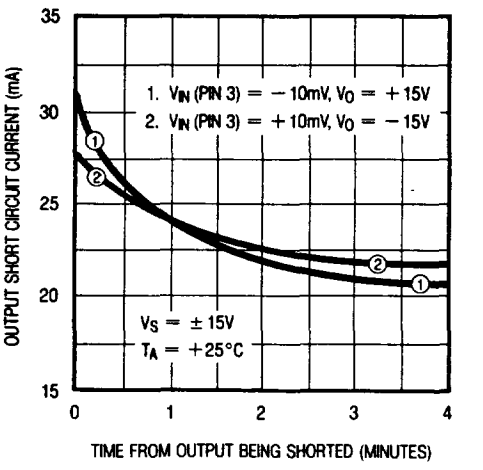
Output Voltage vs Load Resistance



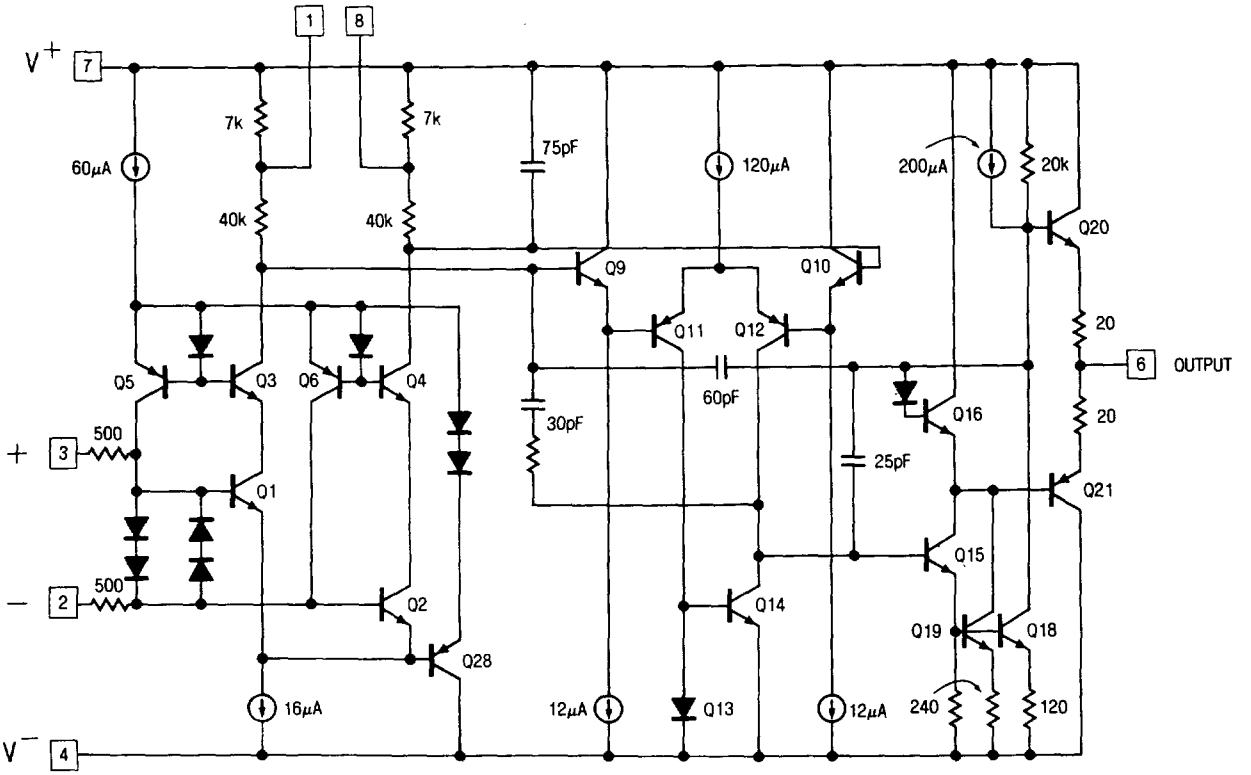
Power Consumption vs Power Supply



Output Short-Circuit Current vs Time

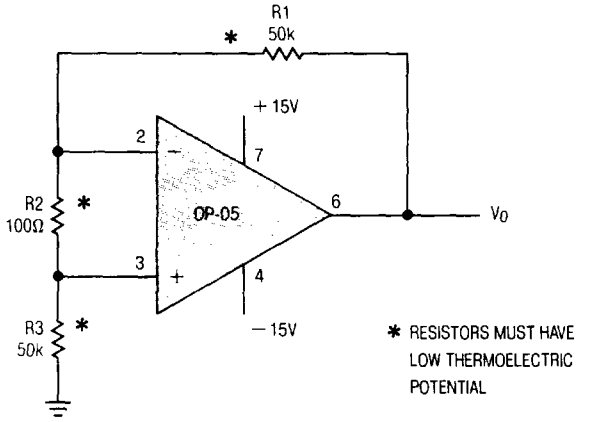


SCHEMATIC DIAGRAM



TEST CIRCUIT DIAGRAMS

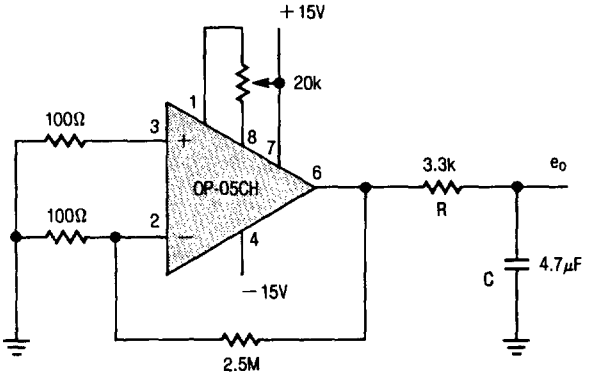
Offset Voltage Test Circuit †



$A_V = 1000$

† This circuit is also used as the burn-in configuration with supply voltages changed to ±20V, R1 = R3 = 10k, R2 = 200Ω, A_V = 100.

Offset Nulling and Low Frequency Noise Test Circuit



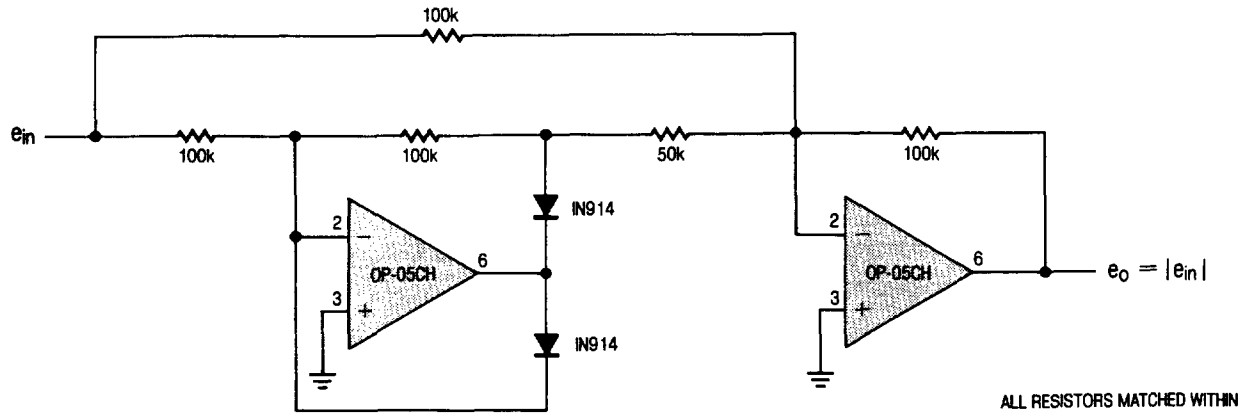
NOTES:
1) RC APPROXIMATELY 10Hz FILTER
2) OBSERVE OUTPUT FOR 10 SECONDS
A_V = 25000

Application Tip

When the OP-05 is used as a replacement in 725, 108/108A, 308/308A applications, removal of external compensation is optional. For conventionally nulled 741 type applications, external trimming should be removed. Care should be taken to avoid thermocouple voltages caused by temperature variations between the input terminals or dissimilar metals.

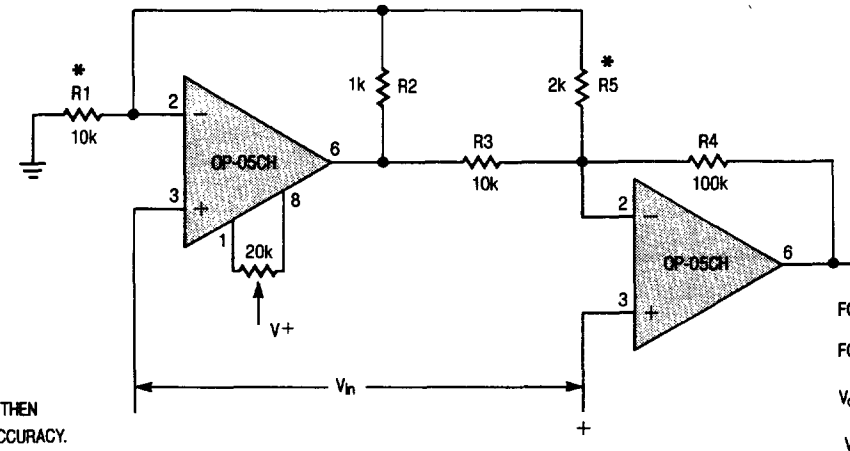
TYPICAL APPLICATIONS

Precision Absolute Value Circuit



ALL RESISTORS MATCHED WITHIN 0.1%

Two Op-Amp Instrumentation Amplifier



FOR MAXIMUM CMRR, $\frac{R2}{R1} = \frac{R3}{R4}$

FOR THIS CONDITION,

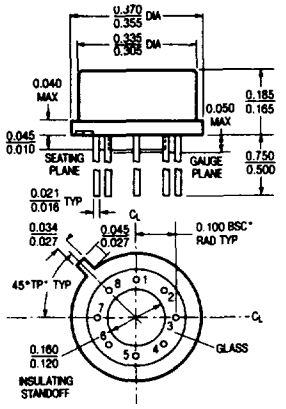
$$V_o = V_{in}\left[\frac{R4}{R3}\right]\left[1 + \frac{R2}{R1} + \frac{R2 + R3}{R5}\right]$$

$\frac{V_o}{V_{in}}$ = 210 FOR VALUES SHOWN

*ADJUST R1 FOR CMRR, THEN ADJUST R5 FOR GAIN ACCURACY. R5 DOES NOT AFFECT CMRR.

PACKAGE DESCRIPTION

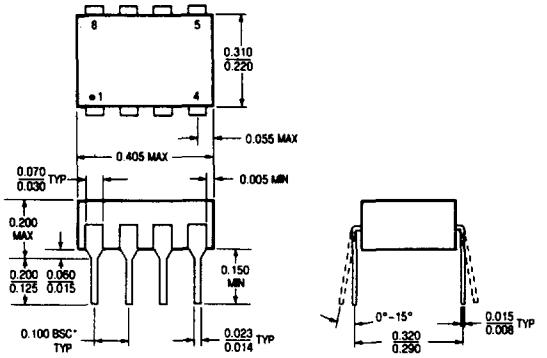
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES

$T_j$max	Θ_{ja}	Θ_{jc}
150°C	150°C/W	45°C/W

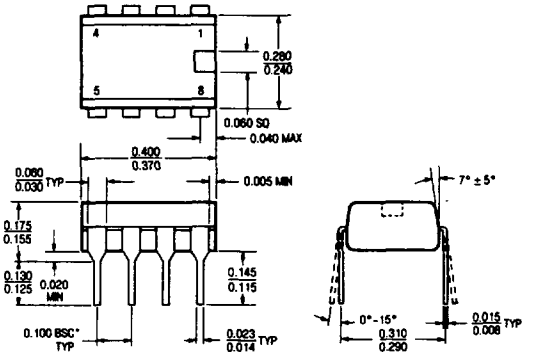
J8 Package
8 Lead Hermetic Dip



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	Θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE.

$T_j$max	Θ_{ja}
100°C	130°C/W