NCV4269A

LDO Linear Regulator - Micropower, DELAY, Adjustable RESET, Sense Output

5.0 V, 3.3 V, 150 mA

The NCV4269A is a 5.0 V and 3.3 V precision micropower voltage regulator with an output current capability of 150 mA.

The output voltage is accurate within ±2.0% with a maximum dropout voltage of 0.5 V at 100 mA. Low quiescent current is a feature drawing only 190 μA with a 1.0 mA load. This part is ideal for any and all battery operated microprocessor equipment.

Microprocessor control logic includes an active reset output RO with delay and a SI/SO monitor which can be used to provide an early warning signal to the microprocessor of a potential impending reset signal. The use of the SI/SO monitor allows the microprocessor to finish any signal processing before the reset shuts the microprocessor down.

The active Reset circuit operates correctly at an output voltage as low as 1.0 V. The Reset function is activated during the power up sequence or during normal operation if the output voltage drops outside the regulation limits.

The reset threshold voltage can be decreased by the connection of an external resistor divider to the R_{ADJ} lead. The regulator is protected against reverse battery, short circuit, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments. The device has also been optimized for EMC conditions.

Features

- 5.0 V and 3.3 V Output Voltage Options, ± 2.0% Accuracy
- Low 190 μA Quiescent Current
- Active Reset Output Low Down to V_Q = 1.0 V
- Adjustable Reset Threshold
- 150 mA Output Current Capability
- Fault Protection
  - +60 V Peak Transient Voltage
  - −40 V Reverse Voltage
  - Short Circuit
  - Thermal Overload
- Early Warning through SI/SO Leads
- Internally Fused Leads in SO−14 and SO−20 Packages
- Integrated Pullup Resistor at Logic Outputs (To Use External Resistors, Select the NCV4279A)
- Very Low Dropout Voltage
- Electrical Parameters Guaranteed Over Entire Temperature Range
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

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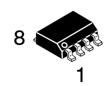
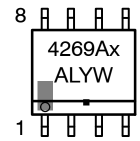
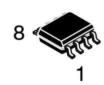
MARKING DIAGRAMS

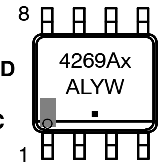


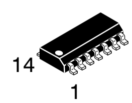
SO−8 D1 SUFFIX CASE 751



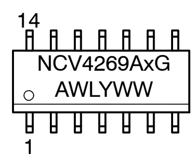


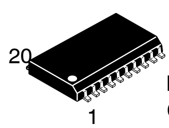
SO−8 EXPOSED PAD PD SUFFIX CASE 751AC



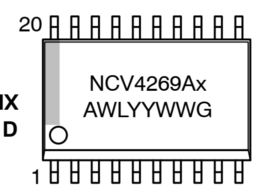


SO−14 D2 SUFFIX CASE 751A





SO−20 DW SUFFIX CASE 751D



X	= 5 (5.0 V Output)	
	= 3 (3.3 V Output)	
A	= Assembly Location	
WL, L	= Wafer Lot	
YY, Y	= Year	
WW, W	= Work Week	
G, ▪	= Pb Free	

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.

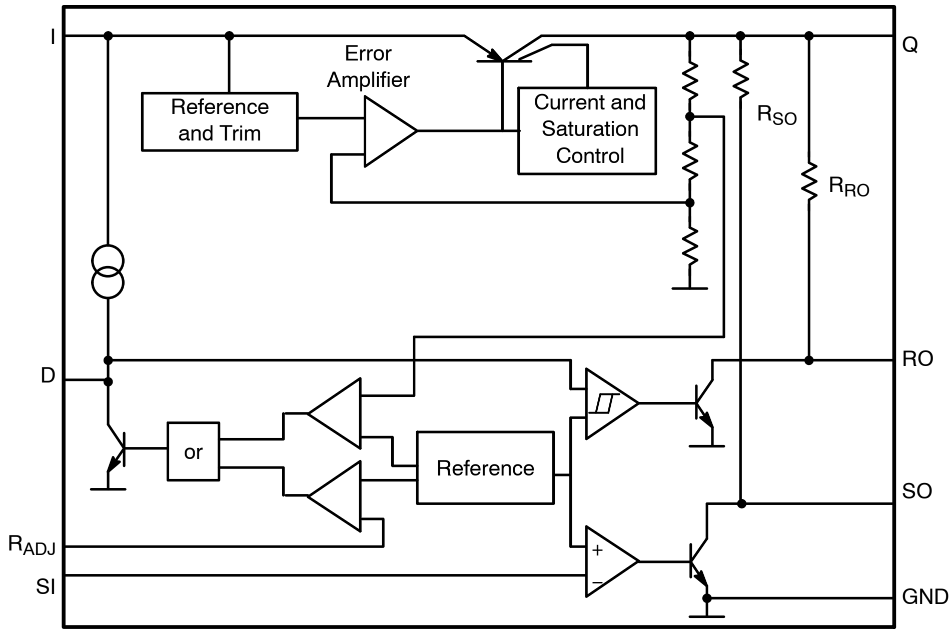
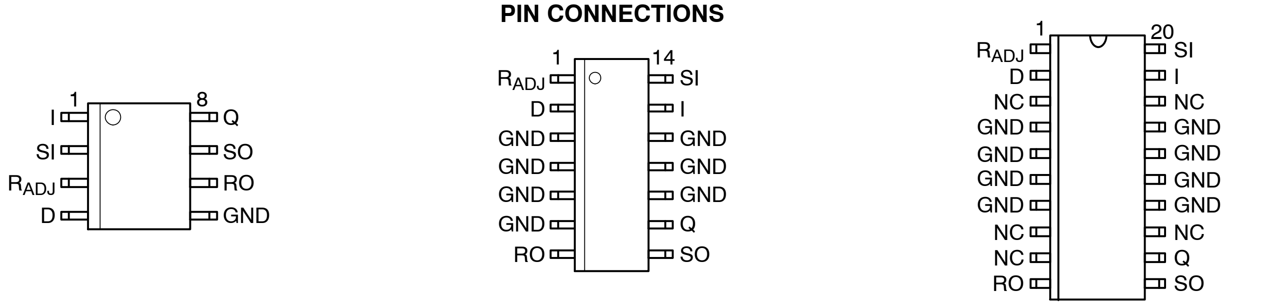


Figure 1. Block Diagram

PIN CONNECTIONS



SO−8 SO−14 SO−20L

PACKAGE PIN DESCRIPTION

Package Pin Number				Pin Symbol	Function
SO−8	SO−8 EP	SO−14	SO−20L		
3	3	1	1	R_{ADJ}	Reset Threshold Adjust; if not used to connect to GND.
4	4	2	2	D	Reset Delay; To Set Time Delay, Connect to GND with Capacitor
5	5	3, 4, 5, 6, 10, 11, 12	4, 5, 6, 7, 14, 15, 16, 17	GND	Ground
–	–	–	3, 8, 9, 13, 18	NC	No connection to these pins from the IC.
6	6	7	10	RO	Reset Output; The Open−Collector Output has a 20 kΩ Pullup Resistor to Q. Leave Open if Not Used.
7	7	8	11	SO	Sense Output; This Open−Collector Output is Internally Pulled Up by 20 kΩ pullup resistor to Q. If not used, keep open.
8	8	9	12	Q	5 V or 3.3 V Output; Connect to GND with a 10 μF Capacitor, ESR < 5 Ω
1	1	13	19	I	Input; Connect to GND Directly at the IC with a Ceramic Capacitor.
2	2	14	20	SI	Sense Input; If not used, Connect to Q.
–	EPAD	–	–	EPAD	Connect to ground potential or leave unconnected

MAXIMUM RATINGS (T_J = −40°C to 150°C)

Parameter	Symbol	Min	Max	Unit
Input to Regulator	V_I I_I	−40 Internally Limited	45 Internally Limited	V
Input Transient to Regulator	V_I	–	60	V
Sense Input	V_{SI} I_{SI}	−40 −1	45 1	V mA
Reset Threshold Adjust	V_{RADJ} I_{RADJ}	−0.3 −10	7 10	V mA
Reset Delay	V_D I_D	−0.3 Internally Limited	7 Internally Limited	V
Ground	I_q	50	–	mA
Reset Output	V_{RO} I_{RO}	−0.3 Internally Limited	7 Internally Limited	V
Sense Output	V_{SO} I_{SO}	−0.3 Internally Limited	7 Internally Limited	V
Regulated Output	V_Q I_Q	−0.5 −10	7.0 –	V mA
Junction Temperature Storage Temperature	T_J T_{STG}	– −50	150 150	°C °C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING RANGE

Input Voltage Operating Range 5.0 Version 3.3 Version	V_I	 5.5 4.4	 45 45	V
Junction Temperature Operating Range	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

LEAD TEMPERATURE SOLDERING AND MSL

Parameter	Symbol	Value
MSL, 20−Lead LS Temperature 265°C Peak (Note 3)	MSL	3
MSL, 8−Lead, 14−Lead, LS Temperature 265°C Peak (Note 3)	MSL	1
MSL, 8−Lead EP, LS Temperature 260°C	MSL	2

1. This device series incorporates ESD protection and exceeds the following ratings:
   Human Body Model (HBM) ≤ 4.0 kV per AEC−Q100−002.
   Machine Model (MM) ≤ 200 V per AEC−Q100−003.
2. Latchup Current Maximum Rating: ≤ 150 mA per AEC−Q100−004.
3. +5°C/−0°C, 40 Sec Max−at−Peak, 60 – 150 Sec above 217°C.

THERMAL CHARACTERISTICS

Characteristic	Test Conditions (Typical Values)	Unit
SO−8 Package (Note 4)		
Junction−to−Pin 4 (Ψ – JL4, Ψ_{L4})	53.8	°C/W
Junction−to−Ambient Thermal Resistance ($R_{\theta JA}$, θ_{JA})	170.9	°C/W
SO−8 EP Package (Note 4)		
Junction−to−Pin 8 (Ψ – JL8, Ψ_{L8})	23.7	°C/W
Junction−to−Ambient Thermal Resistance ($R_{\theta JA}$, θ_{JA})	71.4	°C/W
Junction−to−Pad (Ψ – JPad)	7.7	°C/W
SO−14 Package (Note 4)		
Junction−to−Pin 4 (Ψ – JL4, Ψ_{L4})	18.4	°C/W
Junction−to−Ambient Thermal Resistance ($R_{\theta JA}$, θ_{JA})	111.6	°C/W
SO−20 Package (Note 4)		
Junction−to−Pin 4 (Ψ – JL4, Ψ_{L4})	21.8	°C/W
Junction−to−Ambient Thermal Resistance ($R_{\theta JA}$, θ_{JA})	95.3	°C/W

4. 2 oz copper, 50 mm^2 copper area, 1.5 mm thick FR4

ELECTRICAL CHARACTERISTICS ($-40°C \le T_J \le 150°C$, V_I = 13.5 V unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
REGULATOR						
Output Voltage (5.0 V Version)	V_Q	1 mA $\le I_Q \le$ 100 mA, 6 V $\le V_I \le$ 16 V	4.90	5.00	5.10	V
Output Voltage (3.3 V Version)	V_Q	1 mA $\le I_Q \le$ 100 mA, 5.5 V $\le V_I \le$ 16 V	3.234	3.30	3.366	V
Current Limit	I_Q	–	150	200	500	mA
Current Consumption; $I_q = I_I - I_Q$	I_q	I_Q = 1 mA, RO, SO High	–	190	250	μA
Current Consumption; $I_q = I_I - I_Q$	I_q	I_Q = 10 mA, RO, SO High	–	250	450	μA
Current Consumption; $I_q = I_I - I_Q$	I_q	I_Q = 50 mA, RO, SO High	–	2.0	3.0	mA
Dropout Voltage (5.0 V Version)	V_{dr}	V_I = 5 V, I_Q = 100 mA	–	0.25	0.5	V
Load Regulation	ΔV_Q	I_Q = 5 mA to 100 mA	–	10	20	mV
Line Regulation	ΔV_Q	V_I = 6 V to 26 V I_Q = 1 mA	–	10	30	mV
RESET GENERATOR						
Reset Switching Threshold 5.0 V Version 3.3 V Version	V_{RT}	 – –	 4.50 2.97	 4.65 3.07	 4.80 3.17	V
Reset Adjust Switching Threshold 5.0 V Version 3.3 V Version	$V_{RADJ,TH}$	 V_Q > 3.5 V V_Q > 2.3 V	 1.26 1.26	 1.35 1.35	 1.44 1.44	V
Reset Pullup Resistance	$R_{RO,INT}$	–	10	20	40	kΩ
Reset Output Saturation Voltage	$V_{RO,SAT}$	$V_Q < V_{RT}$, $R_{RO,\ INT}$	–	0.1	0.4	V
Upper Delay Switching Threshold 5.0 V Version 3.3 V Version	V_{UD}	 – –	 1.4 0.7	 1.8 1.23	 2.2 1.6	V
Lower Delay Switching Threshold 5.0 V Version 3.3 V Version	V_{LD}	 – –	 0.3 0.3	 0.45 0.49	 0.60 0.60	V
Saturation Voltage on Delay Capacitor	$V_{D,SAT}$	$V_Q < V_{RT}$	–	–	0.1	V
Charge Current 5.0 V Version 3.3 V Version	$I_{D,C}$	 V_D = 1 V V_D = 1 V	 3.0 3.0	 6.5 4.3	 9.5 7.0	μA
Delay Time L → H	t_d	C_D = 100 nF	17	28	73	ms
Delay Time H → L	t_{RR}	C_D = 100 nF	–	3.15	–	μs
INPUT VOLTAGE SENSE						
Sense Threshold High	$V_{SI,High}$	–	1.24	1.31	1.38	V
Sense Threshold Low	$V_{SI,Low}$	–	1.16	1.20	1.28	V
Sense Output Saturation Voltage	$V_{SO,Low}$	V_{SI} < 1.20 V; V_Q > 3 V; R_{SO}	–	0.1	0.4	V
Sense Resistor Pullup	$R_{SO,INT}$	–	10	20	40	kΩ
Sense Input Current	I_{SI}	–	−1.0	0.1	1.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

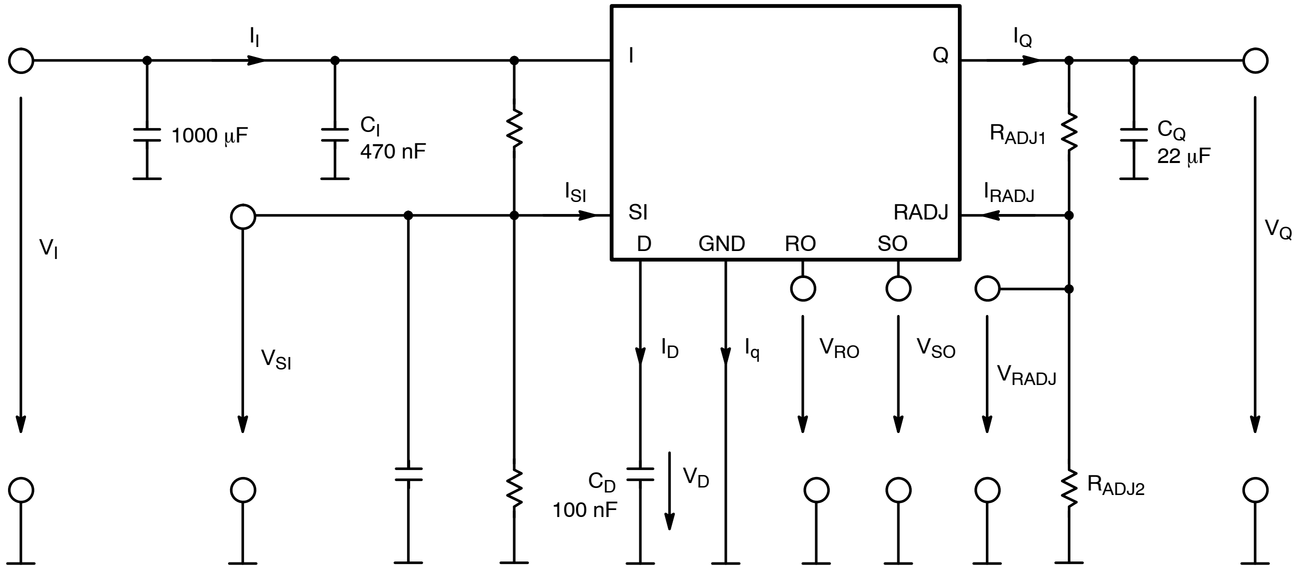


Figure 2. Measuring Circuit

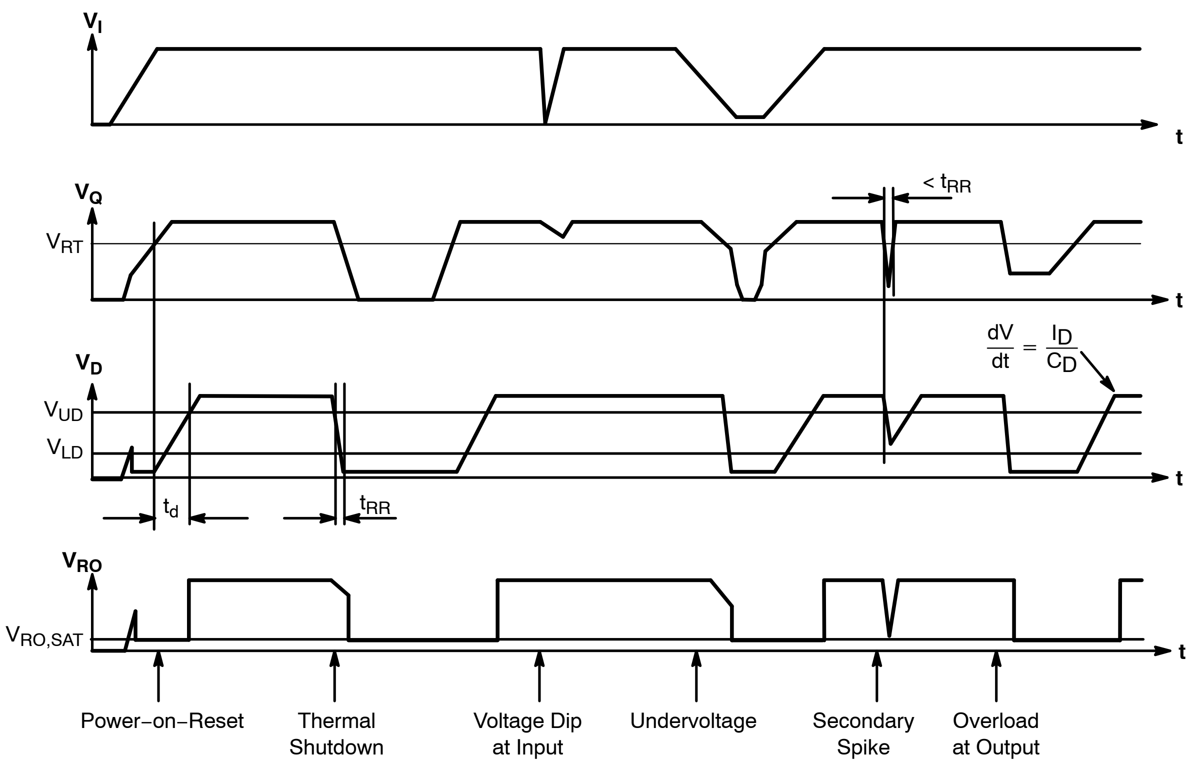


Figure 3. Reset Timing Diagram

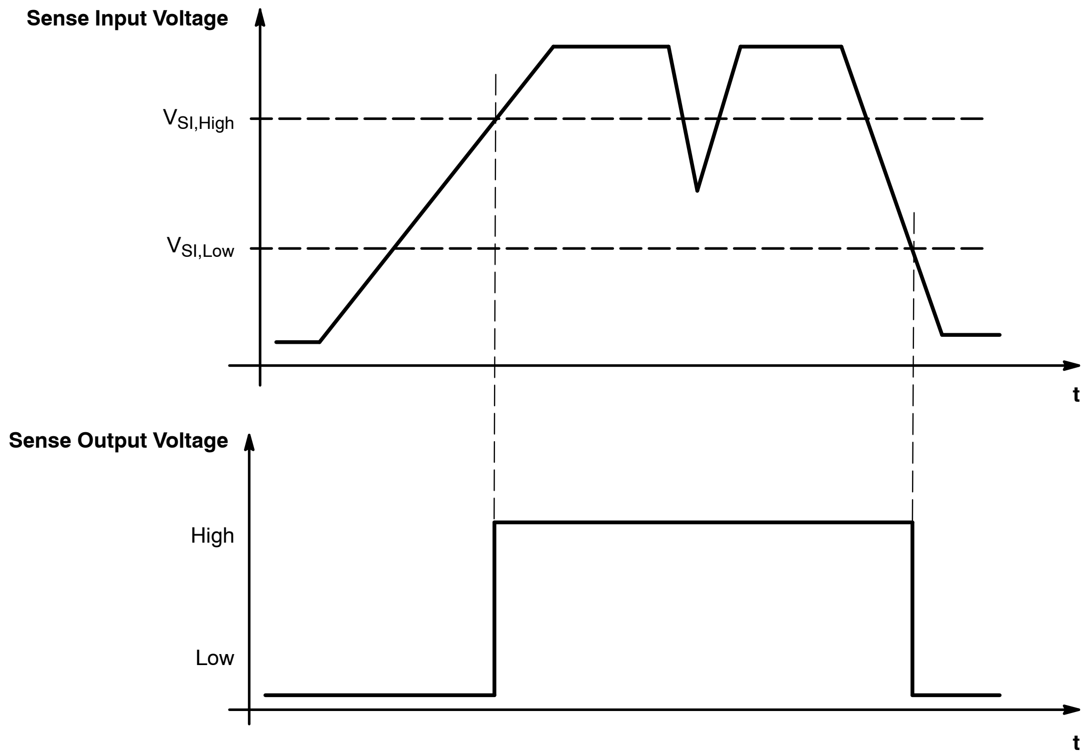


Figure 4. Sense Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS – 5.0 V OPTION

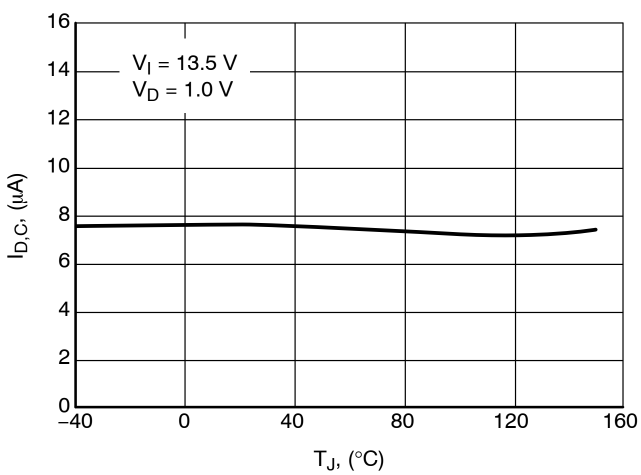


Figure 5. Charge Current $I_{D,C}$ vs. Temperature T_J

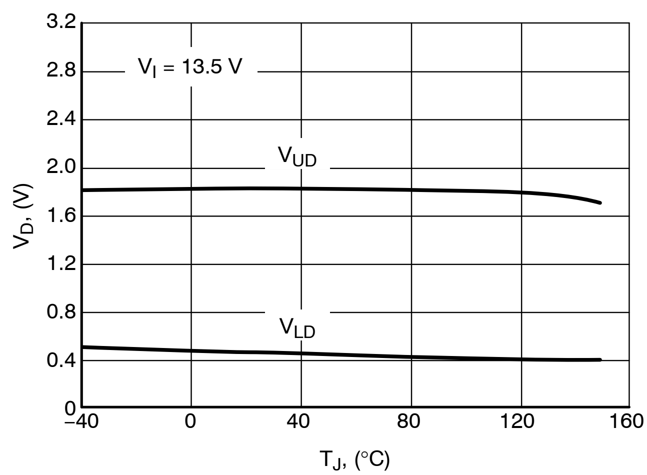


Figure 6. Switching Voltage V_{UD} and V_{LD} vs. Temperature T_J

TYPICAL PERFORMANCE CHARACTERISTICS – 5.0 V OPTION

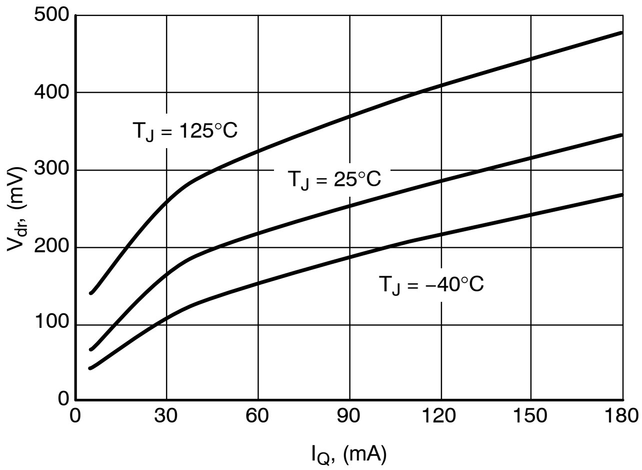


Figure 7. Drop Voltage V_{dr} vs. Output Current I_Q

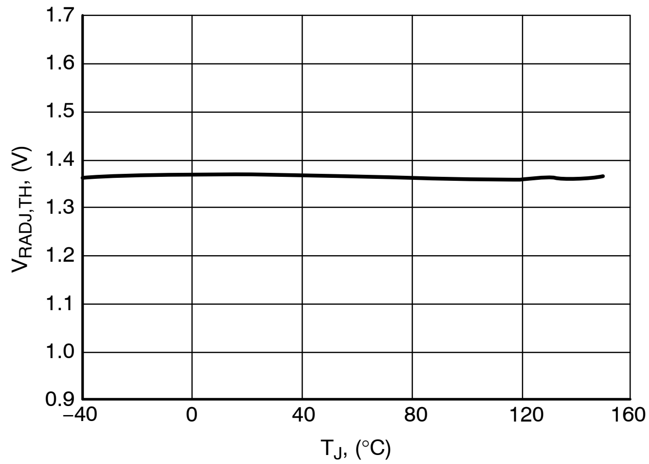


Figure 8. Reset Adjust Switching Threshold, $V_{RADJ,TH}$ vs. Temperature T_J

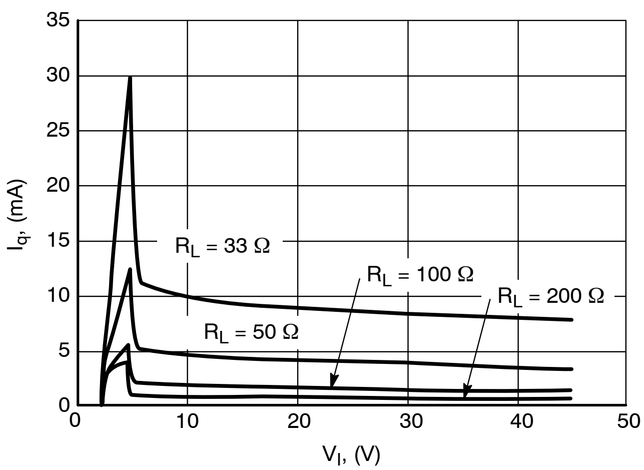


Figure 9. Current Consumption I_q vs. Input Voltage V_I

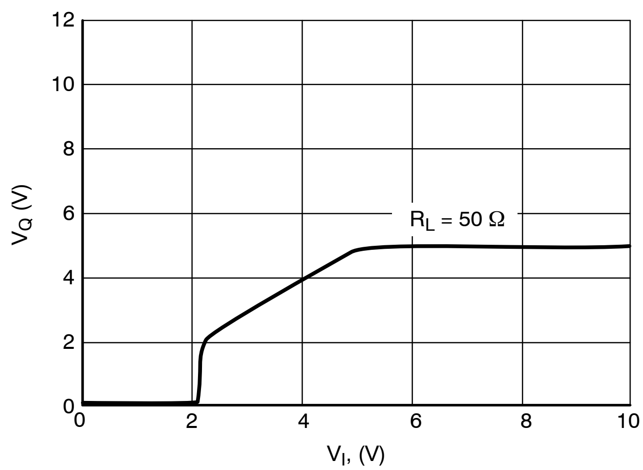


Figure 10. Output Voltage V_Q vs. Input Voltage V_I

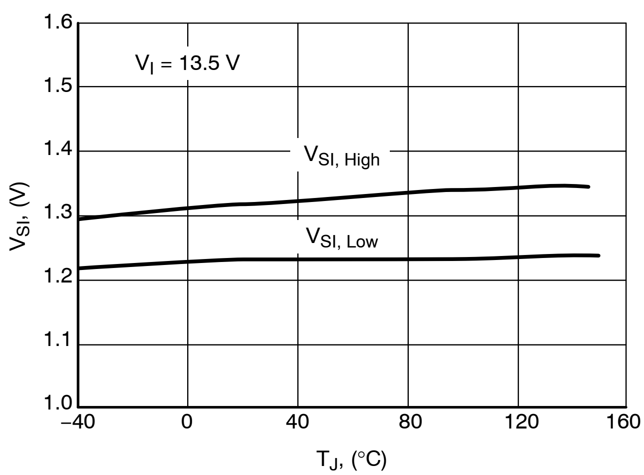


Figure 11. Sense Threshold V_{SI} vs. Temperature T_J

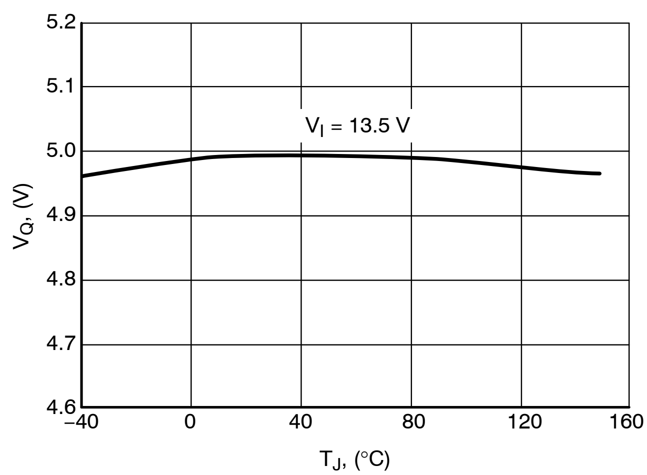


Figure 12. Output Voltage V_Q vs. Temperature T_J

TYPICAL PERFORMANCE CHARACTERISTICS – 5.0 V OPTION

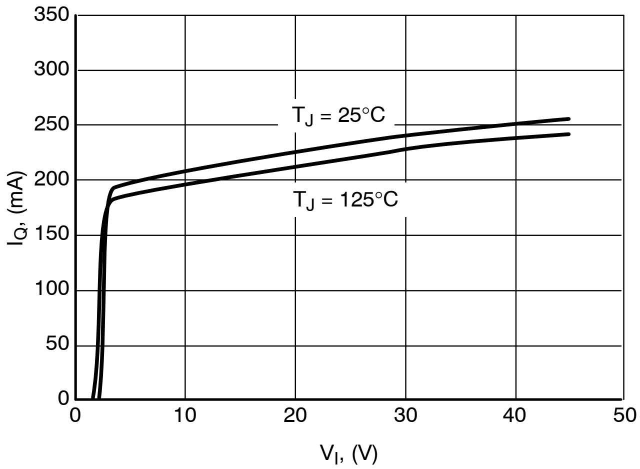


Figure 13. Output Current Limit I_Q vs. Input Voltage V_I

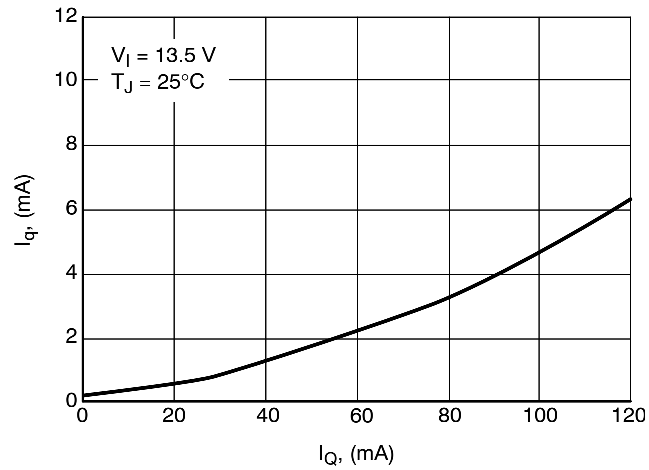


Figure 14. Current Consumption I_q vs. Output Current I_Q

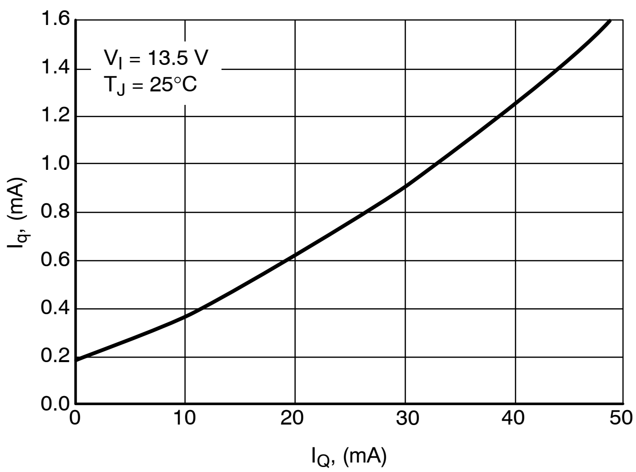


Figure 15. Current Consumption I_q vs. Output Current I_Q

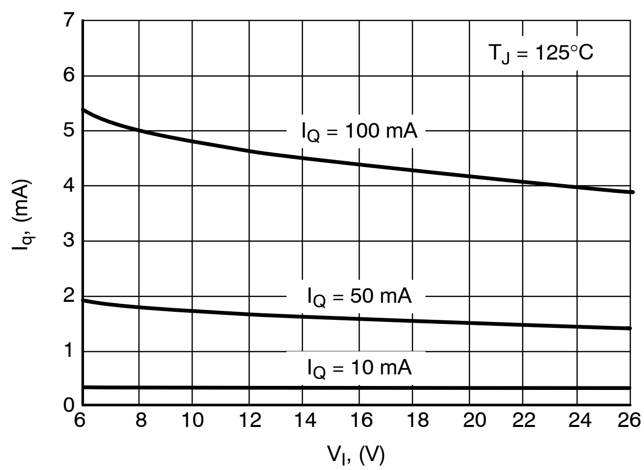


Figure 16. Quiescent Current I_q vs. Input Voltage V_I

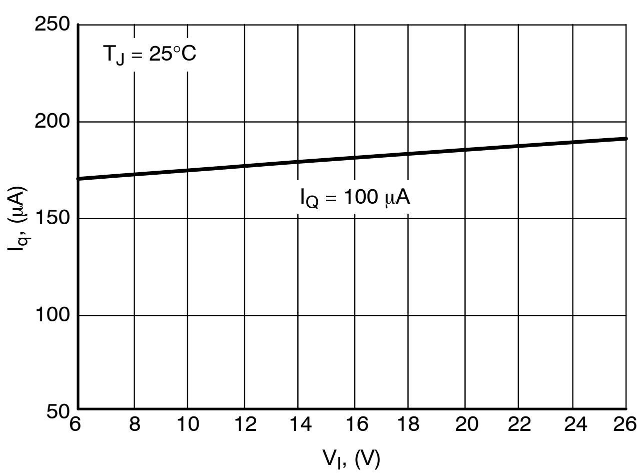


Figure 17. Quiescent Current I_q vs. Input Voltage V_I

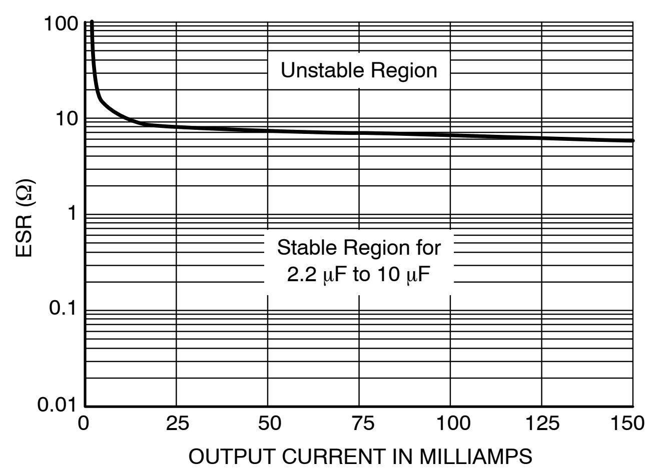


Figure 18. Output Stability, Capacitance ESR vs. Output Load Current

TYPICAL PERFORMANCE CHARACTERISTICS – 3.3 V OPTION

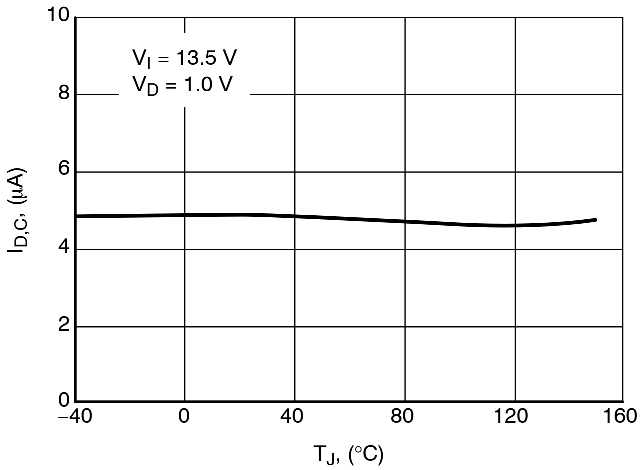


Figure 19. Charge Current $I_{D,C}$ vs. Temperature T_J

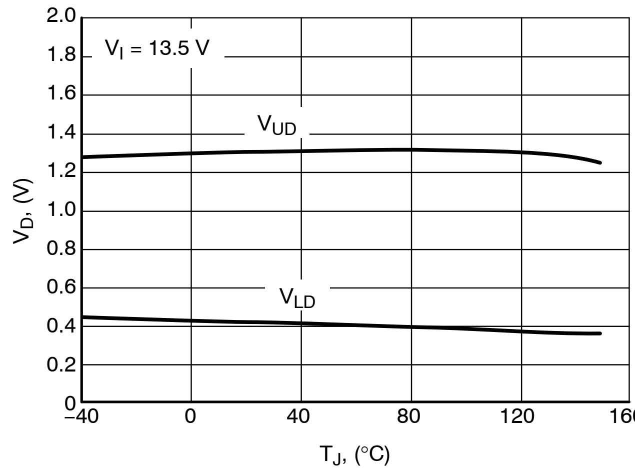


Figure 20. Switching Voltage V_{UD} and V_{LD} vs. Temperature T_J

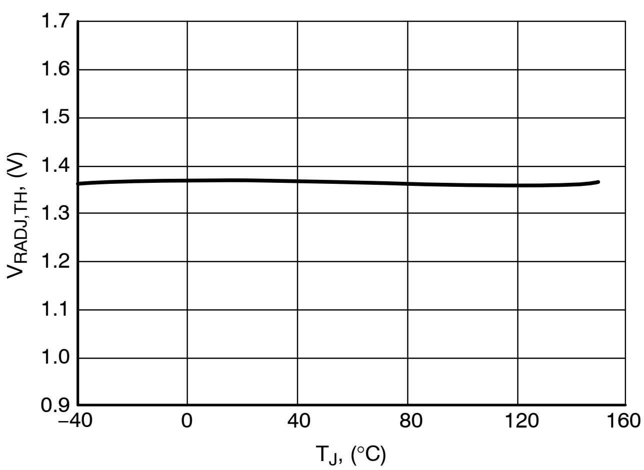


Figure 21. Reset Adjust Switching Threshold, $V_{RADJ,TH}$ vs. Temperature T_J

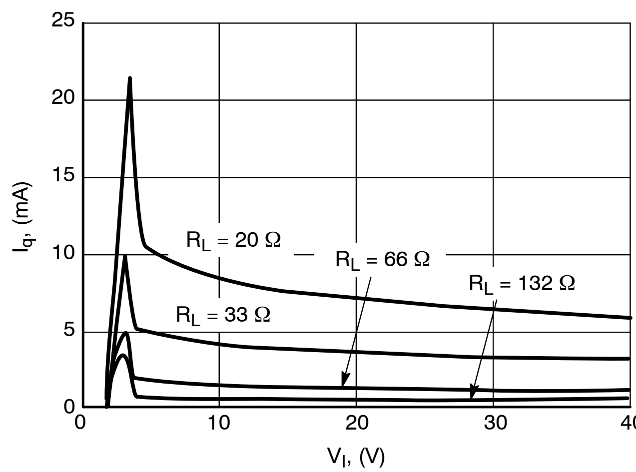


Figure 22. Current Consumption I_q vs. Input Voltage V_I

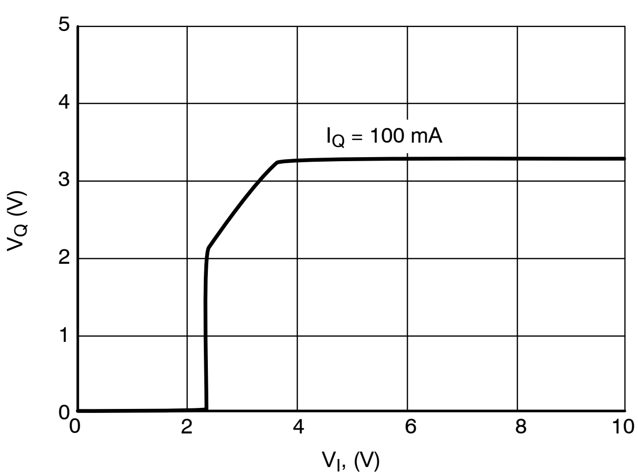


Figure 23. Output Voltage V_Q vs. Input Voltage V_I

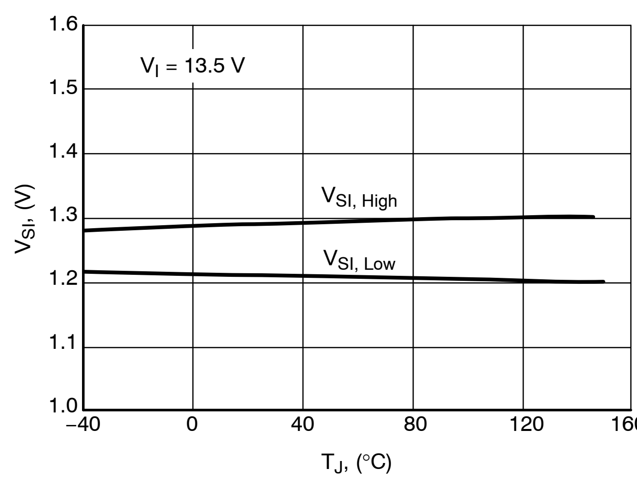


Figure 24. Sense Threshold V_{SI} vs. Temperature T_J

TYPICAL PERFORMANCE CHARACTERISTICS – 3.3 V OPTION

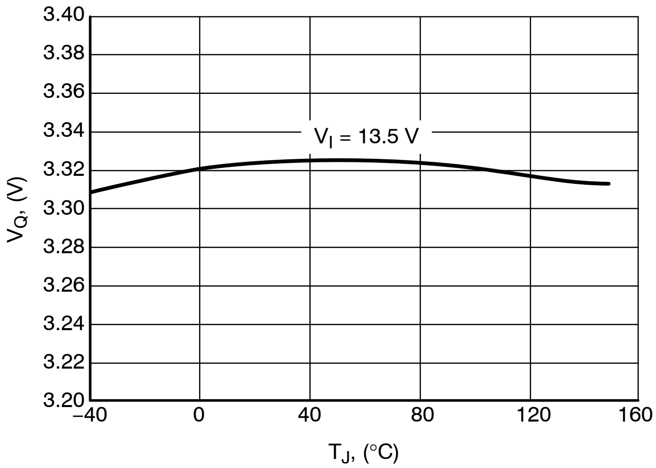


Figure 25. Output Voltage V_Q vs. Temperature T_J

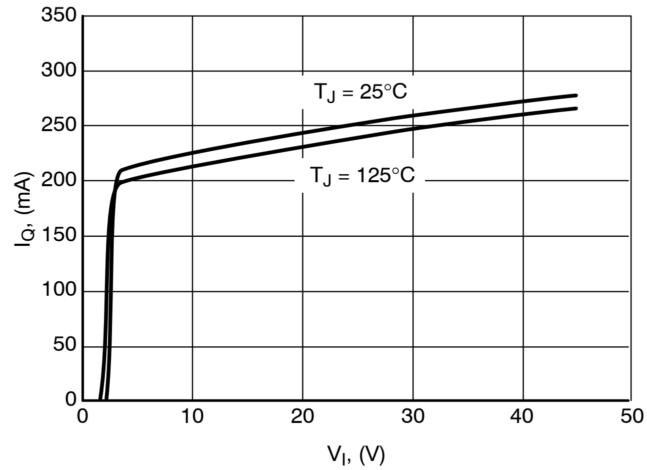


Figure 26. Output Current Limit I_Q vs. Input Voltage V_I

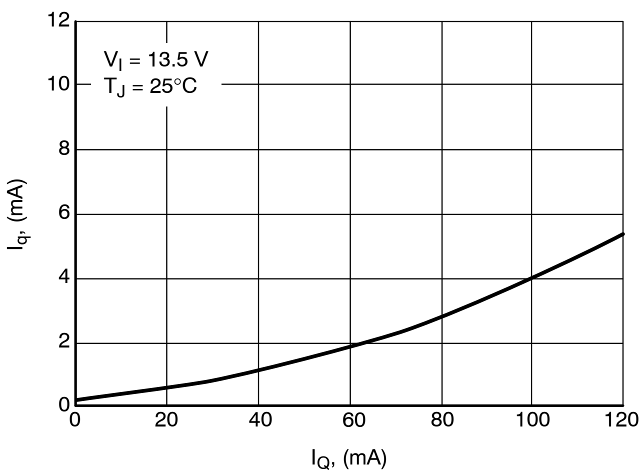


Figure 27. Current Consumption I_q vs. Output Current I_Q

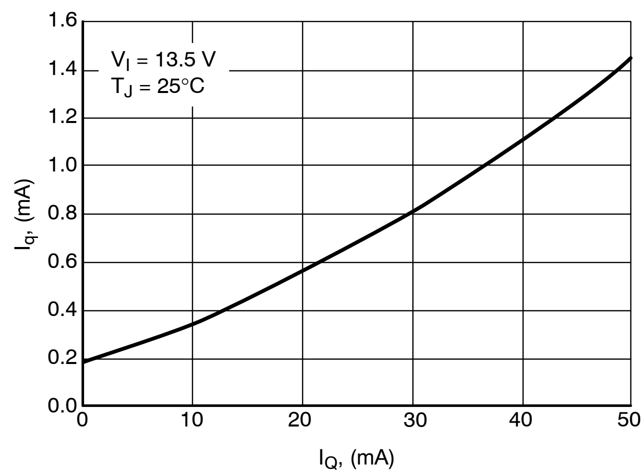


Figure 28. Current Consumption I_q vs. Output Current I_Q

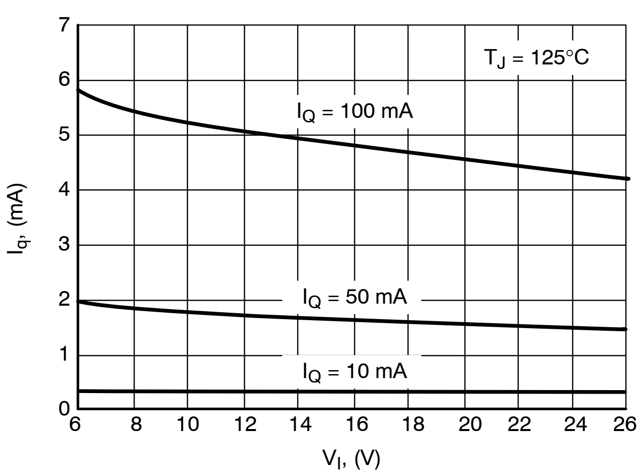


Figure 29. Quiescent Current I_q vs. Input Voltage V_I

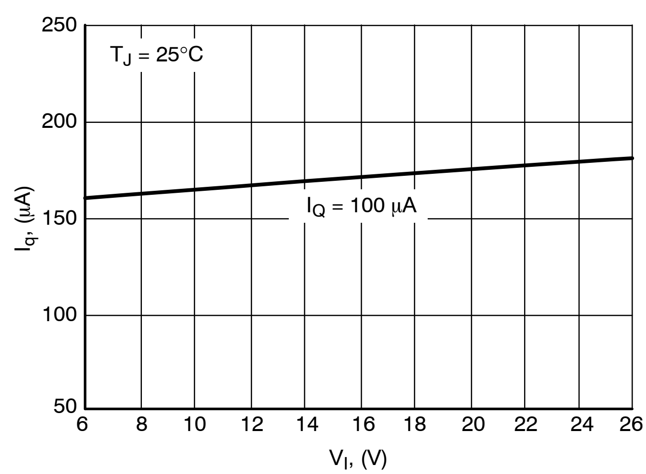


Figure 30. Quiescent Current I_q vs. Input Voltage V_I

TYPICAL PERFORMANCE CHARACTERISTICS – 3.3 V OPTION

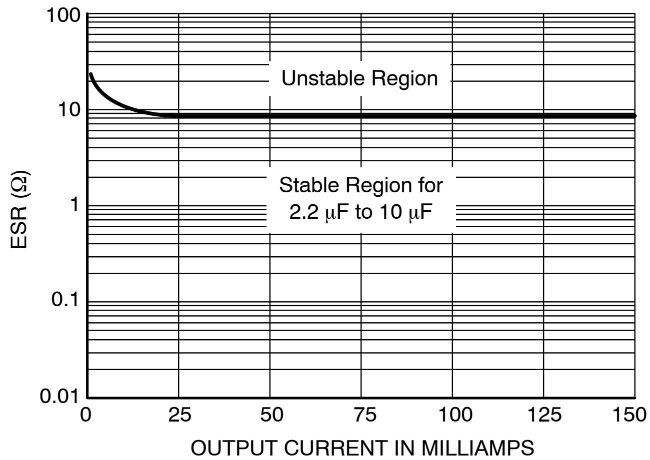


Figure 31. Output Stability, Capacitance ESR vs. Output Load Current

TYPICAL THERMAL CHARACTERISTICS

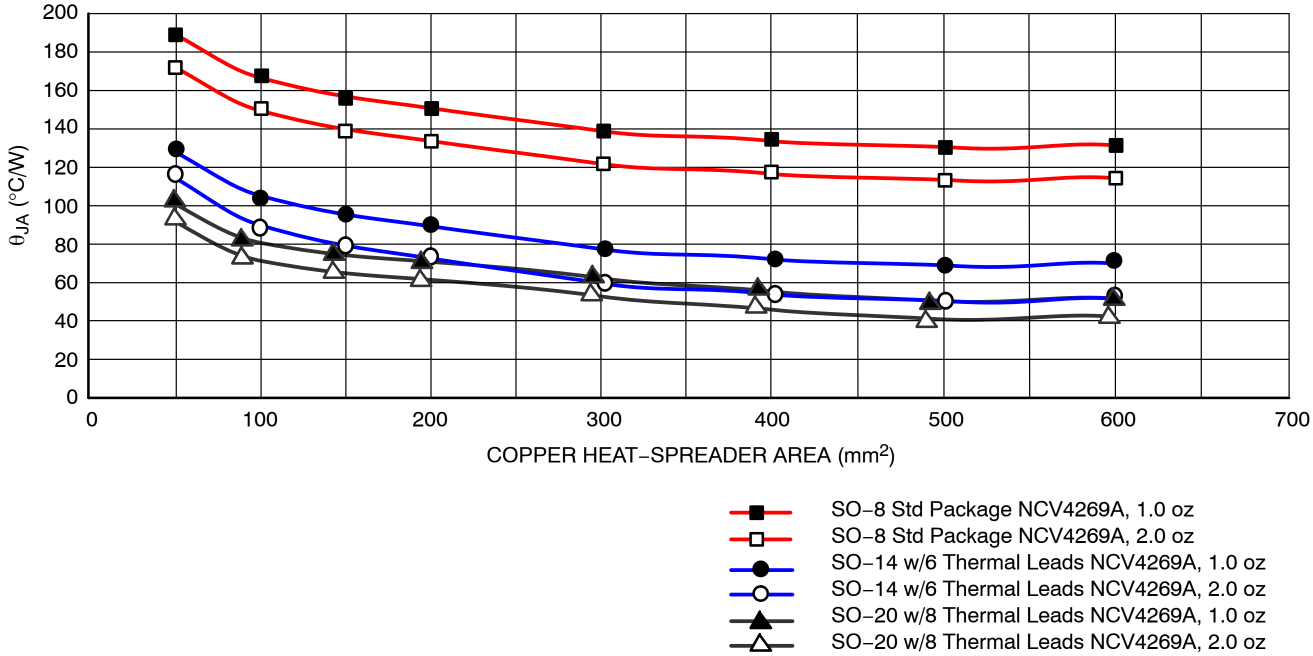


Figure 32. Junction−to−Ambient Thermal Resistance (θ_{JA}) vs. Heat Spreader Area

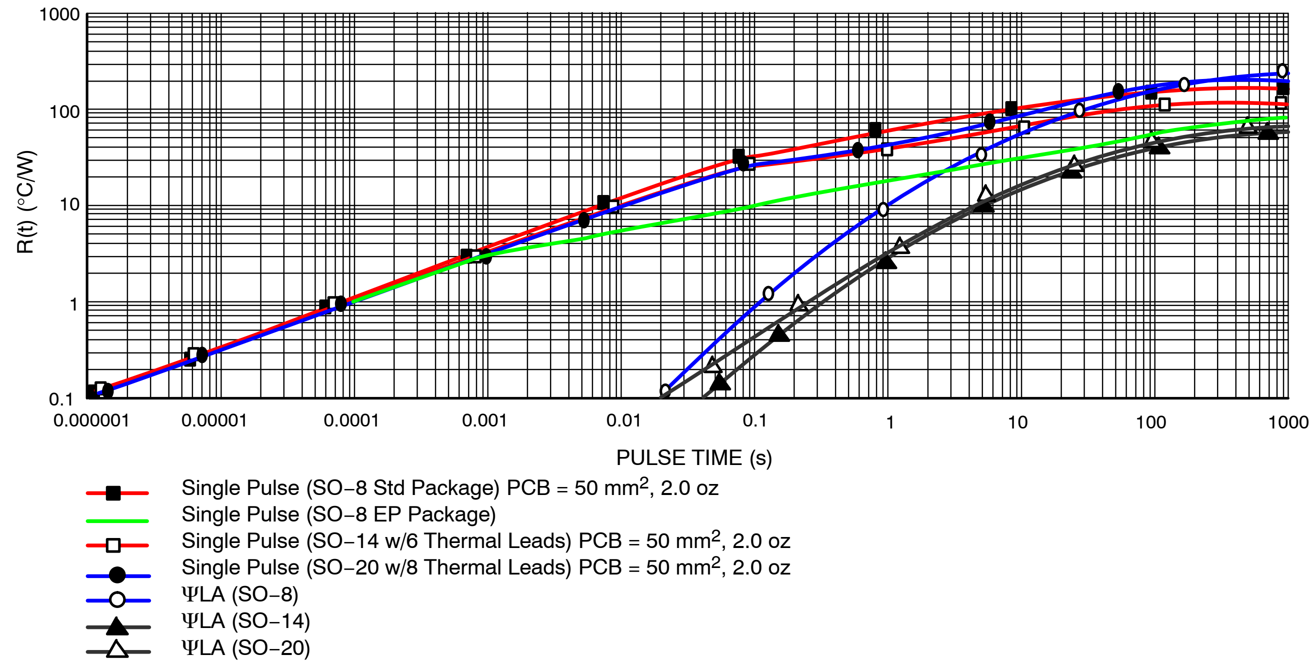


Figure 33. R(t) vs. Pulse Time

APPLICATION DESCRIPTION

OUTPUT REGULATOR

The output is controlled by a precision trimmed reference. The PNP output has base drive quiescent current control for regulation while the input voltage is low, preventing over saturation. Current limit and voltage monitors complement the regulator design to give safe operating signals to the processor and control circuits.

RESET OUTPUT (RO)

A reset signal, Reset Output, RO, (low voltage) is generated as the IC powers up. After the output voltage V_Q increases above the reset threshold voltage V_{RT}, the delay timer D is started. When the voltage on the delay timer V_D passes V_{UD}, the reset signal RO goes high. A discharge of the delay timer V_D is started when V_Q drops and stays below the reset threshold voltage V_{RT}. When the voltage of the delay timer V_D drops below the lower threshold voltage V_{LD} the reset output voltage V_{RO} is brought low to reset the processor.

The reset output RO is an open collector NPN transistor with an internal 20 kΩ pullup resistor connected to the output Q, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC, thereby guaranteeing that RO is valid for V_Q as low as 1.0 V.

RESET ADJUST (R_{ADJ})

The reset threshold V_{RT} can be decreased from a typical value of 4.65 V (3.04 V for 3.3 V Version) to as low as 3.5 V (2.3 V for 3.3 V Version) by using an external voltage divider connected from the Q lead to the pin R_{ADJ}, as shown in Figure 34. The resistor divider keeps the voltage above the $V_{RADJ,TH}$ (typical 1.35 V) for the desired input voltages, and overrides the internal threshold detector. Adjust the voltage divider according to the following relationship:

$$V_{RT} = V_{RADJ,TH} \cdot (R_{ADJ1} + R_{ADJ2}) / R_{ADJ2} \qquad \text{(eq. 1)}$$

If the reset adjust option is not needed, the R_{ADJ} pin should be connected to GND causing the reset threshold to go to its default value.

RESET DELAY (D)

The reset delay circuit provides a delay (programmable by capacitor C_D) on the reset output lead RO. The delay lead D provides charge current $I_{D,C}$ (typically 6.5 μA for 5 V Version or 4.3 μA for 3.3 V Version) to the external delay capacitor C_D during the following times:

1. During Powerup (once the regulation threshold has been exceeded).
2. After a reset event has occurred and the device is back in regulation. The delay capacitor is set to discharge when the regulation (V_{RT}, reset threshold voltage) has been violated. When the delay capacitor discharges to V_{LD}, the reset signal RO pulls low.

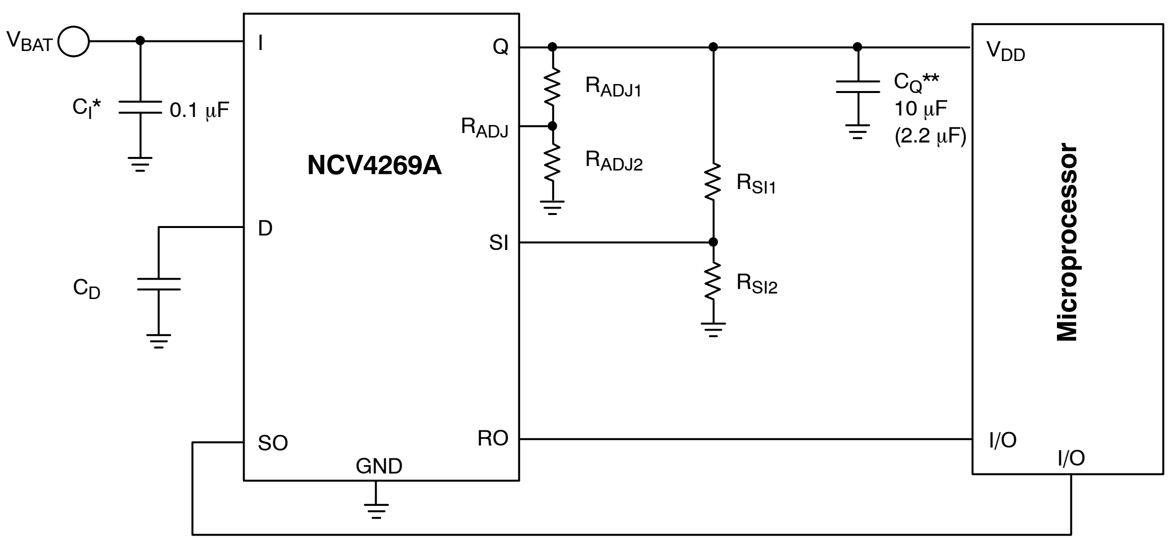
SETTING THE DELAY TIME

The delay time is set by the delay capacitor C_D and the charge current I_D. The time is measured by the delay capacitor voltage charging from the low level of V_{DSAT} to the higher level V_{UD}. The time delay follows the equation:

$$t_d = [C_D (V_{UD} - V_{D,SAT})] / I_{D,C} \qquad \text{(eq. 2)}$$

Example (5 V Version):
Using C_D = 100 nF.
Use the typical value for $V_{D,SAT}$ = 0.1 V.
Use the typical value for V_{UD} = 1.8 V.
Use the typical value for Delay Charge Current I_D = 6.5 μA.

$$t_d = [100\text{ nF} (1.8 - 0.1\text{ V})] / 6.5\ \mu\text{A} = 26.2\text{ ms} \qquad \text{(eq. 3)}$$



*C_I required if regulator is located far from the power supply filter.
** C_Q – minimum cap required for stability is 2.2 μF while higher over/under−shoots may be expected. Cap must operate at minimum temperature expected.

Figure 34. Application Diagram

SENSE INPUT (SI) / SENSE OUTPUT (SO) VOLTAGE MONITOR

An on−chip comparator is available to provide early warning to the microprocessor of a possible reset signal (Figure 4). The output is from an open collector driver with an internal 20 kΩ pull up resistor to output Q. The reset signal typically turns the microprocessor off instantaneously. This can cause unpredictable results with the microprocessor. The signal received from the SO pin will allow the microprocessor time to complete its present task before shutting down. This function is performed by a comparator referenced to the band gap voltage. The actual trip point can be programmed externally using a resistor divider to the input monitor SI (Figure 34). The values for R_{SI1} and R_{SI2} are selected for a typical threshold of 1.20 V on the SI Pin.

SIGNAL OUTPUT

Figure 35 shows the SO Monitor timing waveforms as a result of the circuit depicted in Figure 34. As the output voltage (V_Q) falls, the monitor threshold ($V_{SI,Low}$), is crossed. This causes the voltage on the SO output to go low sending a warning signal to the microprocessor that a reset signal may occur in a short period of time. $T_{WARNING}$ is the time the microprocessor has to complete the function it is currently working on and get ready for the reset shutdown signal. When the voltage on the SO goes low and the RO stays high the current consumption is typically 560 μA at 1 mA load current.

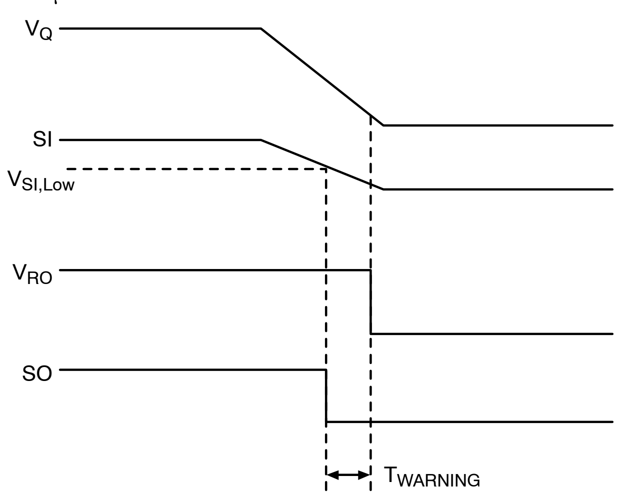


Figure 35. SO Warning Waveform Time Diagram

STABILITY CONSIDERATIONS

The input capacitor C_I in Figure 34 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1.0 Ω in series with C_I.

The output or compensation capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information.

The 10 μF output capacitor C_Q shown in Figure 34 should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed at C_Q is min 2.2 μF and max ESR is 10 Ω. There is no min ESR limit which was proved with MURATA's ceramic caps GRM31MR71A225KA01 (2.2 μF, 10 V, X7R, 1206) and GRM31CR71A106KA01 (10 μF, 10 V, X7R, 1206) directly soldered between output and ground pins.

CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 34) is:

$$P_{D(max)} = [V_{I(max)} - V_{Q(min)}] I_{Q(max)} + V_{I(max)} I_q \quad \text{(eq. 4)}$$

where:

$V_{I(max)}$ is the maximum input voltage,

$V_{Q(min)}$ is the minimum output voltage,

$I_{Q(max)}$ is the maximum output current for the application, and I_q is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = (150°C - T_A) / P_D \quad \text{(eq. 5)}$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram.

HEATSINKS

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad \text{(eq. 6)}$$

where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,

$R_{\theta CS}$ = the case−to−heat sink thermal resistance, and

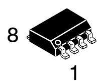
$R_{\theta SA}$ = the heat sink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in data sheets of heatsink manufacturers. Thermal, mounting, and heatsinking considerations are discussed in the ON Semiconductor application note AN1040/D, available on the ON Semiconductor website.

ORDERING INFORMATION

Device	Output Voltage	Package	Shipping†
NCV4269AD150G	5.0 V	SO−8 (Pb−Free)	98 Units/Rail
NCV4269AD150R2G		SO−8 (Pb−Free)	2500 Tape & Reel
NCV4269APD50G		SO−8 EP (Pb−Free)	98 Units/Rail
NCV4269APD50R2G		SO−8 EP (Pb−Free)	2500 Tape & Reel
NCV4269AD250G		SO−14 (Pb−Free)	55 Units/Rail
NCV4269AD250R2G		SO−14 (Pb−Free)	2500 Tape & Reel
NCV4269ADW50G		SO−20L (Pb−Free)	38 Units/Rail
NCV4269ADW50R2G		SO−20L (Pb−Free)	1000 Tape & Reel
NCV4269AD133R2G	3.3 V	SO−8 (Pb−Free)	2500 Tape & Reel

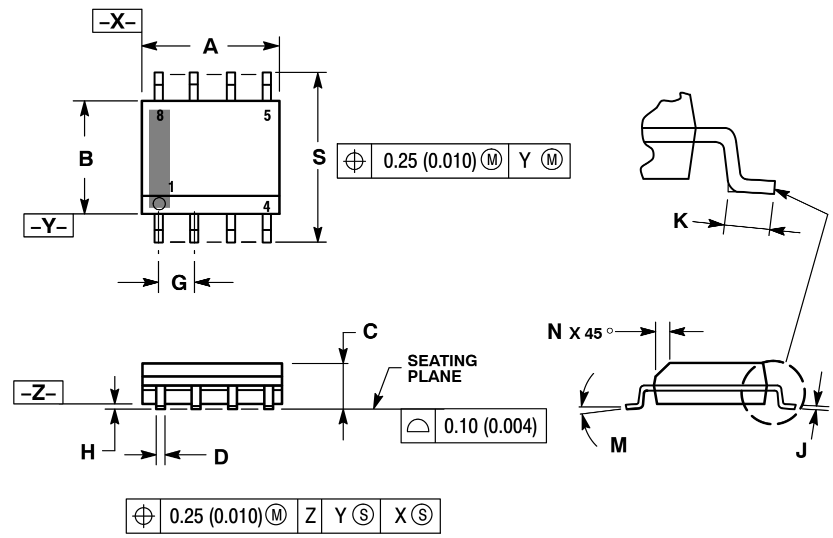
†For information on tape and reel specifications,including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

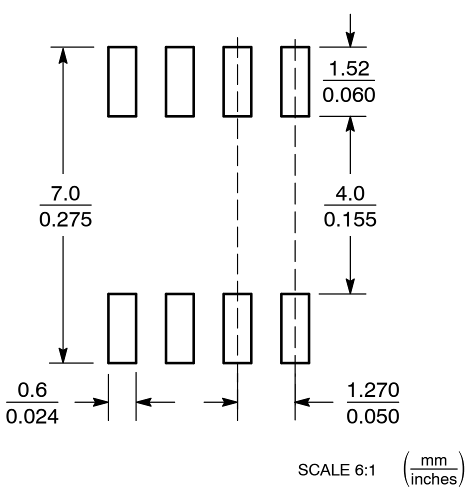
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

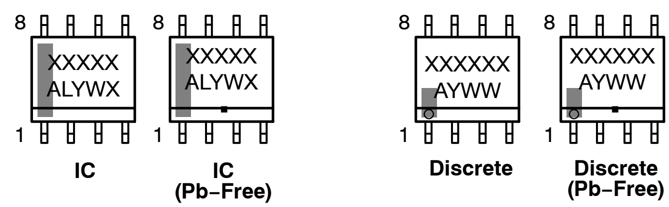
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOIC−8 NB	PAGE 1 OF 2

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

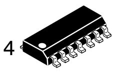
STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

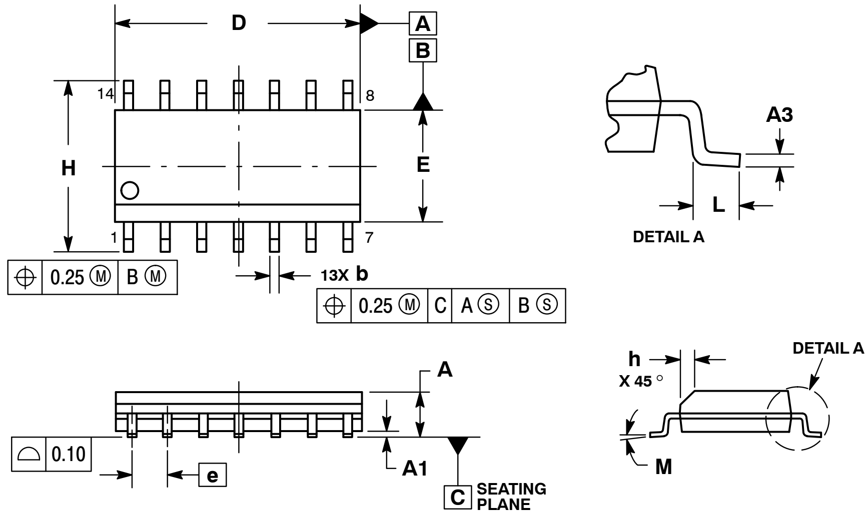
STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1



SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

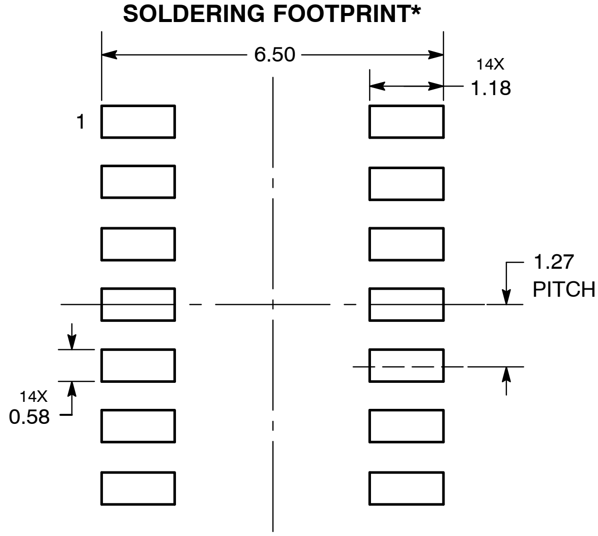
DATE 03 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

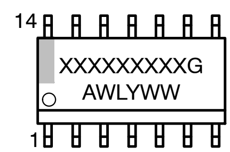
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOIC−14 NB	PAGE 1 OF 2

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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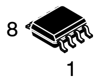
DESCRIPTION:	**SOIC−14 NB**	**PAGE 2 OF 2**



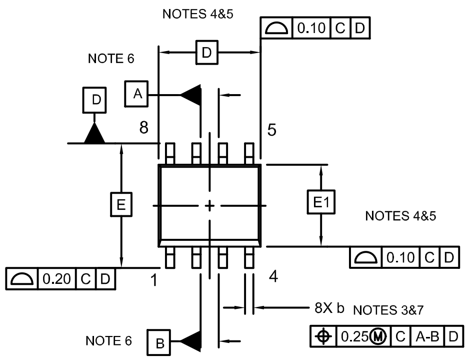
SCALE 1:1

SOIC−8 EP
CASE 751AC
ISSUE D

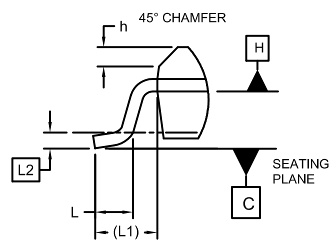
DATE 02 APR 2019

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

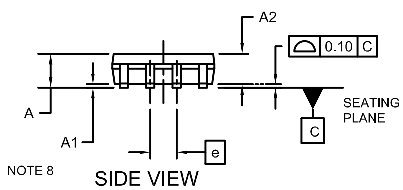


TOP VIEW

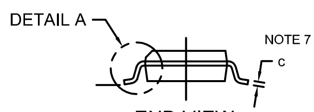


DETAIL A

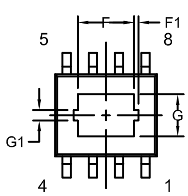
DIM	MILLIMETERS MIN.	NOM..	MAX.
A	1.35	1.55	1.75
A1	---	0.05	0.10
A2	1.35	1.50	1.65
b	0.31	0.41	0.51
c	0.17	0.21	0.23
D		4.90 BSC	
E		6.00 BSC	
E1		3.90 BSC	
e		1.27 BSC	
F	2.24	2.72	3.20
F1	0.15	0.20	0.25
G	1.55	2.03	2.51
G1	0.41	0.46	0.51
h	0.25	0.38	0.50
L	0.40	0.84	1.27
L1		1.04 REF	
L2		0.25 REF	
Ø	0°	4°	8°



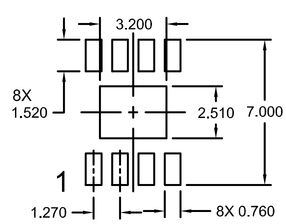
SIDE VIEW



END VIEW



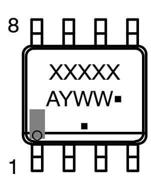
BOTTOM VIEW



RECOMMENDED
MOUNTING FOOTPRINT*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D."

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present and may be in either location. Some products may not follow the Generic Marking.

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DESCRIPTION:	**SOIC−8 EP**	**PAGE 1 OF 1**

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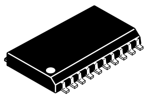
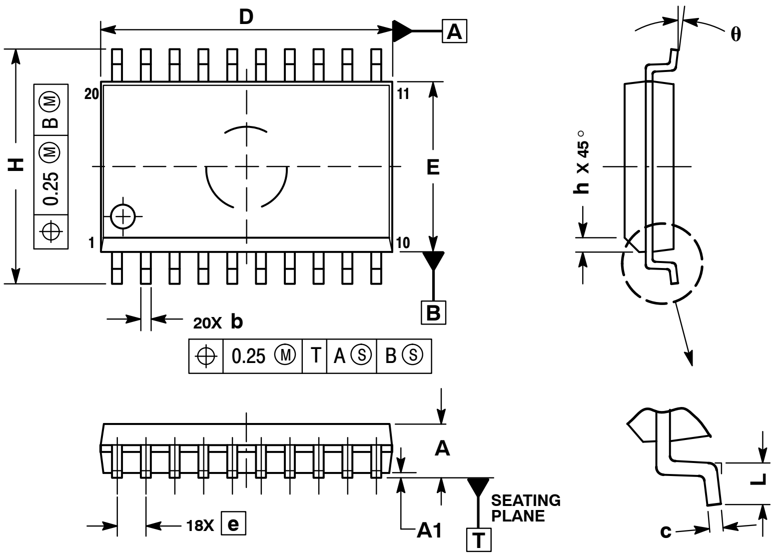


SCALE 1:1

SOIC−20 WB
CASE 751D−05
ISSUE H

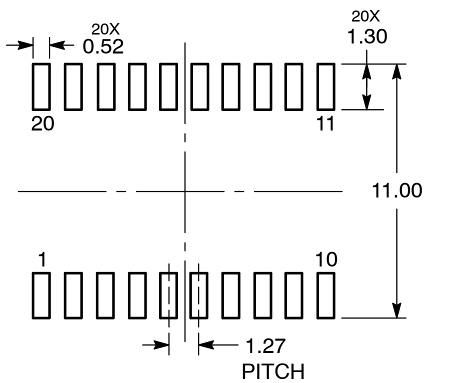
DATE 22 APR 2015



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

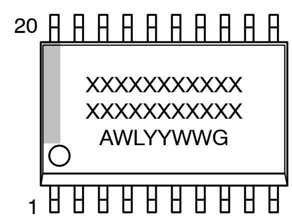
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	SOIC−20 WB	PAGE 1 OF 1

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