## Automotive N-Channel 100 V (D-S) $175{ }^{\circ} \mathrm{C}$ MOSFET



| PRODUCT SUMMARY |  |
| :--- | :---: |
| $\mathrm{V}_{\mathrm{DS}}(\mathrm{V})$ | 100 |
| $\mathrm{R}_{\mathrm{DS}(\text { (on })}(\Omega)$ at $\mathrm{V}_{\mathrm{GS}}=10 \mathrm{~V}$ | 0.095 |
| $\mathrm{I}_{\mathrm{D}}(\mathrm{A})$ per leg | 14.7 |
| Configuration | Single |

## FEATURES

- TrenchFET ${ }^{\circledR}$ power MOSFET
- AEC-Q101 qualified
- $100 \% \mathrm{R}_{\mathrm{g}}$ and UIS tested
- Material categorization:
for definitions of compliance please see www.vishay.com/doc?99912


N-Channel MOSFET

| ORDERING INFORMATION |  |
| :--- | :--- |
| Package | PowerPAK SO-8L |
| Lead (Pb)-free and halogen-free | SQJA70EP <br> (for detailed order number please see www.vishay.com/doc?79771) |



## Notes

a. Package limited
b. Pulse test; pulse width $\leq 300 \mu \mathrm{~s}$, duty cycle $\leq 2 \%$
c. When mounted on 1 " square PCB (FR4 material)
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

SQJA70EP

| SPECIFICATIONS ( $\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$, unless otherwise noted) |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PARAMETER | SYMBOL | TEST CONDITIONS |  | MIN. | TYP. | MAX. | UNIT |
| Static |  |  |  |  |  |  |  |
| Drain-source breakdown voltage | $\mathrm{V}_{\mathrm{DS}}$ | $\mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=250 \mu \mathrm{~A}$ |  | 100 | - | - | V |
| Gate-source threshold voltage | $\mathrm{V}_{\mathrm{GS}(\text { (th) }}$ | $V_{\text {DS }}=V_{G S}, I_{D}=250 \mu \mathrm{~A}$ |  | 2.5 | 3.0 | 3.5 |  |
| Gate-source leakage | $\mathrm{I}_{\text {GSS }}$ | $\mathrm{V}_{\mathrm{DS}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{GS}}= \pm 20 \mathrm{~V}$ |  | - | - | $\pm 100$ | nA |
| Zero gate voltage drain current | Idss | $\mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V}$ | $V_{D S}=100 \mathrm{~V}$ | - | - | 1 | $\mu \mathrm{A}$ |
|  |  | $\mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V}$ | $\mathrm{V}_{\text {DS }}=100 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=125^{\circ} \mathrm{C}$ | - | - | 50 |  |
|  |  | $\mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V}$ | $V_{D S}=100 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=175^{\circ} \mathrm{C}$ | - | - | 150 |  |
| On-state drain current ${ }^{\text {a }}$ | $\mathrm{I}_{\mathrm{D} \text { (on) }}$ | $\mathrm{V}_{\mathrm{GS}}=10 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{DS}} \geq 5 \mathrm{~V}$ | 5 | - | - | A |
| Drain-source on-state resistance ${ }^{\text {a }}$ | $\mathrm{R}_{\mathrm{DS}(\text { (on) }}$ | $\mathrm{V}_{\mathrm{GS}}=10 \mathrm{~V}$ | $\mathrm{I}_{\mathrm{D}}=4 \mathrm{~A}$ | - | 0.078 | 0.095 | $\Omega$ |
|  |  | $\mathrm{V}_{\mathrm{GS}}=10 \mathrm{~V}$ | $\mathrm{I}_{\mathrm{D}}=4 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=125^{\circ} \mathrm{C}$ | - | - | 0.164 |  |
|  |  | $\mathrm{V}_{\mathrm{GS}}=10 \mathrm{~V}$ | $\mathrm{I}_{\mathrm{D}}=4 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=175^{\circ} \mathrm{C}$ | - | - | 0.208 |  |
| Forward transconductance ${ }^{\text {b }}$ | $\mathrm{g}_{\text {fs }}$ | $\mathrm{V}_{\mathrm{DS}}=15 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=4 \mathrm{~A}$ |  | - | 6.5 | - | S |
| Dynamic ${ }^{\text {b }}$ |  |  |  |  |  |  |  |
| Input capacitance | $\mathrm{C}_{\text {iss }}$ | $\mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{DS}}=25 \mathrm{~V}, \mathrm{f}=1 \mathrm{MHz}$ | - | 165 | 220 | pF |
| Output capacitance | $\mathrm{Cosss}^{\text {a }}$ |  |  | - | 120 | 160 |  |
| Reverse transfer capacitance | $\mathrm{C}_{\text {rss }}$ |  |  | - | 12 | 16 |  |
| Total gate charge ${ }^{\text {c }}$ | $\mathrm{Q}_{\mathrm{g}}$ | $\mathrm{V}_{\mathrm{GS}}=10 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{DS}}=50 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=3 \mathrm{~A}$ | - | 4 | 7 | nC |
| Gate-source charge ${ }^{\text {c }}$ | $\mathrm{Q}_{\mathrm{gs}}$ |  |  | - | 1 | - |  |
| Gate-drain charge ${ }^{\text {c }}$ | $\mathrm{Q}_{\mathrm{gd}}$ |  |  | - | 1.25 | - |  |
| Gate resistance | $\mathrm{R}_{\mathrm{g}}$ | $\mathrm{f}=1 \mathrm{MHz}$ |  | 2.4 | 4.9 | 7.5 | $\Omega$ |
| Turn-on delay time ${ }^{\text {c }}$ | $\mathrm{t}_{\mathrm{d}(\mathrm{on})}$ | $\begin{gathered} \mathrm{V}_{\mathrm{DD}}=50 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=33.3 \Omega \\ \mathrm{I}_{\mathrm{D}} \cong 1.5 \mathrm{~A}, \mathrm{~V}_{\mathrm{GEN}}=10 \mathrm{~V}, \mathrm{R}_{\mathrm{g}}=1 \Omega \end{gathered}$ |  | - | 9 | 15 | ns |
| Rise time ${ }^{\text {c }}$ | $\mathrm{t}_{\mathrm{r}}$ |  |  | - | 5 | 10 |  |
| Turn-off delay time ${ }^{\text {c }}$ | $\mathrm{t}_{\mathrm{d} \text { (off) }}$ |  |  | - | 13 | 25 |  |
| Fall time ${ }^{\text {c }}$ | $\mathrm{t}_{\mathrm{f}}$ |  |  | - | 5 | 10 |  |
| Source-Drain Diode Ratings and Characteristics ${ }^{\text {b }}$ |  |  |  |  |  |  |  |
| Pulsed current ${ }^{\text {a }}$ | $I_{\text {SM }}$ |  |  | - | - | 18 | A |
| Forward voltage | $\mathrm{V}_{\text {SD }}$ | $\mathrm{I}_{\mathrm{F}}=4 \mathrm{~A}, \mathrm{~V}_{\mathrm{GS}}=0 \mathrm{~V}$ |  | - | 0.89 | 1.2 | V |
| Body diode reverse recovery time | $\mathrm{t}_{\mathrm{rr}}$ | $\mathrm{I}_{\mathrm{F}}=3 \mathrm{~A}, \mathrm{di} / \mathrm{dt}=100 \mathrm{~A} / \mu \mathrm{s}$ |  | - | 29 | 60 | ns |
| Body diode reverse recovery charge | Qrr |  |  | - | 25 | 50 | nC |
| Reverse recovery fall time | $\mathrm{t}_{\mathrm{a}}$ |  |  | - | 20 | - | ns |
| Reverse recovery rise time | $t_{b}$ |  |  | - | 9 | - | ns |
| Body diode peak reverse recovery current | $\mathrm{I}_{\text {RM(REC }}$ |  |  | - | -1.7 | - | A |

## Notes

a. Pulse test; pulse width $\leq 300 \mu \mathrm{~s}$, duty cycle $\leq 2 \%$
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted)


Output Characteristics


Transconductance


Capacitance


Transfer Characteristics


On-Resistance vs. Drain Current


Gate Charge

TYPICAL CHARACTERISTICS $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted)



Drain Source Breakdown vs. Junction Temperature

THERMAL RATINGS $\left(T_{A}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted)


THERMAL RATINGS $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted)


Normalized Thermal Transient Impedance, Junction-to-Case
Note

- The characteristics shown in the two graphs
- Normalized Transient Thermal Impedance Junction-to-Ambient ( $25^{\circ} \mathrm{C}$ )
- Normalized Transient Thermal Impedance Junction-to-Case ( $25^{\circ} \mathrm{C}$ )
are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size $1^{\prime \prime} \times 1^{\prime \prime} \times 0.062^{\prime \prime}$, double sided with 2 oz. copper, $100 \%$ on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg? 75309.

## PowerPAK ${ }^{\circledR}$ SO-8L Case Outline 2



Topside view (single)


Topside view (dual)


| DIM. | MILLIMETERS |  |  | INCHES |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 1.00 | 1.07 | 1.14 | 0.039 | 0.042 | 0.045 |
| A1 | 0.00 | - | 0.127 | 0.00 | - | 0.005 |
| b | 0.33 | 0.41 | 0.48 | 0.013 | 0.016 | 0.019 |
| b1 | 0.44 | 0.51 | 0.58 | 0.017 | 0.020 | 0.023 |
| b2 | 4.80 | 4.90 | 5.00 | 0.189 | 0.193 | 0.197 |
| b3 | 0.094 |  |  | 0.004 |  |  |
| b4 | 0.47 |  |  | 0.019 |  |  |
| c | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| D | 5.00 | 5.13 | 5.25 | 0.197 | 0.202 | 0.207 |
| D1 | 4.80 | 4.90 | 5.00 | 0.189 | 0.193 | 0.197 |
| D2 | 3.86 | 3.96 | 4.06 | 0.152 | 0.156 | 0.160 |
| D3 | 1.63 | 1.73 | 1.83 | 0.064 | 0.068 | 0.072 |
| e | 1.27 BSC |  |  | 0.050 BSC |  |  |
| E | 6.05 | 6.15 | 6.25 | 0.238 | 0.242 | 0.246 |
| E1 | 4.27 | 4.37 | 4.47 | 0.168 | 0.172 | 0.176 |
| E2 | 2.75 | 2.85 | 2.95 | 0.108 | 0.112 | 0.116 |
| F | - | - | 0.15 | - | - | 0.006 |
| L | 0.62 | 0.72 | 0.82 | 0.024 | 0.028 | 0.032 |
| L1 | 0.92 | 1.07 | 1.22 | 0.036 | 0.042 | 0.048 |
| K | 0.51 |  |  | 0.020 |  |  |
| W | 0.23 |  |  | 0.009 |  |  |
| W1 | 0.41 |  |  | 0.016 |  |  |
| W2 | 2.82 |  |  | 0.111 |  |  |
| W3 | 2.96 |  |  | 0.117 |  |  |
| $\theta$ | $0^{\circ}$ | - | $10^{\circ}$ | $0^{\circ}$ | - | $10^{\circ}$ |
| $\begin{aligned} & 21-149 \\ & 6044 \end{aligned}$ | Nov-20 |  |  |  |  |  |

Note

- Millimeters will govern


## RECOMMENDED MINIMUM PAD FOR PowerPAK ${ }^{\circledR}$ SO-8L SINGLE



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