

FEATURES

- Single power supply
- 500 ps propagation delay input to output
- 125 ps overdrive dispersion
- Differential PECL/LVPECL compatible outputs
- Differential latch control
- Internal latch pull-up resistors
- Power supply rejection greater than 70 dB
- 700 ps minimum pulse width
- Equivalent input rise time bandwidth > 750 MHz
- Typical output rise/fall of 500 ps
- Programmable hysteresis

APPLICATIONS

- Automatic test equipment
- High speed instrumentation
- Scope and logic analyzer front ends
- Window comparators
- High speed line receivers
- Threshold detection
- Peak detection
- High speed triggers
- Patient diagnostics
- Disk drive read channel detection
- Hand-held test instruments
- Zero crossing detectors
- Line receivers and signal restoration
- Clock drivers

FUNCTIONAL BLOCK DIAGRAM

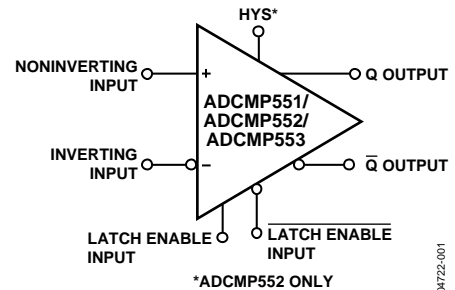


Figure 1.

GENERAL DESCRIPTION

The [ADCMP551/ADCMP552/ADCMP553](#) are single-supply, high speed comparators fabricated on Analog Devices, Inc., proprietary XFCB process. The devices feature a 500 ps propagation delay with less than 125 ps overdrive dispersion. Overdrive dispersion, a measure of the difference in propagation delay under differing overdrive conditions, is a particularly important characteristic of high speed comparators. A separate programmable hysteresis pin is available on the [ADCMP552](#).

A differential input stage permits consistent propagation delay with a common-mode range from -0.2 V to $V_{CCI} - 2.0\text{ V}$. Outputs are complementary digital signals and are fully compatible with PECL and 3.3 V LVPECL logic families. The outputs provide sufficient drive current to directly drive transmission lines terminated in $50\ \Omega$ to $V_{CCO} - 2\text{ V}$. A latch input is included and permits tracking, track-and-hold, or sample-and-hold modes of operation. The latch input pins contain internal pull-ups that set the latch in tracking mode when left open.

The [ADCMP551/ADCMP552/ADCMP553](#) are specified over the -40°C to $+85^{\circ}\text{C}$ industrial temperature range. The [ADCMP551](#) is available in a 16-lead QSOP package; the [ADCMP552](#) is available in a 20-lead QSOP package; and the [ADCMP553](#) is available in an 8-lead MSOP package.

Rev. B

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REVISION HISTORY

3/15—Rev. A to Rev. B

| | |
|---|------------|
| Changed ADCMP55x to ADCMP551/ADCMP552/ADCMP553 | Throughout |
| Changes to Table 3..... | 6 |
| Updated Outline Dimensions | 14 |
| Changes to Ordering Guide | 15 |

6/13—Rev. 0 to Rev. A

| | |
|----------------------------------|----|
| Updated Outline Dimensions | 14 |
| Changes to Ordering Guide | 15 |

10/04—Revision 0: Initial Version

SPECIFICATIONS

$V_{CCI} = 3.3\text{ V}$, $V_{CCO} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1. Electrical Characteristics

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|-------------------------|---|---------------------|-----------|---------------------|------------------------------|
| DC INPUT CHARACTERISTICS | | | | | | |
| Input Voltage Range | | | -0.2 | | $V_{CCI} - 2.0$ | V |
| Input Differential Voltage Range | | | -3 | | +3 | V |
| Input Offset Voltage | V_{OS} | $-IN = 0\text{ V}$, $+IN = 0\text{ V}$ | -10.0 | ± 2.0 | +10.0 | mV |
| Input Offset Voltage Channel Matching | | | | ± 1.0 | | mV |
| Offset Voltage Tempco | $\Delta V_{OS}/dT$ | | | 2.0 | | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current | I_{IN} | $-IN = -0.2\text{ V}$, $+IN = +1.3\text{ V}$ | -28.0 | -6.0 | +5.0 | μA |
| Input Bias Current Tempco | | | | -5.0 | | $\text{nA}/^\circ\text{C}$ |
| Input Offset Current | | | -3.0 | ± 1.0 | +3.0 | μA |
| Input Capacitance | C_{IN} | | | 1.0 | | pF |
| Input Resistance, Differential Mode | | | | 1800 | | k Ω |
| Input Resistance, Common Mode | | | | 1000 | | k Ω |
| Active Gain | A_V | | | 60 | | dB |
| Common-Mode Rejection Ratio | CMRR | $V_{CM} = -0.2\text{ V}$ to $+1.3\text{ V}$ | | 76 | | dB |
| Hysteresis | | $R_{HYS} = \infty$ | | ± 0.5 | | mV |
| LATCH ENABLE CHARACTERISTICS | | | | | | |
| Latch Enable Voltage Range | | | $V_{CCI} - 1.8$ | | $V_{CCI} - 0.8$ | V |
| Latch Enable Differential Voltage Range | | | 0.4 | | 1.0 | V |
| Latch Enable Input High Current | | @ $V_{CCI} - 0.8\text{ V}$ | -150 | | +150 | μA |
| Latch Enable Input Low Current | | @ $V_{CCI} - 1.8\text{ V}$ | -150 | | +150 | μA |
| LE Voltage, Open | | Latch inputs not connected | $V_{CCI} - 0.15$ | | V_{CCI} | V |
| $\overline{\text{LE}}$ Voltage, Open | | Latch inputs not connected | $V_{CCI}/2 - 0.075$ | | $V_{CCI}/2 + 0.075$ | V |
| Latch Setup Time | t_S | $V_{OD} = 250\text{ mV}$ | | 100 | | ps |
| Latch Hold Time | t_H | $V_{OD} = 250\text{ mV}$ | | 100 | | ps |
| Latch to Output Delay | t_{PLOH} , t_{PLOL} | $V_{OD} = 250\text{ mV}$ | | 450 | | ps |
| Latch Minimum Pulse Width | t_{PL} | $V_{OD} = 250\text{ mV}$ | | 700 | | ps |
| DC OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage—High Level | V_{OH} | PECL 50 Ω to $V_{DD} - 2.0\text{ V}$ | $V_{CCO} - 1.15$ | | $V_{CCO} - 0.78$ | V |
| Output Voltage—Low Level | V_{OL} | PECL 50 Ω to $V_{DD} - 2.0\text{ V}$ | $V_{CCO} - 2.00$ | | $V_{CCO} - 1.54$ | V |
| AC OUTPUT CHARACTERISTICS | | | | | | |
| Rise Time | t_R | 10% to 90% | | 510 | | ps |
| Fall Time | t_F | 10% to 90% | | 490 | | ps |
| AC OUTPUT CHARACTERISTICS (ADCMP553) | | | | | | |
| Rise Time | t_R | 10% to 90% | | 440 | | ps |
| Fall Time | t_F | 10% to 90% | | 410 | | ps |
| AC PERFORMANCE | | | | | | |
| Propagation Delay | t_{PD} | $V_{OD} = 1\text{ V}$ | | 500 | | ps |
| | | $V_{OD} = 20\text{ mV}$ | | 625 | | ps |
| Propagation Delay Tempco | $\Delta t_{PD}/dT$ | $V_{OD} = 1\text{ V}$ | | 0.25 | | $\text{ps}/^\circ\text{C}$ |
| Prop Delay Skew—Rising Transition to Falling Transition | | $V_{OD} = 1\text{ V}$ | | 35 | | ps |
| Within Device Propagation Delay Skew—Channel-to-Channel | | $V_{OD} = 1\text{ V}$ | | 35 | | ps |
| Overdrive Dispersion | | $20\text{ mV} \leq V_{OD} \leq 100\text{ mV}$ | | 75 | | ps |
| Overdrive Dispersion | | $50\text{ mV} \leq V_{OD} \leq 1.0\text{ V}$ | | 75 | | ps |
| Slew Rate Dispersion | | $0.4\text{ V/ns} \leq SR \leq 1.33\text{ V/ns}$ | | 75 | | ps |

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|-----------------------------------|--|-------|-----|------|------|
| AC PERFORMANCE (continued) | | | | | | |
| Pulse Width Dispersion | | $700 \text{ ps} \leq \text{PW} \leq 10 \text{ ns}$ | | 25 | | ps |
| Duty Cycle Dispersion | | 33 MHz, 1 V/ns, $V_{\text{CM}} = 0.5 \text{ V}$ | | 10 | | ps |
| Common-Mode Voltage Dispersion | | 1 V swing, $0.3 \text{ V} \leq V_{\text{CM}} \leq 0.8 \text{ V}$ | | 10 | | ps |
| Equivalent Input Rise Time Bandwidth ¹ | BW_{EQ} | 0 V to 1 V swing, 2 V/ns | | 750 | | MHz |
| Maximum Toggle Rate | | >50% output swing | | 800 | | MHz |
| Minimum Pulse Width | PW_{MIN} | $\Delta t_{\text{PD}} < 25 \text{ ps}$ | | 700 | | ps |
| RMS Random Jitter | | $V_{\text{OD}} = 250 \text{ mV}$, 1.3 V/ns, 500 MHz, 50% duty cycle | | 1.1 | | ps |
| Unit-to-Unit Propagation Delay Skew | | | | 50 | | ps |
| POWER SUPPLY (ADCMP551/ADCMP552) | | | | | | |
| Input Supply Current | I_{VCCI} | @ 3.3 V | 8 | 12 | 17 | mA |
| Output Supply Current | I_{VCCO} | @ 3.3 V without load | 3 | 5 | 9 | mA |
| Output Supply Current | | @ 3.3 V with load | 40 | 55 | 70 | mA |
| Input Supply Voltage | V_{CCI} | Dual | 3.135 | 3.3 | 5.25 | V |
| Output Supply Voltage | V_{CCO} | Dual | 3.135 | 3.3 | 5.25 | V |
| Positive Supply Differential | $V_{\text{CCO}} - V_{\text{CCI}}$ | | -0.2 | | +2.3 | V |
| Power Dissipation | P_{D} | Dual, without load | 40 | 55 | 75 | mW |
| Power Dissipation | | Dual, with load | 90 | 110 | 130 | mW |
| DC Power Supply Rejection Ratio— V_{CCI} | $\text{PSRR}_{\text{VCCI}}$ | | | 75 | | dB |
| DC Power Supply Rejection Ratio— V_{CCO} | $\text{PSRR}_{\text{VCCO}}$ | | | 85 | | dB |
| POWER SUPPLY (ADCMP553) | | | | | | |
| Positive Supply Current | I_{VCC} | @ 3.3 V without load | | 9 | 13 | mA |
| Positive Supply Current | | @ 3.3 V with load | | 35 | 42 | mA |
| Positive Supply Voltage | V_{CC} | Dual | 3.135 | 3.3 | 5.25 | V |
| Power Dissipation | P_{D} | Dual, without load | | 30 | 42 | mW |
| Power Dissipation | | Dual, with load | | 60 | 75 | mW |
| DC Power Supply Rejection Ratio— V_{CC} | PSRR_{VCC} | | | 70 | | dB |
| HYSTERESIS (ADCMP552 Only) | | | | | | |
| Programmable Hysteresis | | | 0 | | 40 | mV |

¹ Equivalent input rise time bandwidth assumes a first order input response and is calculated by the following formula: $BW_{\text{EQ}} = .22/\sqrt{(t_{\text{rCOMP}}^2 - t_{\text{rIN}}^2)}$, where t_{rIN} is the 20/80 input transition time applied to the comparator and t_{rCOMP} is the effective transition time as digitized by the comparator input.

ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter | Rating |
|---|------------------|
| Supply Voltages | |
| Input Supply Voltage (V_{CC1} to GND) | –0.5 V to +6.0 V |
| Output Supply Voltage (V_{CC0} to GND) | –0.5 V to +6.0 V |
| Ground Voltage Differential | –0.5 V to +0.5 V |
| Input Voltages | |
| Input Common-Mode Voltage | –0.5 V to +3.5 V |
| Differential Input Voltage | –4.0 V to +4.0 V |
| Input Voltage, Latch Controls | –0.5 V to +5.5 V |
| Output | |
| Output Current | 30 mA |
| Temperature | |
| Operating Temperature, Ambient | –40°C to +85°C |
| Operating Temperature, Junction | 125°C |
| Storage Temperature Range | –65°C to +150°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CONSIDERATIONS

The [ADCMP551](#) 16-lead QSOP package has a θ_{JA} (junction-to-ambient thermal resistance) of 104°C/W in still air.

The [ADCMP552](#) 20-lead QSOP package has a θ_{JA} (junction-to-ambient thermal resistance) of 80°C/W in still air.

The [ADCMP553](#) 8-lead MSOP package has a θ_{JA} (junction-to-ambient thermal resistance) of 130°C/W in still air.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

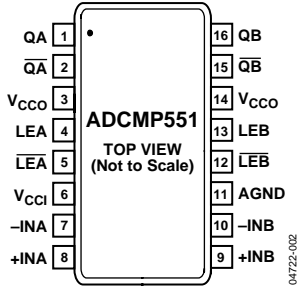


Figure 2. ADCMP551 16-Lead QSOP Pin Configuration

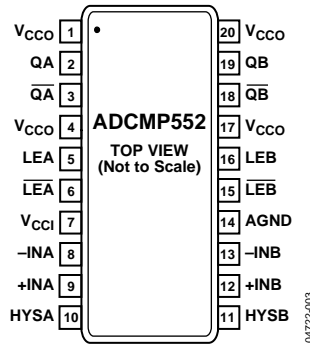


Figure 3. ADCMP552 20-Lead QSOP Pin Configuration

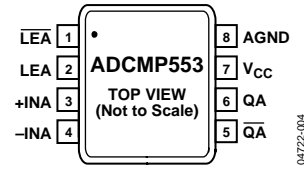


Figure 4. ADCMP553 8-Lead MSOP Pin Configuration

Table 3. Pin Function Descriptions

| Pin No. | | | Mnemonic | Description |
|----------|--------------|----------|------------------|---|
| ADCMP551 | ADCMP552 | ADCMP553 | | |
| 3, 14 | 1, 4, 17, 20 | | V _{cco} | Logic Supply Terminal. |
| 1 | 2 | 6 | QA | One of Two Complementary Outputs for Channel A. QA is logic high if the analog voltage at the noninverting input is greater than the analog voltage at the inverting input (provided the comparator is in the compare mode). See the description of Pin LEA for more information. |
| 2 | 3 | 5 | QA-bar | One of Two Complementary Outputs for Channel A. QA-bar is logic low if the analog voltage at the noninverting input is greater than the analog voltage at the inverting input (provided the comparator is in the compare mode). See the description of Pin LEA for more information. |
| 4 | 5 | 2 | LEA | One of Two Complementary Inputs for Channel A Latch Enable. In compare mode (logic high), the output tracks changes at the input of the comparator. In latch mode (logic low), the output reflects the input state just prior to the comparator being placed into latch mode. LEA must be driven in conjunction with LEA-bar. |
| 5 | 6 | 1 | LEA-bar | One of Two Complementary Inputs for Channel A Latch Enable. In compare mode (logic low), the output tracks changes at the input of the comparator. In latch mode (logic high), the output reflects the input state just prior to the comparator being placed into latch mode. LEA must be driven in conjunction with LEA. |
| 6 | 7 | | V _{cci} | Input Supply Terminal. |
| 7 | 8 | 4 | -INA | Inverting Analog Input of the Differential Input Stage for Channel A. The inverting A input must be driven in conjunction with the noninverting A input. |
| 8 | 9 | 3 | +INA | Noninverting Analog Input of the Differential Input Stage for Channel A. The noninverting A input must be driven in conjunction with the inverting A input. |
| | 10 | | HYSA | Programmable Hysteresis. |
| | 11 | | HYSB | Programmable Hysteresis. |
| 9 | 12 | | +INB | Noninverting Analog Input of the Differential Input Stage for Channel B. The noninverting B input must be driven in conjunction with the inverting B input. |
| 10 | 13 | | -INB | Inverting Analog Input of the Differential Input Stage for Channel B. The inverting B input must be driven in conjunction with the noninverting B input. |
| 11 | 14 | 8 | AGND | Analog Ground. |
| 12 | 15 | | LEB | One of Two Complementary Inputs for Channel B Latch Enable. In compare mode (logic low), the output tracks changes at the input of the comparator. In latch mode (logic high), the output reflects the input state just prior to the comparator being placed into latch mode. LEB must be driven in conjunction with LEB-bar. |

| Pin No. | | | Mnemonic | Description |
|----------|----------|----------|-----------------|---|
| ADCMP551 | ADCMP552 | ADCMP553 | | |
| 13 | 16 | | LEB | One of Two Complementary Inputs for Channel B Latch Enable. In compare mode (logic high), the output tracks changes at the input of the comparator. In latch mode (logic low), the output reflects the input state just prior to the comparator being placed into latch mode. LEB must be driven in conjunction with LEB. |
| 15 | 18 | | \overline{QB} | One of Two Complementary Outputs for Channel B. \overline{QB} is logic low if the analog voltage at the noninverting input is greater than the analog voltage at the inverting input (provided the comparator is in the compare mode). See the description of Pin LEB for more information. |
| 16 | 19 | | QB | One of Two Complementary Outputs for Channel B. QB is logic high if the analog voltage at the noninverting input is greater than the analog voltage at the inverting input (provided the comparator is in the compare mode). See the description of Pin LEB for more information. |
| | | 7 | V _{CC} | Positive Supply Terminal. |

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC1} = 3.3\text{ V}$, $V_{CC0} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

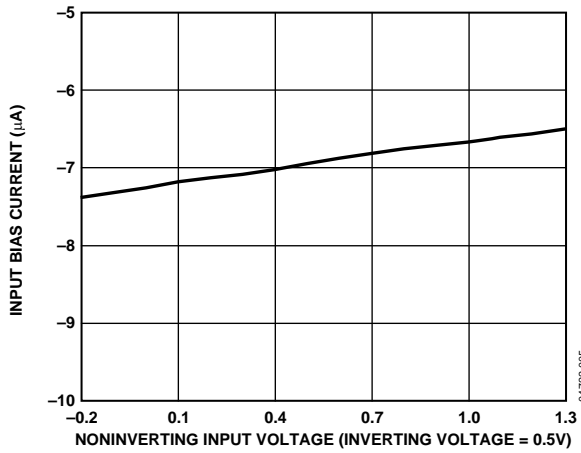


Figure 5. Input Bias Current vs. Input Voltage

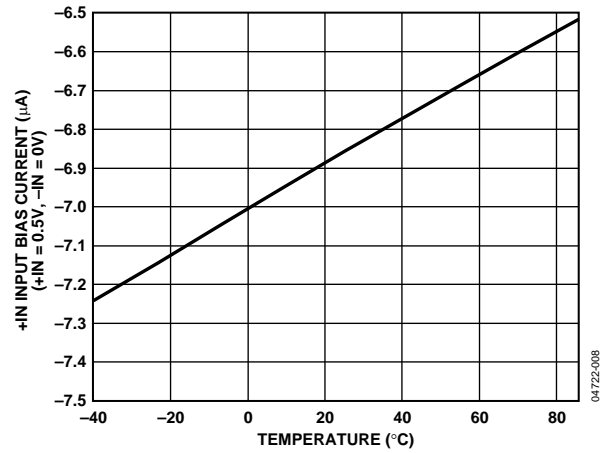


Figure 8. Input Bias Current vs. Temperature

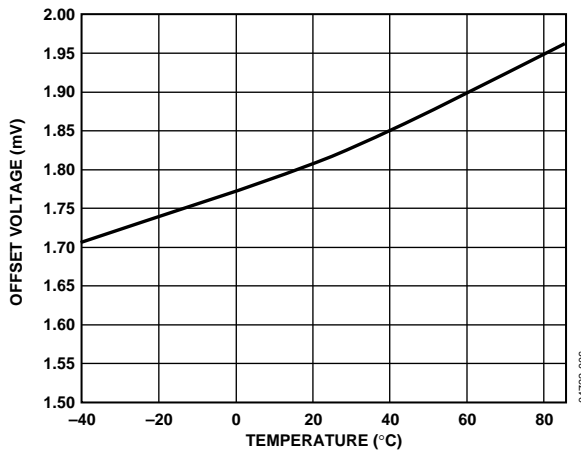


Figure 6. Input Offset Voltage vs. Temperature

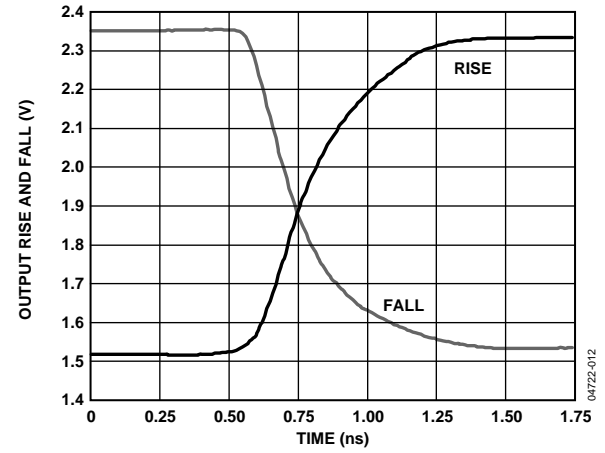


Figure 9. Rise and Fall of Outputs vs. Time

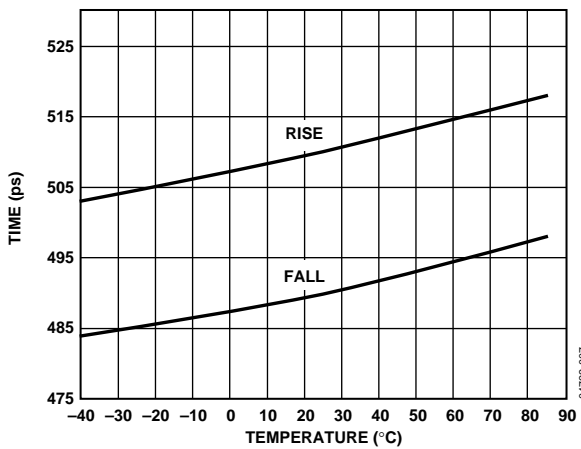


Figure 7. ADCMP551/2 Rise/Fall Time vs. Temperature

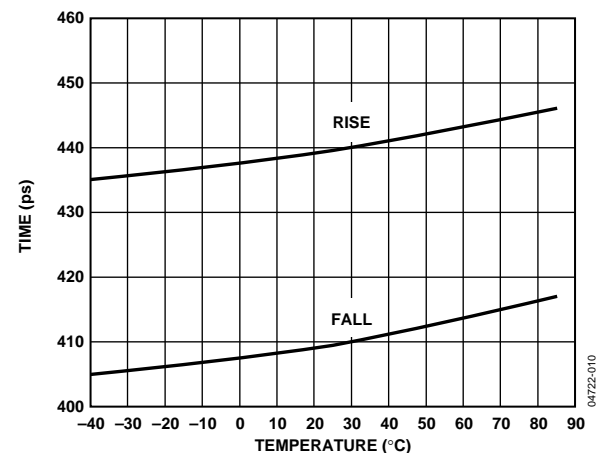


Figure 10. ADCMP553 Rise/Fall Time vs. Temperature

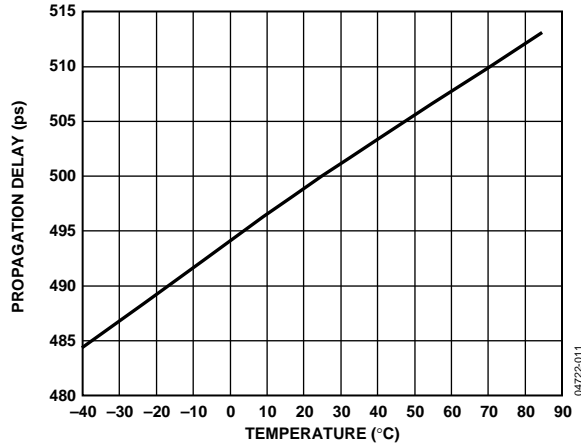


Figure 11. Propagation Delay vs. Temperature

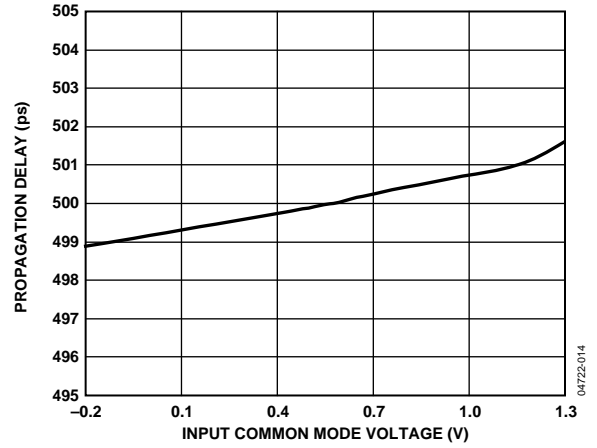


Figure 14. Propagation Delay vs. Common-Mode Voltage

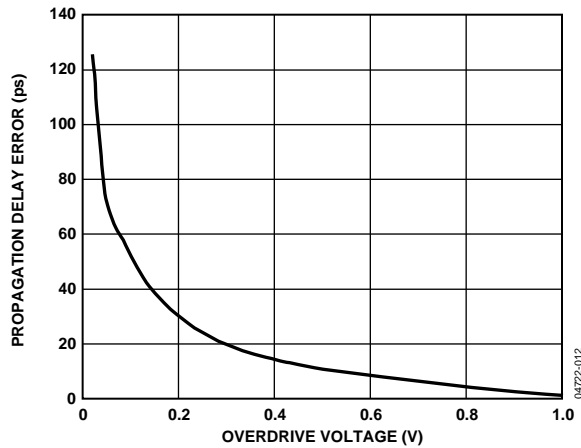


Figure 12. Propagation Delay vs. Overdrive Voltage

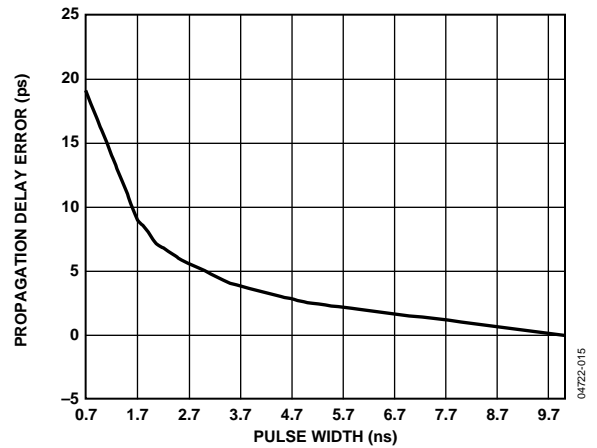


Figure 15. Propagation Delay Error vs. Pulse Width

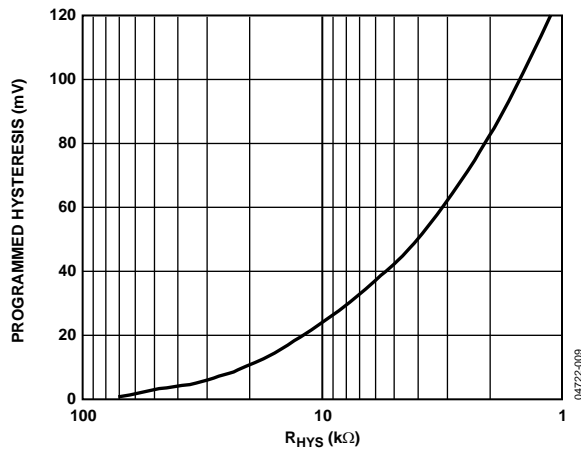


Figure 13. Comparator Hysteresis vs. R_{HYS}

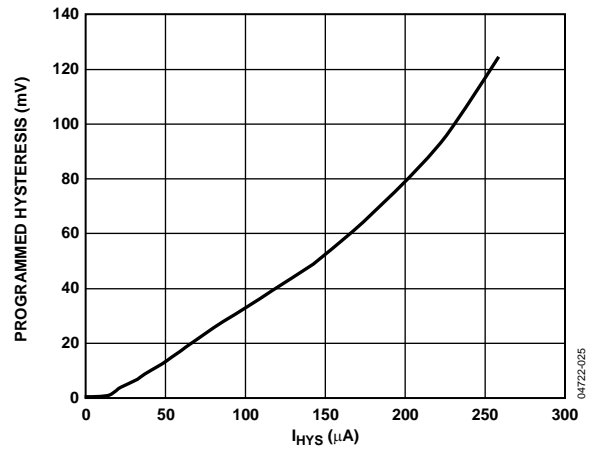


Figure 16. Comparator Hysteresis vs. I_{HYS}

TIMING INFORMATION

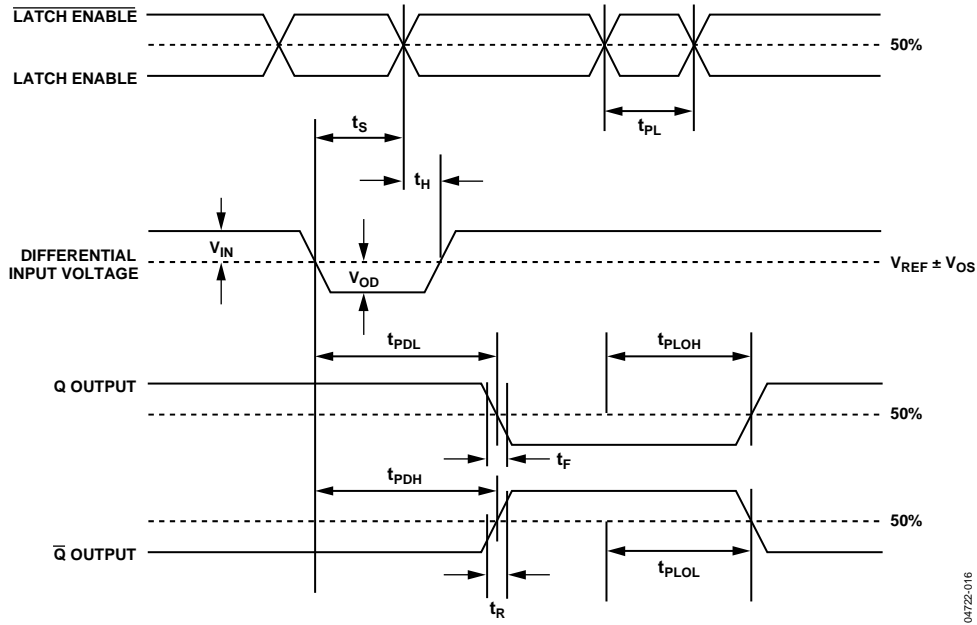


Figure 17. System Timing Diagram

Figure 17 shows the compare and latch features of the ADCMP551/ADCMP552/ADCMP553. Table 4 describes the terms in the diagram.

Table 4. Timing Descriptions

| Symbol | Timing | Description |
|------------|-----------------------------------|--|
| t_{PDH} | Input to Output High Delay | Propagation delay measured from the time the input signal crosses the reference (\pm the input offset voltage) to the 50% point of an output low-to-high transition |
| t_{PDL} | Input to Output Low Delay | Propagation delay measured from the time the input signal crosses the reference (\pm the input offset voltage) to the 50% point of an output high-to-low transition |
| t_{PLOH} | Latch Enable to Output High Delay | Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output low-to-high transition |
| t_{PLOL} | Latch Enable to Output Low Delay | Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output high-to-low transition |
| t_H | Minimum Hold Time | Minimum time after the negative transition of the latch enable signal that the input signal must remain unchanged to be acquired and held at the outputs |
| t_{PL} | Minimum Latch Enable Pulse Width | Minimum time the latch enable signal must be high to acquire an input signal change |
| t_S | Minimum Setup Time | Minimum time before the negative transition of the latch enable signal that an input signal change must be present to be acquired and held at the outputs |
| t_R | Output Rise Time | Amount of time required to transition from a low to a high output as measured at the 20% and 80% points |
| t_F | Output Fall Time | Amount of time required to transition from a high to a low output as measured at the 20% and 80% points |
| V_{OD} | Voltage Overdrive | Difference between the differential input and reference input voltages |

APPLICATIONS INFORMATION

The comparators in the [ADCMP551/ADCMP552/ADCMP553](#) are very high speed devices. Consequently, high speed design techniques must be employed to achieve the best performance. The most critical aspect of any [ADCMP551/ADCMP552/ADCMP553](#) design is the use of a low impedance ground plane. A ground plane, as part of a multilayer board, is recommended for proper high speed performance. Using a continuous conductive plane over the surface of the circuit board can create this, allowing breaks in the plane only for necessary signal paths. The ground plane provides a low inductance ground, eliminating any potential differences at different ground points throughout the circuit board caused by ground bounce. A proper ground plane also minimizes the effects of stray capacitance on the circuit board.

It is also important to provide bypass capacitors for the power supply in a high speed application. A 1 μ F electrolytic bypass capacitor should be placed within 0.5 inches of each power supply pin to ground. These capacitors reduce any potential voltage ripples from the power supply. In addition, a 10 nF ceramic capacitor should be placed as close to the power supply pins as possible on the [ADCMP551/ADCMP552/ADCMP553](#) to ground. These capacitors act as a charge reservoir for the device during high frequency switching.

The LATCH ENABLE input is active low (latched). If the latching function is not used, the LATCH ENABLE input pins may be left open. The internal pull-ups on the latch pins set the latch to transparent mode. If the latch is to be used, valid PECL voltages are required on the inputs for proper operation. The PECL voltages should be referenced to V_{CC1} .

Occasionally, one of the two comparator stages within the [ADCMP551/ADCMP552](#) is not used. The inputs of the unused comparator should not be allowed to float. The high internal gain may cause the output to oscillate (possibly affecting the comparator that is being used) unless the output is forced into a fixed state. This is easily accomplished by ensuring that the two inputs are at least one diode drop apart, while also appropriately connecting the LATCH ENABLE and $\overline{\text{LATCH ENABLE}}$ inputs as described previously.

The best performance is achieved with the use of proper PECL terminations. The open-emitter outputs of the [ADCMP551/ADCMP552/ADCMP553](#) are designed to be terminated through 50 Ω resistors to $V_{CC0} - 2.0$ V or any other equivalent PECL termination. If high speed PECL signals must be routed more than a centimeter, microstrip or stripline techniques may be required to ensure proper transition times and prevent output ringing.

CLOCK TIMING RECOVERY

Comparators are often used in digital systems to recover clock timing signals. High speed square waves transmitted over a distance, even tens of centimeters, can become distorted due to stray capacitance and inductance. Poor layout or improper termination can also cause reflections on the transmission line, further distorting the signal waveform. A high speed comparator can be used to recover the distorted waveform while maintaining a minimum of delay.

OPTIMIZING HIGH SPEED PERFORMANCE

As with any high speed comparator amplifier, proper design and layout techniques should be used to ensure optimal performance from the [ADCMP551/ADCMP552/ADCMP553](#). The performance limits of high speed circuitry can easily be a result of stray capacitance, improper ground impedance, or other layout issues.

Minimizing resistance from source to the input is an important consideration in maximizing the high speed operation of the [ADCMP551/ADCMP552/ADCMP553](#). Source resistance in combination with equivalent input capacitance can cause a lagged response at the input, thus delaying the output. The input capacitance of the [ADCMP551/ADCMP552/ADCMP553](#), in combination with stray capacitance from an input pin to ground, could result in several picofarads of equivalent capacitance. A combination of 3 k Ω source resistance and 5 pF input capacitance yields a time constant of 15 ns, which is significantly slower than the 500 ps capability of the [ADCMP551/ADCMP552/ADCMP553](#). Source impedances should be significantly less than 100 Ω for best performance.

Sockets should be avoided due to stray capacitance and inductance. If proper high speed techniques are used, the [ADCMP551/ADCMP552/ADCMP553](#) should be free from oscillation when the comparator input signal passes through the switching threshold.

COMPARATOR PROPAGATION DELAY DISPERSION

The [ADCMP551/ADCMP552/ADCMP553](#) has been specifically designed to reduce propagation delay dispersion over an input overdrive range of 20 mV to 1 V. Propagation delay overdrive dispersion is the change in propagation delay that results from a change in the degree of overdrive (how far the switching point is exceeded by the input). The overall result is a higher degree of timing accuracy since the [ADCMP551/ADCMP552/ADCMP553](#) is far less sensitive to input variations than most comparator designs.

Propagation delay dispersion is an important specification in critical timing applications such as ATE, bench instruments, and nuclear instrumentation. Overdrive dispersion is defined as the variation in propagation delay as the input overdrive conditions are changed (Figure 18). For the ADCMP551/ADCMP552/ADCMP553, overdrive dispersion is typically 125 ps as the overdrive is changed from 20 mV to 1 V. This specification applies for both positive and negative overdrive since the ADCMP551/ADCMP552/ADCMP553 has equal delays for positive- and negative-going inputs.

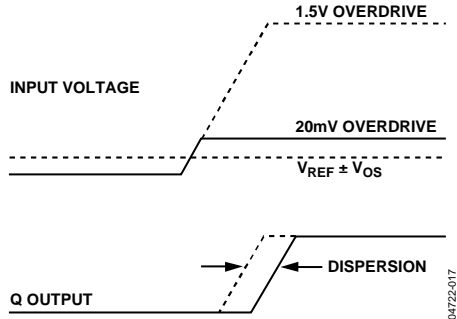


Figure 18. Propagation Delay Dispersion

COMPARATOR HYSTERESIS

The addition of hysteresis to a comparator is often useful in a noisy environment or where it is not desirable for the comparator to toggle between states when the input signal is at the switching threshold. The transfer function for a comparator with hysteresis is shown in Figure 19. If the input voltage approaches the threshold from the negative direction, the comparator switches from a 0 to a 1 when the input crosses $+V_H/2$. The new switching threshold becomes $-V_H/2$. The comparator remains in a 1 state until the $-V_H/2$ threshold is crossed coming from the positive direction. In this manner, noise centered on 0 V input does not cause the comparator to switch states unless it exceeds the region bounded by $\pm V_H/2$.

Positive feedback from the output to the input is often used to produce hysteresis in a comparator (see Figure 23). The major problem with this approach is that the amount of hysteresis varies with the output logic levels, resulting in a hysteresis that is not symmetrical around zero.

In the ADCMP552, hysteresis is generated through the programmable hysteresis pin. A resistor from the HYS pin to V_{CCI} creates a current into the part that is used to generate hysteresis. Hysteresis generated in this manner is independent of output swing and is symmetrical around the trip point. The hysteresis versus resistance curve is shown in Figure 20.

A current source can also be used with the HYS pin. The relationship between the current applied to the HYS pin and the resulting hysteresis is shown in Figure 16.

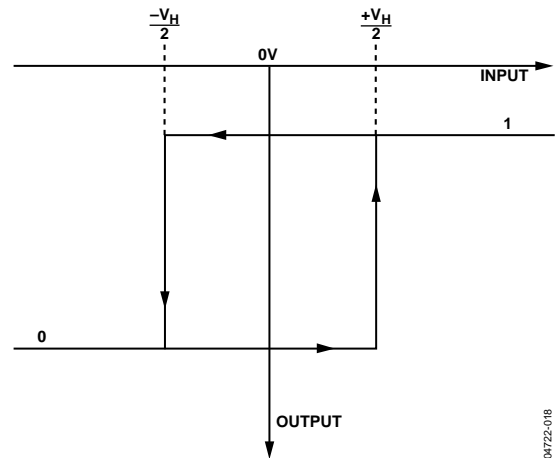


Figure 19. Comparator Hysteresis Transfer Function

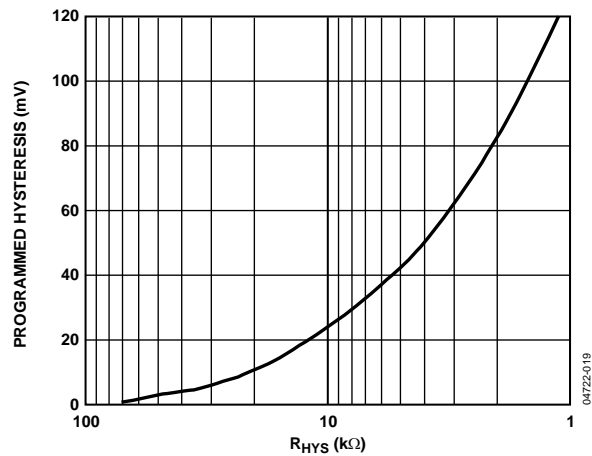


Figure 20. Comparator Hysteresis Transfer Function

MINIMUM INPUT SLEW RATE REQUIREMENT

As for all high speed comparators, a minimum slew rate must be met to ensure that the device does not oscillate when the input crosses the threshold. This oscillation is due in part to the high input bandwidth of the comparator and the parasitics of the package. Analog Devices recommends a slew rate of 1 V/ μ s or faster to ensure a clean output transition. If slew rates less than 1 V/ μ s are used, hysteresis should be added to reduce the oscillation.

TYPICAL APPLICATION CIRCUITS

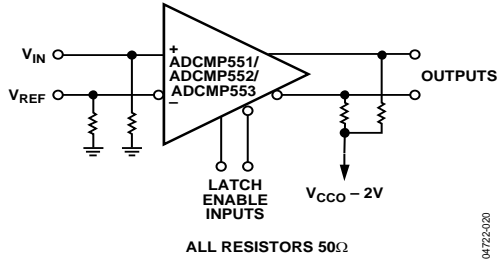


Figure 21. High Speed Sampling Circuits

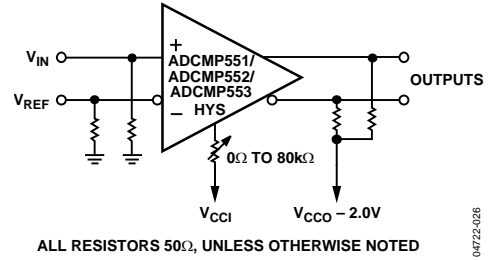


Figure 23. Adding Hysteresis Using the HYS Control Pin

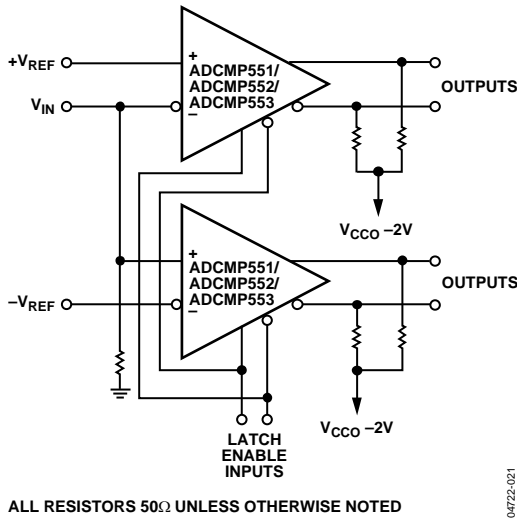


Figure 22. High Speed Window Comparator

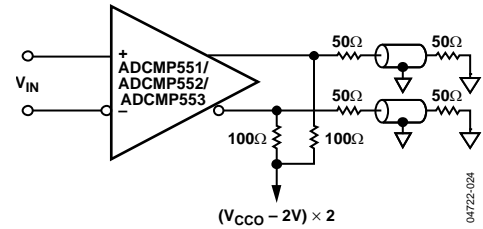
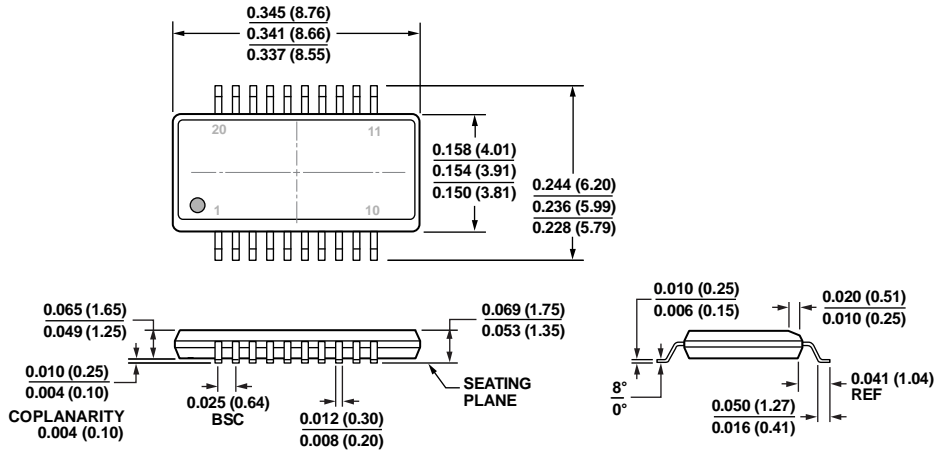


Figure 24. How to Interface a PECL Output to an Instrument with a 50Ω to Ground Input

OUTLINE DIMENSIONS

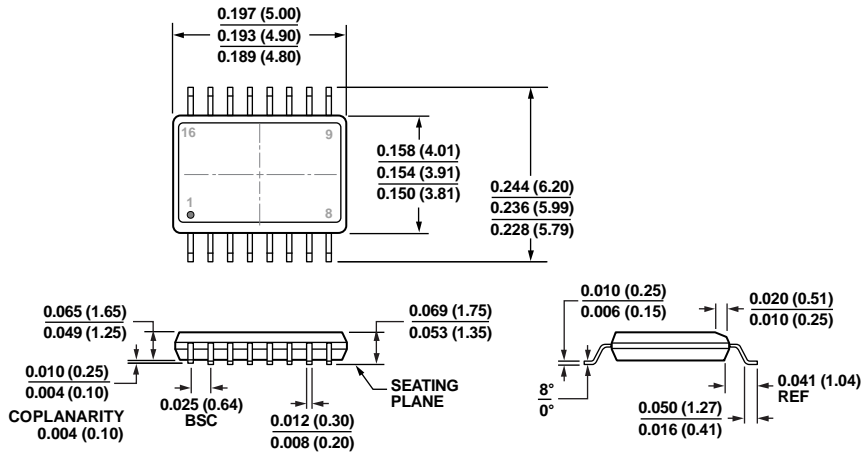


COMPLIANT TO JEDEC STANDARDS MO-137-AD
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 25. 20-Lead Shrink Small Outline Package [QSOP]
 (RQ-20)

Dimensions shown in inches and (millimeters)

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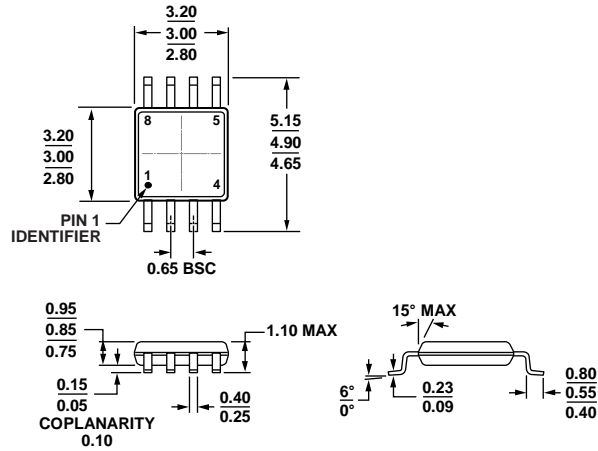


COMPLIANT TO JEDEC STANDARDS MO-137-AB
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 26. 16-Lead Shrink Small Outline Package [QSOP]
 (RQ-16)

Dimensions shown in inches and (millimeters)

09-12-2014-A



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 27. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option | Branding |
|--------------------|-------------------|---|----------------|----------|
| ADCMP551BRQ | -40°C to +85°C | 16-Lead Shrink Small Outline Package [QSOP] | RQ-16 | |
| ADCMP551BRQZ | -40°C to +85°C | 16-Lead Shrink Small Outline Package [QSOP] | RQ-16 | |
| ADCMP551BRQZ-REEL7 | -40°C to +85°C | 16-Lead Shrink Small Outline Package [QSOP] | RQ-16 | |
| EVAL-ADCMP551BRQZ | | Evaluation Board | | |
| ADCMP552BRQ | -40°C to +85°C | 20-Lead Shrink Small Outline Package [QSOP] | RQ-20 | |
| ADCMP552BRQZ | -40°C to +85°C | 20-Lead Shrink Small Outline Package [QSOP] | RQ-20 | |
| EVAL-ADCMP552BRQZ | | Evaluation Board | | |
| ADCMP553BRMZ | -40°C to +85°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | B53 |
| EVAL-ADCMP553BRMZ | | Evaluation Board | | |

¹ Z = RoHS Compliant Part.