MB39C014

1 ch DC/DC Converter IC with PFM/PWM Synchronous Rectification

Description

The MB39C014 is a current mode type 1-channel DC/DC converter IC built-in switching FET, synchronous rectification, and down conversion support. The device is integrated with a switching FET, oscillator, error amplifier, PWM control circuit, reference voltage source, and POWERGOOD circuit.
External inductor and decoupling capacitor are needed only for the external component.
As combining with external parts enables a DC/DC converter with a compact and high load response characteristic, this is suitable as the built-in power supply for such as mobile phone/PDA, DVDs, and HDDs.

Features

- High efficiency : 96% (Max)
- Output current (DC/DC) : 800 mA (Max)
- Input voltage range : 2.5 V to 5.5 V
- Operating frequency : 2.0/3.2 MHz (Typ)
- No flyback diode needed
- Low dropout operation : For 100% on duty
- Built-in high-precision reference voltage generator : 1.20 V ± 2%
- Consumption current in shutdown mode : 1 µA or less
- Built-in switching FET : P-ch MOS 0.3 Ω (Typ) N-ch MOS 0.2 Ω (Typ)
- High speed for input and load transient response in the current mode
- Over temperature protection
- Packaged in a compact package : SON10

Applications

- Flash ROMs
- MP3 players
- Electronic dictionary devices
- Surveillance cameras
- Portable GPS navigators
- Mobile phones etc.

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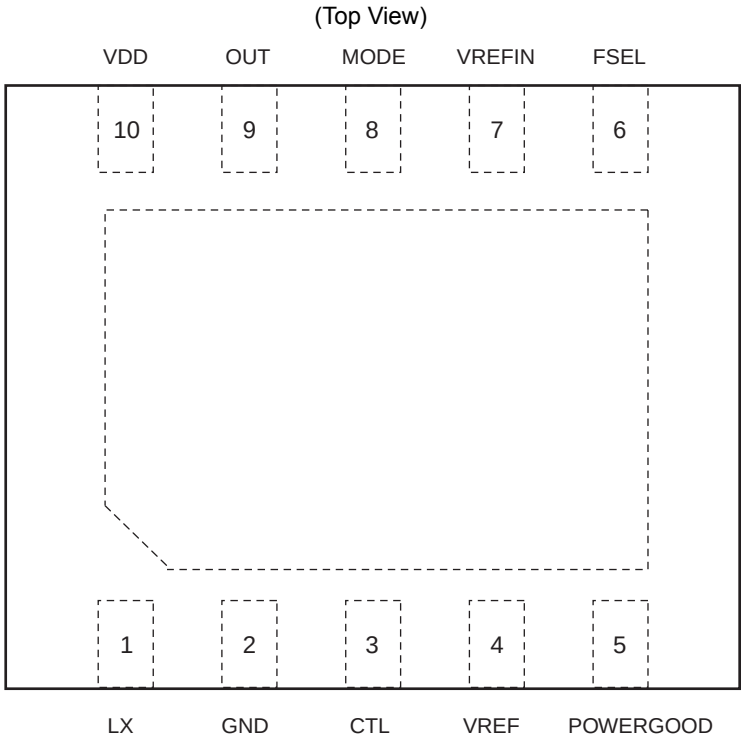
1. Pin Assignment



2. Pin Descriptions

Pin No	Pin Name	I/O	Description
1	LX	O	Inductor connection output pin. High impedance during shut down.
2	GND	—	Ground pin.
3	CTL	I	Control input pin. (L : Shut down / H : Normal operation)
4	VREF	O	Reference voltage output pin.
5	POWERGOOD	O	POWERGOOD circuit output pin. Internally connected to an N-ch MOS open drain circuit.
6	FSEL	I	Frequency switch pin. (L (open) : 2.0 MHz, H : 3.2 MHz)
7	VREFIN	I	Error amplifier (Error Amp) non-inverted input pin.
8	MODE	I	Use pin at L level or leave open.
9	OUT	I	Output voltage feedback pin.
10	VDD	—	Power supply pin.

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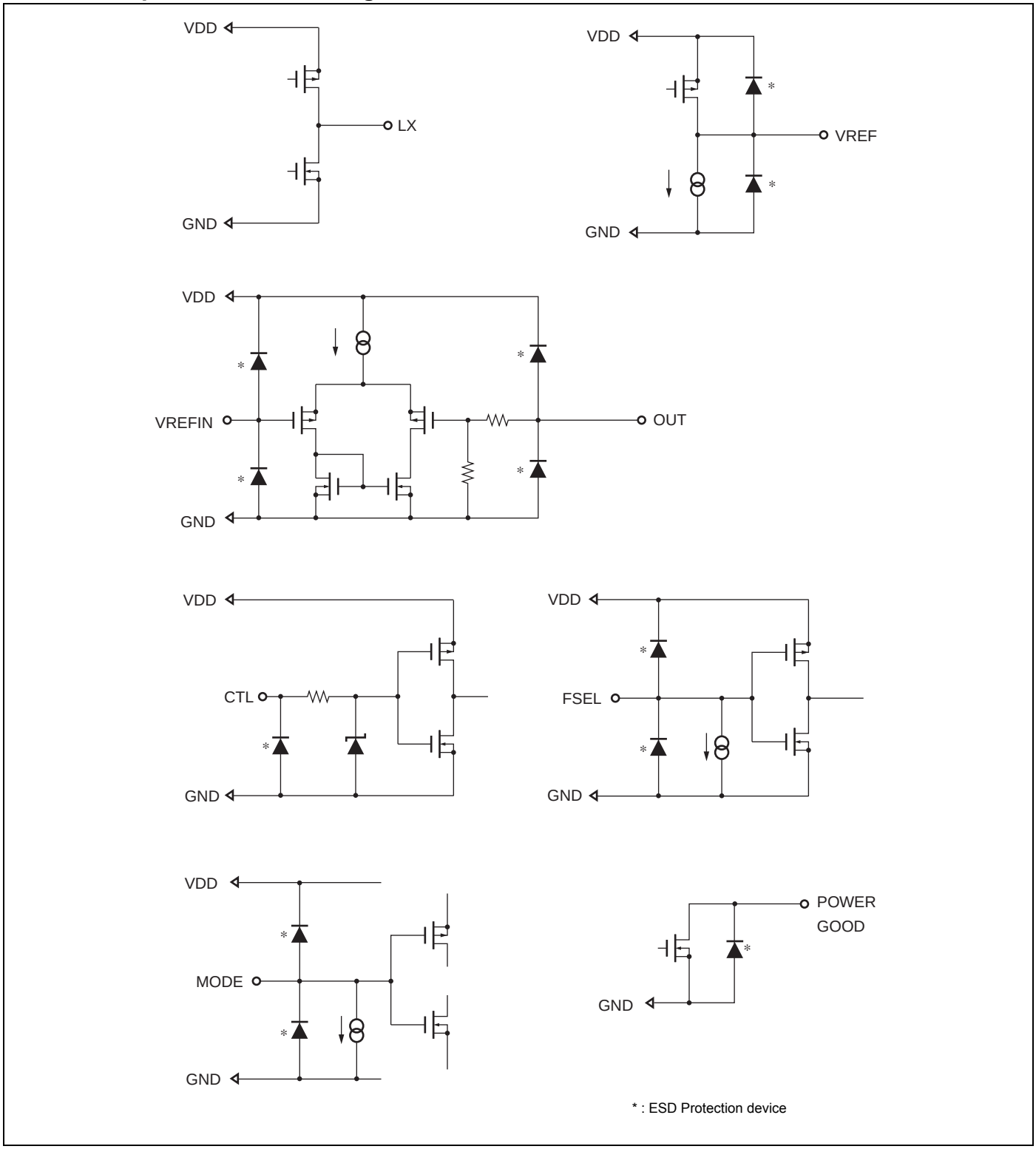
3. I/O Pin Equivalent Circuit Diagram



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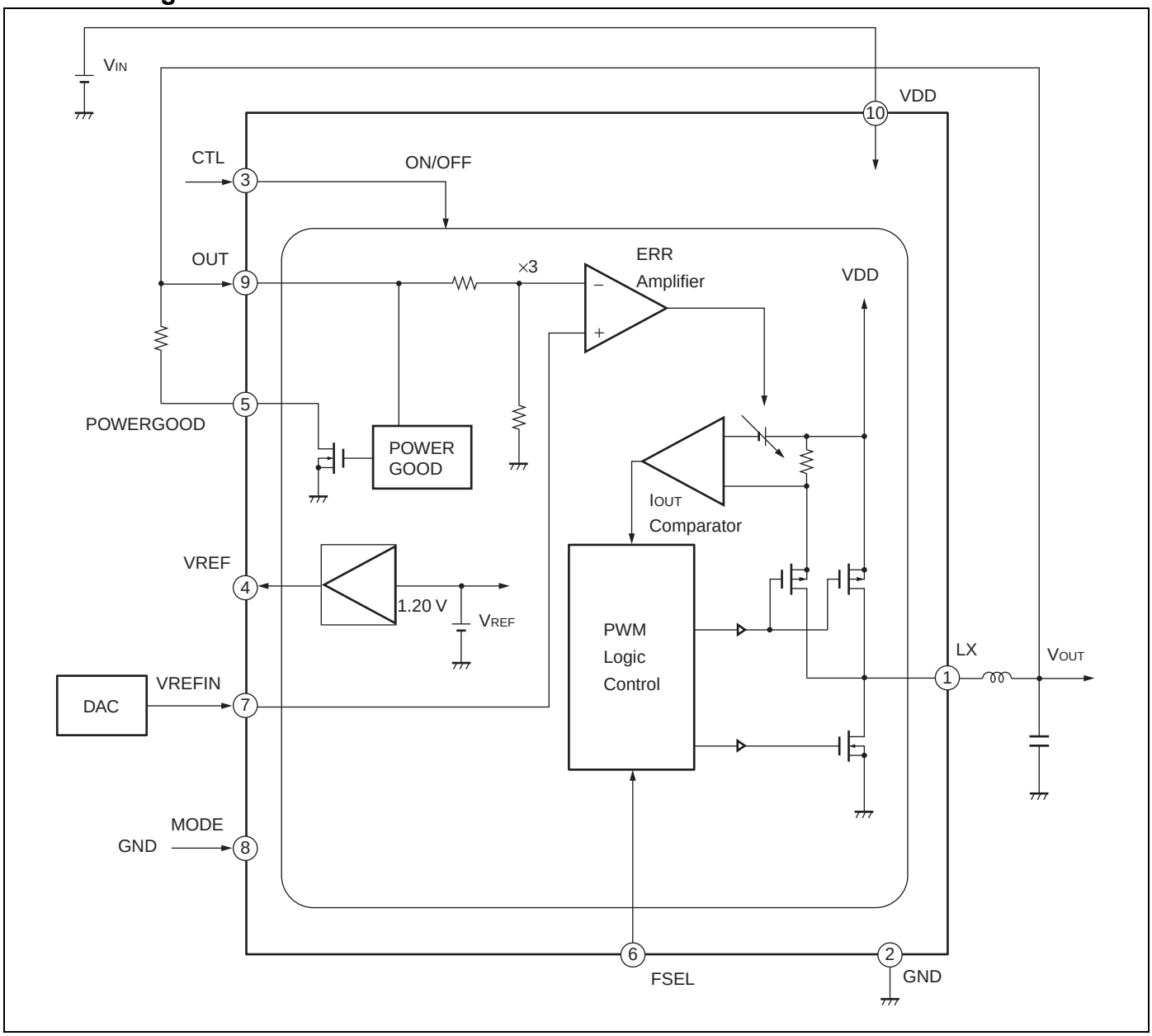
4. Block Diagram



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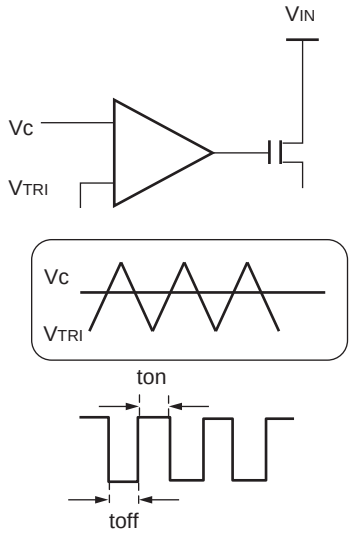
4.1 Current Mode

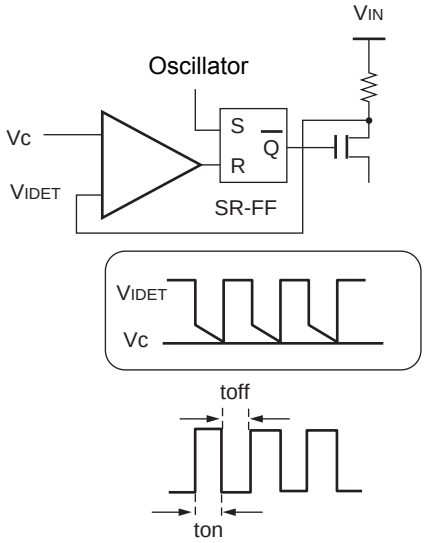
■ Original Voltage Mode Type:
Stabilize the output voltage by comparing two items below and on-duty control.
- ❒ Voltage (VC) obtained through negative feedback of the output voltage by Error Amp
- ❒ Reference triangular wave (V_{TRI})

■ Current Mode Type:
Instead of the triangular wave (V_{TRI}), the voltage (V_{IDET}) obtained through I-V conversion of the sum of currents that flow in the oscillator (rectangular wave generation circuit) and SW FET is used.
Stabilize the output voltage by comparing two items below and on-duty control.
- ❒ Voltage (V_C) obtained through negative feedback of the output voltage by Error Amp
- ❒ Voltage (V_{IDET}) obtained through I-V conversion of the sum of current that flow in the oscillator (rectangular wave generation circuit) and SW FET

Voltage mode type model



Current mode type model



Note :

The above models illustrate the general operation and an actual operation will be preferred in the IC.

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5. Function of Each Block

5.1 PWM Logic Control Circuit

The built-in P-ch and N-ch MOS FETs are controlled for synchronization rectification according to the frequency (2.0 MHz/3.2 MHz) oscillated from the built-in oscillator (square wave oscillation circuit).

5.2 I_{OUT} Comparator Circuit

This circuit detects the current (I_{LX}) which flows to the external inductor from the built-in P-ch MOS FET.

By comparing V_{IDET} obtained through I-V conversion of peak current I_{PK} of I_{LX} with the Error Amp output, the built-in P-ch MOS FET is turned off via the PWM Logic Control circuit.

5.3 Error Amp Phase Compensation Circuit

This circuit compares the output voltage to reference voltages such as VREF. This IC has a built-in phase compensation circuit that is designed to optimize the operation of this IC. This needs neither to be considered nor addition of a phase compensation circuit and an external phase compensation device.

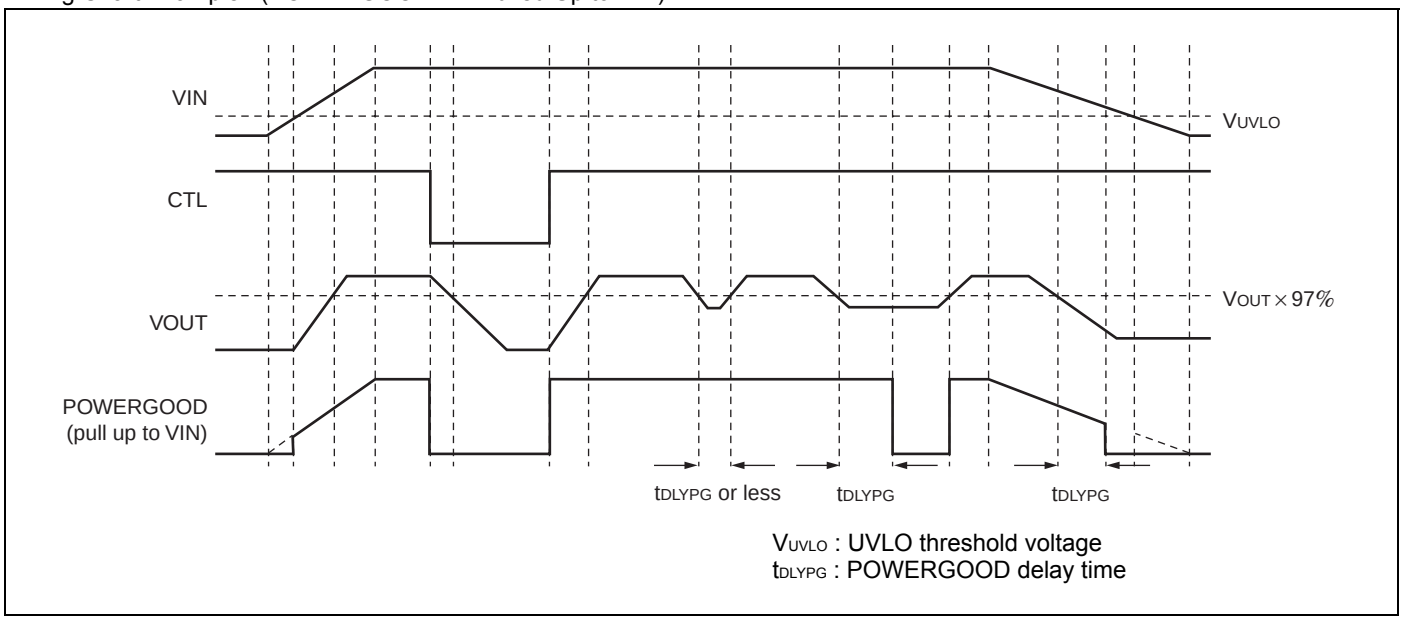
5.4 VREF Circuit

A high accuracy reference voltage is generated with BGR (bandgap reference) circuit. The output voltage is 1.20 V (Typ).

5.5 POWERGOOD Circuit

The POWERGOOD circuit monitors the voltage at the OUT pin. The POWERGOOD pin is open drain output.
Use the pin with pull-up using the external resistor in the normal operation.
When the CTL is at the H level, the POWERGOOD pin becomes the H level. However, if the output voltage drops because of over current and etc, the POWERGOOD pin becomes the L level.

Timing Chart Example : (POWERGOOD Pin Pulled Up to VIN)



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5.6 Protection Circuit

This IC has a built-in over-temperature protection circuit.
The over-temperature protection circuit turns off both N-ch and P-ch switching FETs when the junction temperature reaches +135°C. When the junction temperature comes down to ＋ 110°C, the switching FET is returned to the normal operation.
Since the PWM control circuit of this IC is in the control method in current mode, the current peak value is also monitored and controlled as required.

■ Function Table

MODE		Input		Output		
	Switching Frequency	CTL	FSEL	OUTPUT Pin Voltage	VREF	POWERGOOD
Shutdown mode	—	L	*	Output stop	Output stop	Function stop
Operation mode	2.0 MHz	H	L	VOUT voltage output	1.2 V	Operation
	3.2 MHz	H	H			

* : Don't care

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6. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{DD}	VDD pin	− 0.3	+ 6.0	V
Signal input voltage	V_{ISIG}	OUT pin	− 0.3	V_{DD} + 0.3	V
		CTL, MODE, FSEL pins	− 0.3	V_{DD} + 0.3	
		VREFIN pin	− 0.3	V_{DD} + 0.3	
POWERGOOD pull-up voltage	V_{IPG}	POWERGOOD pin	− 0.3	+ 6.0	V
LX voltage	V_{LX}	LX pin	− 0.3	V_{DD} + 0.3	V
LX peak current	I_{PK}	I_{LX}	—	1.8	A
Power dissipation	P_D	Ta ≤ + 25°C	—	2632*1, *2, *3	mW
			—	980*1, *2, *4	
		Ta = + 85 °C	—	1053*1, *2, *3	mW
			—	392*1, *2, *4	
Operating ambient temperature	Ta	—	− 40	+ 85	°C
Storage temperature	T_{STG}	—	− 55	+ 125	°C

*1 : Power dissipation value between + 25°C and + 85°C is obtained by connecting these two points with a straight line

*2 : When mounted on a four- layer epoxy board of 11.7 cm × 8.4 cm

*3 : Connection at exposure pad with thermal via. (Thermal via 4 holes)

*4 : Connection at exposure pad, without a thermal via.

Notes:

- The use of negative voltages below − 0.3 V to the GND pin may create parasitic transistors on LSI lines, which can cause abnormal operation.
- This device can be damaged if the LX pin is short-circuited to VDD or GND.
- Take measures not to keep the FSEL pin falling below the GND potential of this IC as much as possible. In addition to erroneous operation, the IC may latch up and destroy itself if 110 mA or more current flows from this pin.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

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7. Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{DD}	—	2.5	3.7	5.5	V
VREFIN voltage	V_{REFIN}	—	0.15	—	1.20	V
CTL voltage	V_{CTL}	—	0	—	5.0	V
LX current	I_{LX}	—	—	—	800	mA
POWERGOOD current	I_{PG}	—	—	—	1	mA
VREF output current	I_{ROUT}	2.5 V ≤ V_{DD} ≤ 3.0 V	—	—	0.5	mA
		3.0 V ≤ V_{DD} ≤ 5.5 V	—	—	1	
Inductor value	L	2.0 MHz (FSEL = L)	—	2.2	—	µH
		3.2 MHz (FSEL = H)	—	1.5	—	

Note:

The output current from this device has a situation to decrease if the power supply voltage (V_{IN}) and the DC/DC converter output voltage (V_{OUT}) differ only by a small amount. This is a result of slope compensation and will not damage this device.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges.
Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

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8. Electrical Characteristics

(Ta = +25°C, VDD = 3.7 V, VOUT setting value = 2.5 V, MODE = 0 V)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
DC/DC converter block	Input current	$I_{REFIN}M$	7	V_{REFIN} = 0.833 V	−100	0	+100	nA
		$I_{REFIN}L$		V_{REFIN} = 0.15 V	−100	0	+100	nA
		$I_{REFIN}H$		V_{REFIN} = 1.20 V	−100	0	+100	nA
	Output voltage	V_{OUT}	9	V_{REFIN} = 0.833 V, OUT = −100 mA	2.45	2.50	2.55	V
	Input stability	LINE		2.5 V ≤ V_{DD} ≤ 5.5 V *1	—	10	—	mV
	Load stability	LOAD		− 100 mA ≥ OUT ≥ − 800 mA	—	10	—	mV
	Out pin input impedance	R_{OUT}		OUT = 2.0 V	0.6	1.0	1.5	MΩ
	LX peak current	I_{PK}	1	Output shorted to GND	0.9	1.2	1.7	A
	Oscillation frequency	f_{OSC1}		FSEL = 0 V	1.6	2.0	2.4	MHz
		f_{OSC2}		FSEL = 3.7 V	2.56	3.20	3.84	MHz
	Rise delay time	t_{PG}	3, 9	C1 = 4.7 µF, OUT = 0 A, VOUT = 90%	—	45	80	µs
	SW NMOS FET OFF voltage	V_{NOFF}	1	—	−40*	−20*	0*	mV
	SW PMOS FET ON resistance	R_{ONP}		LX = −100 mA	—	0.30	0.47	Ω
	SW NMOS FET ON resistance	R_{ONN}		LX = −100 mA	—	0.20	0.36	Ω
	LX leak current	$I_{LEAK}M$		0 ≤ LX ≤ V_{DD}*2	−1.0	—	+8.0	µA
		$I_{LEAK}H$		V_{DD} = 5.5 V, 0 ≤ LX ≤ V_{DD}*2	−2.0	—	+16.0	µA
Protection circuit block	Over temperature protection (Junction Temp.)	T_{OTPH}	—	—	+120*	+135*	+155*	°C
		T_{OTPL}			+95*	+110*	+130*	°C
	UVLO threshold voltage	V_{THH}	10	—	2.07	2.20	2.33	V
		V_{THL}			1.92	2.05	2.18	V
	UVLO hysteresis width	V_{HYS}		—	0.08	0.15	0.25	V

* : Standard design value

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(Ta = +25°C, VDD = 3.7 V, VOUT setting value = 2.5 V, MODE = 0 V)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
POWER GOOD block	POWERGOOD threshold voltage	V_{THPG}	5	*3	V_{REFIN} × 3 × 0.93	V_{REFIN} × 3 × 0.97	V_{REFIN} × 3 × 0.99	V
	POWERGOOD delay time	t_{DLYPG1}		FSEL = 0 V	—	250	—	µs
		t_{DLYPG2}		FSEL = 3.7 V	—	170	—	µs
	POWERGOOD output voltage	V_{OL}		POWERGOOD = 250 µA	—	—	0.1	V
	POWERGOOD output current	I_{OH}		POWERGOOD = 5.5 V	—	—	1.0	µA
Control block	CTL threshold voltage	V_{THHCT}	3	—	0.55	0.95	1.45	V
		V_{THLCT}		—	0.40	0.80	1.30	
	CTL pin input current	I_{ICTL}		CTL = 3.7 V	—	—	1.0	µA
	FSEL threshold voltage	V_{THHFS}	6	—	2.96	—	—	V
		V_{THLFS}		—	—	—	0.74	
Reference voltage block	VREF voltage	V_{REF}	4	VREF = −2.7 µA, OUT = −100 mA	1.176	1.200	1.224	V
	VREF load stability	L_{OADREF}		VREF = −1.0 mA	—	—	20	mV
General	Shut down power supply current	I_{VDD1}	10	CTL = 0 V, All circuits in OFF state	—	—	1.0	µA
		I_{VDD1H}		CTL = 0 V, VDD = 5.5 V	—	—	1.0	µA
	Standby power supply current (DC/DC)	I_{VDD2}		CTL = 3.7 V, OUT = 0 A, FSEL = 0 V	—	4.0	8.0	mA
	Power-on invalid current	I_{VDD}		CTL = 3.7 V, VOUT = 90%*4	—	800	1500	µA

*1 : The minimum value of V_{DD} is the 2.5 V or V_{OUT} setting value + 0.6 V, whichever is higher.

*2 : The + leak at the LX pin includes the current of the internal circuit.

*3 : Detected with respect to the output voltage setting value of V_{REFIN}

*4 : Current consumption based on 100% ON-duty (High side FET in full ON state). The SW FET gate drive current is not included because the device is in full ON state (no switching operation). Also the load current is not included.

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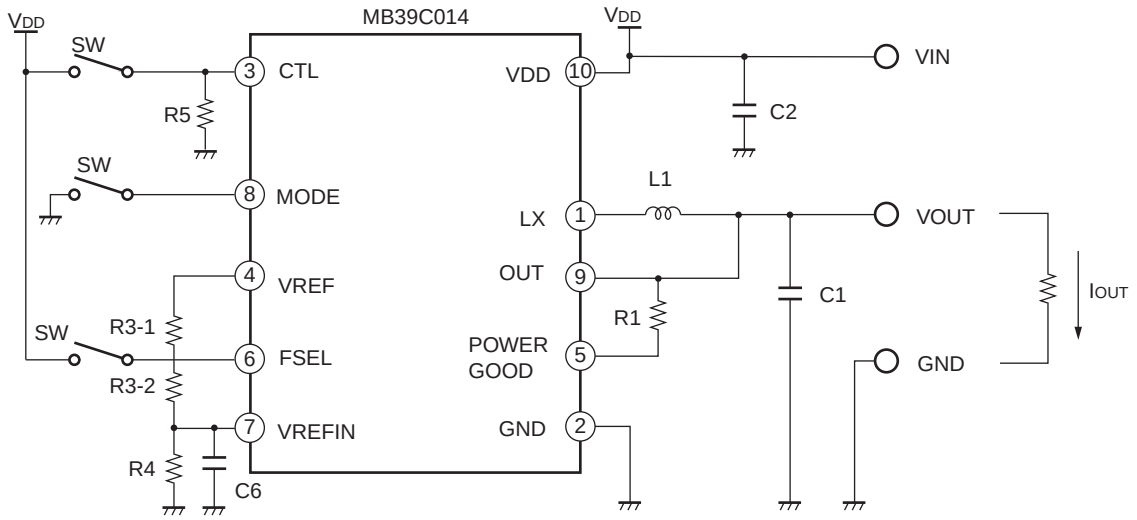
9. Test Circuit for Measuring Typical Operating Characteristics



Output voltage = VREFIN × 2.97

Component	Specification	Vendor	Part Number	Remark
R1	1 MΩ	KOA	RK73G1JTTD D 1 MΩ	
R3-1 R3-2	7.5 kΩ 120 kΩ	SSM SSM	RR0816-752-D RR0816-124-D	At VOUT = 2.5 V setting
R4	300 kΩ	SSM	RR0816-304-D	
R5	1 MΩ	KOA	RK73G1JTTD D 1 MΩ	
C1	4.7 µF	TDK	C2012JB1A475K	
C2	4.7 µF	TDK	C2012JB1A475K	
C6	0.1 µF	TDK	C1608JB1H104K	For adjusting slow start time
L1	2.2 µH	TDK	VLF4012AT-2R2M	2.0 MHz operation
	1.5 µH	TDK	VLF4012AT-1R5M	3.2 MHz operation

Note :

These components are recommended based on the operating tests authorized.

TDK : TDK Corporation
SSM : SUSUMU Co., Ltd
KOA : KOA Corporation

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10. Application Notes

10.1 Selection of Components

10.1.1 Selection of an External Inductor

Basically it dose not need to design inductor. This IC is designed to operate efficiently with a 2.2 µH (2.0 MHz operation) or 1.5 µH (3.2 MHz operation) inductor.

The inductor should be rated for a saturation current higher than the LX peak current value during normal operating conditions, and should have a minimal DC resistance. (100 mΩ or less is recommended.)

LX peak current value I_{PK} is obtained by the following formula.

$$I_{PK} = I_{OUT} + \frac{V_{IN} - V_{OUT}}{L} \times \frac{D}{fosc} \times \frac{1}{2} = I_{OUT} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times fosc \times V_{IN}}$$

L : External inductor value
I_{OUT} : Load current
V_{IN} : Power supply voltage
V_{OUT} : Output setting voltage
D : ON- duty to be switched(= V_{OUT}/V_{IN})
fosc : Switching frequency (2.0 MHz or 3.2 MHz)

ex) At V_{IN} = 3.7 V, V_{OUT} = 2.5 V, I_{OUT} = 0.8 A, L = 2.2 µH, fosc = 2.0 MHz
The maximum peak current value I_{PK};

$$I_{PK} = I_{OUT} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times fosc \times V_{IN}} = 0.8\,A + \frac{(3.7\,V - 2.5\,V) \times 2.5\,V}{2 \times 2.2\,\mu H \times 2\,MHz \times 3.7\,V} \fallingdotseq 0.89\,A$$

10.1.2 I/O Capacitor Selection

- Select a low equivalent series resistance (ESR) for the VDD input capacitor to suppress dissipation from ripple currents.

- Also select a low equivalent series resistance (ESR) for the output capacitor. The variation in the inductor current causes ripple currents on the output capacitor which, in turn, causes ripple voltages an output equal to the amount of variation multiplied by the ESR value. The output capacitor value has a significant impact on the operating stability of the device when used as a DC/DC converter. Therefore, Cypress generally recommends a 4.7 µF capacitor, or a larger capacitor value can be used if ripple voltages are not suitable. If the V_{IN}/V_{OUT} voltage difference is within 0.6 V, the use of a 10 µF output capacitor value is recommended.

- Types of capacitors
  Ceramic capacitors are effective for reducing the ESR and afford smaller DC/DC converter circuit. However, power supply functions as a heat generator, therefore avoid to use capacitor with the F-temperature rating (− 80% to + 20%). Cypress recommends capacitors with the B-temperature rating (± 10% to ± 20%).
  Normal electrolytic capacitors are not recommended due to their high ESR.
  Tantalum capacitor will reduce ESR, however, it is dangerous to use because it turns into short mode when damaged. If you insist on using a tantalum capacitor, Cypress recommends the type with an internal fuse.

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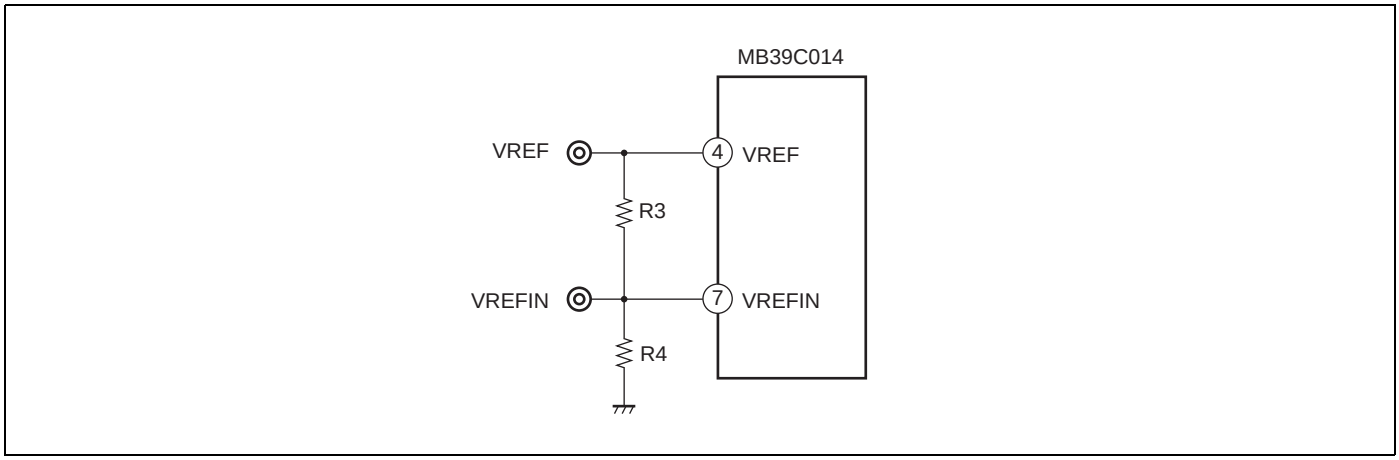
10.2 Output Voltage Setting

The output voltage V_{OUT} of this IC is defined by the voltage input to VREFIN. Supply the voltage for inputting to VREFIN from an external power supply, or set the VREF output by dividing it with resistors.

The output voltage when the VREFIN voltage is set by dividing the VREF voltage with resistors is shown in the following formula.

$$V_{OUT} = 2.97 \times V_{REFIN}, \quad V_{REFIN} = \frac{R4}{R3 + R4} \times V_{REF}$$

($V_{REF} = 1.20$ V)



Note :

Refer to “Application Circuit Examples” for an example of this circuit.

Although the output voltage is defined according to the dividing ratio of resistance, select the resistance value so that the current flowing through the resistance does not exceed the VREF current rating (1 mA) .

10.3 About Conversion Efficiency

The conversion efficiency can be improved by reducing the loss of the DC/DC converter circuit.

The total loss (P_{LOSS}) of the DC/DC converter is roughly divided as follows :

$$P_{LOSS} = P_{CONT} + P_{SW} + P_C$$

P_{CONT} : Control system circuit loss (The power used for this IC to operate, including the gate driving power for internal SW FETs)

P_{SW} : Switching loss (The loss caused during switching of the IC's internal SW FETs)

P_C : Continuity loss (The loss caused when currents flow through the IC's internal SW FETs and external circuits)

The IC's control circuit loss (P_{CONT}) is extremely small, less than 100 mW with no load.

As the IC contains FETs which can switch faster with less power, the continuity loss (P_C) is more predominant as the loss during heavy-load operation than the control circuit loss (P_{CONT}) and switching loss (P_{SW}) .

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Furthermore, the continuity loss (P_C) is divided roughly into the loss by internal SW FET ON-resistance and by external inductor series resistance.

$$P_C = I_{OUT}^2 \times (RDC + D \times R_{ONP} + (1 - D) \times R_{ONN})$$

D : Switching ON-duty cycle (= V_{OUT} / V_{IN})
R_{ONP} : Internal P-ch SW FET ON resistance
R_{ONN} : Internal N-ch SW FET ON resistance
RDC : External inductor series resistance
I_{OUT} : Load current

The above formula indicates that it is important to reduce RDC as much as possible to improve efficiency by selecting components.

10.4 Power Dissipation and Heat Considerations

The IC is so efficient that no consideration is required in most of the cases. However, if the IC is used at a low power supply voltage, heavy load, high output voltage, or high temperature, it requires further consideration for higher efficiency.

The internal loss (P) is roughly obtained from the following formula :

$$P = I_{OUT}^2 \times (D \times R_{ONP} + (1 - D) \times R_{ONN})$$

D : Switching ON-duty cycle (= V_{OUT} / V_{IN})
R_{ONP} : Internal P-ch SW FET ON resistance
R_{ONN} : Internal N-ch SW FET ON resistance
I_{OUT} : Output current

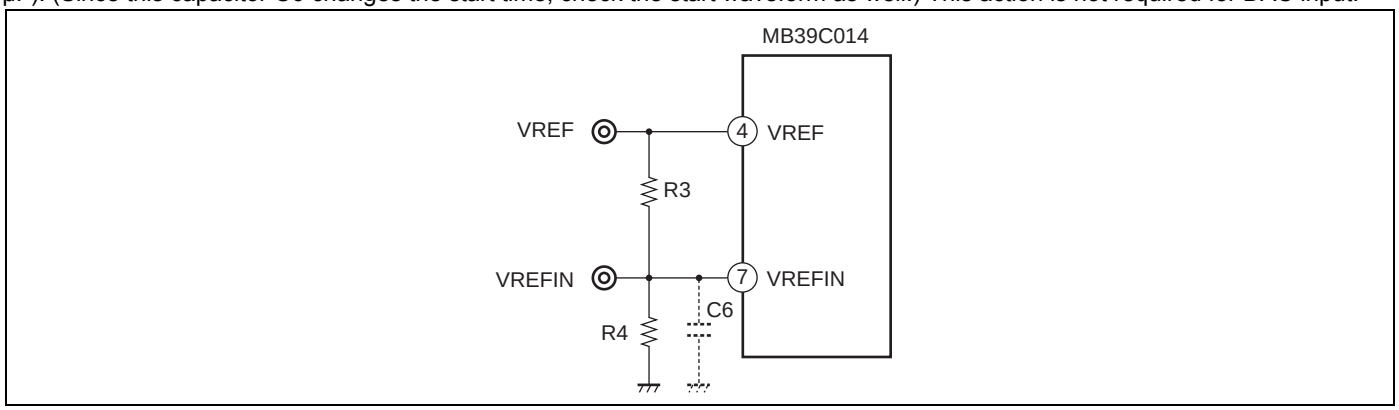
The loss expressed by the above formula is mainly continuity loss. The internal loss includes the switching loss and the control circuit loss as well but they are so small compared to the continuity loss they can be ignored.

In this IC with R_{ONP} greater than R_{ONN}, the larger the on-duty cycle, the greater the loss.

When assuming V_{IN} = 3.7 V, Ta = + 70°C for example, R_{ONP} = 0.42 Ω and R_{ONN} = 0.36 Ω according to the graph “MOS FET ON resistance vs. Operating ambient temperature”. The IC's internal loss P is 144 mW at V_{OUT} = 2.5 V and I_{OUT} = 0.6 A. According to the graph “Power dissipation vs. Operating ambient temperature”, the power dissipation at an operating ambient temperature Ta of + 70°C is 539 mW and the internal loss is smaller than the power dissipation.

10.5 Transient Response

Normally, I_{OUT} is suddenly changed while V_{IN} and V_{OUT} are maintained constant, responsiveness including the response time and overshoot/undershoot voltage is checked. As this IC has built-in Error Amp with an optimized design, it shows good transient response characteristics. However, if ringing upon sudden change of the load is high due to the operating conditions, add capacitor C6 (e.g. 0.1 µF). (Since this capacitor C6 changes the start time, check the start waveform as well.) This action is not required for DAC input.



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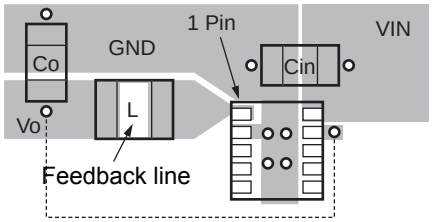
10.6 Board Layout, Design Example

The board layout needs to be designed to ensure the stable operation of this IC.
Follow the procedure below for designing the layout.

- Arrange the input capacitor (Cin) as close as possible to both the VDD and GND pins. Make a thru-hole (TH) near the pins of this capacitor if the board has planes for power and GND.
- Large AC currents flow between this IC and the input capacitor (Cin), output capacitor (C_O), and external inductor (L). Group these components as close as possible to this IC to reduce the overall loop area occupied by this group. Also try to mount these components on the same surface and arrange wiring without thru-hole wiring. Use thick, short, and straight routes to wire the net (The layout by planes is recommended.).
- The feedback wiring to the OUT should be wired from the voltage output pin closest to the output capacitor (C_O). The OUT pin is extremely sensitive and should thus be kept wired away from the LX pin of this IC as far as possible.
- If applying voltage to the VREFIN pin through dividing resistors, arrange the resistors so that the wiring can be kept as short as possible. Also arrange them so that the GND pin of the VREFIN resistor is close to the IC's GND pin. Further, provide a GND exclusively for the control line so that the resistor can be connected via a path that does not carry current. If installing a bypass capacitor for the VREFIN, put it close to the VREFIN pin.
- Try to make a GND plane on the surface to which this IC will be mounted. For efficient heat dissipation when using the SON-10 package, Cypress recommends providing a thermal via in the footprint of the thermal pad.

10.7 Layout Example of IC SW Components



10.8 Notes for Circuit Design

- The switching operation of this IC works by monitoring and controlling the peak current which, incidentally, serves as form of short-circuit protection. However, do not leave the output short-circuited for long periods of time. If the output is short-circuited where VIN < 2.9 V, the current limit value (peak current to the inductor) tends to rise. Leaving in the short-circuit state, the temperature of this IC will continue rising and activate the thermal protection.
  Once the thermal protection stops the output, the temperature of the IC will go down and operation will resume, after which the output will repeat the starting and stopping.
  Although this effect will not destroy the IC, the thermal exposure to the IC over prolonged hours may affect the peripherals surrounding it.

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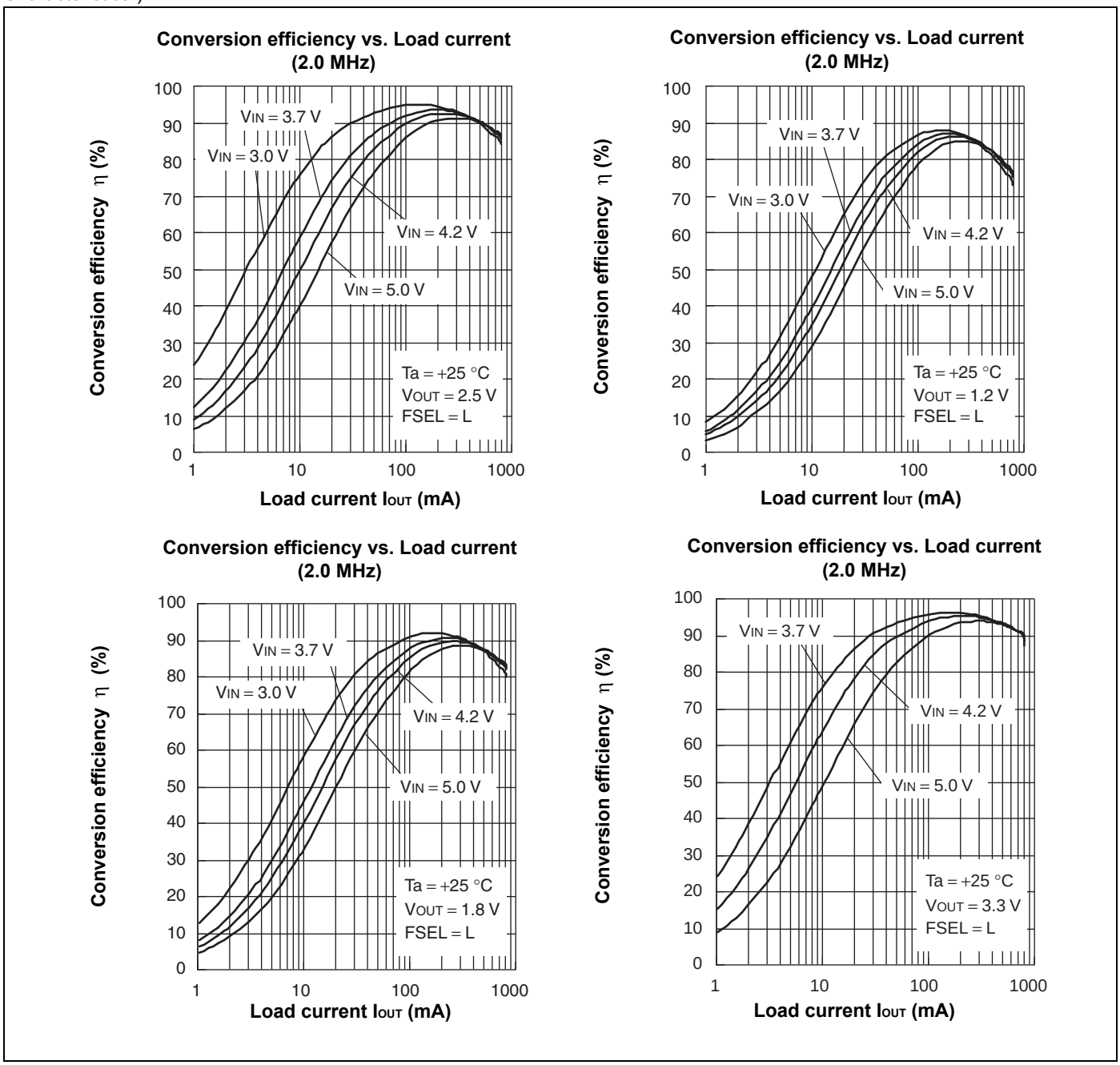
11. Example of Standard Operation Characteristics

(Shown below is an example of characteristics for connection according to"Test Circuit for Measuring Typical Operating Characteristics").



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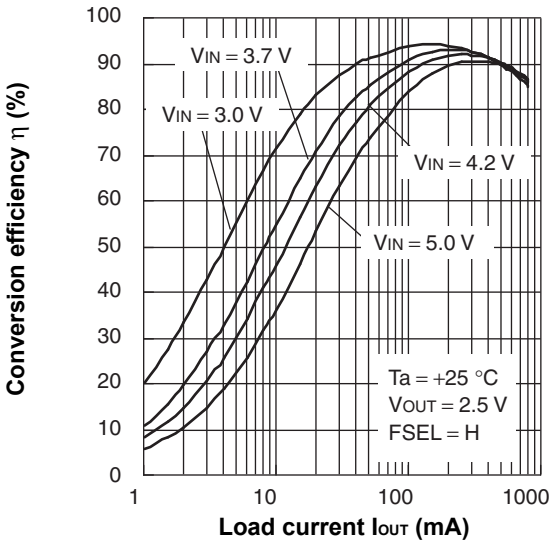
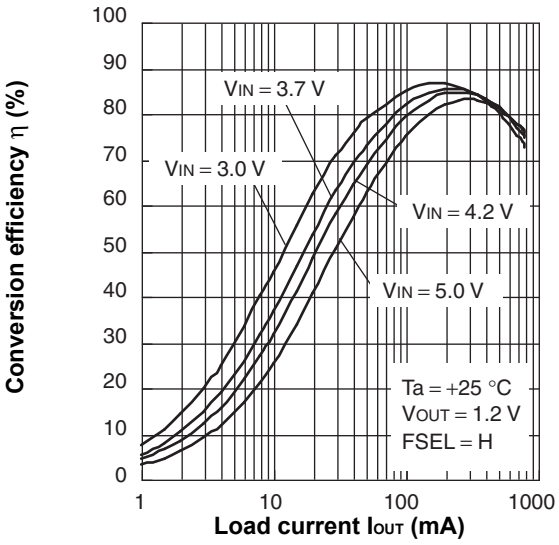
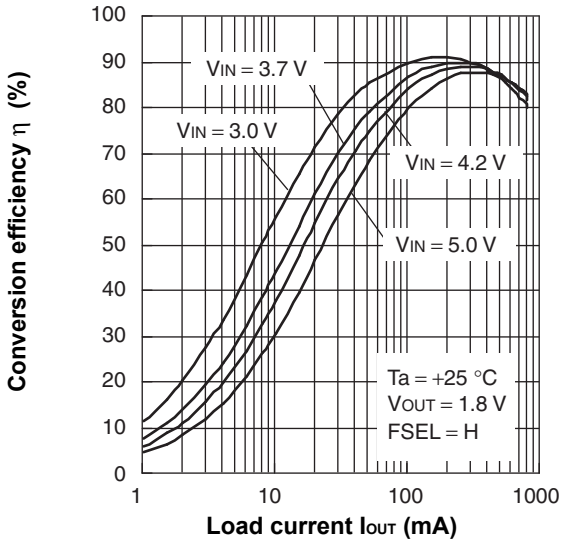
Conversion efficiency vs. Load current (3.2 MHz)



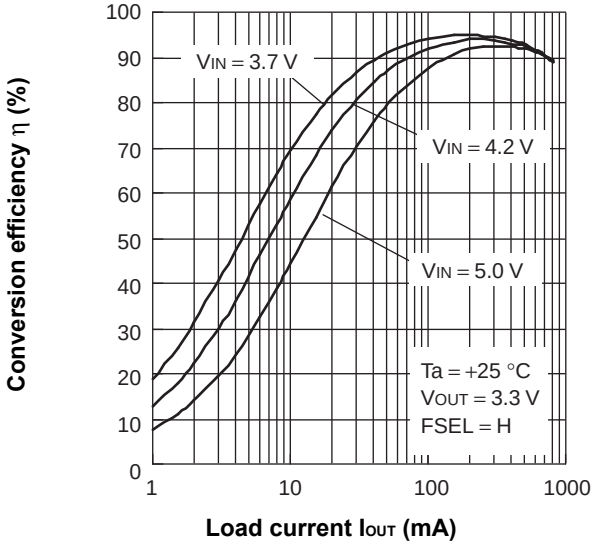
Conversion efficiency vs. Load current (3.2 MHz)



Conversion efficiency vs. Load current (3.2 MHz)



Conversion efficiency vs. Load current (3.2 MHz)



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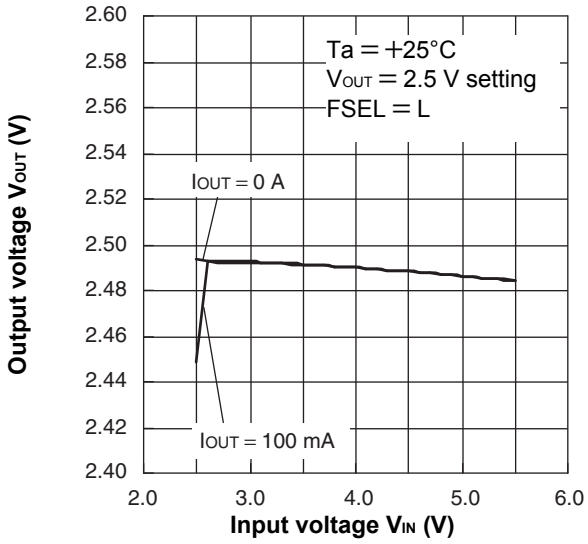
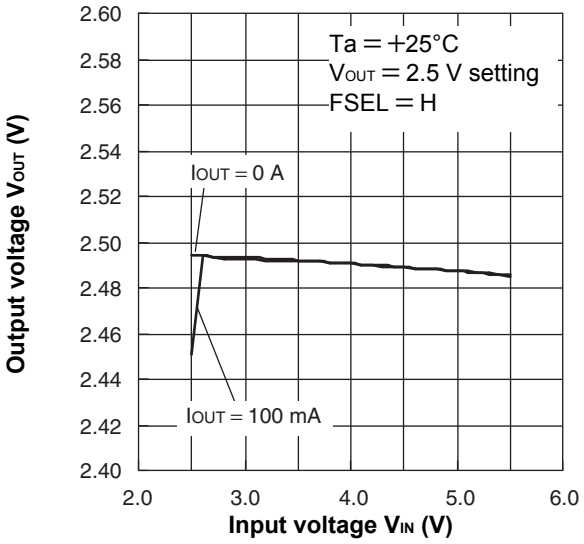
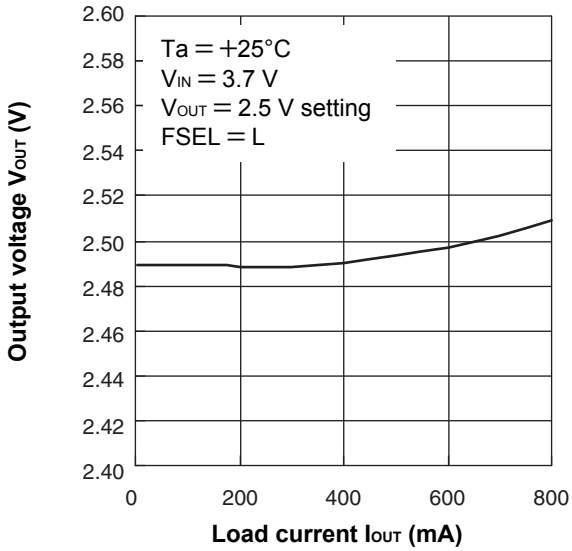
Output voltage vs. Input voltage (2.0 MHz)



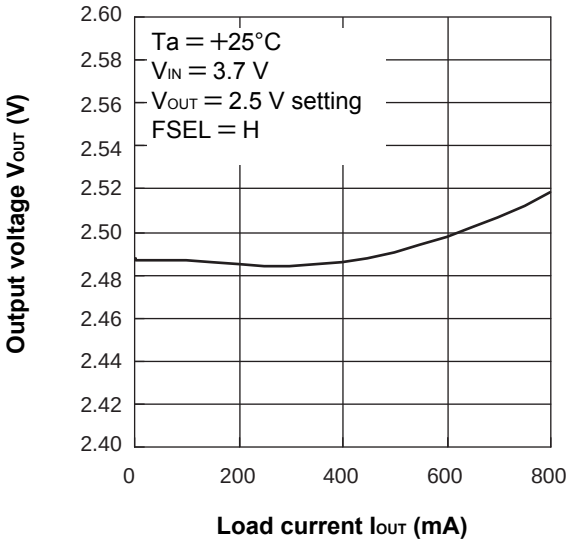
Output voltage vs. Input voltage (3.2 MHz)



Output voltage vs. Load current (2.0 MHz)

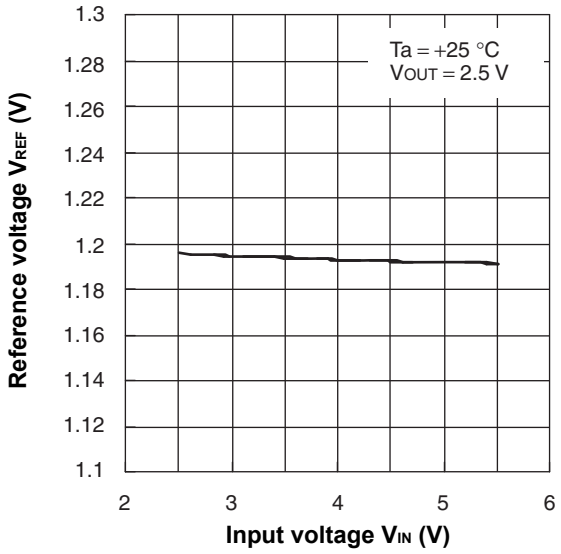


Output voltage vs. Load current (3.2 MHz)

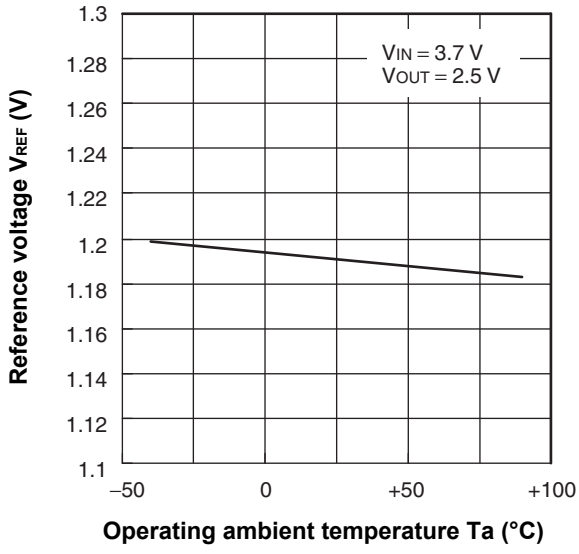


Downloaded from Arrow.com.

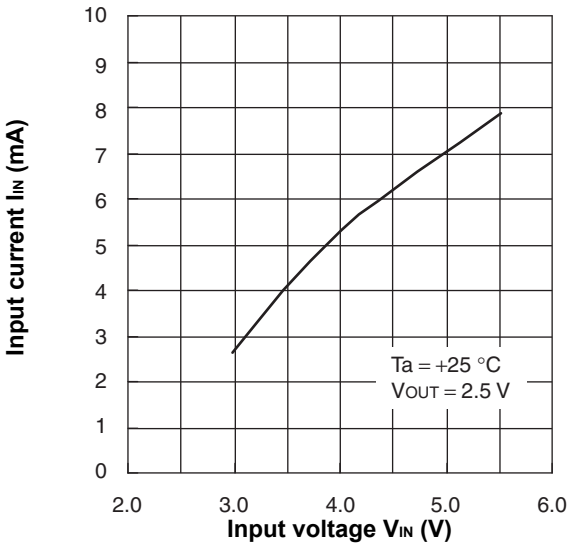
Reference voltage vs. Input voltage



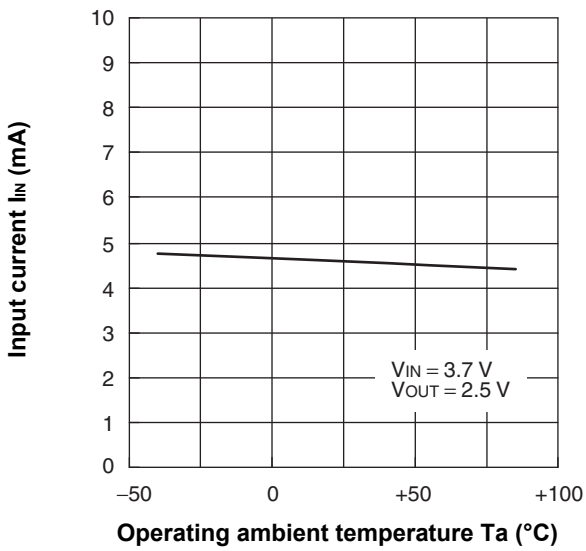
Reference voltage vs. Operating ambient temperature



Input current vs. Input voltage



Input current vs. Operating ambient temperature



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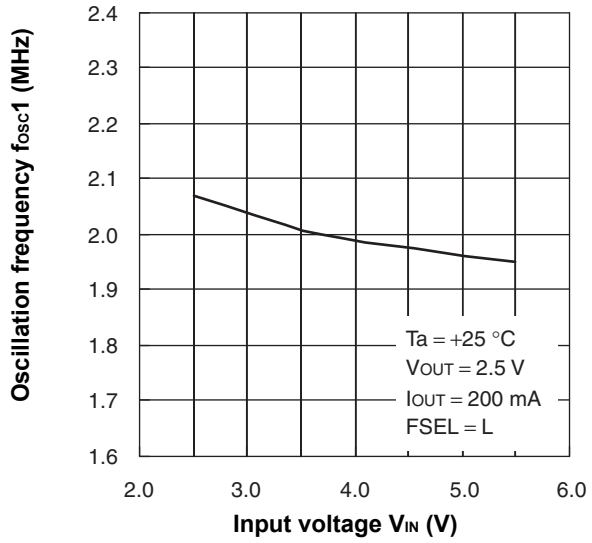
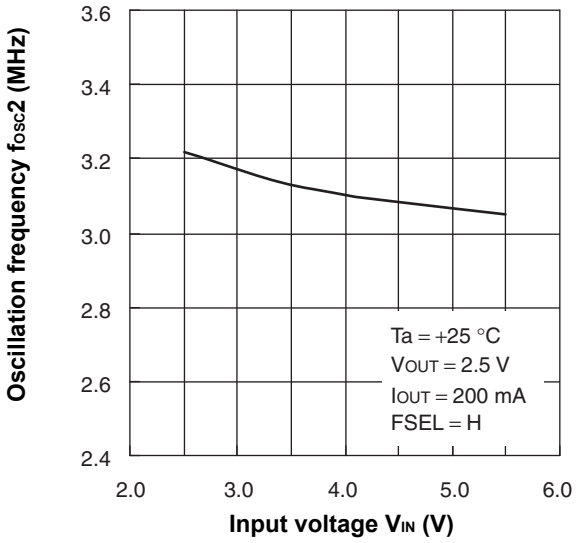
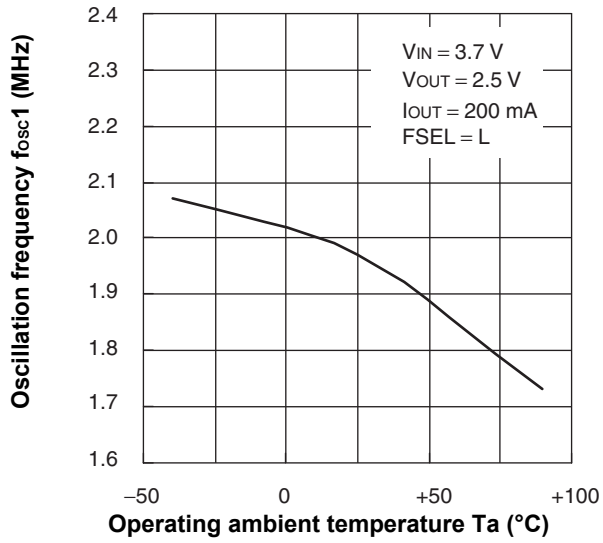
Oscillation frequency vs. Input voltage (2.0 MHz)



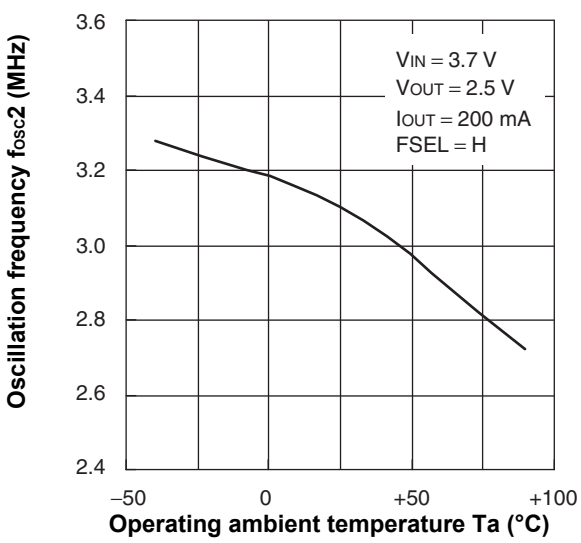
Oscillation frequency vs. Input voltage (3.2 MHz)



Oscillation frequency vs. Operating ambient temperature (2.0 MHz)



Oscillation frequency vs. Operating ambient temperature (3.2 MHz)



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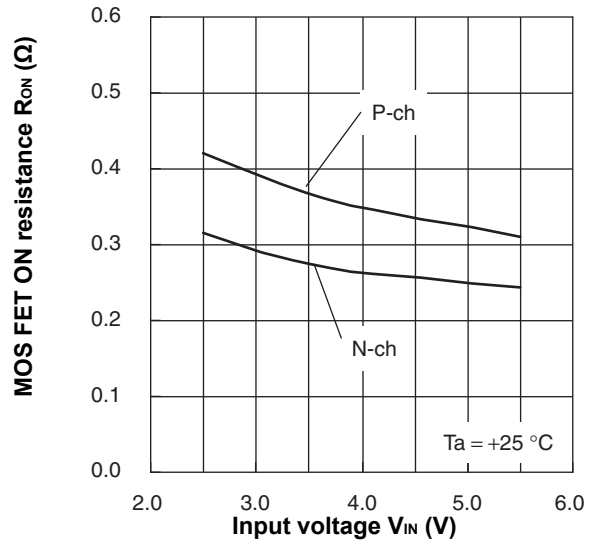
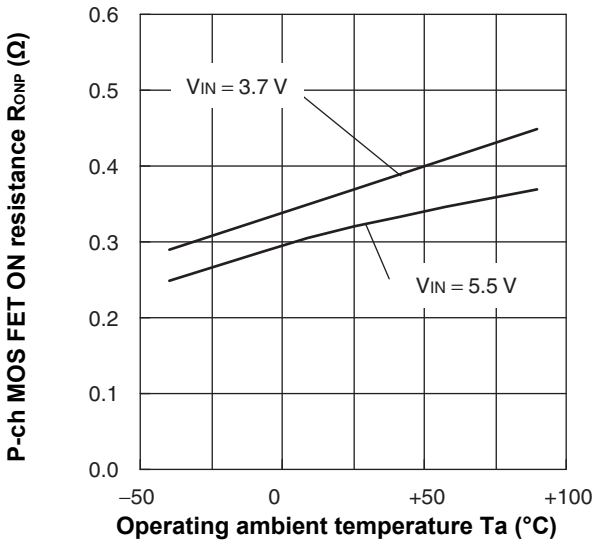
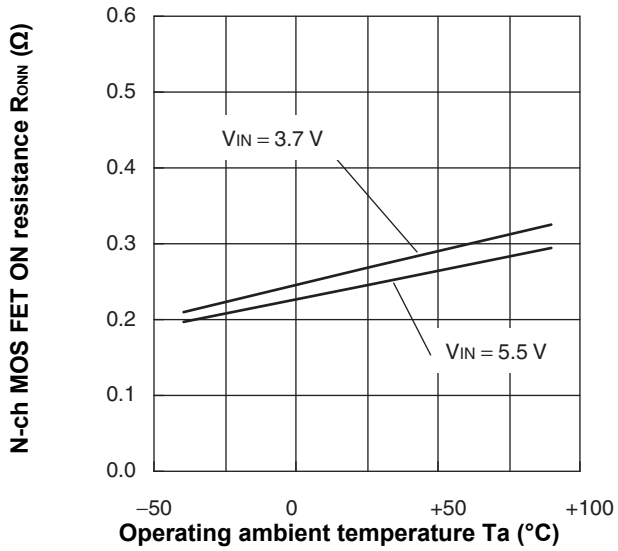
MOS FET ON resistance vs. Input voltage



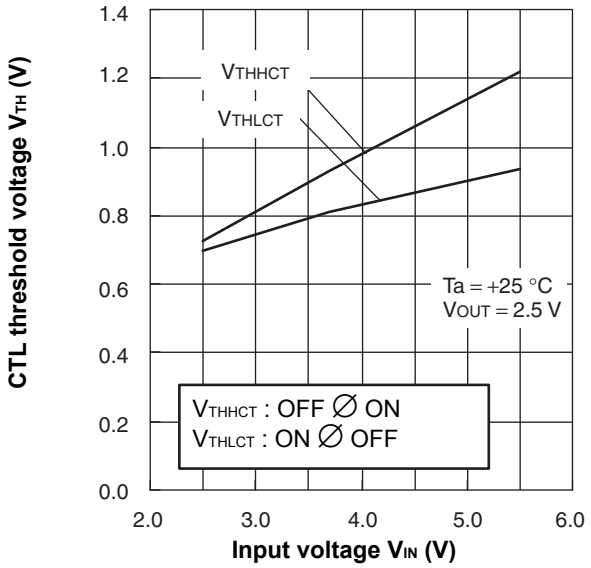
P-ch MOS FET ON resistance vs. Operating ambient temperature



N-ch MOS FET ON resistance vs. Operating ambient temperature



CTL threshold voltage V_{TH} vs. Input voltage



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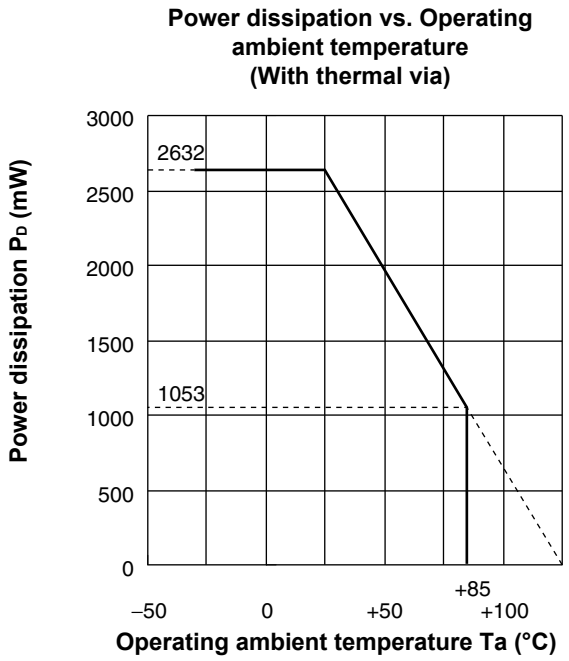
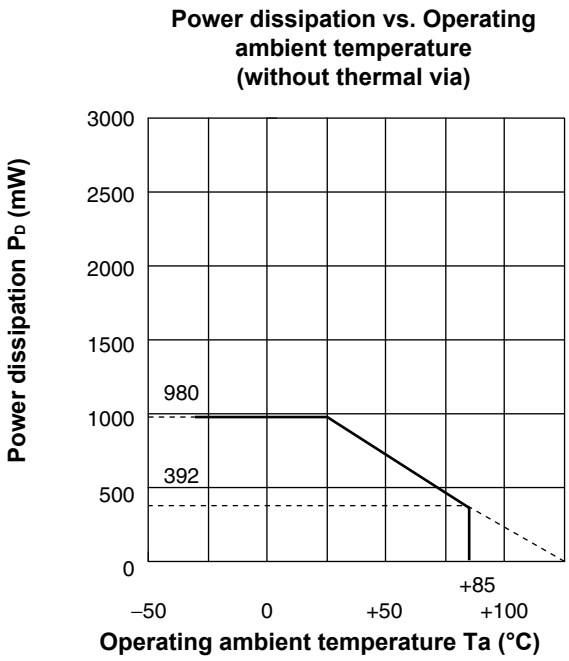
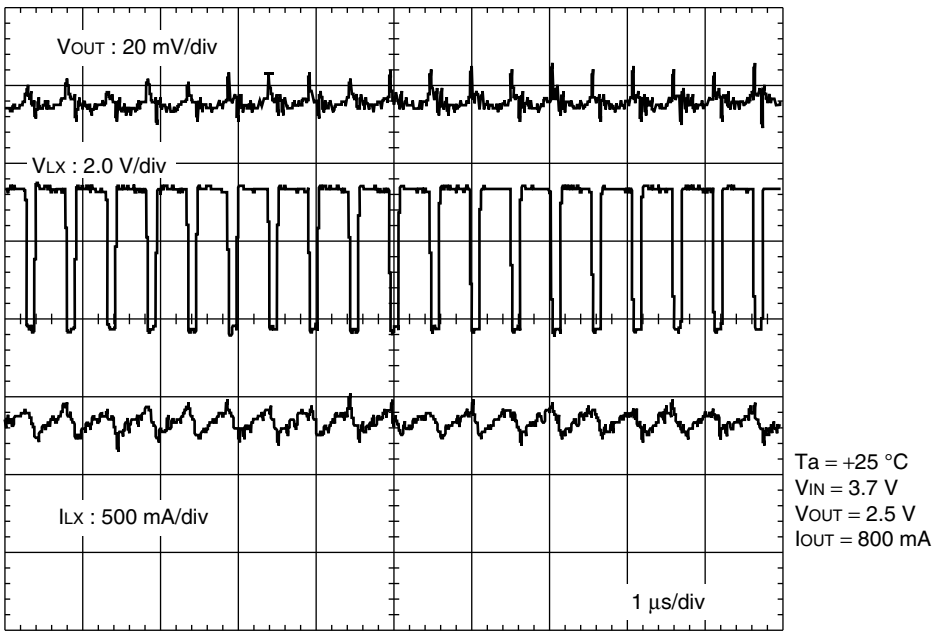




■ Switching Waveforms



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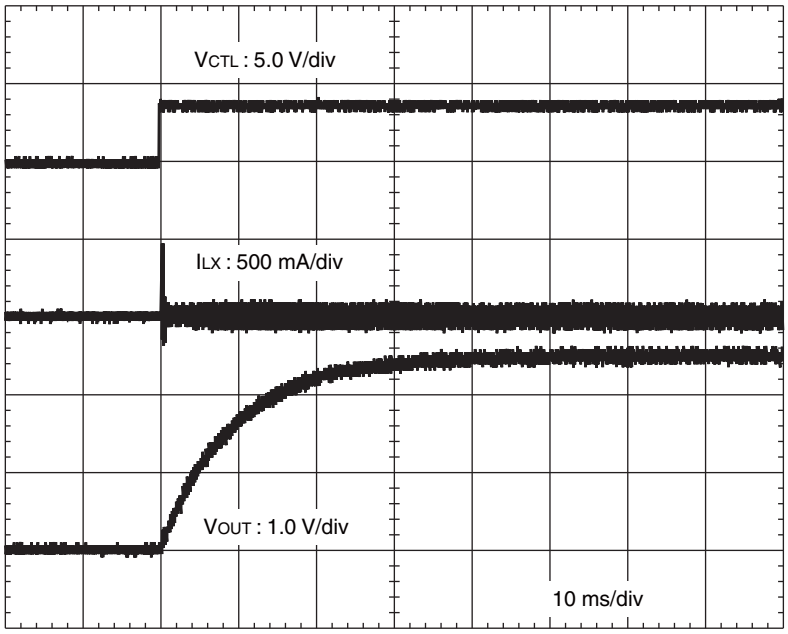
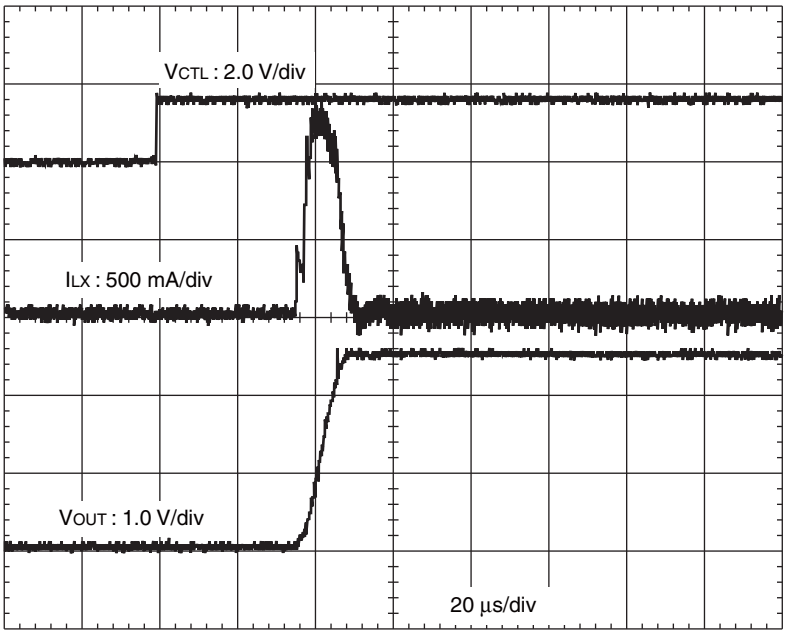
■ Startup Waveform



Ta = +25 °C
VIN = 3.7 V
VOUT = 2.5 V
IOUT = 0 A
VREFIN Capacitor value = 0.1 µF



Ta = +25 °C
VIN = 3.7 V
VOUT = 2.5 V
IOUT = 0 A
No VREFIN Capacitor

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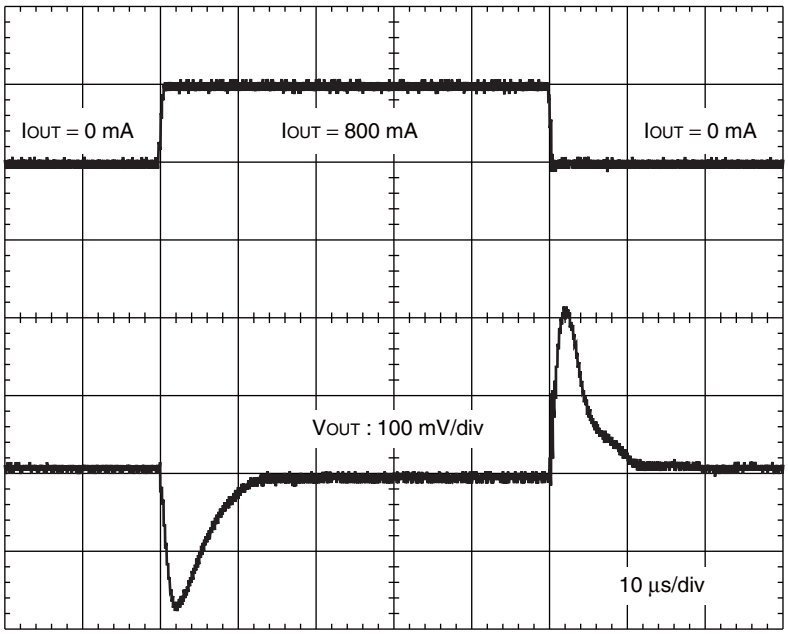
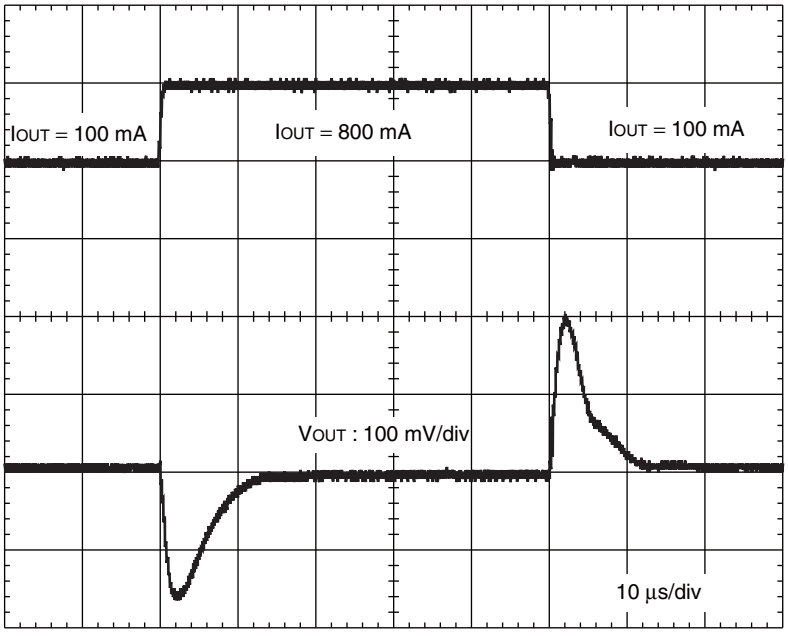
■ Output Waveforms at Sudden Load Changes (0 mA ↔ 800 mA)



Ta = +25 °C
VIN = 3.7 V
VOUT = 2.5 V
VREFIN Capacitor value = 0.1 µF

■ Output Waveforms at Sudden Load Changes (100 mA ↔ 800 mA)



Ta = +25°C
VIN = 3.7 V
VOUT = 2.5 V
VREFIN Capacitor value = 0.1 µF

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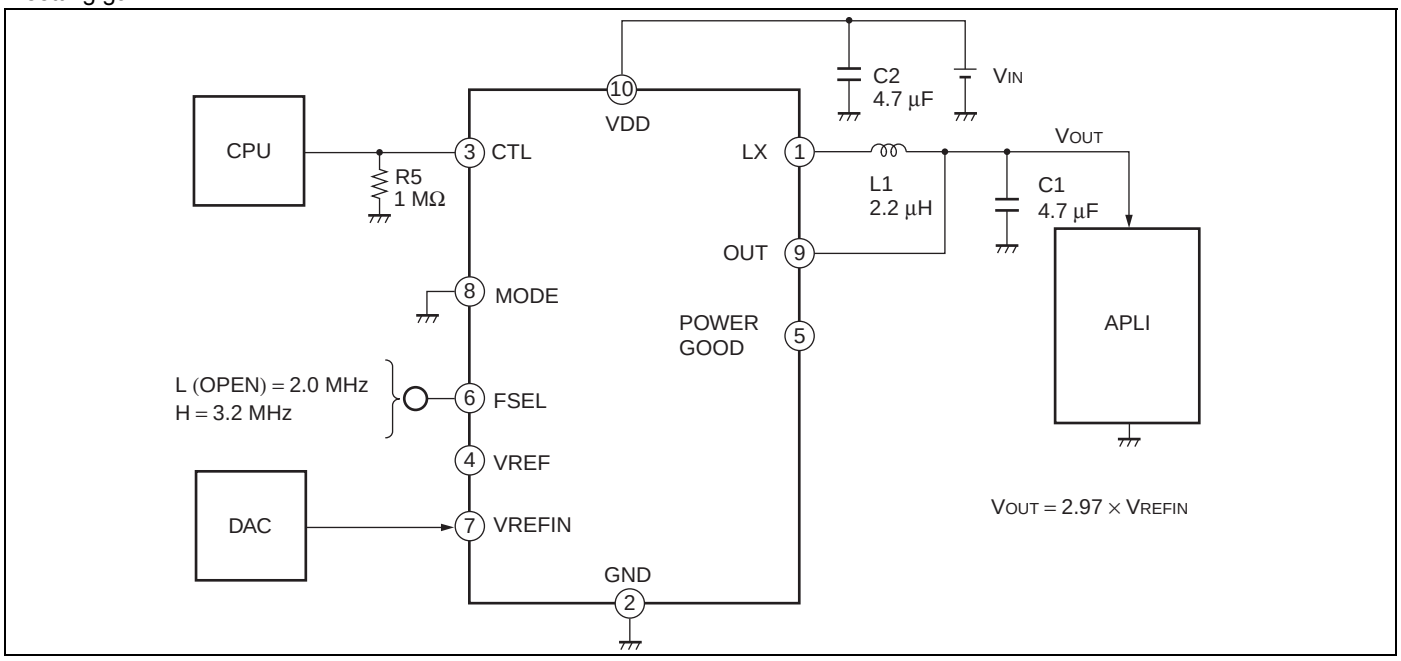
12. Application Circuit Examples

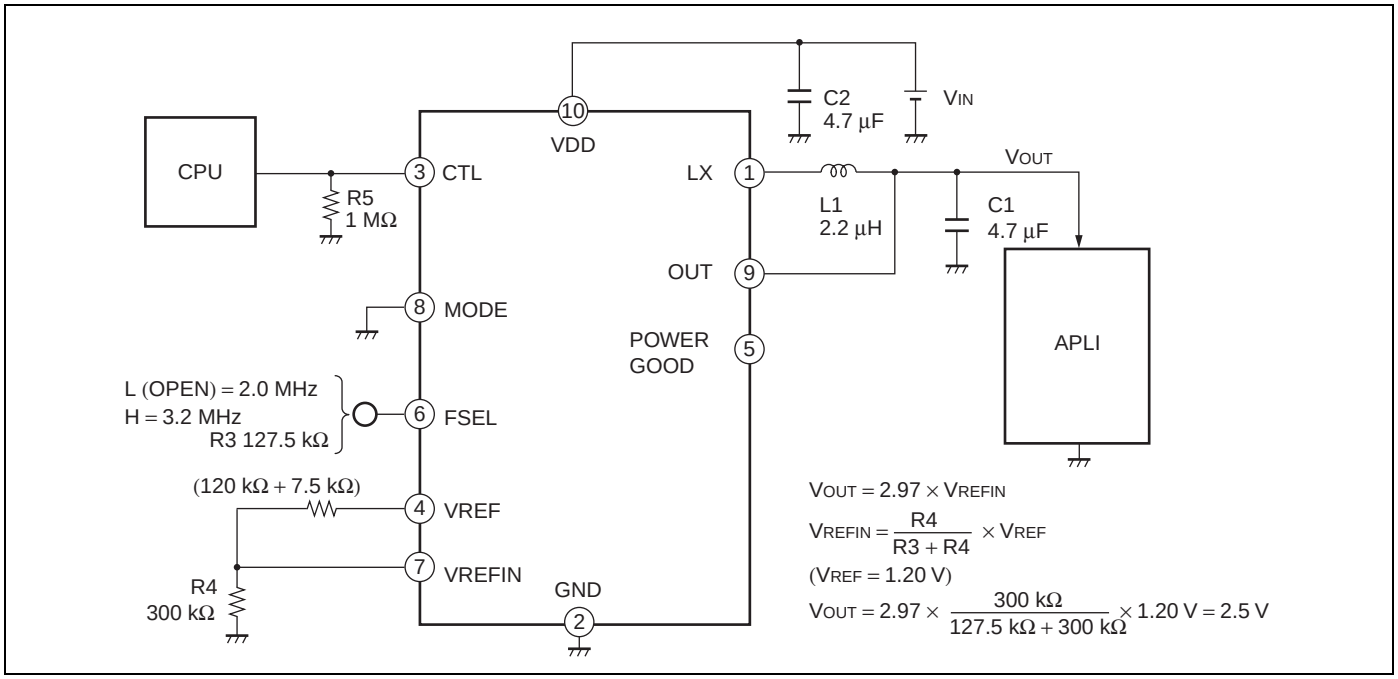
12.1 Application Circuit Example 1

■ An external voltage is input to the reference voltage external input (VREFIN) , and the V_{OUT} voltage is set to 2.97 times the V_{OUT} setting gain.



12.2 Application Circuit Example 2

■ The voltage of VREF pin is input to the reference voltage external input (VREFIN) by the dividing resistors. The V_{OUT} voltage is set to 2.5 V.



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12.3 Application Circuit Example Components List

Component	Item	Part Number	Specification	Package	Vendor
L1	Inductor	VLF4012AT-2R2M	2.2 µH, RDC = 76 mΩ	SMD	TDK
		MIPW3226D2R2M	2.2 µH, RDC = 100 mΩ	SMD	FDK
C1	Ceramic capacitor	C2012JB1A475K	4.7 µF (10 V)	2012	TDK
C2	Ceramic capacitor	C2012JB1A475K	4.7 µF (10 V)	2012	TDK
R3	Resistor	RK73G1JTTD D 7.5 kΩ RK73G1JTTD D 120 kΩ	7.5 kΩ 120 kΩ	1608 1608	KOA
R4	Resistor	RK73G1JTTD D 300 kΩ	300 kΩ	1608	KOA
R5	Resistor	RK73G1JTTD D	1 MΩ ± 0.5%	1608	KOA

TDK : TDK Corporation

FDK : FDK Corporation

KOA : KOA Corporation

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13. Usage Precautions

1. Do not Configure the IC Over the Maximum Ratings

If the IC is used over the maximum ratings, the LSI may be permanently damaged.
It is preferable for the device to normally operate within the recommended usage conditions. Usage outside of these conditions can adversely affect reliability of the LSI.

2. Use the Devices Within Recommended Operating Conditions

The recommended operating conditions are the conditions under which the LSI is guaranteed to operate.
The electrical ratings are guaranteed when the device is used within the recommended operating conditions and under the conditions stated for each item.

3. Printed Circuit Board Ground Lines Should be Set up With Consideration for Common Impedance

4. Take Appropriate Static Electricity Measures.

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.

5. Do not Apply Negative Voltages.

The use of negative voltages below −0.3 V may create parasitic transistors on LSI lines, which can cause abnormal operation.

14. Ordering Information

Part Number	Package	Remarks
MB39C014PN-❑❑❑E1	10-pin plastic SON (WNK010)	–

15. RoHS Compliance Information

The LSI products of Cypress with “E1” are compliant with RoHS Directive, and has observed the standard of lead, cadmium, mercury, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenylethers (PBDE).

A product whose part number has trailing characters “E1” is RoHS compliant.

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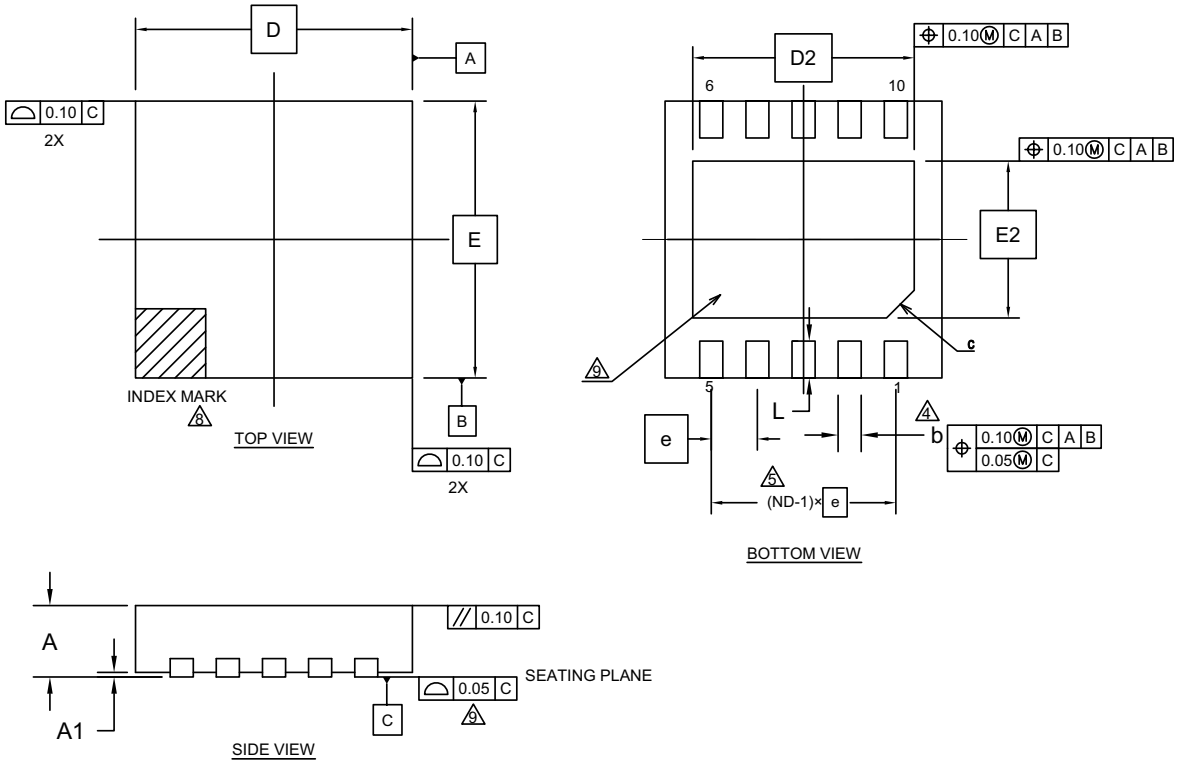
16. Package Dimension

Package Code: WNK010



SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	——	——	0.75
A_1	0.00	——	0.05
D	3.00 BSC		
E	3.00 BSC		
b	0.22	0.25	0.28
D_2	2.40 BSC		
E_2	1.70 BSC		
e	0.50 BSC		
c	0.30 REF		
L	0.30	0.40	0.50

NOTE

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCINC CONFORMS TO ASME Y14.5-1994.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL. THE DIMENSION "b"SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. JEDEC SPECIFICATION NO. REF : N/A

002-15676 Rev. **

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Document History

Document Title: MB39C014 1 ch DC/DC Converter IC with PFM/PWM Synchronous Rectification Document Number: 002-08361				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	TAOA	11/21/2008	Migrated to Cypress and assigned document number 002-08361. No change to document contents or format.
*A	5490964	TAOA	10/24/2016	Updated to Cypress template.
*B	5633455	HIXT	02/17/2017	Updated Pin Assignment: Change the package name from LCC-10P-M04 to WNK010 Updated Ordering Information: Change the package name from LCC-10P-M04 to WNK010 Deleted the words, “Lead Free version”, in the Remarks. Deleted “Marking Format (Lead Free Version)” Deleted “Labeling Sample (Lead Free Version)” Deleted “Evaluation Board Specification” Deleted “EV Board Ordering Information” Updated Package Dimension: Updated to Cypress format
*C	5761100	MASG	06/05/2017	Adapted Cypress new logo.

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PSoC® Solutions

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Technical Support

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