High IP3, 700 MHz to 2800 MHz, Double Balanced, Passive Mixer, IF Amplifier, and Wideband LO Amplifier

Data Sheet

ADL5811

FEATURES

RF frequency: 700 MHz to 2800 MHz continuous
LO frequency: 250 MHz to 2800 MHz, high-side or low-side inject
IF range: 30 MHz to 450 MHz
Power conversion gain of 7.5 dB at 1900 MHz
SSB noise figure of 10.7 dB at 1900 MHz
Input IP3 of 27.5 dBm at 1900 MHz
Input P1dB of 12.7 dBm at 1900 MHz
Typical LO drive of 0 dBm
Single-ended, 50 Ω RF port
Single-ended or balanced LO input port
Single-supply operation: 3.6 V to 5.0 V
Serial port interface control on all functions
Exposed paddle 5 mm × 5 mm, 32-lead LFCSP package

APPLICATIONS

Multiband/multistandard cellular base station receivers
Wideband radio link diversity downconverters
Multimode cellular extenders and broadband receivers

FUNCTIONAL BLOCK DIAGRAM

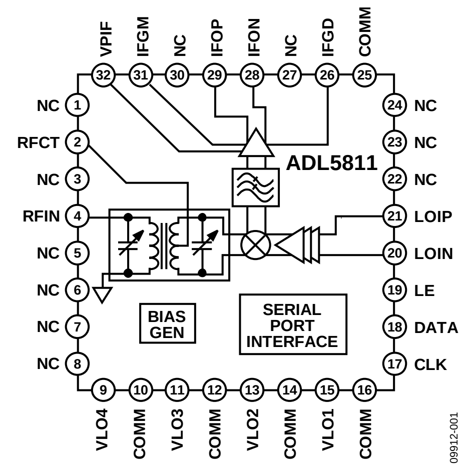

Figure 1.

GENERAL DESCRIPTION

The ADL5811 uses revolutionary new broadband, square wave limiting, local oscillator (LO) amplifiers to achieve an unprecedented radio frequency (RF) bandwidth of 700 MHz to 2800 MHz. Unlike conventional narrow-band sine wave LO amplifier solutions, this permits the LO to be applied either above or below the RF input over an extremely wide bandwidth. Because energy storage elements are not used, the dc current consumption also decreases with decreasing LO frequency.

The ADL5811 uses highly linear, doubly balanced, passive mixer cores along with integrated RF and LO balancing circuits to allow single-ended operation. The ADL5811 incorporates programmable RF baluns, allowing optimal performance over a 700 MHz to 2800 MHz RF input frequency. The balanced passive mixer arrangement provides outstanding LO-to-RF and LO-to-IF leakages, excellent RF-to-IF isolation, and excellent intermodulation performance over the full RF bandwidth.

The balanced mixer cores also provide extremely high input linearity, allowing the device to be used in demanding wideband applications where in-band blocking signals may otherwise result in the degradation of dynamic range. Blocker noise figure performance is comparable to narrow-band passive mixer designs. High linearity IF buffer amplifiers follow the passive mixer cores, yielding typical power conversion gains of 7.5 dB, and can be used with a wide range of output impedances. For low voltage applications, the ADL5811 is capable of operation at voltages down to 3.6 V with substantially reduced current. Two logic bits are provided to power down (<1.5 mA) the circuit when desired.

All features of the ADL5811 are controlled via a 3-wire serial port interface, resulting in optimum performance and minimum external components.

The ADL5811 is fabricated using a BiCMOS high performance IC process. The device is available in a 32-lead, 5mm × 5mm, LFCSP package and operates over a −40°C to +85°C temperature range. An evaluation board is also available.

Rev. A Document Feedback

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REVISION HISTORY

3/2017—Rev. 0 to Rev. A

Changed CP-32-13 to CP-32-20 ... Throughout
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Changes to Ordering Guide ... 28

7/2011—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, RF power = −10 dBm, LO power = 0 dBm, R1 = 910 Ω, Z_O = 50 Ω, optimum SPI settings, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF INPUT INTERFACE					
Return Loss	Tunable to >20 dB broadband via serial port		15		dB
Input Impedance			50		Ω
RF Frequency Range		700		2800	MHz
OUTPUT INTERFACE					
Output Impedance	Differential impedance, f = 200 MHz		260‖1.0		Ω‖pF
IF Frequency Range		30		450	MHz
DC Bias Voltage[1]	Externally generated		V_S		V
LO INTERFACE					
LO Power		−6	0	+10	dBm
Return Loss			13		dB
Input Impedance			50		Ω
LO Frequency Range	Low-side or high-side LO	250		2800	MHz
DYNAMIC PERFORMANCE					
Power Conversion Gain	Including 4:1 IF port transformer and PCB loss		7.5		dB
Voltage Conversion Gain	Z_{SOURCE} = 50 Ω, differential Z_{LOAD} = 200 Ω differential		13.9		dB
SSB Noise Figure			10.7		dB
SSB Noise Figure Under Blocking	5 dBm blocker present ±10 MHz from wanted RF input, LO source filtered		20.7		dB
Input Third-Order Intercept	f_{RF1} = 1900 MHz, f_{RF2} = 1901 MHz, f_{LO} = 1697 MHz, each RF tone at −10 dBm		27.5		dBm
Input Second-Order Intercept	f_{RF1} = 1900 MHz, f_{RF2} = 2000 MHz, f_{LO} = 1697 MHz, each RF tone at −10 dBm		62		dBm
Input 1 dB Compression Point			12.7		dBm
LO-to-IF Output Leakage	Unfiltered IF output		−40		dBm
LO-to-RF Input Leakage			−25		dBm
RF-to-IF Output Isolation			26		dB
IF/2 Spurious	−10 dBm input power		−73		dBc
IF/3 Spurious	−10 dBm input power		−75		dBc
POWER INTERFACE					
Supply Voltage, V_S		3.6	5	5.5	V
Quiescent Current	Resistor programmable IF current		185		mA
Power-Down Current			1.4		mA

[1] Supply voltage must be applied from external circuit through choke inductors.

TIMING CHARACTERISTICS

Low logic level ≤ 0.4 V, and high logic level ≥ 1.4 V.

Table 2. Serial Interface Timing

Parameter	Limit	Unit	Test Conditions/Comments
t_1	20	ns minimum	LE setup time
t_2	10	ns minimum	DATA-to-CLK setup time
t_3	10	ns minimum	DATA-to-CLK hold time
t_4	25	ns minimum	CLK high duration
t_5	25	ns minimum	CLK low duration
t_6	10	ns minimum	CLK-to-LE setup time
t_7	20	ns minimum	LE pulse width

Timing Diagram

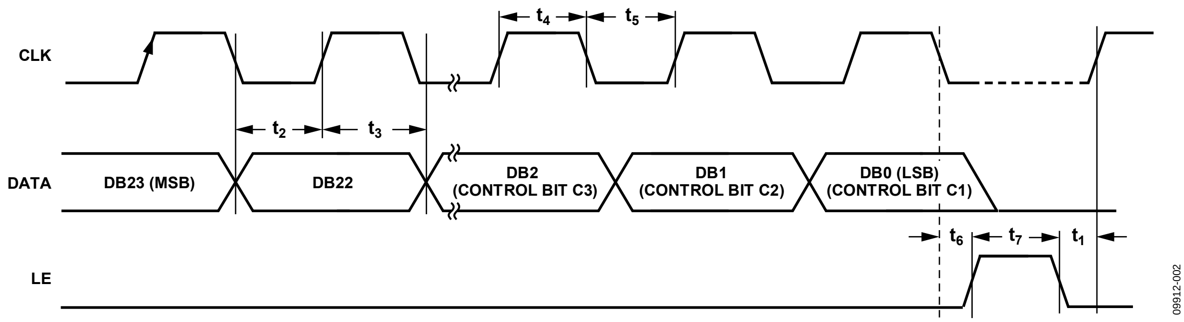


Figure 2. Timing Diagram

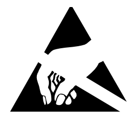
ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage, V_{POS}	5.5 V
CLK, DATA, LE	5.5 V
IF Output Bias	6.0 V
RF Input Power	20 dBm
LO Input Power	13 dBm
Internal Power Dissipation	1.1 W
θ_{JA} (Exposed Paddle Soldered Down)	25°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

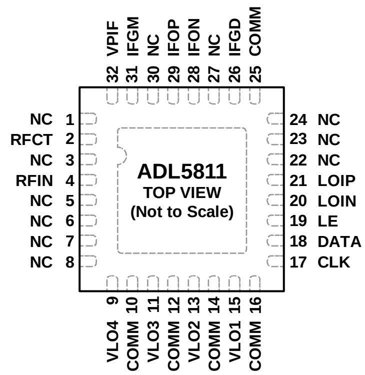
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. CAN BE GROUNDED.
2. EXPOSED PAD MUST BE CONNECTED TO GROUND.

09912-003

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 5 to 8, 22 to 24, 27, 30	NC	No Connect. Can be grounded.
2	RFCT	RF Balun Center Tap (AC Ground).
4	RFIN	RF Input. Should be ac-coupled.
9, 11, 13, 15	VLO4, VLO3, VLO2, VLO1	Positive Supply Voltages for LO Amplifier.
10, 12, 14, 16, 25	COMM	Ground.
17, 18, 19	CLK, DATA, LE	Serial Port Interface Control.
20	LOIN	Ground Return for LO Input.
21	LOIP	LO Input. Should be ac-coupled.
26	IFGD	Supply Return for IF Amplifier. Must be grounded.
28, 29	IFOP, IFON	IF Differential Open-Collector Outputs. Should be pulled up to V_{CC} using external inductors.
31	IFGM	IF Amplifier Bias Control.
32	VPIF	Supply Voltage for IF Amplifier.
	EPAD	Exposed pad must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, RF power = −10 dBm, LO power = 0 dBm, R1 = 910 Ω, Z_O = 50 Ω, optimum SPI settings, unless otherwise noted.

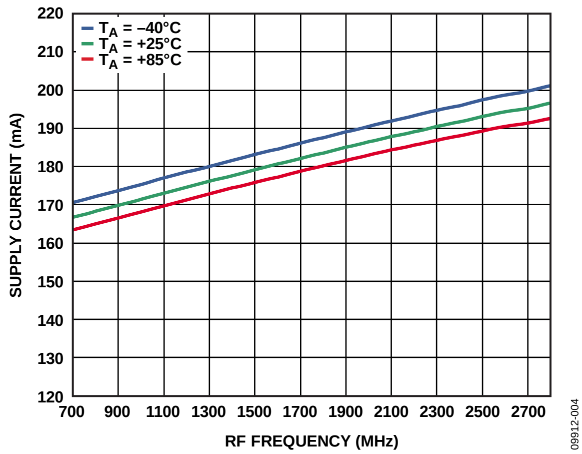


Figure 4. Supply Current vs. RF Frequency

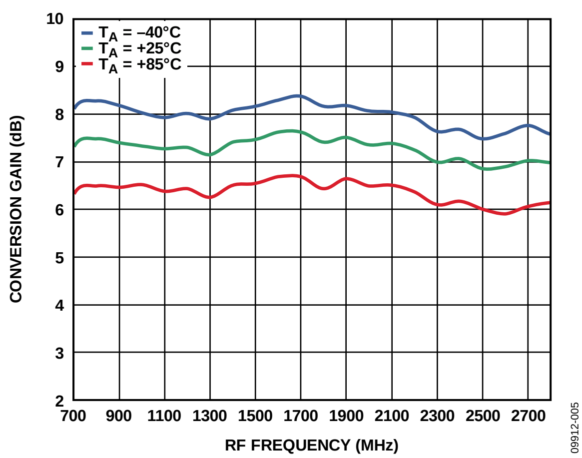


Figure 5. Power Conversion Gain vs. RF Frequency

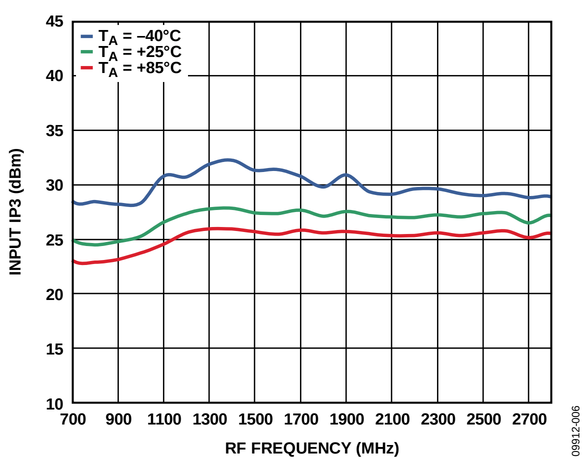


Figure 6. Input IP3 vs. RF Frequency

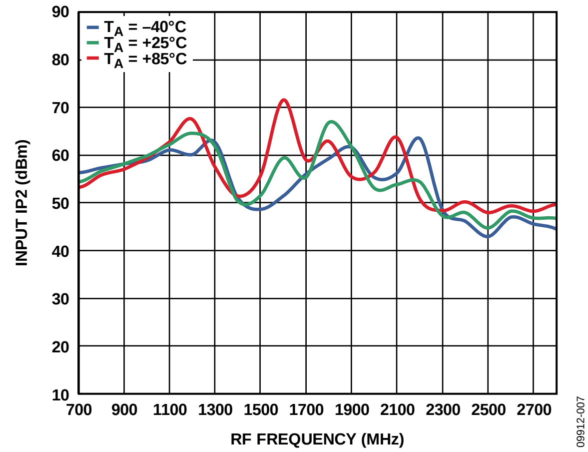


Figure 7. Input IP2 vs. RF Frequency

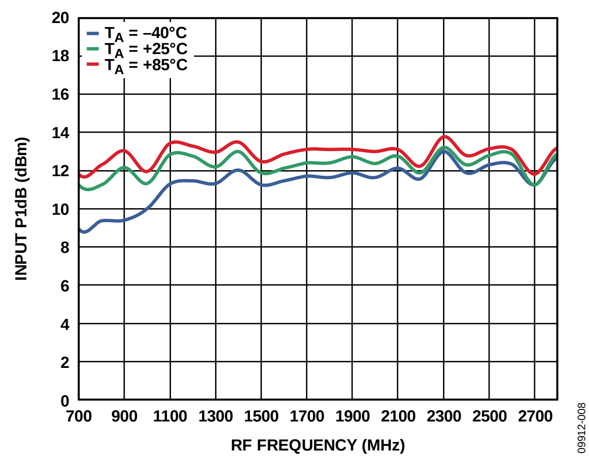


Figure 8. Input P1dB vs. RF Frequency

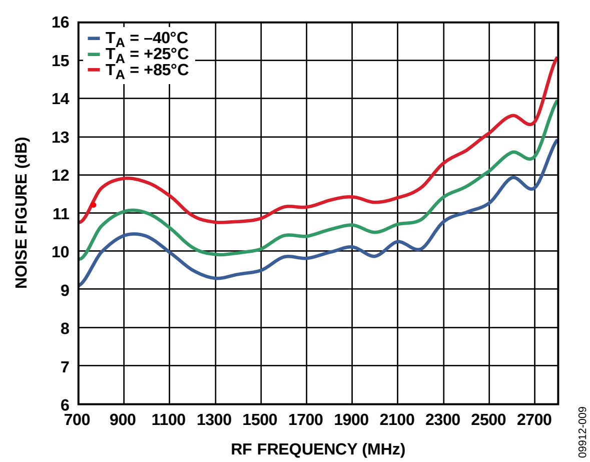


Figure 9. SSB Noise Figure vs. RF Frequency

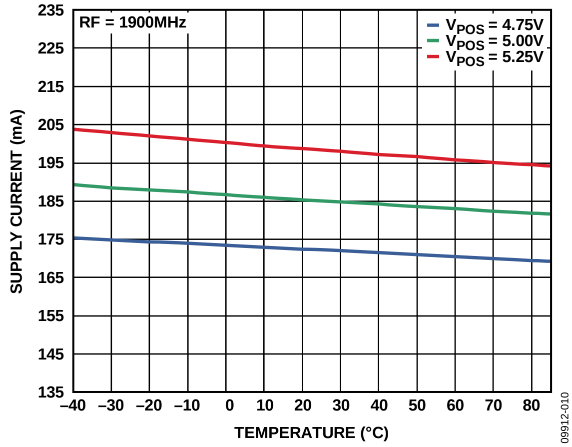


Figure 10. Supply Current vs. Temperature

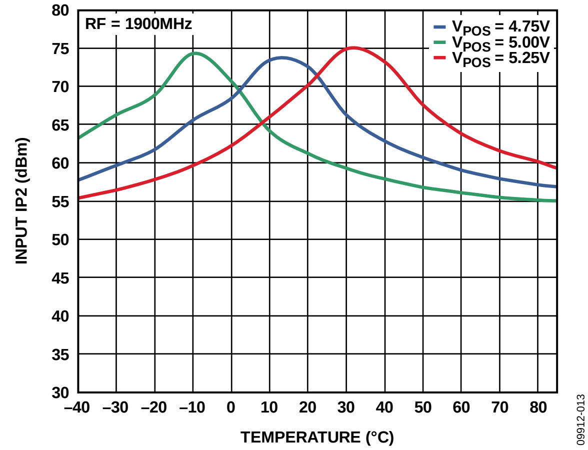


Figure 13. Input IP2 vs. Temperature

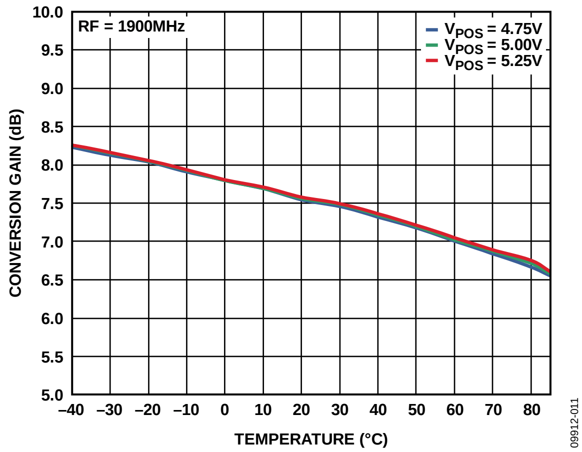


Figure 11. Power Conversion Gain vs. Temperature

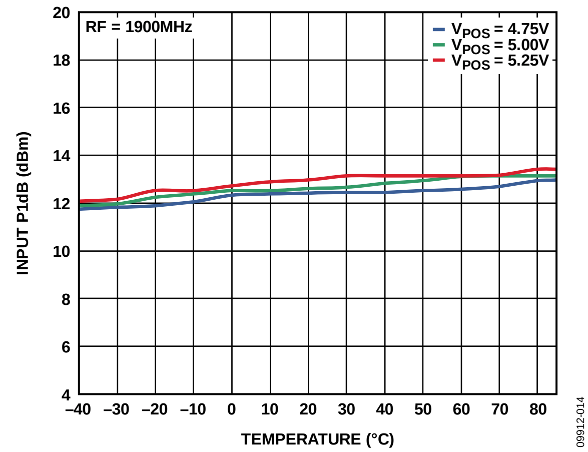


Figure 14. Input P1dB vs. Temperature

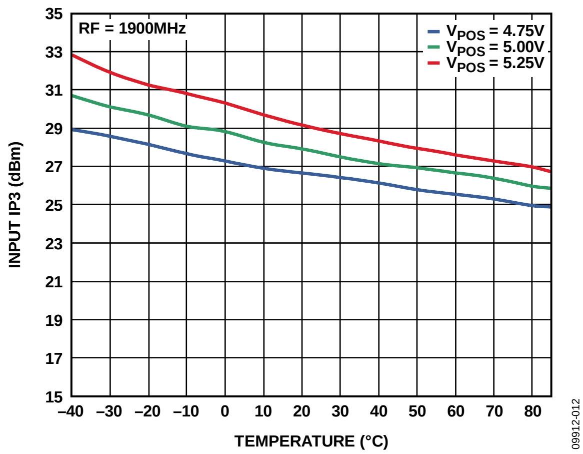


Figure 12. Input IP3 vs. Temperature

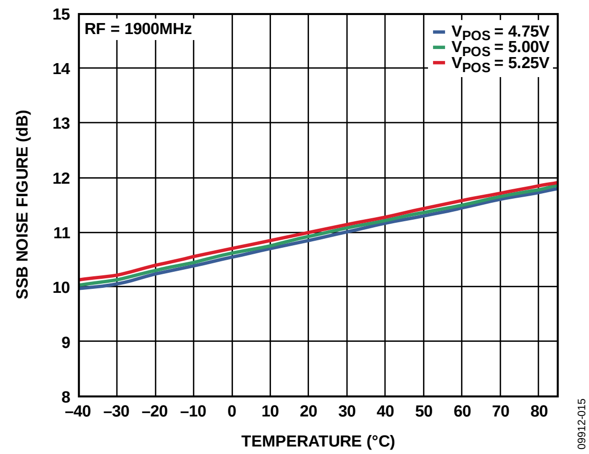


Figure 15. SSB Noise Figure vs. Temperature

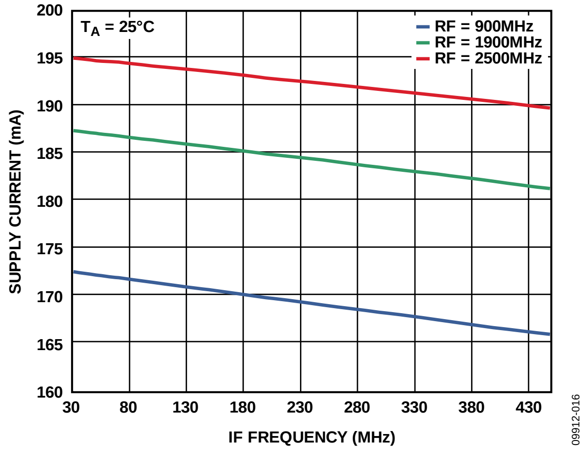


Figure 16. Supply Current vs. IF Frequency

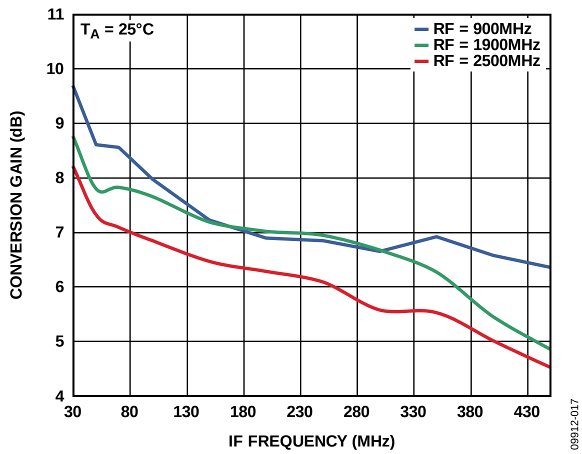


Figure 17. Power Conversion Gain vs. IF Frequency

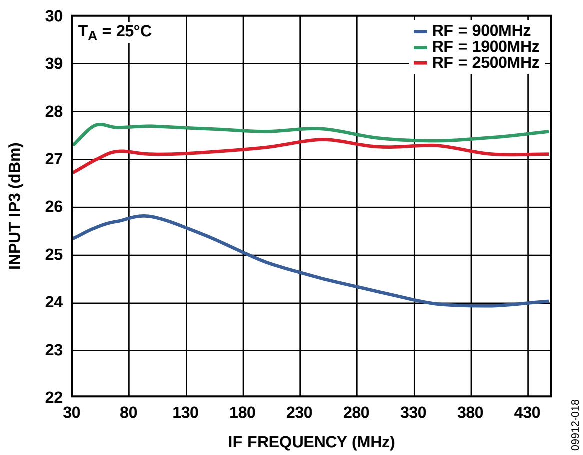


Figure 18. Input IP3 vs. IF Frequency

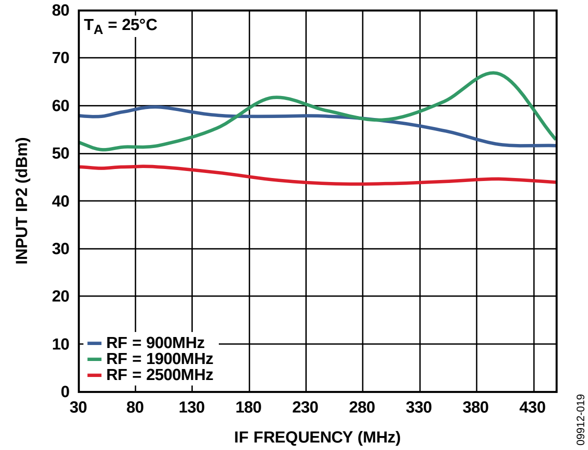


Figure 19. Input IP2 vs. IF Frequency

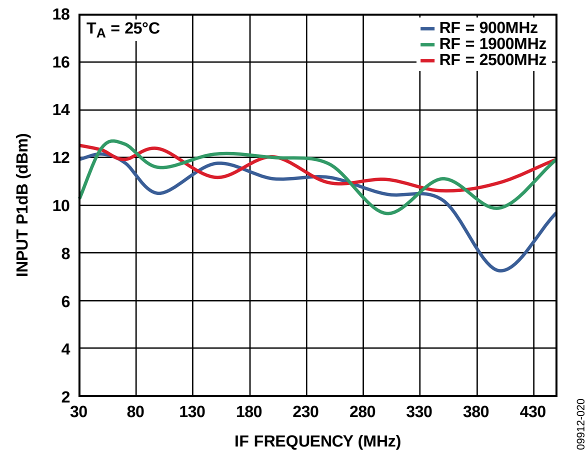


Figure 20. Input P1dB vs. IF Frequency

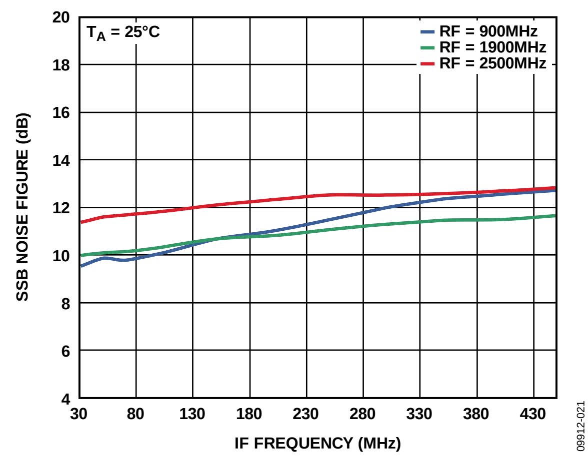


Figure 21. SSB Noise Figure vs. IF Frequency

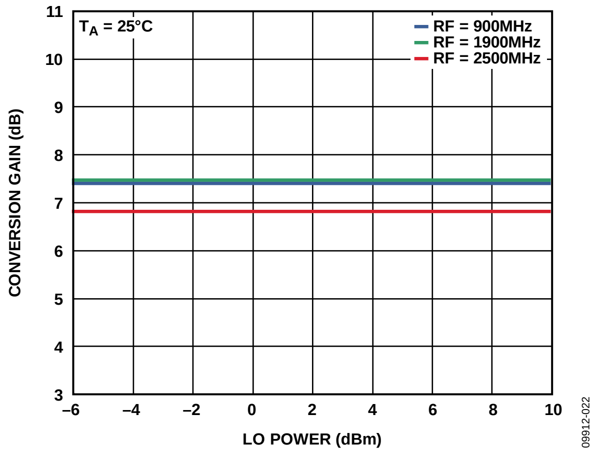


Figure 22. Power Conversion Gain vs. LO Power

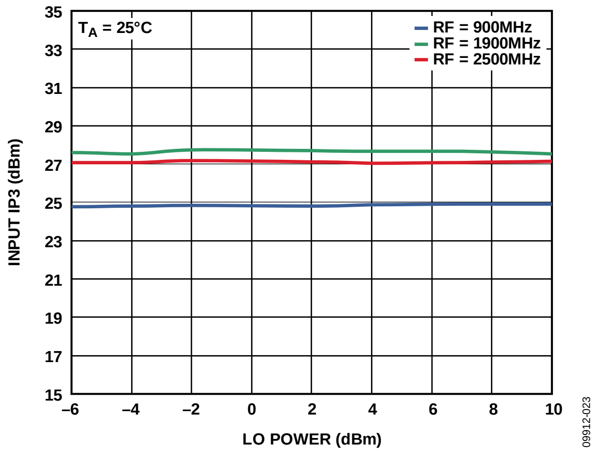


Figure 23. Input IP3 vs. LO Power

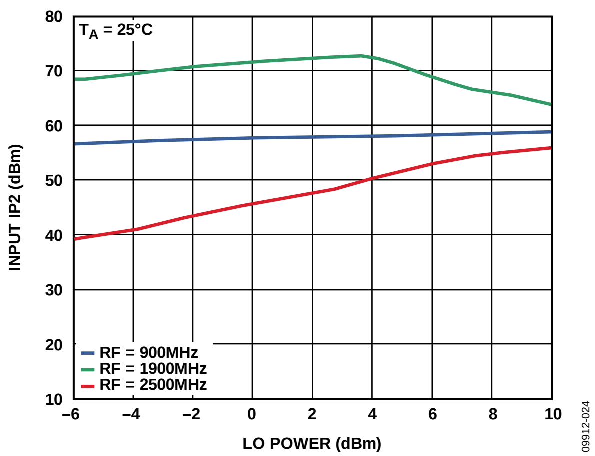


Figure 24. Input IP2 vs. LO Power

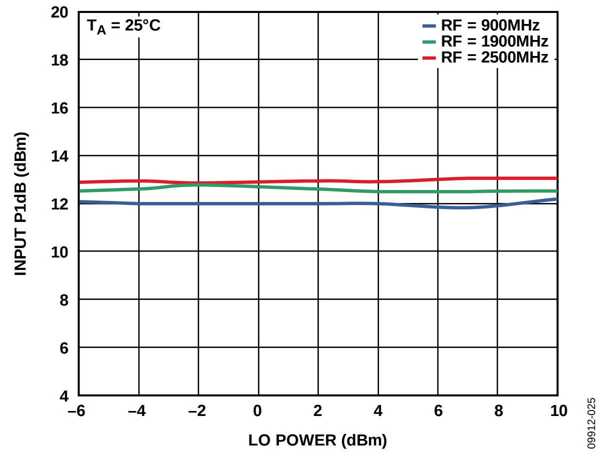


Figure 25. Input P1dB vs. LO Power

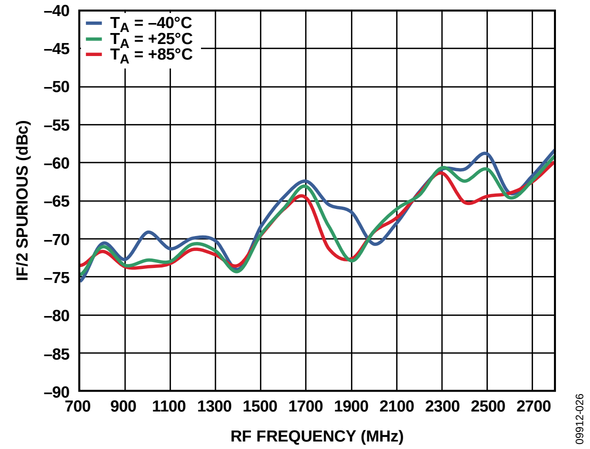


Figure 26. IF/2 Spurious vs. RF Frequency, RF Power = –10 dBm

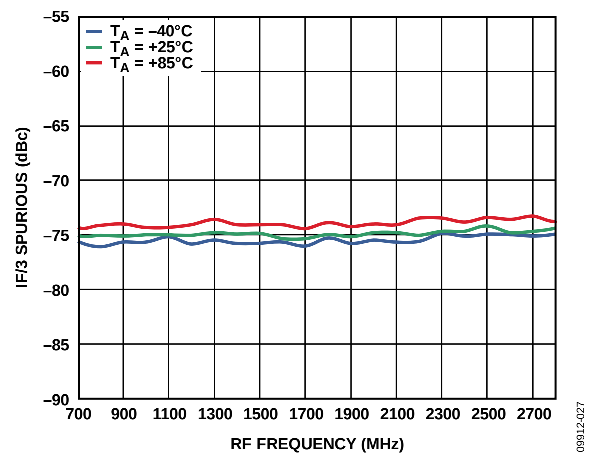


Figure 27. IF/3 Spurious vs. RF Frequency, RF Power = –10 dBm

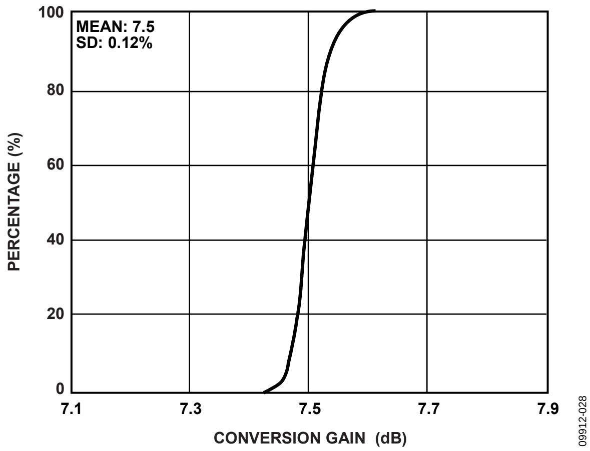


Figure 28. Conversion Gain Distribution

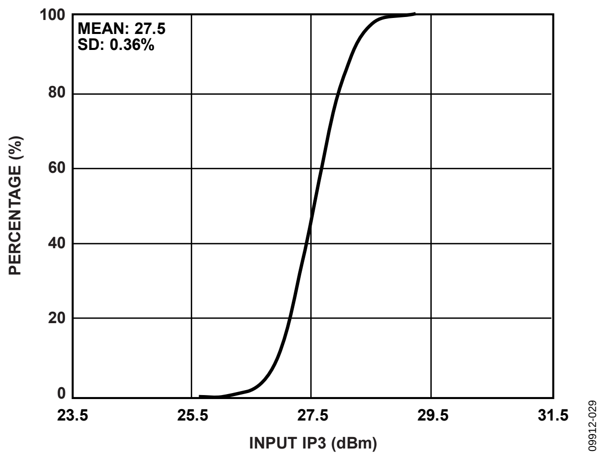


Figure 29. Input IP3 Distribution

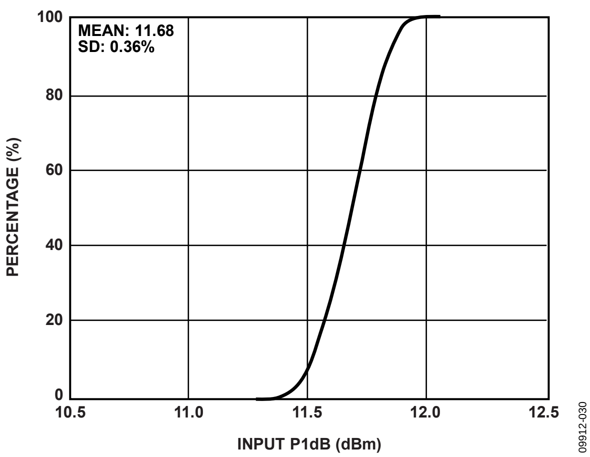


Figure 30. Input P1dB Distribution

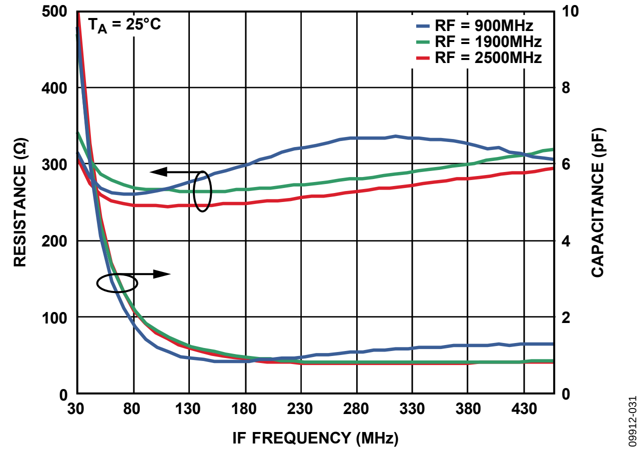


Figure 31. IF Output Impedance (R Parallel C Equivalent)

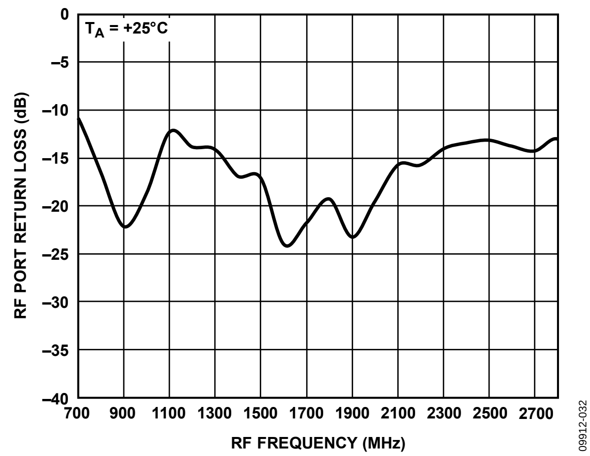


Figure 32. RF Port Return Loss, Fixed IF vs. RF Frequency

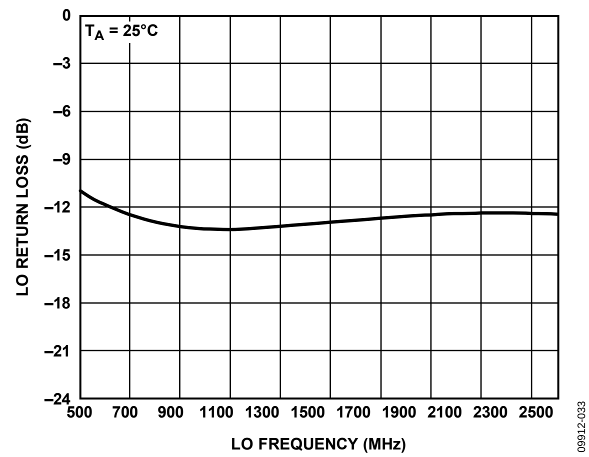


Figure 33. LO Return Loss

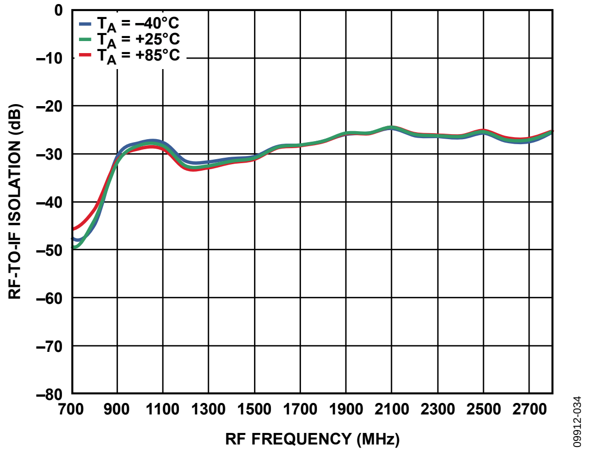


Figure 34. RF-to-IF Isolation vs. RF Frequency

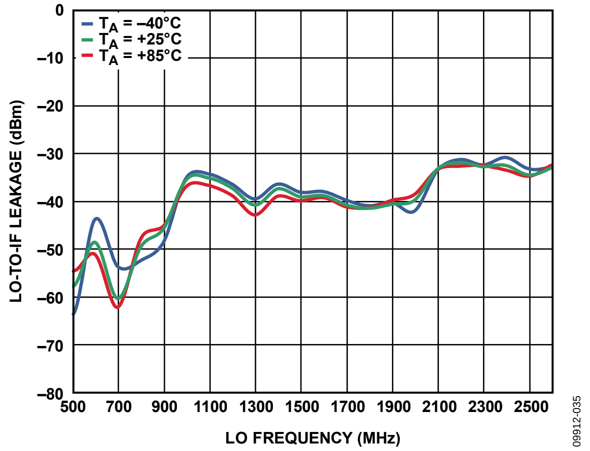


Figure 35. LO-to-IF Leakage vs. LO Frequency

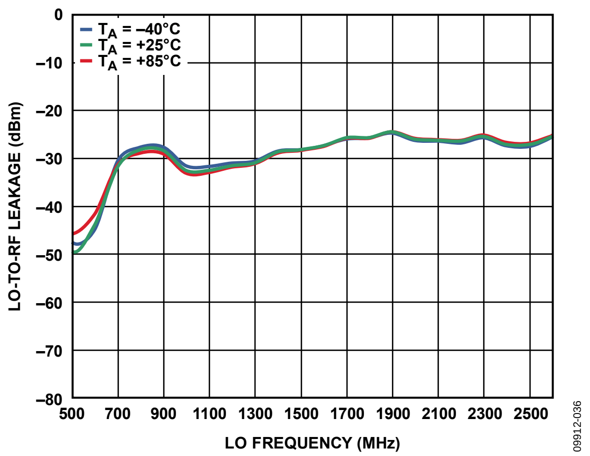


Figure 36. LO-to-RF Leakage vs. LO Frequency

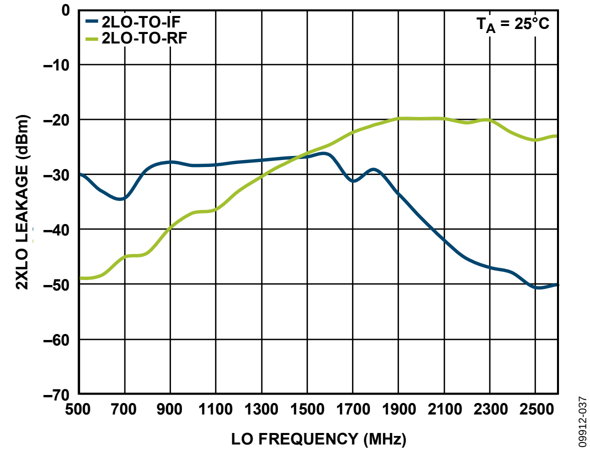


Figure 37. 2XLO Leakage vs. LO Frequency

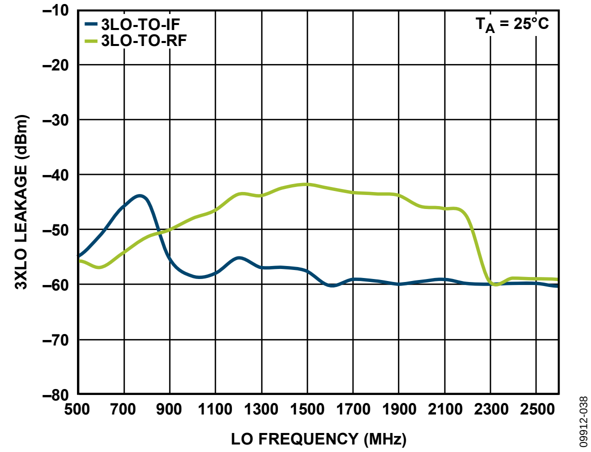


Figure 38. 3XLO Leakage vs. LO Frequency

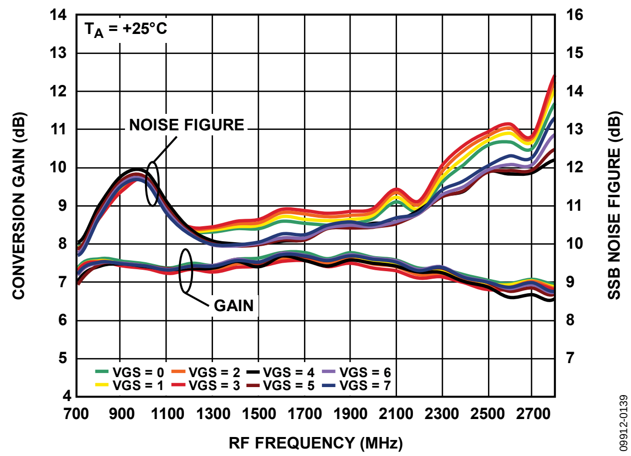


Figure 39. Power Conversion Gain and SSB Noise Figure vs. RF Frequency for All VGS Settings

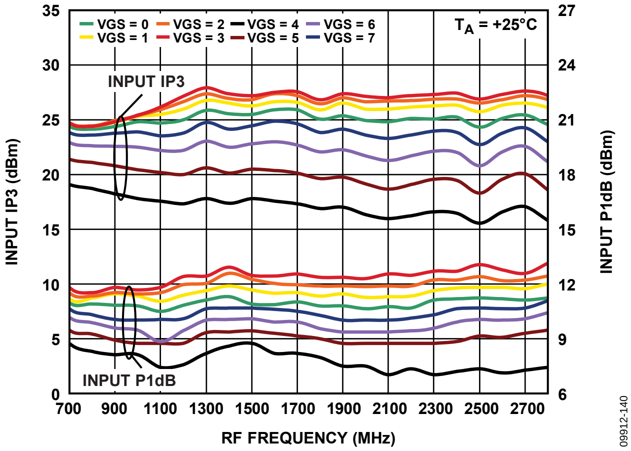


Figure 40. Input IP3 and Input P1dB vs. RF Frequency for All VGS Settings

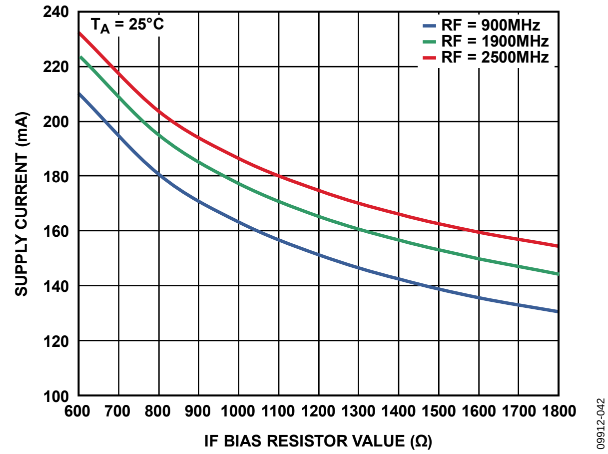


Figure 42. Supply Current vs. IF Bias Resistor Value

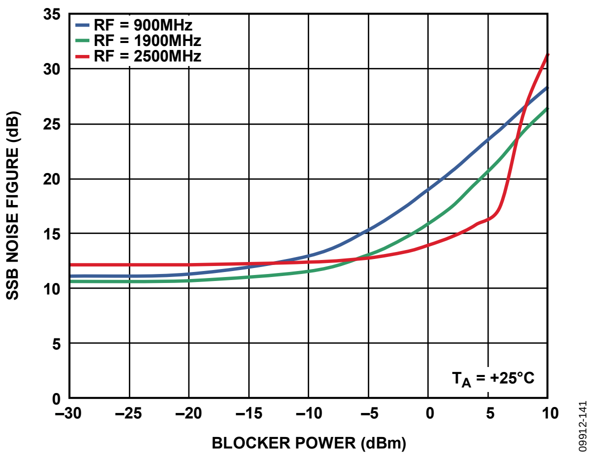


Figure 41. SSB Noise Figure vs. 10 MHz Offset Blocker Level

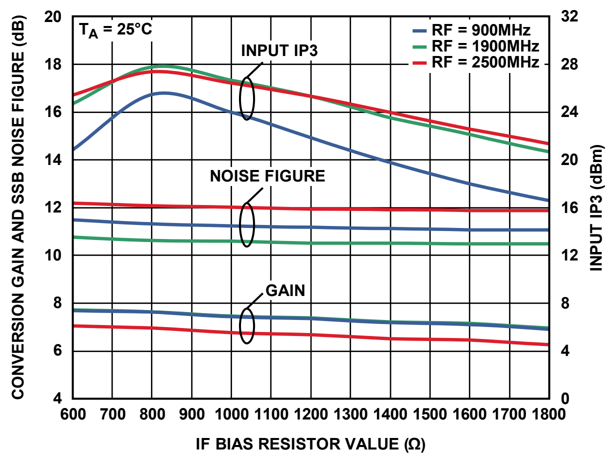


Figure 43. Power Conversion Gain, SSB Noise Figure, and Input IP3 vs. IF Bias Resistor Value

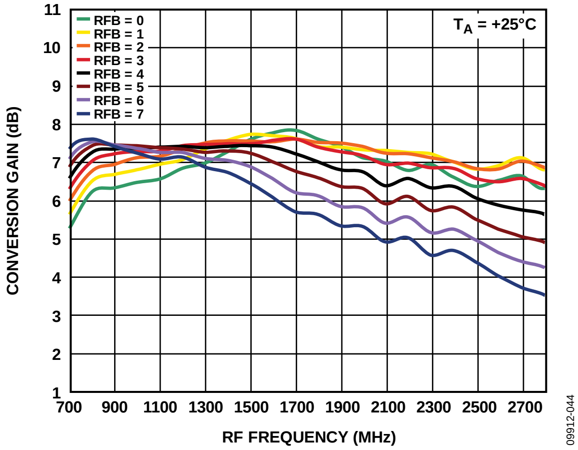


Figure 44. Conversion Gain vs. RF Frequency for All RFB Settings

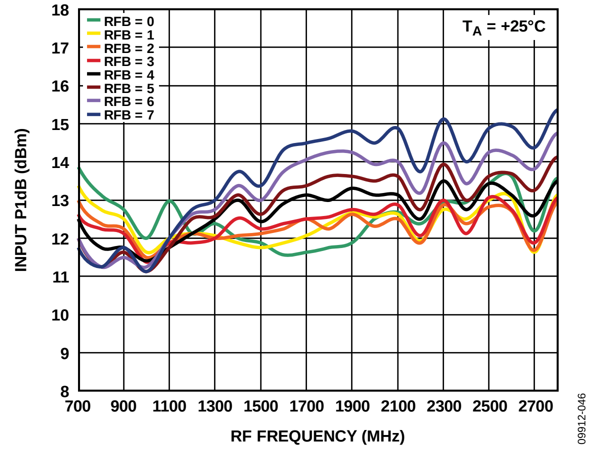


Figure 46. Input P1dB vs. RF Frequency for All RFB Settings

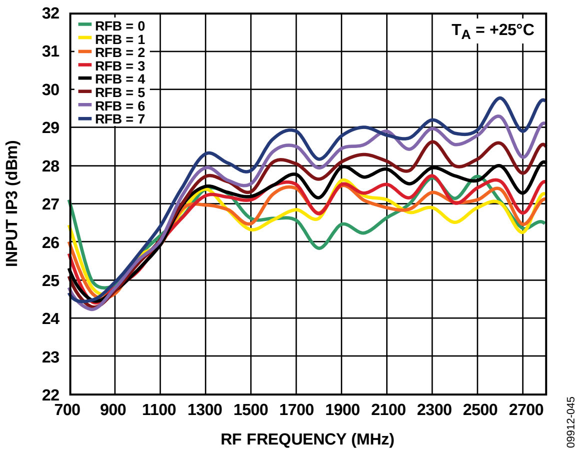


Figure 45. Input IP3 vs. RF Frequency for All RFB Settings

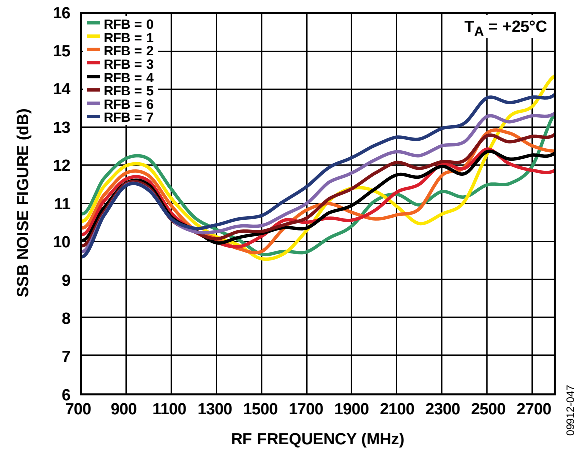


Figure 47. SSB Noise Figure vs. RF Frequency for All RFB Settings

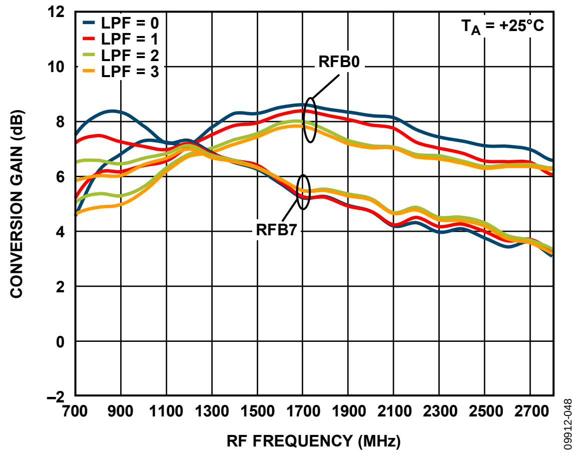


Figure 48. Conversion Gain vs. RF Frequency for All LPF Settings at RFB7 and RFB0

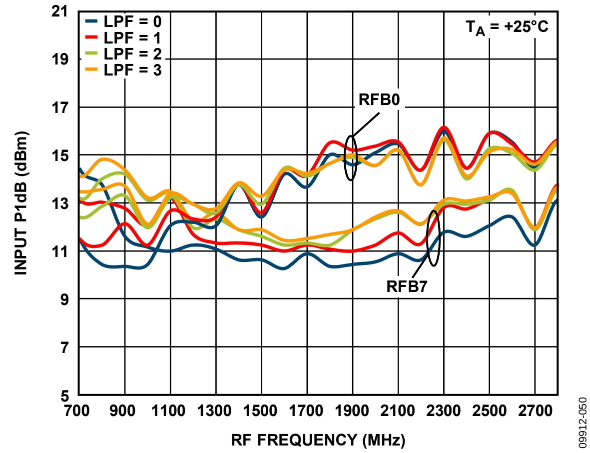


Figure 50. Input P1dB vs. RF Frequency for All LPF Settings at RFB7 and RFB0

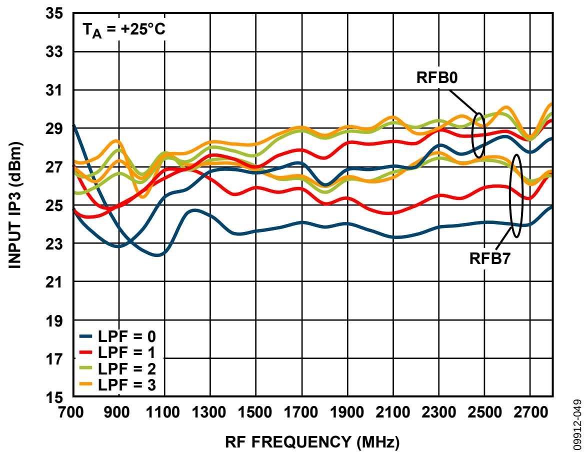


Figure 49. Input IP3 vs. RF Frequency for All LPF Settings at RFB7 and RFB0

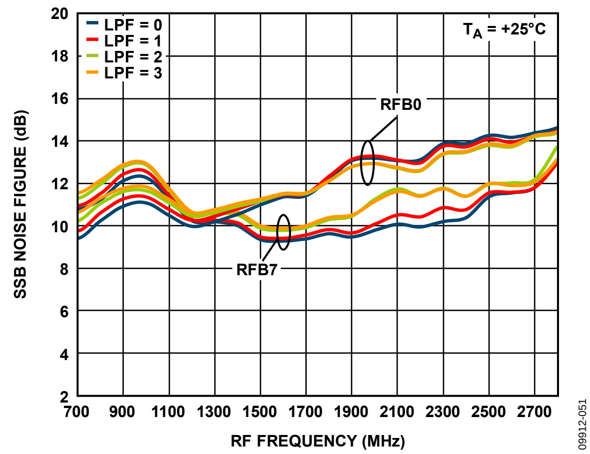


Figure 51. SSB Noise Figure vs. RF Frequency for All LPF Settings at RFB7 and RFB0

3.6 V PERFORMANCE

V_S = 3.6 V, T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, RF power = −10 dBm, LO power = 0 dBm, R1 = 800 Ω, Z_O = 50 Ω, optimum SPI settings, unless otherwise noted.

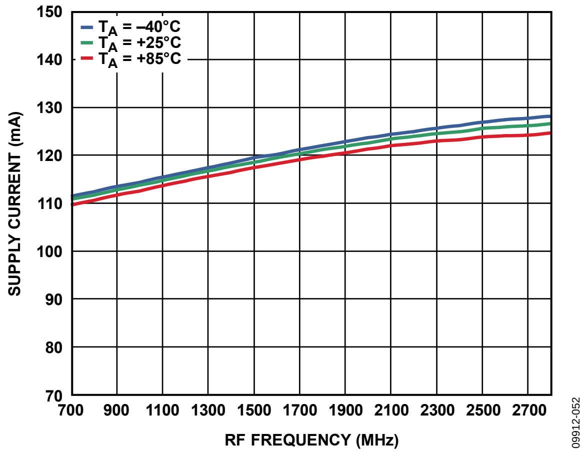


Figure 52. Supply Current vs. RF Frequency at 3.6 V

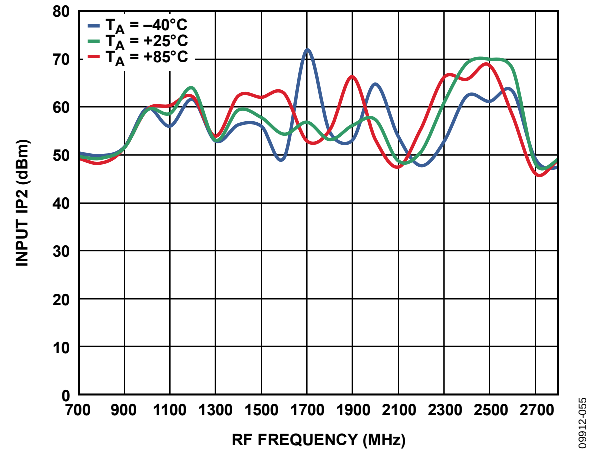


Figure 55. Input IP2 vs. RF Frequency at 3.6 V

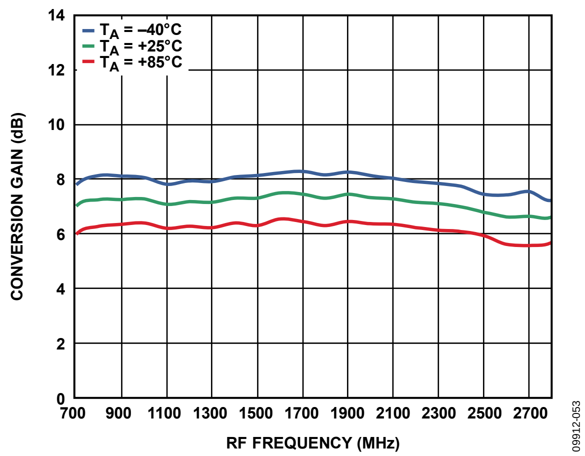


Figure 53. Power Conversion Gain vs. RF Frequency at 3.6 V

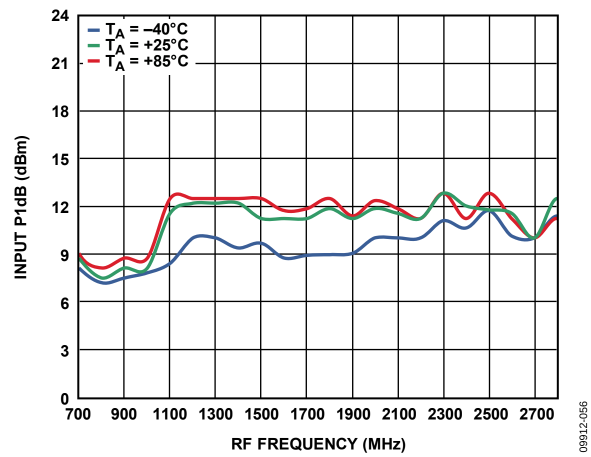


Figure 56. Input P1dB vs. RF Frequency at 3.6 V

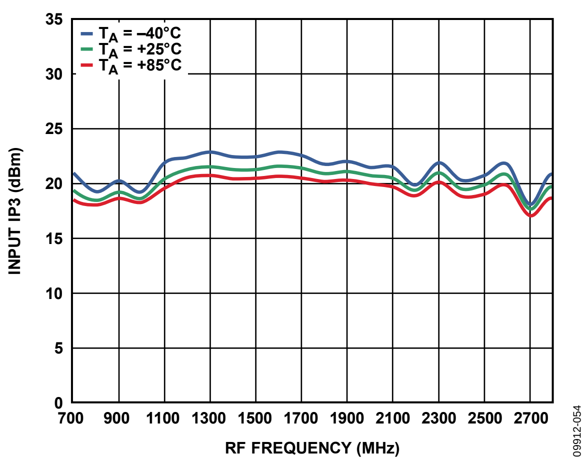


Figure 54. Input IP3 vs. RF Frequency at 3.6 V

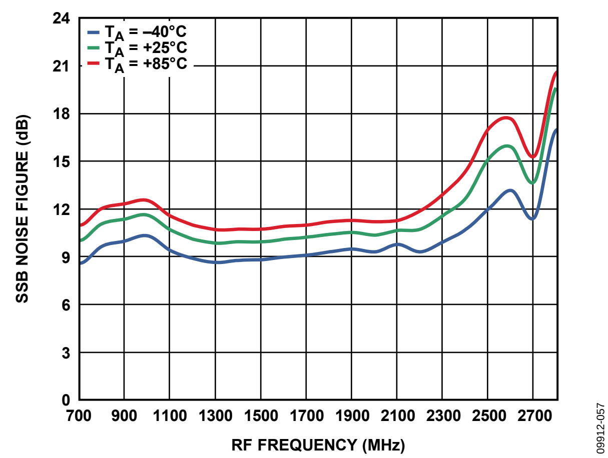


Figure 57. SSB Noise Figure vs. RF Frequency at 3.6 V

SPURIOUS PERFORMANCE

$(N \times f_{RF}) - (M \times f_{LO})$ spur measurements were made using the standard evaluation board. Mixer spurious products are measured in dBc from the IF output power level. Data was measured only for frequencies less than 6 GHz. Typical noise floor of the measurement system = −100 dBm.

5 V Performance

V_S = 5 V, T_A = 25°C, RF power = −10 dBm, LO power = 0 dBm, R1 = 910 Ω, Z_O = 50 Ω, optimum SPI settings, unless otherwise noted.

Table 5. RF = 900 MHz, LO = 697 MHz

		M															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
N	0		−54.2	−31.4	−41.5	−29.4	−58.5	−49.3	−70.5	−52.9							
	1	−37.8	0.0	−38.7	−19.6	−51.6	−38.0	−62.9	−52.4	−70.2	−57.9						
	2	−65.0	−54.4	−69.6	−53.4	−72.5	−82.3	−93.5	−97.4	−93.0	−98.8	<−100	<−100				
	3	−94.0	−86.7	<−100	−91.0	<−100	−95.3	<−100	<−100	<−100	<−100	<−100	<−100	<−100			
	4	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100		
	5	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	6	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	7		<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	8			<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	9					<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	10						<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	11							<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	12								<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	13										<−100	<−100	<−100	<−100	<−100	<−100	<−100
	14											<−100	<−100	<−100	<−100	<−100	<−100
	15												<−100	<−100	<−100	<−100	<−100

Table 6. RF = 1900 MHz, LO = 1697 MHz

		M															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
N	0		−34.9	−30.7	−66.0												
	1	−33.2	0.0	−56.6	−51.3	−77.8											
	2	−75.0	−78.5	−71.5	−85.2	−80.3	<−100										
	3	<−100	<−100	<−100	−89.5	−94.8	<−100	<−100									
	4		<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100							
	5				<−100	<−100	<−100	<−100	<−100	<−100	<−100						
	6					<−100	<−100	<−100	<−100	<−100	<−100	<−100					
	7						<−100	<−100	<−100	<−100	<−100	<−100	<−100				
	8							<−100	<−100	<−100	<−100	<−100	<−100	<−100			
	9								<−100	<−100	<−100	<−100	<−100	<−100	<−100		
	10									<−100	<−100	<−100	<−100	<−100	<−100	<−100	
	11										<−100	<−100	<−100	<−100	<−100	<−100	<−100
	12											<−100	<−100	<−100	<−100	<−100	<−100
	13													<−100	<−100	<−100	<−100
	14														<−100	<−100	<−100
	15															<−100	<−100

Table 7. RF = 2500 MHz, LO = 2297 MHz

		M															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
N	0		−28.6	−45.7													
	1	−32.5	0.0	−53.0	−52.4												
	2	−91.2	−82.8	−60.5	−80.8	−97.3											
	3		<−100	<−100	−87.7	<−100	<−100										
	4			<−100	<−100	<−100	<−100	<−100									
	5				<−100	<−100	<−100	<−100	<−100	<−100							
	6					<−100	<−100	<−100	<−100	<−100	<−100						
	7							<−100	<−100	<−100	<−100	<−100					
	8								<−100	<−100	<−100	<−100	<−100				
	9									<−100	<−100	<−100	<−100	<−100			
	10										<−100	<−100	<−100	<−100	<−100		
	11											<−100	<−100	<−100	<−100	<−100	
	12												<−100	<−100	<−100	<−100	<−100
	13													<−100	<−100	<−100	<−100
	14														<−100	<−100	<−100
	15															<−100	<−100

3.6 V Performance

V_S = 3.6 V, T_A = 25°C, RF power = −10 dBm, LO power = 0 dBm, R1 = 800 Ω, Z_O = 50 Ω, optimum SPI settings, unless otherwise noted.

Table 8. RF = 900 MHz, LO = 697 MHz

		M															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
N	0		−45.5	−35.1	−44.1	−30.2	−49.9	−48.7	−66.6	−66.5							
	1	−41.0	0.0	−37.3	−18.9	−54.8	−40.4	−62.4	−53.2	−73.0	−66.8						
	2	−59.2	−54.7	−78.2	−54.8	−62.8	−83.1	−78.3	−96.1	−79.5	−96.2	−96.2	<−100				
	3	−90.0	−81.9	<−100	−73.9	−89.6	−79.4	<−100	−95.3	<−100	<−100	<−100	<−100	<−100			
	4	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100		
	5	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	6	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	7		<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	8			<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	9					<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	10						<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	11							<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	12								<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	13										<−100	<−100	<−100	<−100	<−100	<−100	<−100
	14											<−100	<−100	<−100	<−100	<−100	<−100
	15												<−100	<−100	<−100	<−100	<−100

Table 9. RF = 1900 MHz, LO = 1697 MHz

		M															
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
N	**0**		−46.6	−30.5	−78.5												
	1	−33.4	0.0	−57.0	−53.8	−79.5											
	2	−68.9	−77.2	−69.2	−72.8	−75.2	<−100										
	3	<−100	<−100	<−100	−74.4	−94.0	<−100	<−100									
	4		<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100							
	5				<−100	<−100	<−100	<−100	<−100	<−100	<−100						
	6					<−100	<−100	<−100	<−100	<−100	<−100	<−100					
	7						<−100	<−100	<−100	<−100	<−100	<−100	<−100				
	8							<−100	<−100	<−100	<−100	<−100	<−100	<−100			
	9								<−100	<−100	<−100	<−100	<−100	<−100	<−100		
	10									<−100	<−100	<−100	<−100	<−100	<−100	<−100	
	11										<−100	<−100	<−100	<−100	<−100	<−100	<−100
	12											<−100	<−100	<−100	<−100	<−100	<−100
	13													<−100	<−100	<−100	<−100
	14														<−100	<−100	<−100
	15															<−100	<−100

Table 10. RF = 2500 MHz, LO = 2297 MHz

		M															
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
N	**0**		−30.0	−51.1													
	1	−32.1	0.0	−53.6	−51.7												
	2	−89.0	−78.0	−65.5	−72.9	−88.2											
	3		<−100	<−100	−73.5	<−100	<−100										
	4			<−100	<−100	<−100	<−100	<−100									
	5				<−100	<−100	<−100	<−100	<−100	<−100							
	6					<−100	<−100	<−100	<−100	<−100	<−100						
	7							<−100	<−100	<−100	<−100	<−100					
	8								<−100	<−100	<−100	<−100	<−100				
	9									<−100	<−100	<−100	<−100	<−100			
	10										<−100	<−100	<−100	<−100	<−100		
	11											<−100	<−100	<−100	<−100	<−100	
	12												<−100	<−100	<−100	<−100	<−100
	13													<−100	<−100	<−100	<−100
	14														<−100	<−100	<−100
	15															<−100	<−100

CIRCUIT DESCRIPTION

The ADL5811 consists of two primary components: the RF subsystem and the LO subsystem. The combination of design, process, and packaging technology allows the functions of these subsystems to be integrated into a single die, using mature packaging and interconnection technologies to provide a high performance device with excellent electrical, mechanical, and thermal properties. The wideband frequency response and flexible frequency programming simplifies the receiver design, saves on-board space, and minimizes the need for external components.

The RF subsystem consists of an integrated, tunable, low loss RF balun; a double balanced, passive MOSFET mixer; a tunable sum termination network; and an IF amplifier.

The LO subsystem consists of a multistage limiting LO amplifier. The purpose of the LO subsystem is to provide a large, fixed amplitude, balanced signal to drive the mixer independent of the level of the LO input. A block diagram of the device is shown in Figure 58.

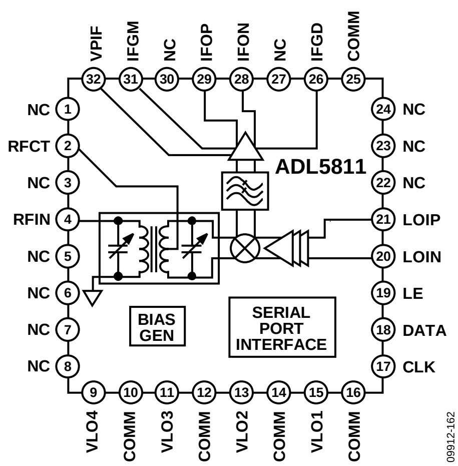


Figure 58. Block Diagram

RF SUBSYSTEM

The single-ended, 50 Ω RF input is internally transformed to a balanced signal using a tunable, low loss, unbalanced-to-balanced (balun) transformer. This transformer is made possible by an extremely low loss metal stack, which provides both excellent balance and dc isolation for the RF port. Although the port can be dc connected, it is recommended that a blocking capacitor be used to avoid running excessive dc current through the part. The RF balun can easily support an RF input frequency range of 700 MHz to 2800 MHz. This balun is tuned over the frequency range by SPI controlled switched capacitor networks at the input and output of the RF balun.

The resulting balanced RF signal is applied to a passive mixer that commutates the RF input in accordance with the output of the LO subsystem. The passive mixer is essentially a balanced, low loss switch that adds minimum noise to the frequency translation. The only noise contribution from the mixer is due to the resistive loss of the switches, which is in the order of a few ohms.

Because the mixer is inherently broadband and bidirectional, it is necessary to properly terminate all idler (M × N product) frequencies generated by the mixing process. Terminating the mixer avoids the generation of unwanted intermodulation products and reduces the level of unwanted signals at the input of the IF amplifier, where high peak signal levels can compromise the compression and intermodulation performance of the system. This termination is accomplished by the addition of a programmable low-pass filter network between the IF amplifier and the mixer and in the feedback elements in the IF amplifier.

The IF amplifier is a balanced feedback design that simultaneously provides the desired gain, noise figure, and input impedance that is required to achieve the overall performance. The balanced open-collector output of the IF amplifier, with an impedance modified by the feedback within the amplifier, permits the output to be connected directly to a high impedance filter, a differential amplifier, or an analog-to-digital converter (ADC) input while providing optimum second-order intermodulation suppression. The differential output impedance of the IF amplifier is approximately 200 Ω. If operation in a 50 Ω system is desired, the output can be transformed to 50 Ω by using a 4:1 transformer or an LC impedance matching network.

The intermodulation performance of the design is generally limited by the IF amplifier. The IP3 performance can be optimized by adjusting the low-pass filter between the mixer and the IF amplifier. Further optimization can be made by adjusting the IF current with an external resistor. Figure 42 and Figure 43 illustrate how various IF resistors affect the performance with a 5 V supply. Additionally, dc current can be saved by increasing the IF resistor. It is permissible to reduce the IF amplifier's dc supply voltage to as low as 3.3 V, further reducing the dissipated power of the part. (Note that no performance enhancement is obtained by reducing the value of these resistors, and excessive dc power dissipation may result.)

Because the mixer is bidirectional, the tuning of the RF and IF ports is linked and it is possible for the user to optimize gain, noise figure, IP3, and impedance match via the SPI. This feature permits high performance operation and is achieved entirely using SPI control. Additionally, the performance of the mixer can be improved by setting the optimum gate voltage on the passive mixer, which is also controlled by the SPI to enable optimum performance of the part. See the Applications Information section for examples of this tuning.

LO SUBSYSTEM

The LO amplifier is designed to provide a large signal level to the mixer to obtain optimum intermodulation and compression performance. The resulting LO amplifier provides very high performance over a wide range of LO input frequencies.

The ideal waveshape for switching the passive mixer is a square wave at the LO frequency to cause the mixer to switch through its resistive region (from on to off and off to on) as rapidly as possible. While it has always been possible to generate such a square wave, the amount of dc current required to generate a large amplitude square wave at high frequencies has made it impractical to create such a mixer. Novel circuitry within the ADL5811 permits the generation of a near-square wave output at frequencies of up to 2800 MHz with dc current that compares favorably with that employed by narrow-band passive mixers.

The input stages of the LO amplifier provide common-mode rejection, permitting the LO input to be driven either single ended or balanced. For a single-ended input, either LOIP or LOIN can be grounded. It is desirable to dc block the LO inputs to avoid damaging the part by the accidental application of a large dc voltage to the part. In addition, the LO inputs are internally dc blocked.

Because the LO amplifier is inherently wideband, the ADL5811 can be driven with either high-side or low-side LO by simply setting the optimum RF balun and LPF inputs to the SPI.

The LO amplifier converts a variable level, single or balanced input signal (−6 dBm to +10 dBm) to a hard voltage limited, balanced signal internally to drive the mixer. Excellent performance can be obtained with a 0 dBm input level; however, the circuit continues to function at considerably lower levels of LO input power.

The performance of this amplifier is critical in achieving a high intercept passive mixer without degrading the noise floor of the system. This is a critical requirement in an interferer rich environment, such as cellular infrastructure, where blocking interferers can limit mixer performance. Blocking dynamic range can benefit from a higher level of LO drive, which pushes the LO amplifier stages harder into compression and causes them to switch harder and to limit the small signal gain of the chain. Both of these conditions are beneficial to low noise figure under blocking. NF under blocking can be improved several decibels for LO input power levels above 0 dBm.

The LO amplifier topology inherently minimizes the dc current based on the LO operating voltage and the LO operating frequency. It is permissible to reduce the LO supply voltage down as low as 3.6 V, which drops the dc current rapidly. The mixer dynamic range varies accordingly with the LO supply voltage. No external biasing resistor is required for optimizing the LO amplifier.

In addition, the ADL5811 has a power-down mode that can be used with any supply voltage applied to the part.

All of the SPI inputs are designed to work with any logic family that provides a Logic 0 input level of less than 0.4 V and a Logic 1 input level that exceeds 1.4 V.

All pins, including the RF pins, are ESD protected and have been tested up to a level of 2000 V HBM and 1250 V CDM.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

The ADL5811 mixer is designed to downconvert radio frequencies (RF) primarily between 700 MHz and 2800 MHz to lower intermediate frequencies (IF) between 30 MHz and 450 MHz. Figure 59 depicts the basic connections of the mixer. It is recommended to ac couple RF and LO input ports to prevent nonzero dc voltages from damaging the RF balun or LO input circuit. A RFIN capacitor value of 22 pF is recommended.

IF PORT

The mixer differential IF interface requires pull-up choke inductors to bias the open-collector outputs and to set the output match. The shunting impedance of the choke inductors used to couple dc current into the IF amplifier should be selected to provide the desired output return loss.

The real part of the output impedance is approximately 200 Ω, as seen in Figure 31, which matches many commonly used SAW filters without the need for a transformer. This results in a voltage conversion gain that is approximately 6 dB higher than the power conversion gain. When a 50 Ω output impedance is needed, use a 4:1 impedance transformer, as shown in Figure 59.

BIAS RESISTOR SELECTION

An external resistor, R1, is used to adjust the bias current of the integrated amplifier at the IF terminal. It is necessary to have a sufficient amount of current to bias both the internal IF amplifier to optimize dc current vs. optimum input IP3 performance. Figure 42 and Figure 43 provide the reference for the bias resistor selection when lower power consumption is considered at the expense of conversion gain and input IP3 performance.

VGS PROGRAMMING

The ADL5811 allows programmability for internal gate-to-source voltages for optimizing mixer performance over the desired frequency bands. The ADL5811 defaults the VGS setting to 0. Power conversion gain, input IP3, NF, and input P1dB can be optimized, as shown in Figure 39 and Figure 40.

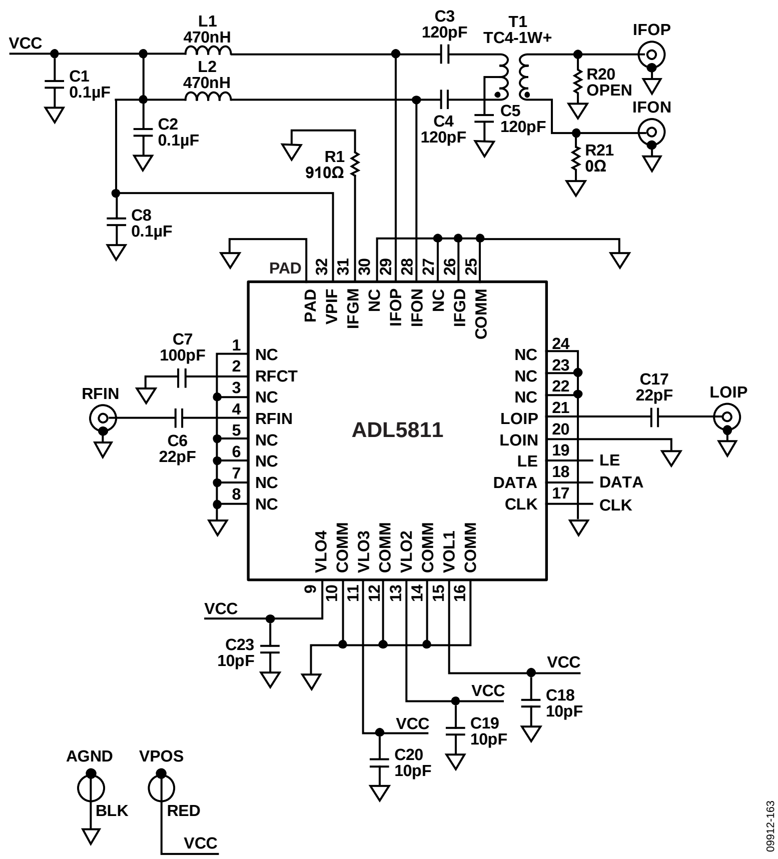


Figure 59. Basic Connections

LOW-PASS FILTER PROGRAMMING

The ADL5811 allows programmability for the low-pass filter terminating the mixer output. This filter helps to block sum term mixing products at the expense of some noise figure and gain and can significantly increase input IP3. The ADL5811 defaults the LPF setting to 0. Power conversion gain, input IP3, NF, and input P1dB can be optimized, as shown in Figure 48 to Figure 51.

RF BALUN PROGRAMMING

The ADL5811 allows programmability for the RF balun by allowing capacitance to be switched into both the input and the output, which allows the balun to be tuned to cover the entire frequency band (700 MHz to 2800 MHz). Under most circumstances, the input and output can be tuned together though sometimes it may be advantageous for matching reasons to tune them separately. The ADL5811 defaults the RFB setting to 0. Power conversion gain, input IP3, NF, and input P1dB can be optimized, as shown in Figure 44 to Figure 47.

REGISTER STRUCTURE

Figure 60 illustrates the register map of the ADL5811. The ADL5811 only uses Register 5. Because of this, set all of the control bits to 5. When set to 0, the ENBL bit, DB7, enables the part. By setting this bit to 1, the mixer is powered down. The RFB IN CAP DAC and RFB OUT CAP DAC bits are used to tune the RF balun. In most cases, they are tuned together with the higher settings, 7, tuning for the low frequencies, and with the lower settings, 0, tuning for the high frequencies. There are times where it becomes advantageous to tune the input and output of the RF balun separately and that ability is provided.

The LPF bits control the low-pass filter settings at the IF output. The ability to tune the low-pass filter allows some trade-off between gain, noise figure, and input IP3 with higher settings, 7, providing higher input IP3 at the cost of some gain and noise figure, and lower settings, 0, providing higher gain and lower NF at the cost of lower input IP3. The VGS bits control the VGS settings of the mixer core and allow further tuning of the device.

Table 11 lists the optimum settings characterized for each frequency band. All register bits default to 0.

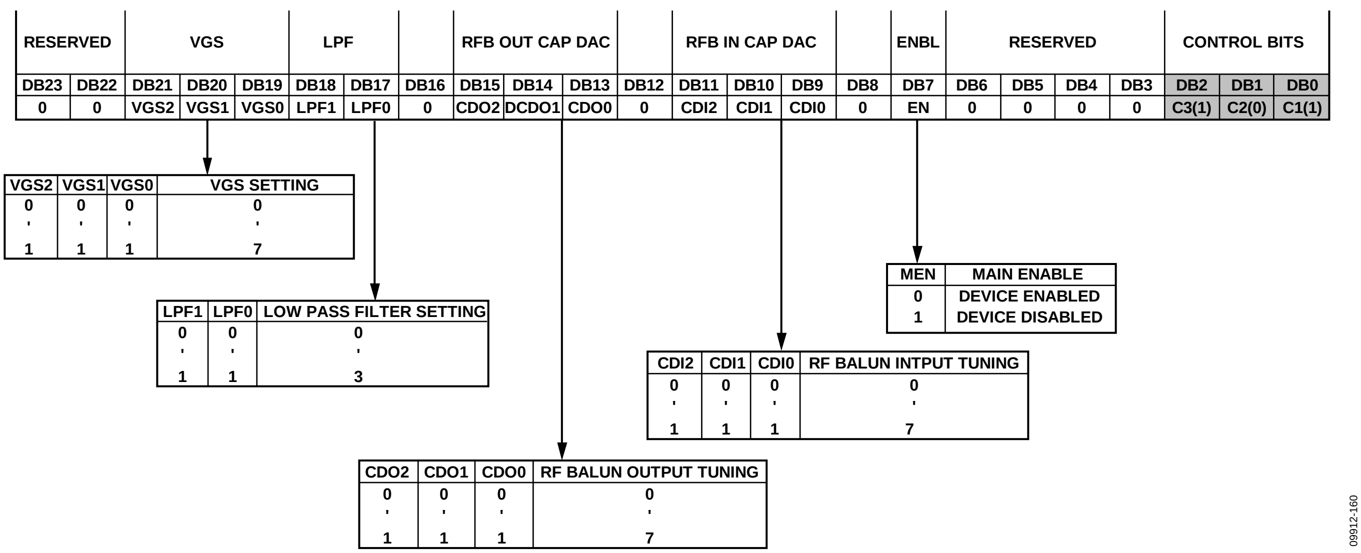


Figure 60. ADL5811 Register Maps

Table 11. Optimum Settings

RF Frequency (MHz)	LO Frequency (MHz)	VGS	LPF	RFB OUT CAP DAC	RFB IN CAP DAC
700	497	3	1	7	7
800	597	1	1	6	6
900	697	2	1	6	6
1000	797	1	1	4	4
1100	897	3	1	7	7
1200	997	3	3	5	5
1300	1097	3	3	5	5
1400	1197	3	3	4	4
1500	1297	3	3	4	4
1600	1397	3	3	3	3
1700	1497	3	3	3	3
1800	1597	3	3	3	3
1900	1697	3	3	2	2
2000	1797	3	3	2	2
2100	1897	3	3	1	1
2200	1997	2	3	2	2
2300	2097	3	2	2	2
2400	2197	2	2	2	2
2500	2297	3	3	1	1
2600	2397	3	2	2	2
2700	2497	1	2	2	2
2800	2597	3	2	1	1

EVALUATION BOARD

An evaluation board is available for the ADL5811. The standard evaluation board schematic is presented in Figure 61. The USB interface circuitry schematic is presented in Figure 64. The evaluation board layout is shown in Figure 62 and Figure 63.

The evaluation board is fabricated using Rogers® 3003 material. Table 12 details the configuration for the mixer characterization. The evaluation board software is available on www.analog.com.

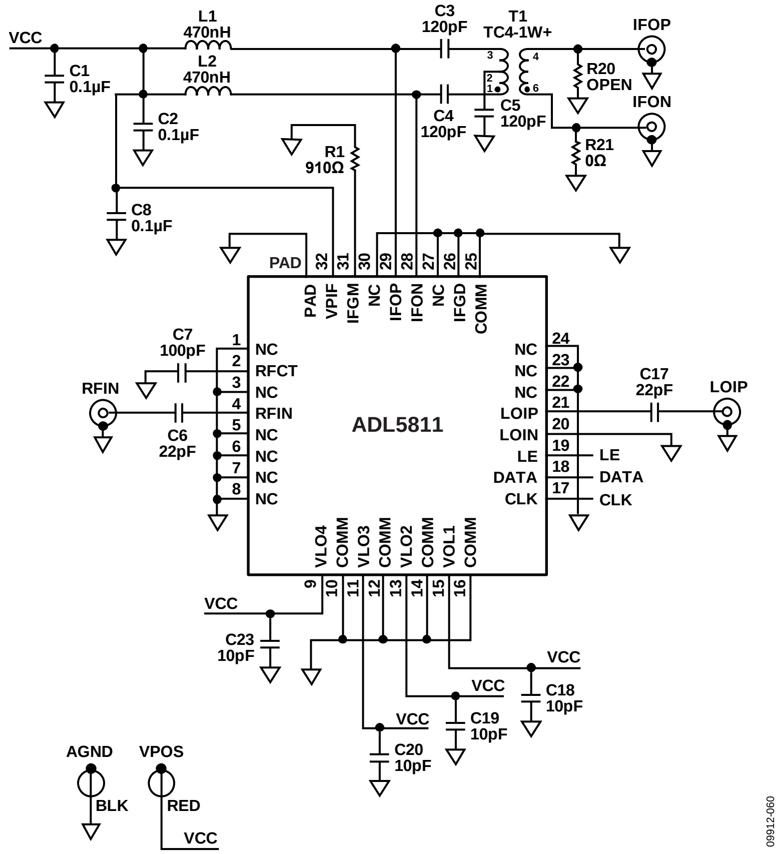


Figure 61. Evaluation Board Schematic

Table 12. Evaluation Board Configuration

Components	Description	Default Conditions
C1, C2, C8, C18, C19, C20, C23	Power supply decoupling. Nominal supply decoupling consists of a 0.1 µF capacitor to ground in parallel with a 10 pF capacitor to ground positioned as close to the device as possible.	C1, C2 = 0.1 µF (size 0402), C8, C18, C19, C20, C23 = 10 pF (size 0402)
C6, C7, RFIN	RF input interface. The input channel is ac-coupled through C6. C7 provides bypassing for the center tap of the RF input balun.	C6 = 22 pF (size 0402), C7 = 100 pF (size 0402)
C3, C4, C5, L1, L2, R20, R21, T1, IFOP, IFON	IF output interface. The open-collector IF output interfaces are biased through pull-up choke inductors, L1 and L2. T1 is a 4:1 impedance transformer used to provide a single-ended IF output interface, with C5 providing center-tap bypassing. Remove R21 for balanced output operation.	C3, C4, C5 = 120 pF (size 0402), L1, L2 = 470 nH (size 0603), R20 = open, R21 = 0 Ω (size 0402), T1 = TC4-1W+ (Mini-Circuits®)
C17, LOIP	LO interface. C17 provides ac coupling for the LOIP local oscillator input.	C17 = 22 pF (size 0402)
R1	Bias control. R1 sets the bias point for the internal IF amplifier.	R1 = 910 Ω (size 0402)

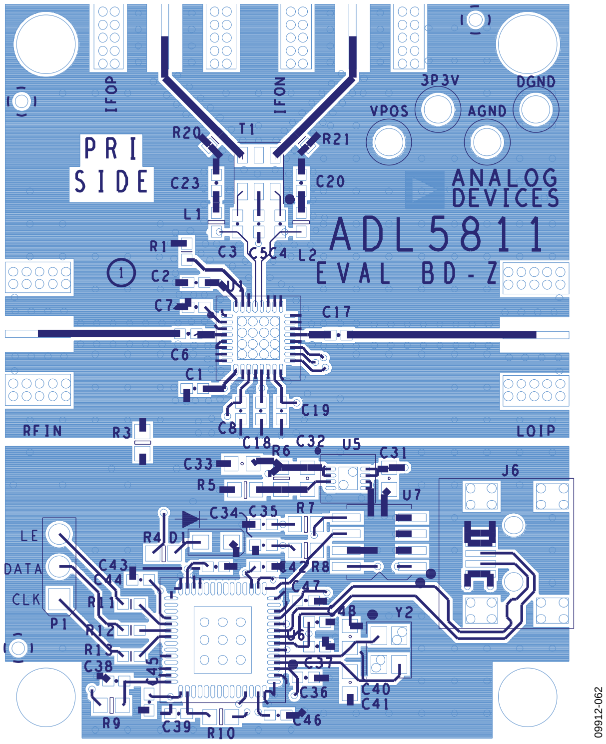


Figure 62. Evaluation Board Top Layer

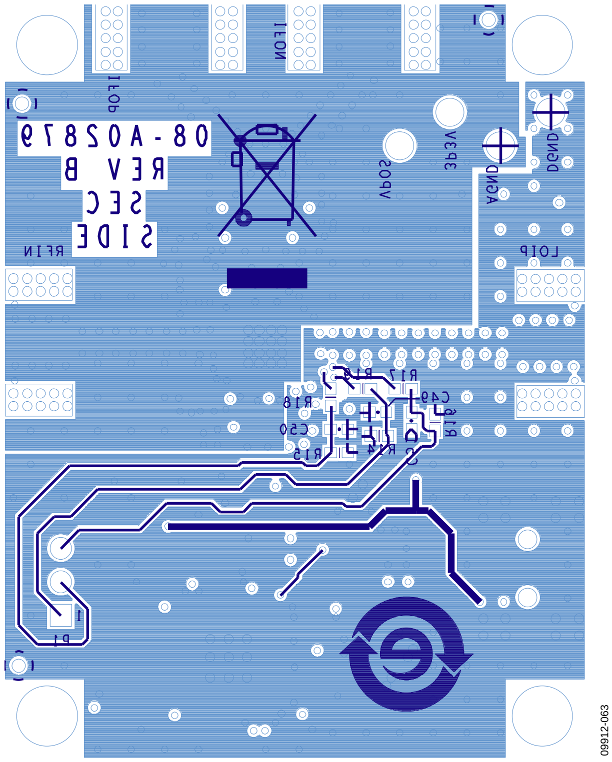


Figure 63. Evaluation Board Bottom Layer

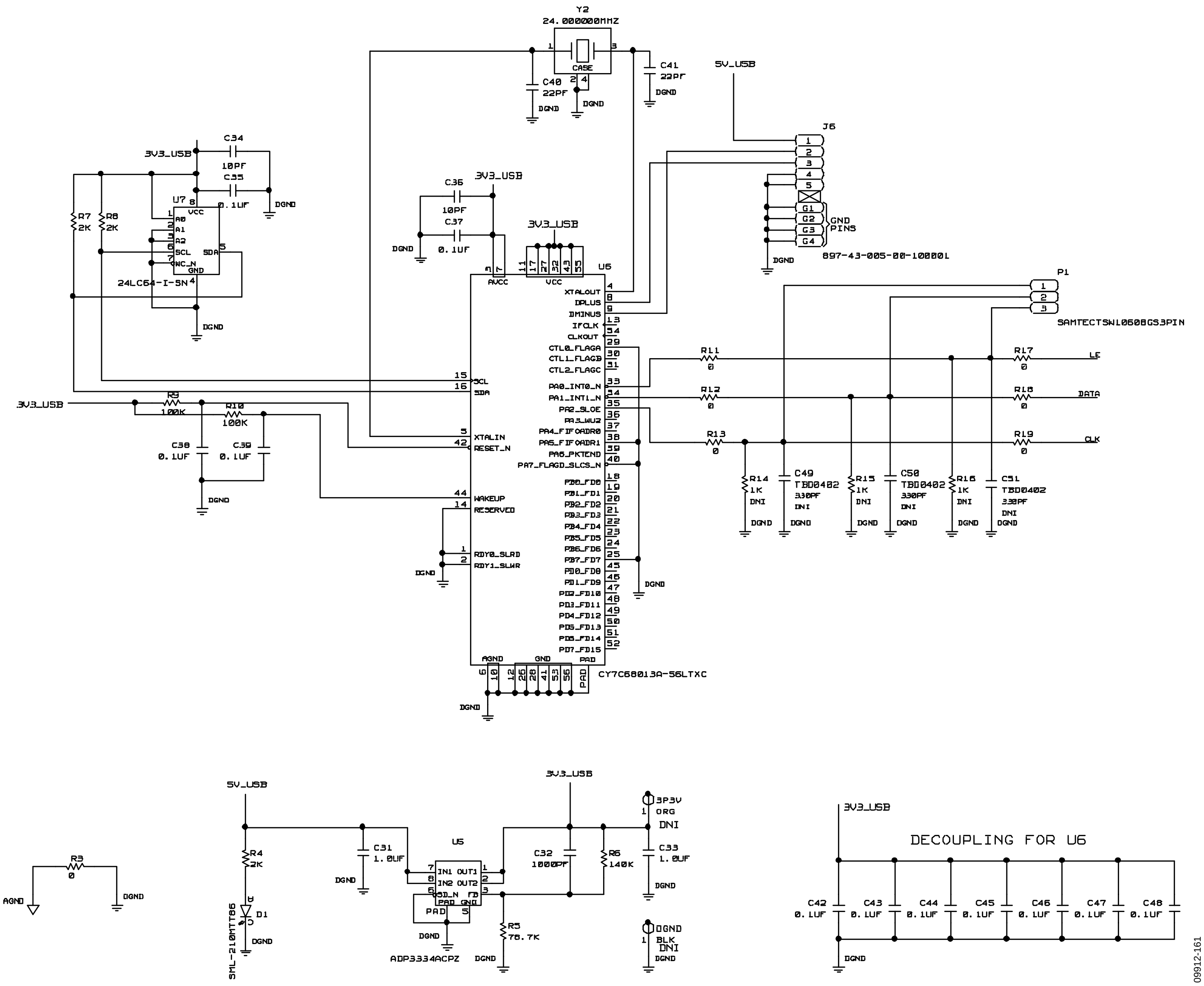


Figure 64. USB Interface Circuitry on the Evaluation Board

OUTLINE DIMENSIONS

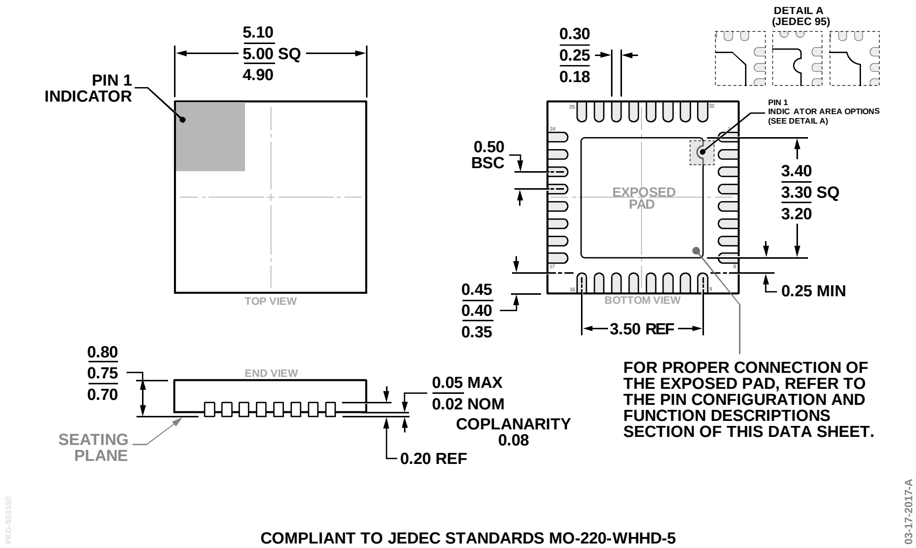


Figure 65. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Quantity
ADL5811ACPZ-R7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-20	1500
ADL5811-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.