



14 Gbps, 2:1 SELECTOR w/ PROGRAMMABLE OUTPUT VOLTAGE & POSITIVE SUPPLY

Typical Applications

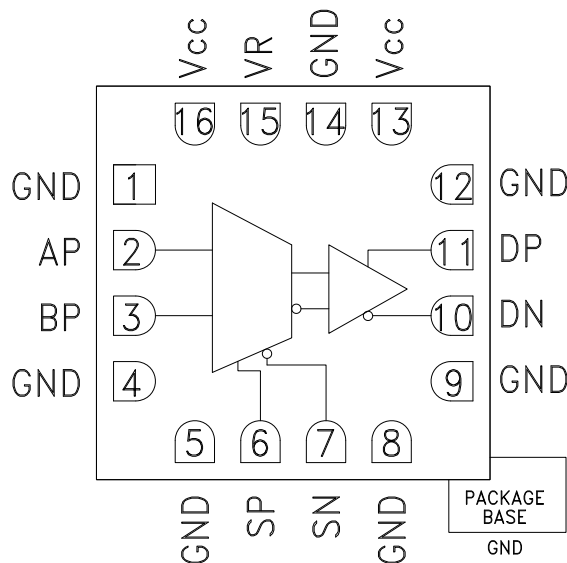
The HMC748LC3C is ideal for:

- 2:1 Multiplexer up to 14 Gbps
- RF ATE Applications
- Broadband Test & Measurement
- Serial Data Transmission up to 14 Gbps
- Redundant Path Switching
- Built-in Test

Features

- Supports High Data Rates: up to 14 Gbps
- Single-ended inputs
- Differential & Single-Ended Outputs
- Fast Rise and Fall Times: 22 / 22 ps
- Low Power Consumption: 250 mW typ.
- Programmable Differential Output Voltage Swing: 600 - 1200 mV
- Propagation Delay: 125 ps
- Single Supply: +3.3 V
- 16 Lead Ceramic 3x3 mm SMT Package: 9 mm²

Functional Diagram



General Description

The HMC748LC3C is a 2:1 Selector designed to support data transmission rates of up to 14 Gbps, and selector port operation of up to 14 GHz. The selector routes one of the two single-ended inputs to the differential output upon assertion of the proper select port. The HMC748LC3C also features an output level control pin, VR, that allows for loss compensation or for signal level optimization.

All select differential inputs to the HMC748LC3C are CML and terminated on-chip with 50 ohms to the positive supply, Vcc, and may be AC or DC coupled. The single-ended inputs to the HMC748LC3C are CML terminated on-chip with 50 ohms to the positive supply, GND, and may be DC coupled. The differential CML outputs are source terminated to 50 ohms and may also be AC or DC coupled. Outputs can be connected directly to a 50 ohm Vcc terminated system, while DC blocking capacitors may be used if the terminating system is 50 ohms to ground. The HMC748LC3C operates from a single + 3.3 V supply and is available in ROHS-compliant 3x3 mm SMT package.

Electrical Specifications, $T_A = +25^\circ\text{C}$, $V_{CC} = 3.3\text{ V}$, $V_R = 3.3\text{ V}$

| Parameter | Conditions | Min. | Typ. | Max | Units |
|----------------------------------|------------|------|------|-----|-------|
| Power Supply Voltage | | 3.0 | 3.3 | 3.6 | V |
| Power Supply Current | | | 76 | | mA |
| Maximum Data Rate | | | 14 | | Gbps |
| Maximum Select Rate | | | 14 | | GHz |
| Maximum Serial Transmission Rate | | | 26 | | Gbps |

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14 Gbps, 2:1 SELECTOR w/ PROGRAMMABLE OUTPUT VOLTAGE & POSITIVE SUPPLY

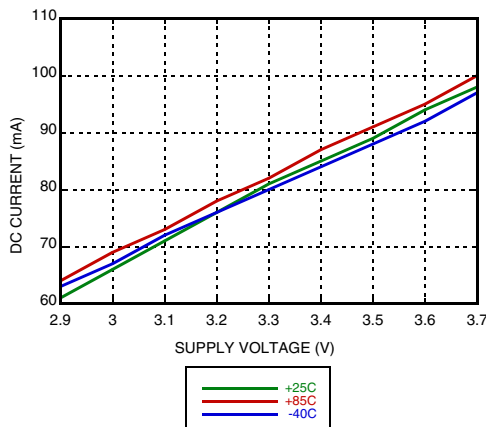
Electrical Specifications (continued)

| Parameter | Conditions | Min. | Typ. | Max | Units |
|--|--|-------------|-------------|-------------|---------|
| Input Vcm | Vin = 600 mVp-p | Vcc - 0.375 | Vcc - 0.300 | Vcc - 0.275 | V |
| Input High Voltage | | | Vcc - 0.1 | Vcc - 0.5 | V |
| Input Low Voltage | | Vcc - 0.1 | Vcc - 0.5 | | V |
| Input Return Loss | Frequency <14 GHz | | 10 | | dB |
| Output Amplitude | Single-Ended, peak-to-peak | | 550 | | mVp-p |
| | Differential, peak-to-peak | | 1100 | | mVp-p |
| Output High Voltage | | | 3.29 | | V |
| Output Low Voltage | | | 2.74 | | V |
| Output Rise / Fall Time | Differential, 20% - 80% | | 22 / 22 | | ps |
| Output Return Loss | Frequency <13 GHz | | 10 | | dB |
| Random Jitter, Jr | rms ^[1] | | | 0.2 | ps rms |
| Deterministic Jitter, Jd | peak-to-peak, 2 ¹⁵ -1 PRBS input ^[2] | | 2 | | ps, p-p |
| Propagation Delay, A or B to D _{OUT} , t _d | | | 125 | | ps |
| Propagation Delay Select to Data, t _{ds} | | | 135 | | ps |
| Set Up & Hold Time, t _{SH} | | | 6 | | ps |
| VR Pin Current | VR = 3.3 V | | 2 | | mA |
| VR Pin Current | VR = 3.7 V | | | 3.5 | mA |

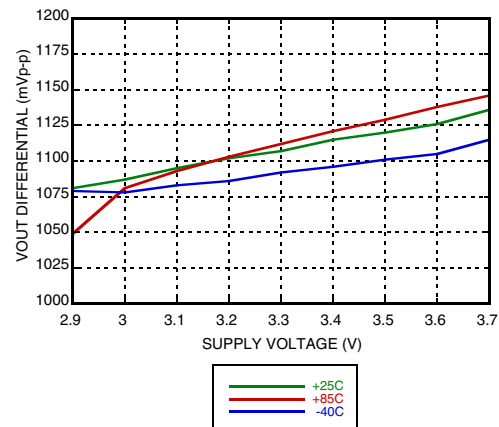
[1] Upper limit of random jitter, Jr, determined by measuring and integrating output phase noise with a sinusoidal input at 5, 10, and 13.5 GHz over temperature

[2] Deterministic jitter calculated by simultaneously measuring the jitter of a 200 mV, 12.5 GHz, 2¹⁵-1 PRBS input, and a single-ended output

DC Current vs. Supply Voltage ^[1] ^[2]



Output Differential Voltage vs. Supply Voltage ^[1] ^[2]



[1] VR = 3.3 V

[2] Frequency = 13 GHz

[3] Vcc = 3.3 V

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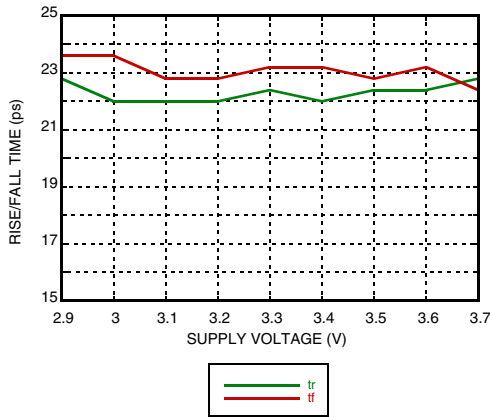
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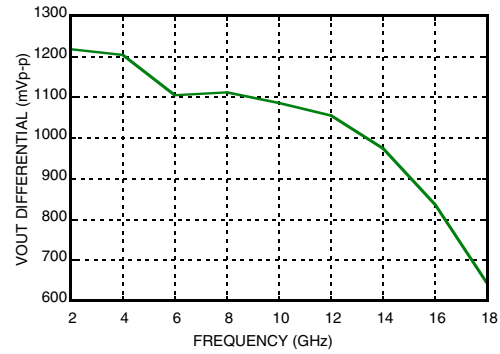
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HIGH SPEED LOGIC - SMT

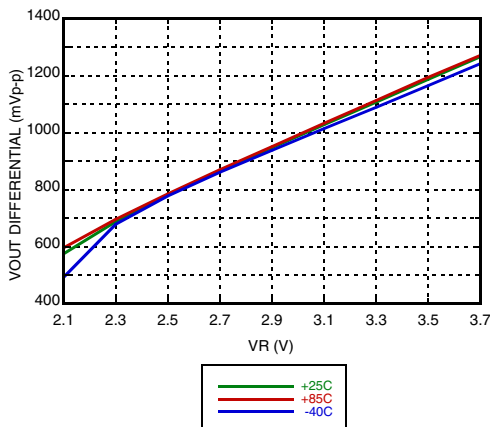
Rise / Fall Time vs. Supply Voltage [1] [2]



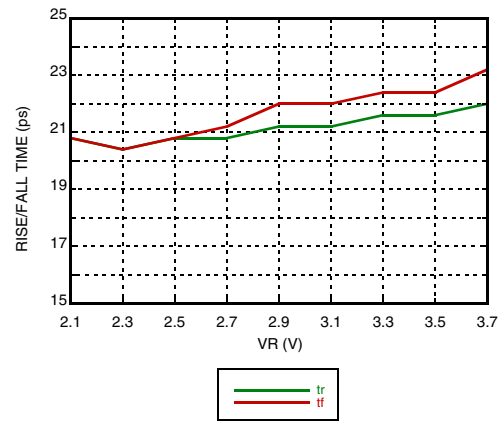
Output Differential vs. Frequency [1] [3]



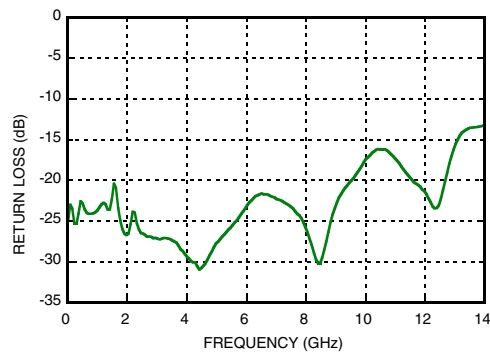
Output Differential Voltage vs. VR [1] [2]



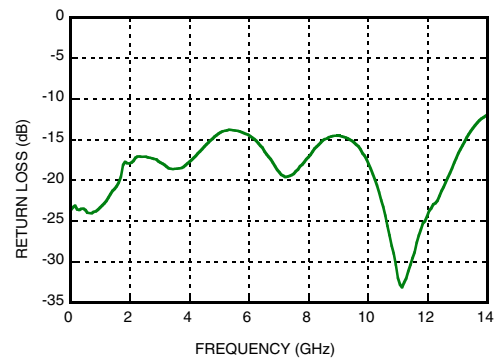
Rise / Fall Time vs. VR [1] [2]



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



[1] Vcc = 3.3 V

[2] Frequency = 13 GHz

[3] Vcc = 3.3 V

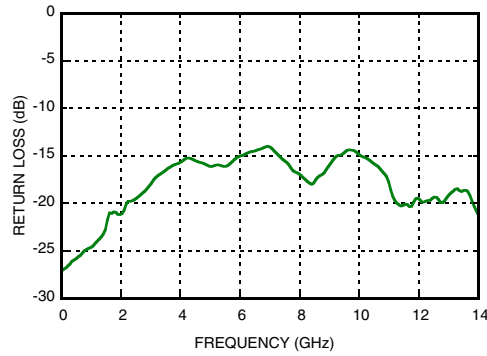
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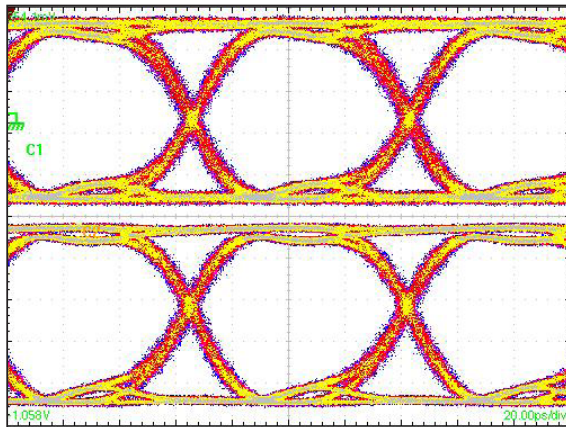
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Select Port Return Loss vs. Frequency

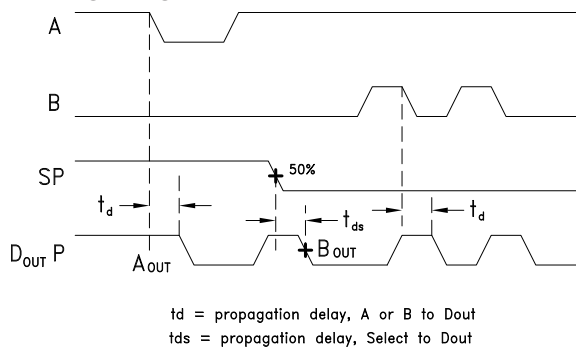


Eye Diagram



[1] Test Conditions:
 Waveform generated with an Agilent N4903A J-Bert.
 Rate = 13 GHz
 Eye Diagram data presented on a Tektronix CSA 8000
 Device is AC coupled to scope.

Timing Diagram



Truth Table

| Inputs | Outputs |
|--------|---------|
| S | DP |
| H | A -> D |
| L | B -> D |

H - Positive voltage level
 L - Negative voltage level

Notes:
 D = DP - DN
 S = SP - SN

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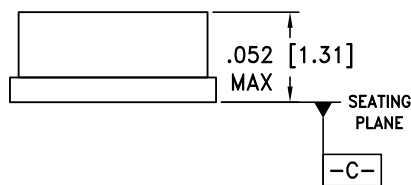
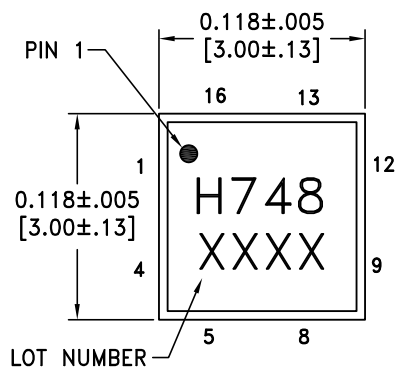
Absolute Maximum Ratings

| | |
|--|----------------------------|
| Power Supply Voltage (Vcc) | Vcc -0.5 V to 3.75 V |
| Input Signals | Vcc - 2.0 V to Vcc + 0.5 V |
| Output Signals | Vcc - 1.5 V to Vcc + 0.5 V |
| Continuous Pdiss (T = 85 °C) (derate 17 mW/°C above 85 °C) | 0.68 W |
| Thermal Resistance (R _{th j-p})worst case junction to package paddle | 59 °C/W |
| Maximum Junction Temperature | 125 °C |
| Storage Temperature | -65 °C to +150 °C |
| Operating Temperature | -40 °C to +85 °C |
| ESD Sensitivity (HBM) | Class 1B |

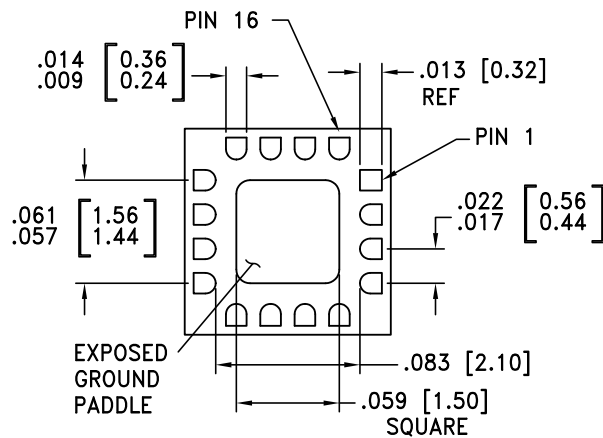


ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



BOTTOM VIEW



NOTES:

- PACKAGE BODY MATERIAL: ALUMINA
- LEAD AND GROUND PADDLE PLATING:
30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
- DIMENSIONS ARE IN INCHES [MILLIMETERS].
- LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
- PACKAGE WARP SHALL NOT EXCEED 0.05 mm DATUM -C-
- ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
- PADDLE MUST BE SOLDERED TO GND.

Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking [2] |
|-------------|-----------------------|------------------|------------|---------------------|
| HMC748LC3C | Alumina, White | Gold over Nickel | MSL3 [1] | H748 XXXX |


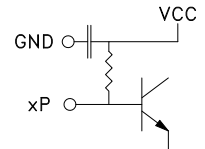
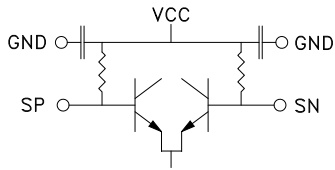
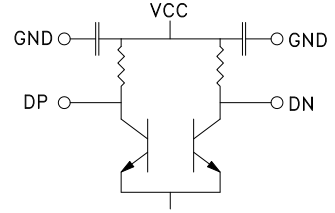

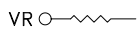
[1] Max peak reflow temperature of 260 °C

[2] 4-Digit lot number XXXX



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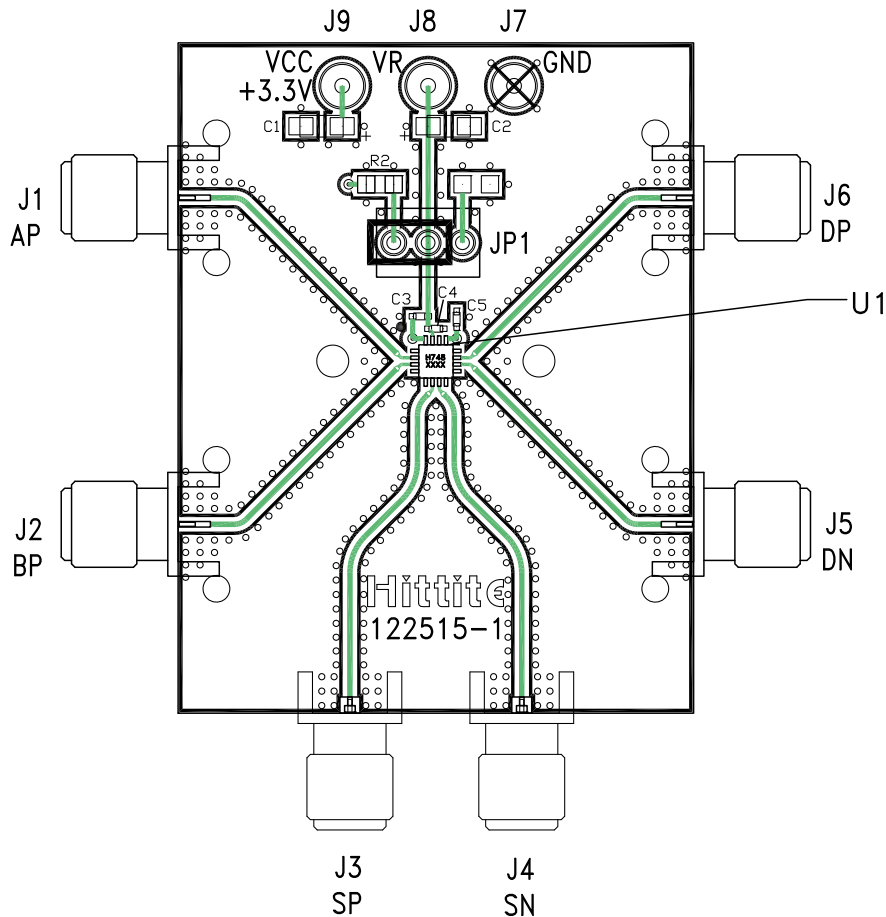
Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|---------------------|----------|---|---|
| 1, 4, 5, 8, 9, 12 | GND | Signal Grounds |  |
| 2, 3 | AP, BP | Single-Ended Data Inputs: Current Mode Logic (CML) referenced to positive supply. |  |
| 6, 7 | SP, SN | Differential Select Inputs: Current Mode Logic (CML) referenced to positive supply. |  |
| 10, 11 | DN, DP | Differential Data Outputs: Current Mode Logic (CML) referenced to positive supply. |  |
| 13, 16 | Vcc | Positive Supply | |
| 14, Package Base | GND | Supply Ground |  |
| 15 | VR | Output level control. Output level may be adjusted by applying a voltage to VR per "Output Differential vs. VR" plot. |  |



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Evaluation PCB



List of Materials for Evaluation PCB 122517 [1]

| Item | Description |
|---------|---|
| J1 - J6 | PCB Mount SMA RF Connectors |
| J7 - J9 | DC Pin |
| JP1 | Shorting Jumper |
| C1, C2 | 4.7 μF Capacitor, Tantalum |
| C3 - C5 | 100 pF Capacitor, 0402 Pkg. |
| R2 | 10 Ohm Resistor, 0603 Pkg. |
| U1 | HMC748LC3C High Speed Logic, 2:1 Selector |
| PCB [2] | 122515 Evaluation Board |

[1] Reference this number when ordering complete evaluation PCB

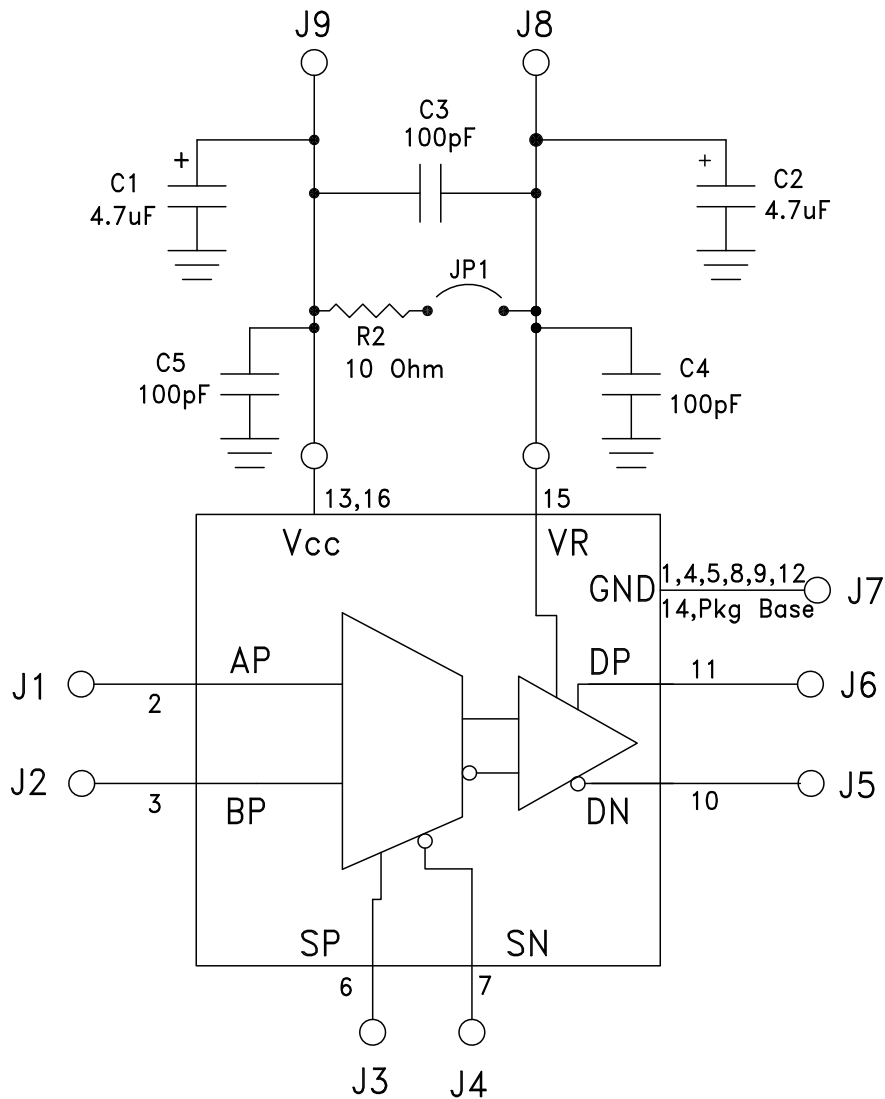
[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed package base should be connected to GND. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to Vcc for normal operation.

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Application Circuit



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