256-Position, Two-Time Programmable, I^{2}C Digital Potentiometer

FEATURES

- 256-position digital potentiometer
- Two-time programmable (TTP) set-and-forget resistance setting allows second-chance permanent programming
- Unlimited adjustments prior to one-time programming (OTP) activation
- OTP overwrite allows dynamic adjustments with user-defined preset
- End to end resistance: 2.5 kΩ, 10 kΩ, and 50 kΩ
- Compact 10-lead MSOP: 3 mm × 4.9 mm package
- Fast settling time: t_S = 5 µs typical in power-up
- Full read/write of wiper register
- Power-on preset to midscale
- Extra package address decode pins: AD0 and AD1
- Single supply: 2.7 V to 5.5 V
- Low temperature coefficient: 35 ppm/°C
- Low power: I_{DD} = 6 µA maximum
- Wide operating temperature: −40°C to +125°C
- Software replaces MicroConverter® in factory programming applications

APPLICATIONS

- Systems calibration
- Electronics level setting
- Mechanical trimmers replacement in new designs
- Permanent factory PCB settings
- Transducer adjustment of pressure, temperature, position, chemical, and optical sensors
- RF amplifier biasing
- Gain control and offset adjustments

FUNCTIONAL BLOCK DIAGRAM

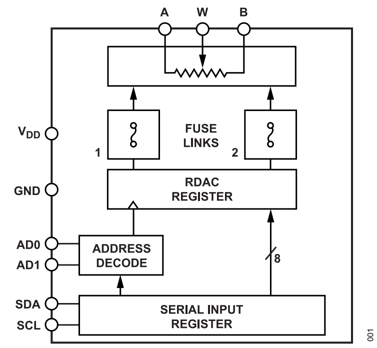

Figure 1.

GENERAL DESCRIPTION

The AD5170 is a 256-position, two-time programmable, digital potentiometer that employs fuse link technology, giving users two opportunities to permanently program the resistance setting. The digital potentiometer, VR, and RDAC terms are used interchangeably. For users who do not need to program the digital potentiometer setting in memory more than once, the OTP feature is a cost-effective alternative to EEMEM. The AD5170 performs the same electronic adjustment function as mechanical potentiometers or variable resistors with enhanced resolution, solid-state reliability, and superior low temperature coefficient performance.

The AD5170 is programmed using a 2-wire, I^{2}C-compatible digital interface. Unlimited adjustments are allowed before permanently setting the resistance value, and there are two opportunities for permanent programming. During OTP activation, a permanent blow fuse command freezes the wiper position (analogous to placing epoxy on a mechanical trimmer).

Unlike traditional OTP digital potentiometers, the AD5170 has a unique temporary OTP overwrite feature that allows for new adjustments even after the fuse is blown. However, the OTP setting is restored during subsequent power-up conditions. This feature allows users to treat these digital potentiometers as volatile potentiometers with a programmable preset.

For applications that program the AD5170 at the factory, Analog Devices, Inc., offers device programming software that runs on Windows NT®, Windows® 2000, and Windows XP operating systems. This software effectively replaces any external I^{2}C controllers, thus enhancing the time-to-market of the user's systems.

Rev. H

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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1/2022—Rev. G to Rev. H

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Changed Timing Characteristics: 2.5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ Section to Timing Characteristics: 2.5 kΩ, 10 kΩ, and 50 kΩ Section ... 5
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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS: 2.5 KΩ

V_{DD} = 5 V ± 10% or 3 V ± 10%, V_A = V_{DD}, V_B = 0 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−2	±0.1	+2	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−14	±2	+14	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	−20		+55	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$			35		ppm/°C
R_{WB} (Wiper Resistance)	R_{WB}	Code = 0x00, V_{DD} = 5 V		160	200	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (SPECIFICATIONS APPLY TO ALL VRs)						
Differential Nonlinearity[4]	DNL		−1.5	±0.1	+1.5	LSB
Integral Nonlinearity[4]	INL		−2	±0.6	+2	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	−14	−5.5	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	4.5	12	LSB
RESISTOR TERMINALS						
Voltage Range[5]	V_A, V_B, V_W		GND		V_{DD}	V
Capacitance A, Capacitance B[6]	C_A, C_B	f = 1 MHz, measured to GND, code = 0x80		45		pF
Capacitance W[6]	C_W	f = 1 MHz, measured to GND, code = 0x80		60		pF
Shutdown Supply Current[7]	I_{A_SD}	V_{DD} = 5.5 V		0.01	1	µA
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High (SDA and SCL)[8]	V_{IH}	V_{DD} = 5 V	0.7 V_{DD}		V_{DD} + 0.5	V
Input Logic Low (SDA and SCL)[8]	V_{IL}	V_{DD} = 5 V	−0.5		+0.3 V_{DD}	V
Input Logic High (AD0 and AD1)	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low (AD0 and AD1)	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}		2.7		5.5	V
OTP Supply Voltage[8, 9]	V_{DD_OTP}	T_A = 25°C	5.6	5.7	5.8	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3.5	6	µA
OTP Supply Current[8, 10, 11]	I_{DD_OTP}	V_{DD_OTP} = 5.7 V, T_A = 25°C		100		mA
Power Dissipation[12]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			33	µW
Power Supply Sensitivity	PSS	V_{DD} = 5 V ± 10%, code = midscale		±0.02	±0.08	%/%
DYNAMIC CHARACTERISTICS[13]						
–3 dB Bandwidth	BW	R_{AB} = 2.5 kΩ, code = 0x80		4.8		MHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.1		%
V_W Settling Time	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band		1		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 1.25 kΩ, f = 1 kHz		3.2		nV/√Hz

1 Typical specifications represent average readings at 25°C and V_{DD} = 5 V.

2 Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. Parts are guaranteed monotonic.

3 V_{AB} = V_{DD}, wiper (V_W) = no connect.

SPECIFICATIONS

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit

[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and $V_B = 0$ V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.

[5] The A, B, and W resistor terminals have no limitations on polarity with respect to each other.

[6] Guaranteed by design and not subject to production test.

[7] Measured at the A terminal. The A terminal is open circuited in shutdown mode.

[8] The minimum voltage requirement on the V_{IH} is 0.7 V × V_{DD}. For example, V_{IH} minimum = 3.5 V when V_{DD} = 5 V. It is typical for the SCL and SDA resistors to be pulled up to V_{DD}. However, care must be taken to ensure that the minimum V_{IH} is met when the SCL and SDA are driven directly from a low voltage logic controller without pull-up resistors.

[9] Different from operating power supply; power supply for OTP is used one time only.

[10] Different from operating current; supply current for OTP lasts approximately 400 ms for use one time only.

[11] See Figure 25 for the energy plot during OTP program.

[12] P_{DISS} is calculated from (I_{DD} × V_{DD}). CMOS logic level inputs result in minimum power dissipation.

[13] All dynamic characteristics use V_{DD} = 5 V.

ELECTRICAL CHARACTERISTICS: 10 KΩ AND 50 KΩ

V_{DD} = 5 V ± 10% or 3 V ± 10%, $V_A = V_{DD}$, V_B = 0 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−1	±0.1	+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−2.5	±0.25	+2.5	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	−20		+20	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$			35		ppm/°C
R_{WB} (Wiper Resistance)	R_{WB}	Code = 0x00, V_{DD} = 5 V		160	200	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (SPECIFICATIONS APPLY TO ALL VRs)						
Differential Nonlinearity[4]	DNL		−1	±0.1	+1	LSB
Integral Nonlinearity[4]	INL		−1	±0.3	+1	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	−2.5	−1	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	1	2.5	LSB
RESISTOR TERMINALS						
Voltage Range[5]	V_A, V_B, V_W		GND		V_{DD}	V
Capacitance A, Capacitance B[6]	C_A, C_B	f = 1 MHz, measured to GND, code = 0x80		45		pF
Capacitance W[6]	C_W	f = 1 MHz, measured to GND, code = 0x80		60		pF
Shutdown Supply Current[7]	I_{A_SD}	V_{DD} = 5.5 V		0.01	1	μA
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High (SDA and SCL)[8]	V_{IH}	V_{DD} = 5 V	0.7 V_{DD}		V_{DD} + 0.5	V
Input Logic Low (SDA and SCL)[8]	V_{IL}	V_{DD} = 5 V	−0.5		+0.3 V_{DD}	V
Input Logic High (AD0 and AD1)	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low (AD0 and AD1)	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	μA
Input Capacitance[6]	C_{IL}			5		pF

SPECIFICATIONS

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
POWER SUPPLIES						
Power Supply Range	V_{DD}		2.7		5.5	V
OTP Supply Voltage[8, 9]	V_{DD_OTP}		5.6	5.7	5.8	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3.5	6	µA
OTP Supply Current[8, 10, 11]	I_{DD_OTP}	V_{DD_OTP} = 5.7 V, T_A = 25°C		100		mA
Power Dissipation[12]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			33	µW
Power Supply Sensitivity	PSS	V_{DD} = 5 V ± 10%, code = midscale		±0.02	±0.08	%/%
DYNAMIC CHARACTERISTICS[13]						
−3 dB Bandwidth	BW	R_{AB} = 10 kΩ, code = 0x80		600		kHz
		R_{AB} = 50 kΩ, code = 0x80		100		kHz
Total Harmonic Distortion	THD_W	V_A =1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ		0.1		%
V_W Settling Time (10 kΩ/50 kΩ)	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band		2		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 5 kΩ, f = 1 kHz		9		nV/√Hz

1 Typical specifications represent average readings at 25°C and V_{DD} = 5 V.

2 Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. Parts are guaranteed monotonic.

3 V_{AB} = V_{DD}, wiper (V_W) = no connect.

4 INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.

5 The A, B, and W resistor terminals have no limitations on polarity with respect to each other.

6 Guaranteed by design and not subject to production test.

7 Measured at the A terminal. The A terminal is open circuited in shutdown mode.

8 The minimum voltage requirement on the V_{IH} is 0.7 V × V_{DD}. For example, V_{IH} minimum = 3.5 V when V_{DD} = 5 V. It is typical for the SCL and SDA resistors to be pulled up to V_{DD}. However, care must be taken to ensure that the minimum V_{IH} is met when the SCL and SDA are driven directly from a low voltage logic controller without pull-up resistors.

9 Different from operating power supply, power supply OTP is used one time only.

10 Different from operating current, supply current for OTP lasts approximately 400 ms for use one time only.

11 See Figure 25 for the energy plot during OTP program.

12 P_{DISS} is calculated from (I_{DD} × V_{DD}). CMOS logic level inputs result in minimum power dissipation.

13 All dynamic characteristics use V_{DD} = 5 V.

TIMING CHARACTERISTICS: 2.5 KΩ, 10 KΩ, AND 50 KΩ

V_{DD} = 5 V ± 10% or 3 V ± 10%, V_A = V_{DD}; V_B = 0 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I^2C INTERFACE TIMING CHARACTERISTICS[1] (SPECIFICATIONS APPLY TO ALL PARTS)						
SCL Clock Frequency	f_{SCL}				400	kHz
t_{BUF} Bus Free Time Between Stop and Start	t_1		1.3			µs
$t_{HD;STA}$ Hold Time (Repeated Start)	t_2	After this period, the first clock pulse is generated	0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6			µs
$t_{SU;STA}$ Setup Time for Repeated Start Condition	t_5		0.6			µs

SPECIFICATIONS

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
$t_{HD;DAT}$ Data Hold Time[2]	t_6				0.9	μs
$t_{SU;DAT}$ Data Setup Time	t_7		100			ns
t_F Fall Time of Both SDA and SCL Signals	t_8				300	ns
t_R Rise Time of Both SDA and SCL Signals	t_9				300	ns
$t_{SU;STO}$ Setup Time for Stop Condition	t_{10}		0.6			μs
OTP Program Time	t_{11}			400		ms

[1] See Figure 2 for locations of measured values.

[2] The maximum $t_{HD;DAT}$ must be met only if the device does not stretch the low period (t_{LOW}) of the SCL signal.

Timing Diagram

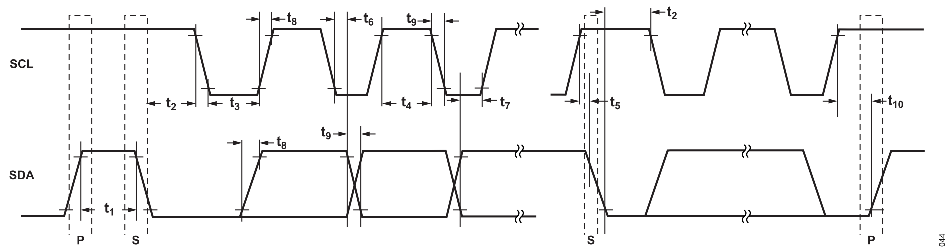


Figure 2. I²C Interface Detailed Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

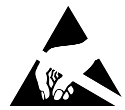
Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_A, V_B, V_W to GND	V_{DD}
Terminal Current, A to B, A to W, B to W[1]	
Pulsed	±20 mA
Continuous	±5 mA
Digital Inputs and Output Voltage to GND	0 V to 7 V
Operating Temperature Range	−40°C to +125°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Thermal Resistance[2]	
θ_{JA}: 10-Lead MSOP	230°C/W

[1] Maximum terminal current is bound by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[2] Package power dissipation = $(T_{JMAX} − T_A)/\theta_{JA}$.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

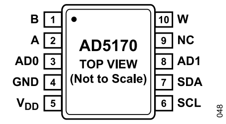


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	B	B Terminal. GND ≤ V_B ≤ V_{DD}.
2	A	A Terminal. GND ≤ V_A ≤ V_{DD}.
3	AD0	Programmable Address Bit 0 for Multiple Package Decoding.
4	GND	Digital Ground.
5	V_{DD}	Positive Power Supply. Specified for operation from 2.7 V to 5.5 V. For OTP programming, the V_{DD} supply must be within the 5.6 V to 5.8 V range and capable of driving 100 mA.
6	SCL	Serial Clock Input. Positive edge triggered. Requires a pull-up resistor. If it is driven directly from a logic controller without the pull-up resistor, ensure that V_{IH} minimum is 0.7 V × V_{DD}.
7	SDA	Serial Data Input/Output. Requires a pull-up resistor. If it is driven directly from a logic controller without the pull-up resistor, ensure that V_{IH} minimum is 0.7 V × V_{DD}.
8	AD1	Programmable Address Bit 1 for Multiple Package Decoding.
9	NC	No Connect.
10	W	W Terminal. GND ≤ V_W ≤ V_{DD}.

TYPICAL PERFORMANCE CHARACTERISTICS

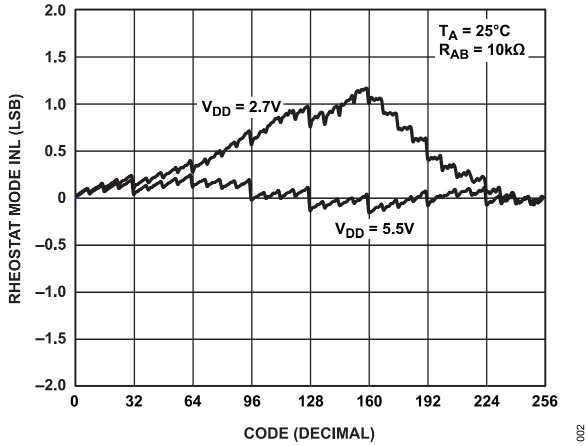


Figure 4. R-INL vs. Code vs. Supply Voltages

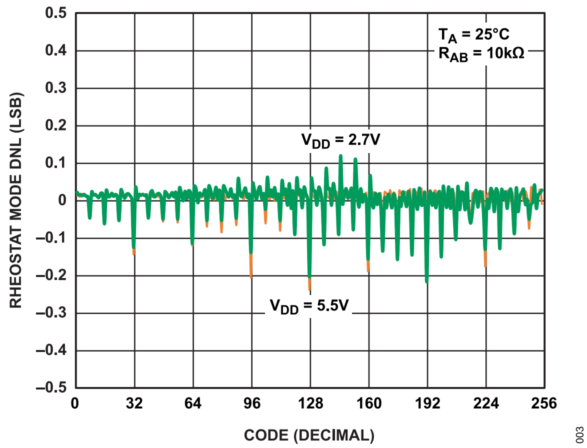


Figure 5. R-DNL vs. Code vs. Supply Voltages

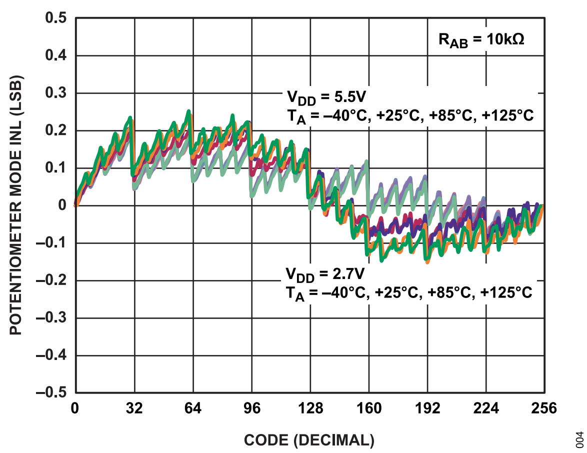


Figure 6. INL vs. Code vs. Temperature

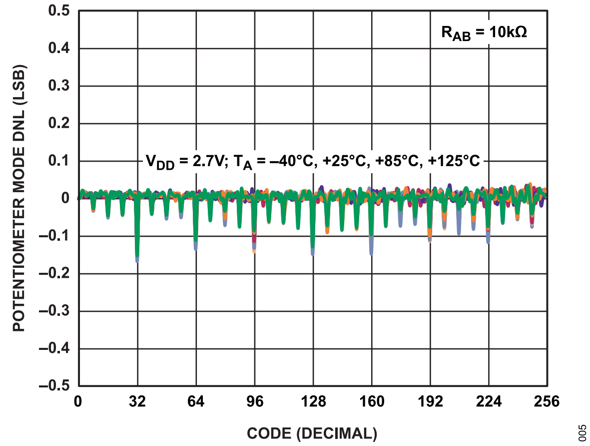


Figure 7. DNL vs. Code vs. Temperature

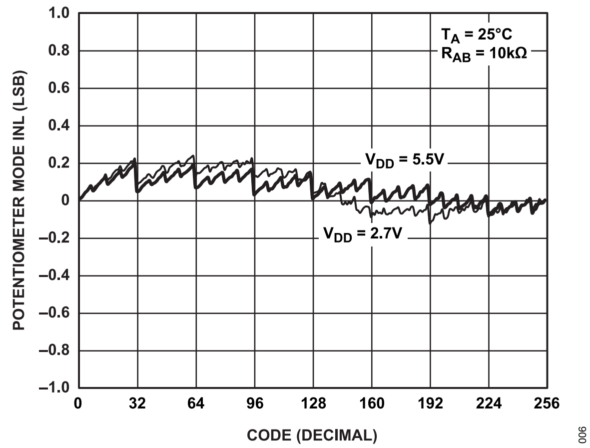


Figure 8. INL vs. Code vs. Supply Voltages

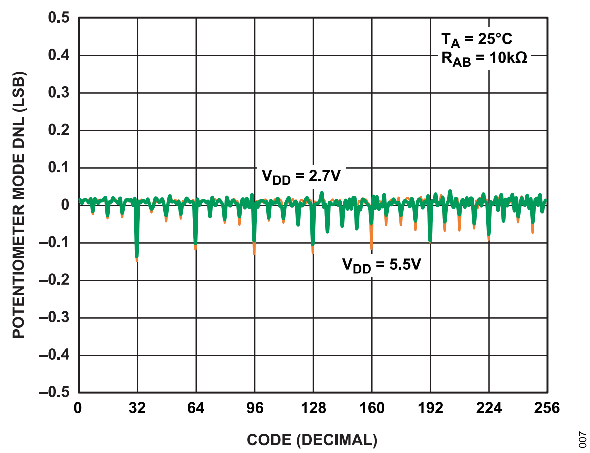


Figure 9. DNL vs. Code vs. Supply Voltages

TYPICAL PERFORMANCE CHARACTERISTICS

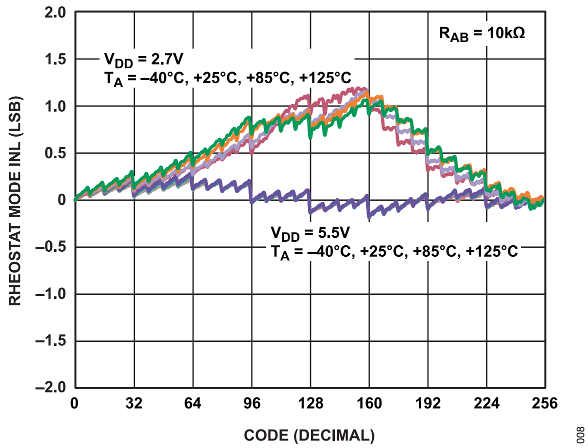


Figure 10. R-INL vs. Code vs. Temperature

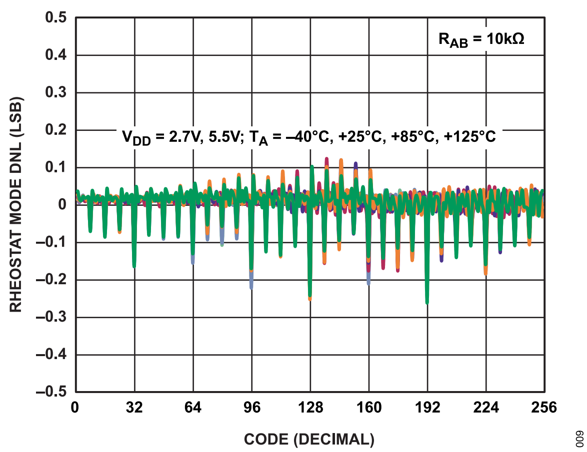


Figure 11. R-DNL vs. Code vs. Temperature

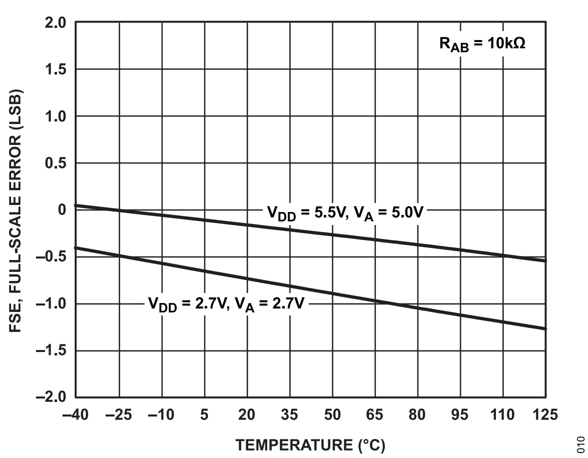


Figure 12. Full-Scale Error vs. Temperature

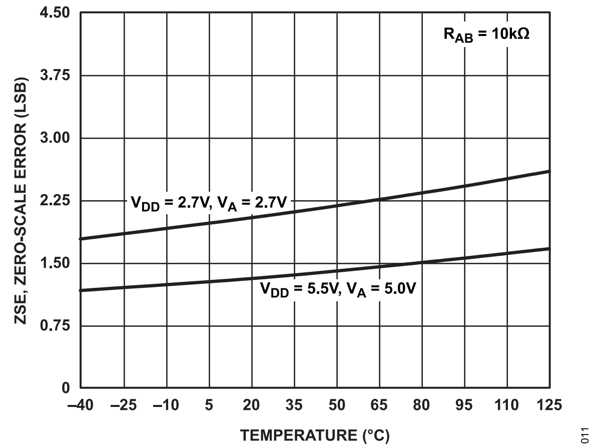


Figure 13. Zero-Scale Error vs. Temperature

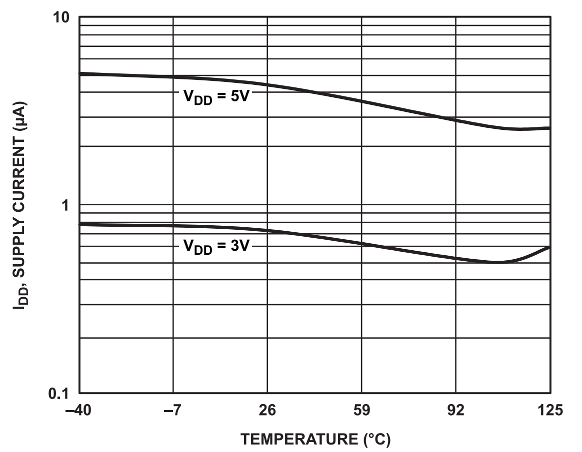


Figure 14. I_{DD}, Supply Current vs. Temperature

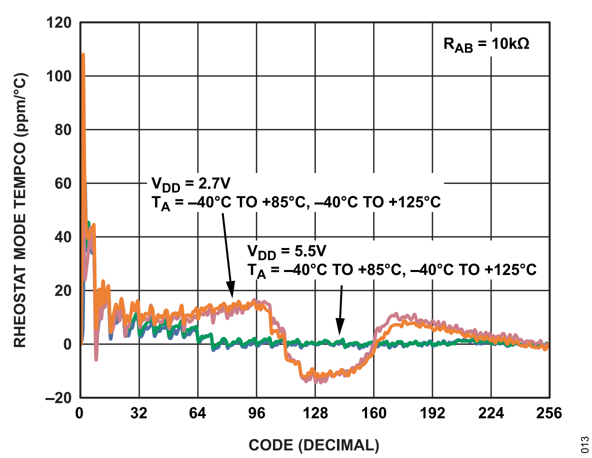


Figure 15. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

TYPICAL PERFORMANCE CHARACTERISTICS

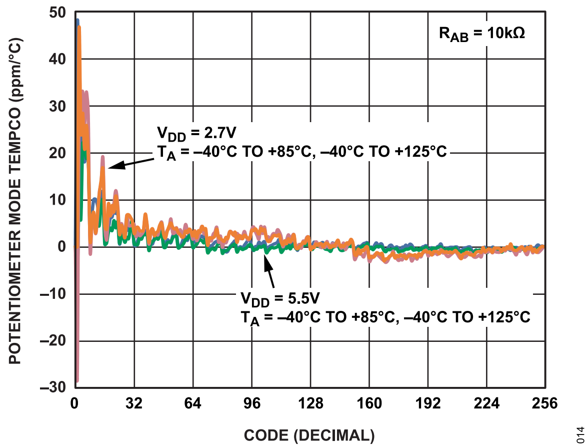


Figure 16. Potentiometer Mode Tempco $\Delta V_{WB}/\Delta T$ vs. Code

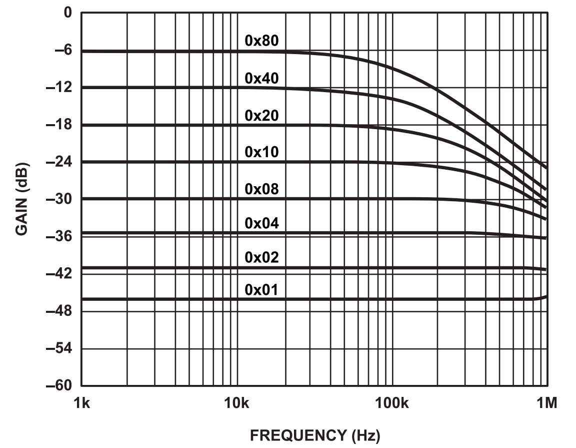


Figure 19. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ

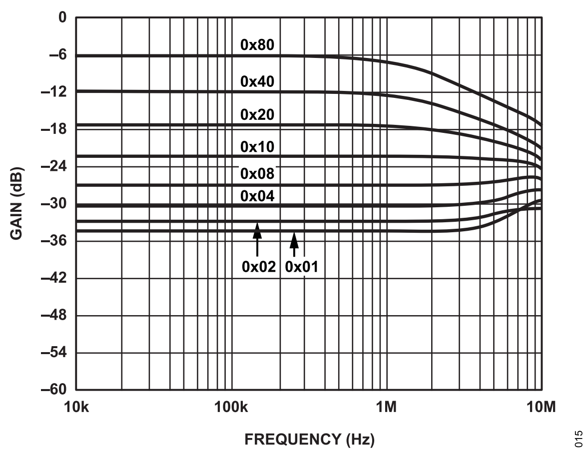


Figure 17. Gain vs. Frequency vs. Code, R_{AB} = 2.5 kΩ

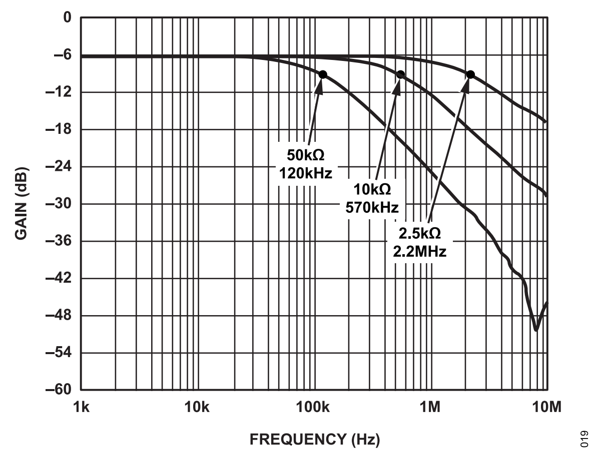


Figure 20. −3 dB Bandwidth at Code = 0x80

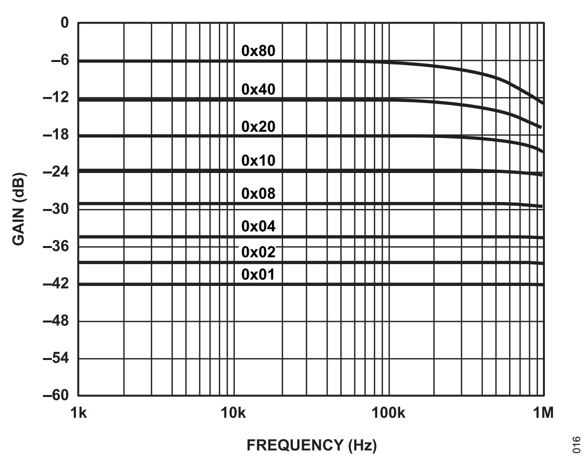


Figure 18. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ

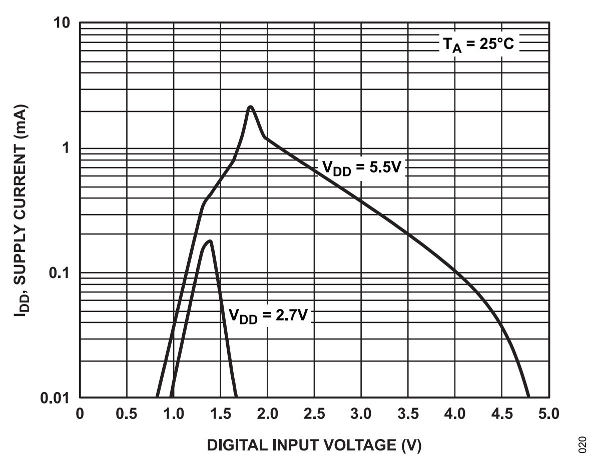


Figure 21. I_{DD}, Supply Current vs. Digital Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

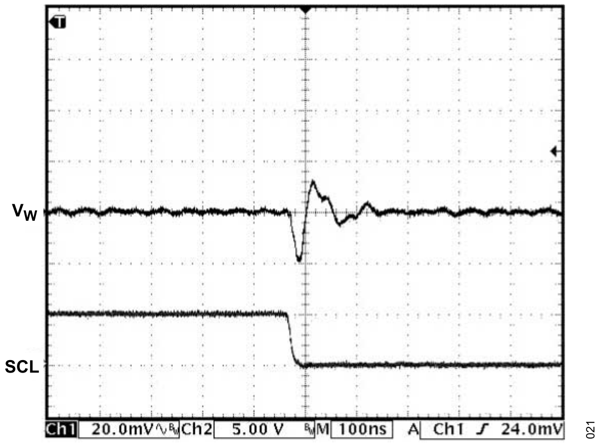


Figure 22. Digital Feedthrough

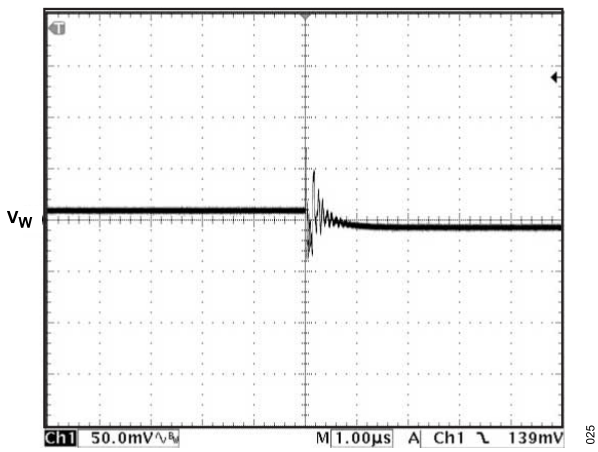


Figure 23. Midscale Glitch, Code 0x80 to Code 0x7F

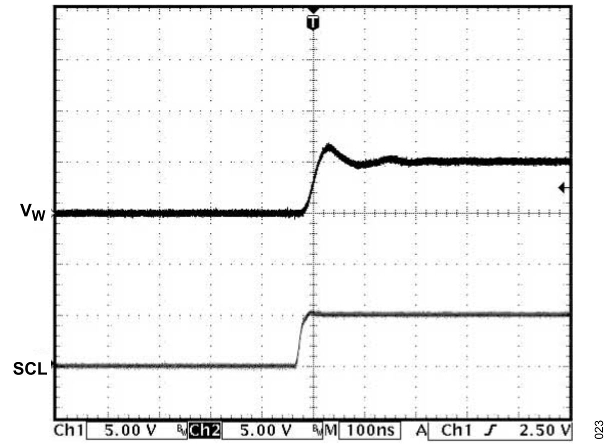


Figure 24. Large Signal Settling Time

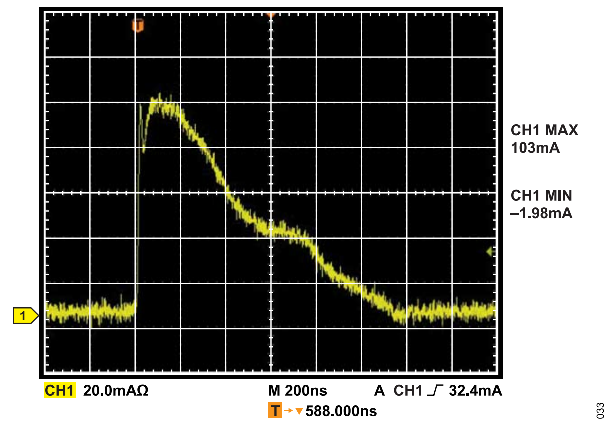


Figure 25. OTP Program Energy Plot for Single Fuse

TEST CIRCUITS

Figure 26 to Figure 31 illustrate the test circuits that define the test conditions used in the product specification tables.

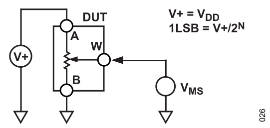


Figure 26. Test Circuit for Potentiometer Divider Nonlinearity Error (INL, DNL)

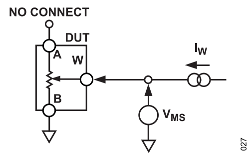


Figure 27. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

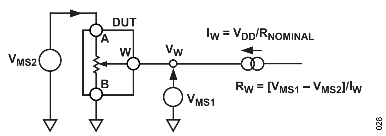


Figure 28. Test Circuit for Wiper Resistance

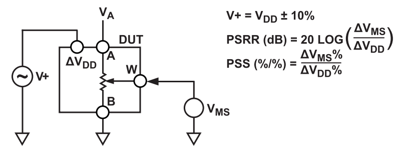


Figure 29. Test Circuit for Power Supply Sensitivity (PSS, PSRR)

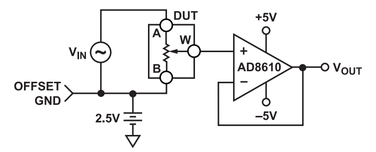


Figure 30. Test Circuit for Gain vs. Frequency

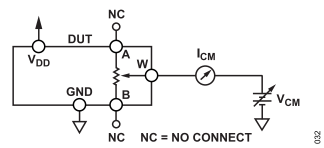


Figure 31. Test Circuit for Common-Mode Leakage Current

THEORY OF OPERATION

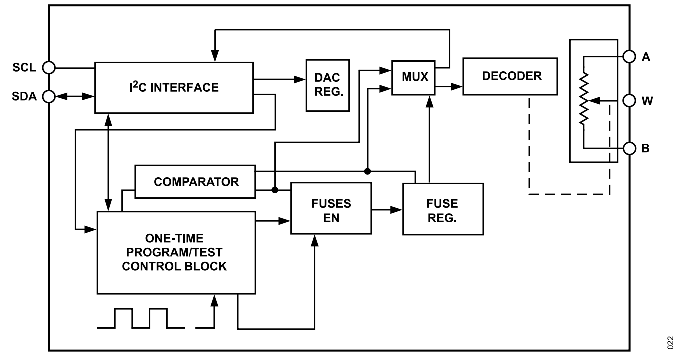


Figure 32. Detailed Functional Block Diagram

The AD5170 is a 256-position, digitally controlled, variable resistor (VR) that employs fuse link technology to achieve memory retention of the resistance setting.

An internal power-on preset places the wiper at midscale during power-on. If the OTP function is activated, the device powers up at the user-defined permanent setting.

ONE-TIME PROGRAMMING (OTP)

Prior to OTP activation, the AD5170 presets to midscale during initial power-on. After the wiper is set at the desired position, the resistance can be permanently set by programming the T bit high along with the proper coding (see Table 9 and Table 11) and one-time V_{DD_OTP}. Note that fuse link technology of the AD517x family of digital potentiometers requires that V_{DD_OTP} between 5.6 V and 5.8 V blow the fuses to achieve a given nonvolatile setting. On the other hand, V_{DD} can be 2.7 V to 5.5 V during operation. For system supplies that are lower than 5.6 V, an external supply for one-time programming is required. Note that the user is allowed only one attempt in blowing the fuses. If the user fails to blow the fuses at the first attempt, the structures of the fuses may have changed such that they can never be blown, regardless of the energy applied at subsequent events. For details, see the Power Supply Considerations section.

The device control circuit has two validation bits, E1 and E0, that can be read back to check the programming status (see Table 6). Users should always read back the validation bits to ensure that the fuses are properly blown. After the fuses are blown, all fuse latches are enabled upon subsequent power-on; therefore, the output corresponds to the stored setting. Figure 32 shows a detailed functional block diagram.

Table 6. Validation Status

E1	E0	Status
0	0	Ready for programming.
1	0	Fatal error. Some fuses are not blown. Do not retry. Discard this unit.
1	1	Successful. No further programming is possible.

PROGRAMMING THE VARIABLE RESISTOR AND VOLTAGE—RHEOSTAT OPERATION

The nominal resistance (R_{AB}) between Terminal A and Terminal B is available in 2.5 kΩ, 10 kΩ, and 50 kΩ. The nominal resistance of the VR has 256 contact points that are accessed by the wiper terminal, plus the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings.

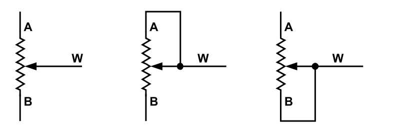


Figure 33. Rheostat Mode Configuration

Assuming that a 10 kΩ part is used, the first connection of the wiper starts at Terminal B for Data 0x00. Because there is a 160 Ω wiper contact resistance, such a connection yields a minimum of 320 Ω (2 × 160 Ω) resistance between Terminal W and Terminal B. The second connection is the first tap point, which corresponds to 359 Ω ($R_{WB} = R_{AB}/256 + 2 \times R_W$ = 39 Ω + 2 × 160 Ω) for Data 0x01. The third connection is the next tap point, representing 398 Ω (2 × 39 Ω + 2 × 160 Ω) for Data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10,281 Ω (R_{AB} − 1 LSB + 2 × R_W).

THEORY OF OPERATION

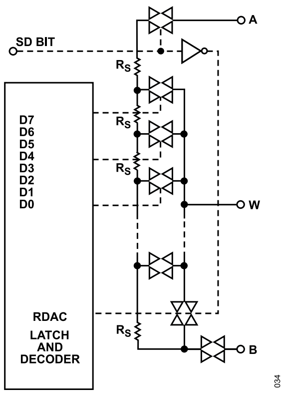


Figure 34. Equivalent RDAC Circuit

The general equation that determines the digitally programmed output resistance between Terminal W and Terminal B is

$$R_{WB}\ (D) = \frac{D}{256} \times R_{AB} + 2 \times R_W \qquad (1)$$

where:
D is the decimal equivalent of the binary code loaded in the 8-bit RDAC register.
R_{AB} is the end to end resistance.
R_W is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if R_{AB} = 10 kΩ and Terminal A is open-circuited, the output resistance, R_{WB}, is set for the RDAC latch codes, as shown in Table 7.

Table 7. Codes and Corresponding R_{WB} Resistance

D (Dec)	R_{WB} (Ω)	Output State
255	10,281	Full scale (R_{AB} − 1 LSB + 2 × R_W)
128	5320	Midscale
1	359	1 LSB
0	320	Zero scale (wiper contact resistance)

Note that in the zero-scale condition, a finite wiper resistance of 160 Ω is present. Take care to limit the current flow between Terminal W and Terminal B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper (Terminal W) and Terminal A also produces a digitally controlled, complementary resistance, R_{WA}. When these terminals are used, Terminal B can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}\ (D) = \frac{256 - D}{256} \times R_{AB} + 2 \times R_W \qquad (2)$$

For R_{AB} = 10 kΩ and Terminal B open circuited, Table 8 shows some examples of the output resistance (R_{WA}) vs. the RDAC latch codes.

Table 8. Codes and Corresponding R_{WA} Resistance

D (Dec)	R_{WA} (Ω)	Output State
255	359	Full scale
128	5320	Midscale
1	10,281	1 LSB
0	10,320	Zero scale

Typical device-to-device matching is process-lot dependent and can vary by up to ±30%. Because the resistance element is processed using thin film technology, the change in R_{AB} with temperature has a very low 35 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER—VOLTAGE OUTPUT OPERATION

The digital potentiometer easily generates a voltage divider at wiper to B and wiper to A proportional to the input voltage at A to B. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across A to B, W to A, and W to B can be at either polarity.

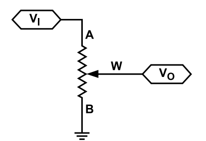


Figure 35. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for approximation, connecting Terminal A to 5 V and Terminal B to ground produces an output voltage at the wiper to B starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across Terminal A and Terminal B divided by the 256 positions of the potentiometer divider. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to Terminal A and Terminal B is

$$V_W(D) = \frac{D}{256}V_A + \frac{256 - D}{256}V_B \qquad (3)$$

For a more accurate calculation, which includes the effect of wiper resistance, V_W, the following equation can be used:

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}}V_A + \frac{R_{WA}(D)}{R_{AB}}V_B \qquad (4)$$

Operation of the digital potentiometer in divider mode results in a more accurate operation over temperature. Unlike rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors, R_{WA} and R_{WB}, and not the absolute values. Therefore, the temperature drift reduces to 15 ppm/°C.

THEORY OF OPERATION

ESD PROTECTION

All digital inputs, SDA, SCL, AD0, and AD1, are protected with a series input resistor and parallel Zener ESD structures, as shown in Figure 36 and Figure 37.

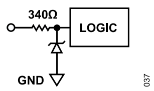


Figure 36. ESD Protection of Digital Pins

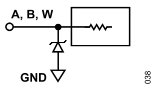


Figure 37. ESD Protection of Resistor Terminals

TERMINAL VOLTAGE OPERATING RANGE

The AD5170 V_{DD}-to-GND power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on Terminal A, Terminal B, and Terminal W that exceed V_{DD} or GND are clamped by the internal forward-biased diodes (see Figure 38).

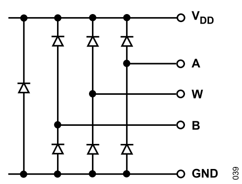


Figure 38. Maximum Terminal Voltages Set by V_{DD} and GND

POWER-UP SEQUENCE

Because the ESD protection diodes limit the voltage compliance at Terminal A, Terminal B, and Terminal W, it is important to power V_{DD}/GND before applying any voltage to Terminal A, Terminal B, and Terminal W (see Figure 38). Otherwise, the diode is forward-biased such that V_{DD} is powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is GND, V_{DD}, the digital inputs, and then $V_A/V_B/V_W$. The relative order of powering V_A, V_B, V_W, and the digital inputs is not important as long as they are powered up after GND/V_{DD}.

POWER SUPPLY CONSIDERATIONS

To minimize the package pin count, both the one-time programming and normal operating voltage supplies share the same V_{DD} terminal of the AD5170. The AD5170 employs fuse link technology that requires 5.6 V to 5.8 V for blowing the internal fuses to achieve a given setting, but normal V_{DD} can be anywhere between 2.7 V and 5.5 V after the fuse programming process. As a result, dual voltage supplies and isolation are needed if system V_{DD} is lower than the required V_{DD_OTP}. The fuse programming supply (either an on-board regulator or rack-mount power supply) must be rated at 5.6 V to 5.8 V and be able to provide a 100 mA current for 400 ms for successful OTP.

When the fuse programming is complete, the V_{DD_OTP} supply must be removed to allow normal operation at 2.7 V to 5.5 V, and the device consumes current in the μA range.

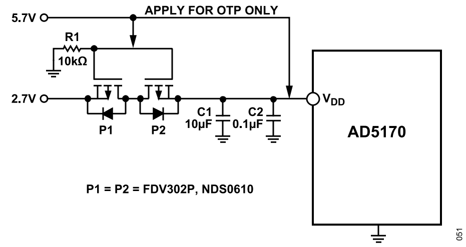


Figure 39. Isolate 5.7 V OTP Supply from 2.7 V Normal Operating Supply

For example, for those who operate their systems at 2.7 V, use of the bidirectional, low threshold, P-Channel MOSFETs is recommended for the isolation of the supply. As shown in Figure 39, this assumes that the 2.7 V system voltage is applied first, and the P1 and P2 gates are pulled to ground, thus turning on P1 and, subsequently, P2. As a result, V_{DD} of the AD5170 approaches 2.7 V. When the AD5170 setting is found, the factory tester applies the V_{DD_OTP} to both the V_{DD} and the MOSFETs gates, turning off P1 and P2. The OTP command is executed at this time to program the AD5170 while the 2.7 V source is protected. When the fuse programming is complete, the tester withdraws the V_{DD_OTP} and the setting for the AD5170 is permanently fixed.

The AD5170 achieves the OTP function by blowing internal fuses. Users should always apply the 5.6 V to 5.8 V one-time-program voltage requirement at the first fuse programming attempt. Failure to comply with this requirement can lead to a change in the fuse structures, rendering programming inoperable.

Care should be taken when SCL and SDA are driven from a low voltage logic controller. Users must ensure that the logic high level is between 0.7 V × V_{DD} and V_{DD} + 0.5 V. Refer to the Level Shifting for Different Voltage Operation section.

Poor PCB layout introduces parasitics that can affect the fuse programming. Therefore, it is recommended to add a 10 μF tantalum capacitor in parallel with a 1 nF ceramic capacitor as close as possible to the V_{DD} pin. The type and value chosen for both capacitors are important. This combination of capacitor values provides both a fast response and larger supply current handling with minimum supply droop during transients. As a result, these capacitors increase the OTP programming success by not inhibiting the proper energy needed to blow the internal fuses. Additionally, C1 minimizes transient disturbance and low frequency ripple, and C2 reduces high frequency noise during normal operation.

LAYOUT CONSIDERATIONS

It is good practice to employ compact, minimum lead length, layout design. The leads to the inputs should be as direct as possible, with a minimum conductor length. Ground paths should have low resistance and low inductance.

THEORY OF OPERATION

Note that the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

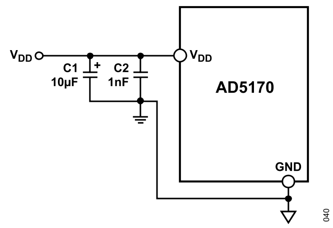


Figure 40. Power Supply Bypassing

CONTROLLING THE AD5170

There are two ways of controlling the AD5170. Users can program the device with either computer software or external I^{2}C controllers.

SOFTWARE PROGRAMMING

Due to the advantages of the one-time programmable feature, consider programming the device in the factory before shipping the final product to the end users. Analog Devices offers device programming software that can be implemented in the factory on PCs running Windows 95 or later. As a result, external controllers are not required, significantly reducing development time. The program is an executable file that does not require knowledge of programming languages or programming skills, and it is easy to set up and to use. Figure 41 shows the software interface. The software can be downloaded from the AD5170 product page.

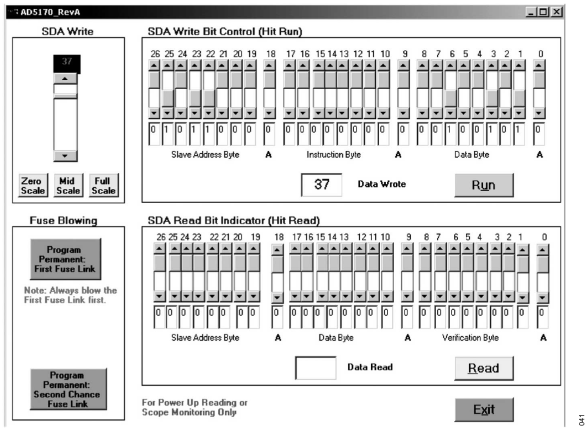


Figure 41. AD5170 Computer Software Interface

CONTROLLING THE AD5170

Write

The AD5170 starts at midscale after power-up prior to OTP programming. To increment or decrement the resistance, move the scroll bars on the left. To write any specific value, use the bit pattern in the upper screen and click **Run**. The format of writing data to the device is shown in Table 9. Once the desired setting is found, click **Program Permanent: First Fuse Link** to blow the internal fuse links.

Table 9. Write Mode

S	0	1	0	1	1	AD1	AD0	$\overline{W}$	A	2T	SD	T	0	OW	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Instruction Byte									Data Byte									

Table 10. SDA Bit Definitions and Descriptions

Bit	Description
S	Start condition.
P	Stop condition.
A	Acknowledge.
AD0, AD1	Package pin-programmable address bits.
X	Don't care.
$\overline{W}$	Write.
R	Read.
2T	Second fuse link array for two-time programming. Logic 0 corresponds to first trim. Logic 1 corresponds to second trim. Note that blowing Trim 2 before Trim 1 effectively disables Trim 1 and, in turn, allows only one-time programming.
SD	Shutdown connects wiper to Terminal B and open circuits Terminal A. It does not change the contents of the wiper register.
T	OTP programming bit. Logic 1 permanently programs the wiper.
OW	Overwrite the fuse setting and program the digital potentiometer to a different setting. Note that upon power-up, the digital potentiometer presets to either midscale or fuse setting, depending on whether the fuse link is blown.
D7, D6, D5, D4, D3, D2, D1, and D0	Data bits.
E1, E0	OTP validation bits:
	0, 0 = ready to program.
	1, 0 = fatal error. Some fuses are not blown. Do not retry. Discard this unit.
	1, 1 = programmed successfully. No further adjustments are possible.

CONTROLLING THE AD5170

Read

Table 11. Read Mode

S	0	1	0	1	1	AD1	AD0	R	A	D7	D6	D5	D4	D3	D2	D1	D0	A	E1	E0	X	X	X	X	X	X	A	P
	Slave Address Byte									Data Byte									Validation Byte									

To read the validation bits and data from the device, click **Read**. The format of the read bits is shown in Table 11.

DEVICE PROGRAMMING

To apply the device programming software in the factory, modify a parallel port cable and configure Pin 2, Pin 3, Pin 15, and Pin 25 for SDA_write, SCL, SDA_read, and DGND, respectively, for the control signals (see Figure 42). Also, lay out the PCB of the AD5170 with SCL and SDA pads, as shown in Figure 43, such that pogo pins can be inserted for factory programming.

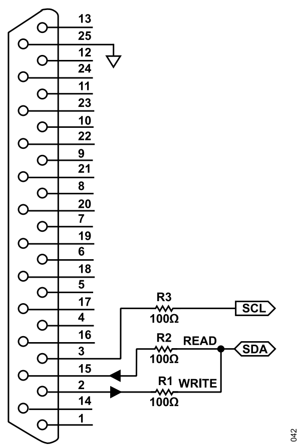


Figure 42. Parallel Port Connection (Pin 2 = SDA_write, Pin 3 = SCL, Pin 15 = SDA_read, and Pin 25 = DGND)

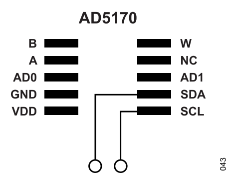


Figure 43. Recommended AD5170 PCB Layout

CONTROLLING THE AD5170

I²C CONTROLLER PROGRAMMING

Write Bit Pattern

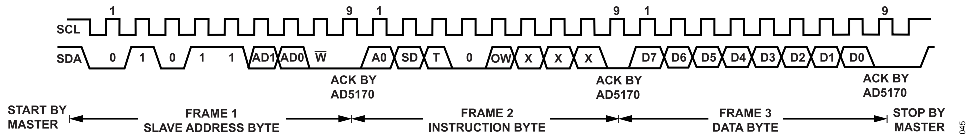


Figure 44. Writing Data to the RDAC Register

Read Bit Pattern

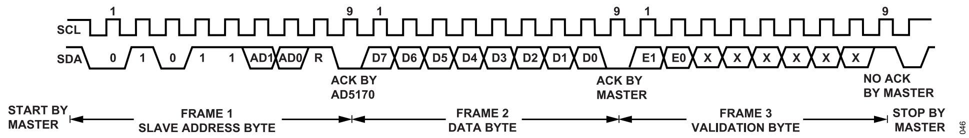


Figure 45. Reading Data from the RDAC Register

I²C-COMPATIBLE, 2-WIRE SERIAL BUS

The following section describes how the 2-wire, I²C serial bus protocol operates (see Figure 44 and Figure 45).

The master initiates a data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 44). The following byte is the slave address byte, which consists of the slave address followed by an R/$\overline{W}$ bit (this bit determines whether data is read from or written to the slave device). AD0 and AD1 are configurable address bits that allow up to four devices on one bus (see Table 9).

The slave address corresponding to the transmitted address bits responds by pulling the SDA line low during the ninth clock pulse (this is called the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its serial register. If the R/$\overline{W}$ bit is high, the master reads from the slave device. If the R/$\overline{W}$ bit is low, the master writes to the slave device.

In write mode, the second byte is the instruction byte. The first MSB of the instruction byte, 2T, is the second trim enable bit. A logic low selects the first array of the fuses, and a logic high selects the second array of the fuses. This means that after blowing the fuses with Trim 1, the user still has another chance to blow them again with Trim 2. Note that using Trim 2 before Trim 1 effectively disables Trim 1 and, in turn, allows only one-time programming.

The second MSB, SD, is a shutdown bit. A logic high causes an open circuit at Terminal A and shorts the wiper to Terminal B. This operation yields almost 0 Ω in rheostat mode or 0 V in potentiometer mode. Note that the shutdown operation does not disturb the contents of the register. When brought out of shutdown, the previous setting is applied to the RDAC. In addition, new settings can be programmed during shutdown. When the part is returned from shutdown, the corresponding VR setting is applied to the RDAC.

The third MSB, T, is the OTP programming bit. A logic high blows the polyfuses and programs the resistor setting permanently. For example, if the user wants to blow the first array of fuses, the instruction byte is 00100XXX. To blow the second array of fuses, the instruction byte is 10100XXX. A logic low of the T bit simply allows the device to act as a typical volatile digital potentiometer.

The fourth MSB must always be Logic 0.

The fifth MSB, OW, is an overwrite bit. When raised to a logic high, OW allows the RDAC setting to be changed even after the internal fuses are blown. However, when OW is returned to Logic 0, the position of the RDAC returns to the setting prior to the overwrite. Because OW is not static, if the device is powered off and on, the RDAC presets to midscale or to the setting at which the fuses were blown, depending on whether the fuses are permanently set.

The remainder of the bits in the instruction byte are don't care bits (see Figure 44).

After acknowledging the instruction byte, the last byte in write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 2).

In read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses (a slight difference from write mode, with eight data bits followed by an acknowledge bit). Similarly, transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 45).

Following the data byte, the validation byte contains two validation bits, E0 and E1. These bits signify the status of the one-time programming (see Figure 45).

CONTROLLING THE AD5170

After all the data bits are read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition (see Figure 44).

In read mode, the master issues a no acknowledge for the 9th clock pulse (that is, the SDA line remains high). The master brings the SDA line low before the 10th clock pulse and then brings the SDA line high to establish a stop condition (see Figure 45).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. For example, after the RDAC has acknowledged its slave address and instruction bytes in write mode, the RDAC output updates on each successive byte. If different instructions are needed, the write/read mode has to start again with a new slave address, instruction, and data byte. Similarly, a repeated read function of the RDAC is also allowed.

Multiple Devices on One Bus

Figure 46 shows four AD5170s on the same serial bus. Each has a different slave address because the states of their AD0 and AD1 pins are different, which allows each device on the bus to be written to or read from independently. The master device output bus line drivers are open-drain pull-downs in a fully I^{2}C-compatible interface.

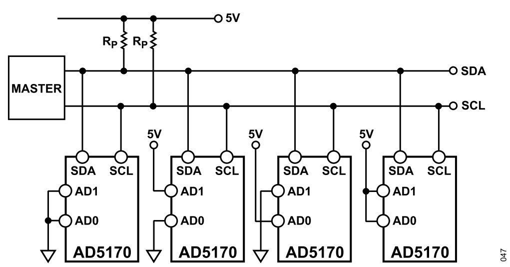


Figure 46. Multiple AD5170s on One I^{2}C Bus

LEVEL SHIFTING FOR DIFFERENT VOLTAGE OPERATION

If the SCL and SDA signals come from a low voltage logic controller and are below the minimum V_{IH} level (0.7 V × V_{DD}), level shift the signals for read/write communications between the AD5170 and the controller. Figure 47 shows one of the implementations. For example, when SDA1 is at 2.5 V, M1 turns off and SDA2 becomes 5 V. When the SDA1 is at 0 V, M1 turns on and the SDA2 approaches 0 V. As a result, proper level shifting is established. M1 and M2 should be low threshold, N-channel power MOSFETs, such as the FDV301N.

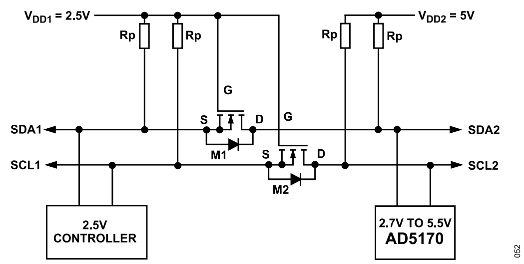


Figure 47. Level Shifting for Different Voltage Operation

OUTLINE DIMENSIONS

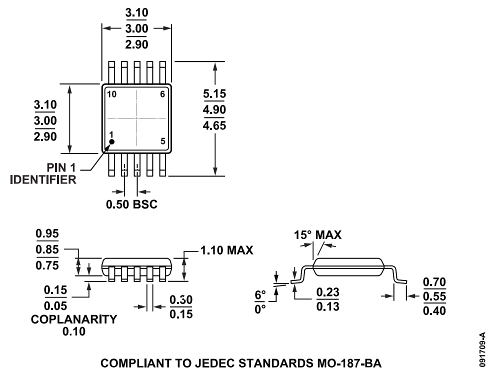


Figure 48. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

Updated: October 11, 2021

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option	Marking Code
AD5170BRMZ10	-40°C to +125°C	10-Lead MSOP	Tube, 50	RM-10	DD4
AD5170BRMZ10-RL7	-40°C to +125°C	10-Lead MSOP	Reel, 1000	RM-10	DD4
AD5170BRMZ2.5	-40°C to +125°C	10-Lead MSOP	Tube, 50	RM-10	DD7
AD5170BRMZ2.5-RL7	-40°C to +125°C	10-Lead MSOP	Reel, 1000	RM-10	DD7
AD5170BRMZ50	-40°C to +125°C	10-Lead MSOP	Tube, 50	RM-10	DD6

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).