S6AP111A28

2ch DC/DC Converter IC with PWM Synchronous Rectification

Description

S6AP111A28 is an Nch MOS drive-compatible 2ch DC/DC Converter IC with synchronous rectification that is equipped with a bottom detection comparator. It supports low on-duty operation to allow stable output of low voltages when there is a large difference between input and output voltages. It supports high-speed responses and achieves high efficiency. CH1 can change the internal reference voltage and is suitable for the power supply of POL.

Features

- High efficiency: 96% (maximum)
- High accuracy reference voltage: +/-0.7% (+25°C)
- Input voltage range: 6V to 28V
- Output voltage setting range: 0.75V to 5.5V
- CH1 reference voltage with built-in variable function
- Built-in boost switch
- Over voltage protection function
- Under voltage protection function
- Over current detection function
- Built-in soft start circuit: 1.4 ms (typical)
- Built-in discharge control circuit
- Built-in synchronous rectification type output steps for Nch MOS FET
- Standby current: 0 μA (typical)
- Small package: TSSOP-24

Applications

- Industrial equipment
- Multi-function printers
- Storage devices
- Servers and PCs

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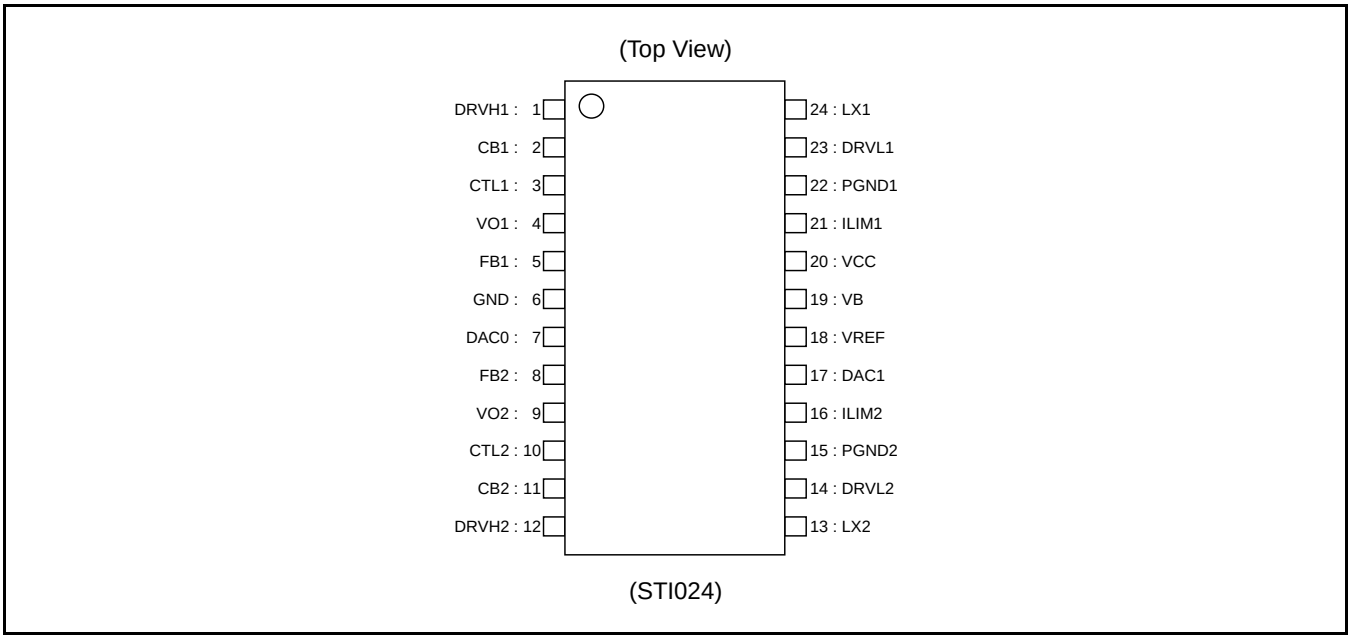
1. Pin Assignment

Figure 1-1. Pin Assignment



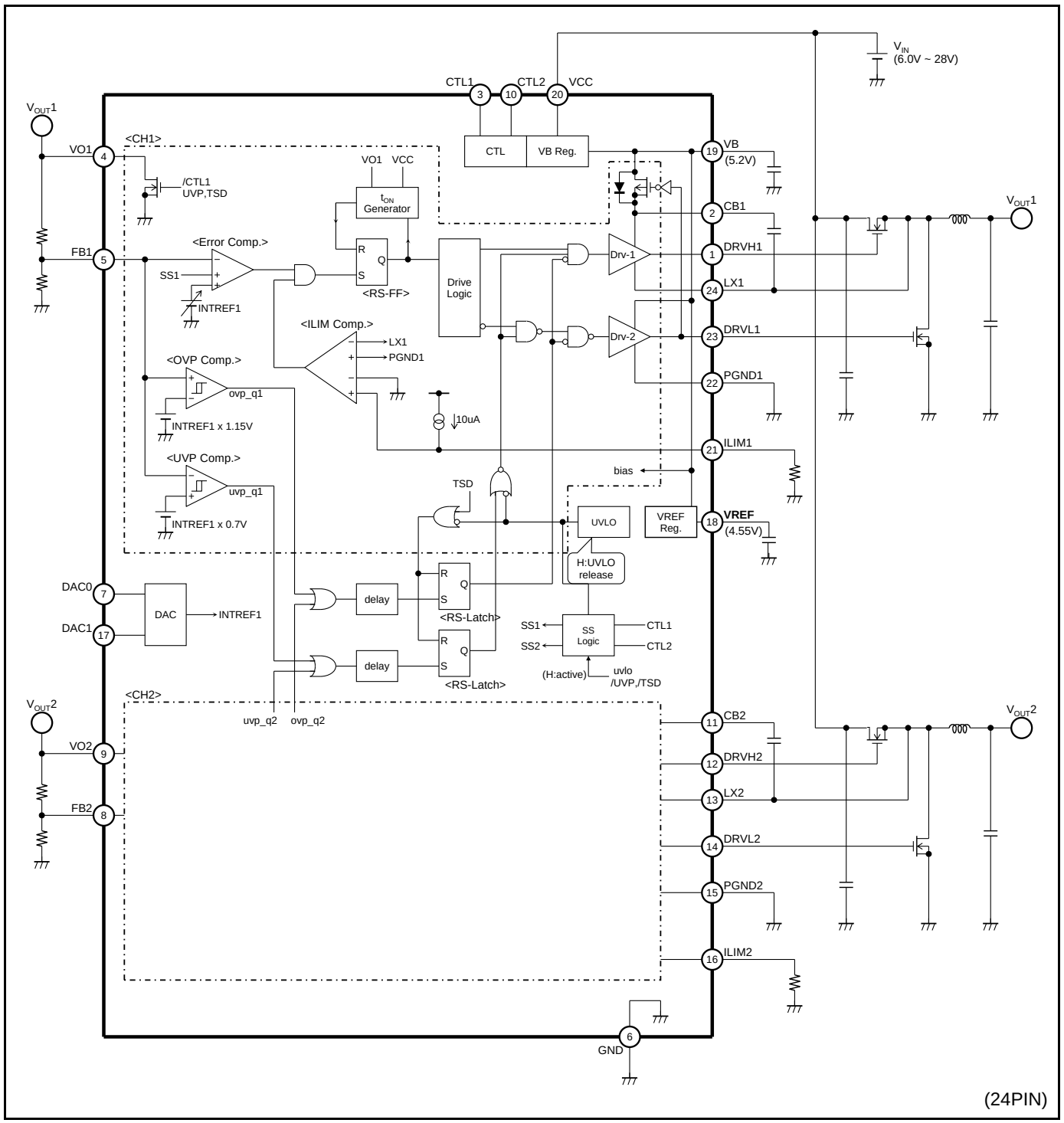
2. Pin Descriptions

Table 2-1. Pin Descriptions

Pin Number	Pin Name	I/O	Function Description
1	DRVH1	O	CH1 output pin for external high side FET gate drive.
2	CB1	-	CH1 bootstrap capacitor connection pin.
3	CTL1	I	CH1 control pin.
4	VO1	I	CH1 input pin for DC/DC output voltage.
5	FB1	I	CH1 feedback pin for DC/DC output voltage.
6	GND	-	Ground pin.
7	DAC0	I	CH1 DAC input pin for change the internal reference voltage.
8	FB2	I	CH2 feedback pin for DC/DC output voltage.
9	VO2	I	CH2 input pin for DC/DC output voltage.
10	CTL2	I	CH2 control pin.
11	CB2	-	CH2 bootstrap capacitor connection pin.
12	DRVH2	O	CH2 output pin for external high side FET drive.
13	LX2	-	CH2 inductor and external high side FET source connection pin.
14	DRVL2	O	CH2 output pin for external synchronous rectification-side FET gate drive.
15	PGND2	-	Ground pin for CH2 output circuit.
16	ILIM2	I	CH2 over current detection level setting voltage input pin.
17	DAC1	I	CH1 DAC input pin for change the internal reference voltage.
18	VREF	O	Control circuit bias output pin.
19	VB	O	Output circuit bias output pin.
20	VCC	I	Power supply pin for the reference voltage and control circuit.
21	ILIM1	I	CH1 over current detection level setting voltage input pin.
22	PGND1	O	Ground pin for CH1 output circuit.
23	DRVL1	O	CH1 output pin for external synchronous rectification-side FET gate drive.
24	LX1	-	CH1 inductor and external high side FET source connection pin.

3. Block Diagram

Figure 3-1. Block Diagram



4. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		
			Min	Max	Unit
Power supply voltage	V_{VCC}	-	-0.3	+36	V
CB pin input voltage	V_{CB}	CB1 and 2 pins	-0.3	+42	V
LX pin input voltage	V_{LX}	LX1 and 2 pins	-2.0	+36	V
Voltage between CB and LX	V_{CBLX}	-	-0.3	+6.9	V
Control input voltage	V_I	CTL1 and 2 pins	-0.3	+30	V
Input voltage	V_{FB}	FB1 and 2 pins	-0.3	+6.9	V
	V_{VO}	VO1 and 2 pins	-0.3	+6.9	V
	V_{ILIM}	ILIM 1 and 2 pins	-0.3	+6.9	V
	V_{DAC}	DAC 0 and 1 pins	-0.3	+6.9	V
Power Dissipation[*1]	P_D	Ta ≤ +25°C	0	1333	mW
Storage temperature	T_{STG}	-	-55	+125	°C

*1: Given that the IC is mounted on four-layer FR-4 board.

WARNING:

1. Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

5. Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{VCC}	-	6	-	28	V
CB pin input voltage	V_{CB}	-	-	-	V_{VCC} +VB	V
CTL pin input voltage	V_I	CTL1 and 2 pins	0	-	28	V
Input voltage	V_{FB}	FB1 and 2 pins	0	-	VREF	V
	V_{VO}	VO1 and 2 pins	0	-	VB	V
	V_{ILIM}	ILIM1 and 2 pins	30	-	200	mV
	V_{DAC}	DAC0 and 1 pins	0	-	VB	V
Peak output current	I_{OUT}	DRVH1 and 2 pins, DRVL1 and 2 pins Duty ≤ 5% (t = 1/f_{OSC}xDuty)	-1200	-	+1200	mA
CB pin capacity	C_{CB}	-	-	0.1	1.0	µF
Bias voltage output capacity	C_{VB}	-	-	2.2	10	µF
Reference voltage output capacity	C_{REF}	-	-	1.0	4.7	µF
Operating ambient temperature	Ta	-	-40	+25	+85	°C

WARNING:

1. The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.
2. Any use of semiconductor devices will be under their recommended operating condition.
3. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
4. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

6. Electrical Characteristics

VCC = 12V, CTL1,2 = 5V, Ta = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Bias Voltage Block [VB Reg.]						
Output voltage	V_{VB}	-	5.04	5.20	5.36	V
Input stability	LINE	VCC = 6V to 28V	-	10	100	mV
Load stability	LOAD	VB = 0A to -1 mA	-	10	100	mV
Short circuit output current	I_{OS}	VB = 0V	-220	-140	-100	mA
Bias Voltage Block [VREF Reg.]						
VREF output voltage	VVREF	VREF pin	4.45	4.55	4.65	V
Under Voltage Lock Out Protection [UVLO]						
UVLO VB Threshold voltage	V_{TLH}	VB pin	3.9	4.2	4.5	V
	V_{THL}	VB pin	3.3	3.6	3.9	V
Hysteresis width	V_H	VB pin	-	0.6(*1)	-	V
UVLO VREF Threshold voltage	V_{TLH}	VREF pin	3.5	3.8	4.1	V
	V_{THL}	VREF pin	3.3	3.6	3.9	V
Hysteresis width	V_H	VREF pin	-	0.2(*1)	-	V
Soft start/Discharge Block [Soft-Start, Discharge]						
Soft start time	t_{SS}	FB1, 2 = 0.735V	0.9	1.4	1.9	ms
Electrical discharge resistance	R_D	CTL1,2 = 0V, VO1, 2 = 0.5V	-	35	70	Ω
Discharge end voltage	V_O	CTL1,2 = 0V, VO1, 2 pins	0.1	0.2	0.3	V
ON/OFF Time Generator Block [t_{ON} Generator]						
ON time	t_{ON1}	VCC = 12V, VO1 = 1.2V	320	400	480	ns
	t_{ON2}	VCC = 12V, VO2 = 1.8V	320	400	480	ns
Minimum ON time	t_{ONMIN}	VCC = 12V, VO1, 2 = 0V	-	140	170	ns
Minimum OFF time	t_{OFFMIN}	-	-	380	560	ns
Error Comparison Block [Error Comp.]						
Threshold voltage [Ch1]	V_{TH11}	DAC1, DAC0 = 0,0 DC threshold	0.797	0.802	0.807	V
	V_{TH12}	DAC1, DAC0 = 0,1 DC threshold	0.829	0.834	0.839	V
	V_{TH13}	DAC1, DAC0 = 1,0 DC threshold	0.862	0.867	0.872	V
	V_{TH14}	DAC1, DAC0 = 1,1 DC threshold	0.765	0.770	0.775	V
Threshold voltage [Ch2]	V_{TH2}	DC threshold	0.768	0.773	0.778	V
FB pin input current	I_{FB}	FB1, 2 = 0.8V	-0.1	0	0.1	µA
VO pin input current	I_{VO}	VO1, 2 = 2V	-	20	29	µA

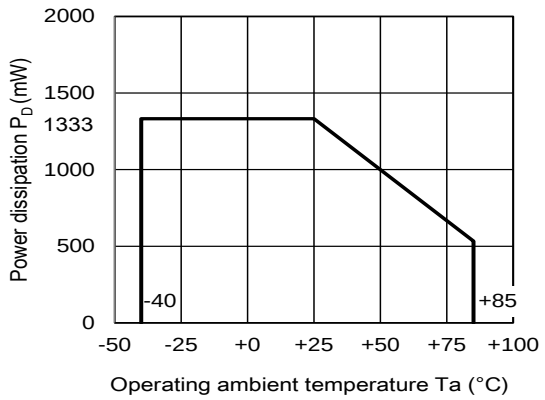
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Over voltage Protection Circuit Block [OVP Comp.]						
Over voltage detecting voltage	V_{OVP}	Error Comp. input	INTREF ×1.11	INTREF ×1.15	INTREF ×1.19	V
Over voltage detection delay time	t_{OVP}	-	-	50(*1)	-	µs
Under voltage Protection Circuit Block [UVP Comp.]						
Under voltage detecting voltage	V_{UVP}	Error Comp. input	INTREF ×0.65	INTREF ×0.70	INTREF ×0.75	V
Under voltage detection delay time	t_{UVP}	-	1.2(*1)	1.7(*1)	2.2(*1)	ms
Thermal shutdown Protection Circuit Block [TSD]						
Protection temperature	T_{TSDH}	-	-	+150(*1)	-	°C
	T_{TSDL}	-	-	+125(*1)	-	°C
DAC Block [DAC]						
DAC input "H" condition	V_{IH}	DAC1, DAC0 pins	2.64	-	VB	V
DAC input "L" condition	V_{IL}	DAC1, DAC0 pins	0	-	0.66	V
Output Block [DRV]						
High side output on resistance	R_{OH}	DRVH1, 2 = -100 mA	-	5	7	Ω
	R_{OL}	DRVH1, 2 = 100 mA	-	1.5	2.5	Ω
Low side output on resistance	R_{OH}	DRVL1, 2 = -100 mA	-	4	6	Ω
	R_{OL}	DRVL1, 2 = 100 mA	-	1	2	Ω
Output source current	I_{SOURCE}	LX1, 2 = 0V, CB1, 2 = VB DRVH1, 2 = 2.5 DUTY ≤ 5%	-	-0.4(*1)	-	A
		LX1, 2 = 0V, CB1, 2 = VB DRVL1, 2 = 2.5V DUTY ≤ 5%	-	-0.5(*1)	-	A
Output sink current	I_{SINK}	LX1, 2 = 0V, CB1, 2 = VB DRVH1, 2 = 2.5V DUTY ≤ 5%	-	0.7(*1)	-	A
		LX1, 2 = 0V, CB1, 2 = VB DRVL1, 2 = 2.5V DUTY ≤ 5%	-	0.9(*1)	-	A
Deadtime	T_D	LX1, 2 = 0V, BST1, 2 = VB	-	30(*1)	-	ns
Boost switch on resistance	R_{BST}	IVB = 30 mA	-	30	40	Ω
Leakage current	I_{LEAK}	CB1, 2 = 33.2V, LX1, 2 = 28V	-	0.1	1	µA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Over Current Detection Block [Current Sense]						
ILIM pin source current	I_{ILIM}	ILIM1, 2 = 0.1V	-12.5	-10	-8.3	µA
ILIM pin source current Temperature slope	T_{ILIM}	-	-	4200(*1)	-	ppm /°C
Overcurrent detection offset voltage	$V_{OFFILIM}$	ILIMx − (PGNDx−LXx) PGNDx − LX = 60 mV	-20	0	20	mV
Overcurrent detection Setting range	V_{ILIM}	ILIM input	30	-	200	mV
Control Block [CTL1, 2]						
On condition	V_{ON}	CTL1,2 pin	2	-	28	V
Off condition	V_{OFF}	CTL1,2 pin	0	-	0.8	V
Hysteresis width	V_H	CTL1,2 pin	-	0.4(*1)	-	V
Input current	I_{CTLH}	CTL1,2 = 5V	-	25	40	µA
	I_{CTLL}	CTL1,2 = 0V	-	0	1	µA
All Devices						
Standby current	I_{CCS}	VCC = 12V, CTL1,2 = 0V	-	0	10	µA
Power supply current	I_{CC}	VCC = 12V, LX1, 2 = 0V, FB1, 2 = 1.0V	-	1.3	1.8	mA

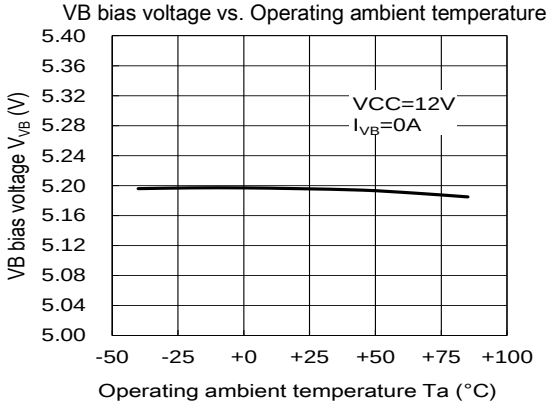
*1: This parameter is not be specified. This should be used as a reference to support designing the circuits.

7. Typical Characteristics

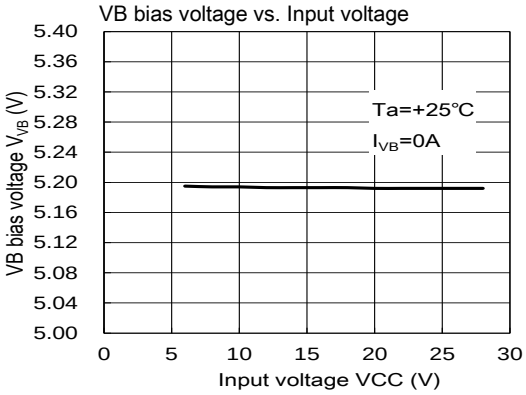
Power dissipation vs. Operating ambient temperature



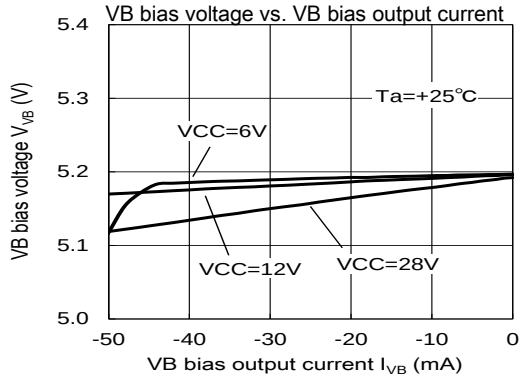
VB bias voltage vs. Operating ambient temperature



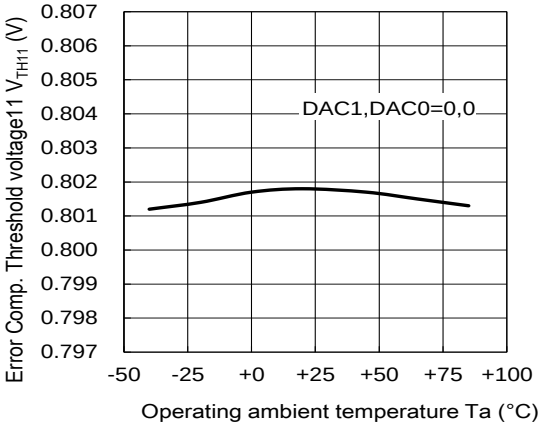
VB bias voltage vs. Input voltage



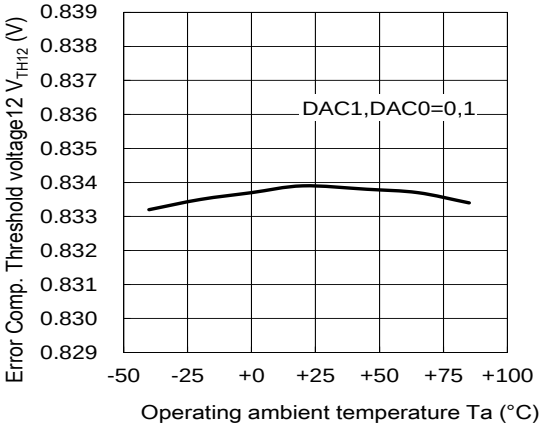
VB bias voltage vs. VB bias output current



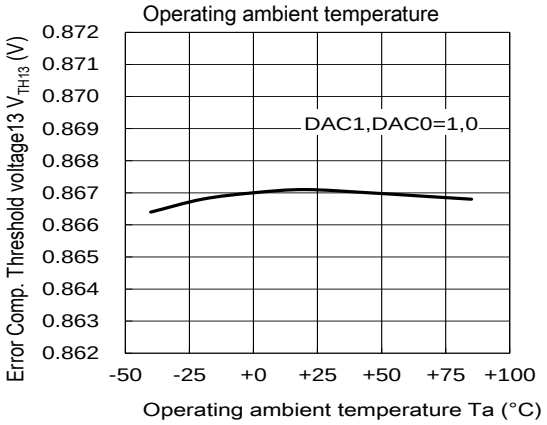
Error Comp. Threshold voltage (V_{TH11}) vs. Operating ambient temperature



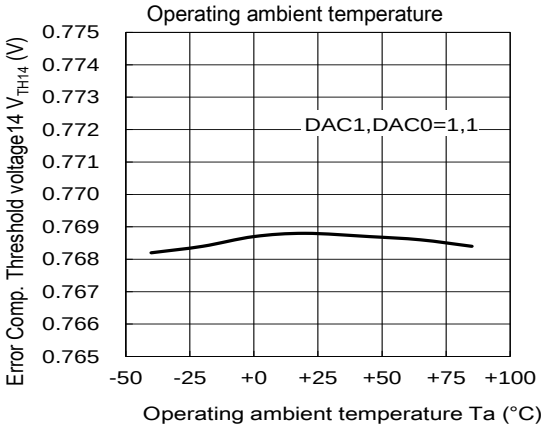
Error Comp. Threshold voltage (V_{TH12}) vs. Operating ambient temperature



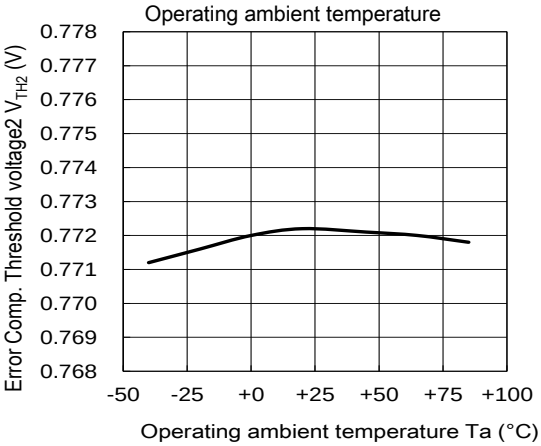
Error Comp. Threshold voltage (V_{TH13}) vs. Operating ambient temperature



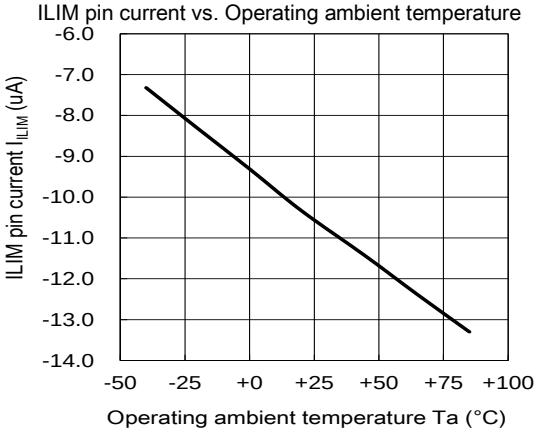
Error Comp. Threshold voltage (V_{TH14}) vs. Operating ambient temperature



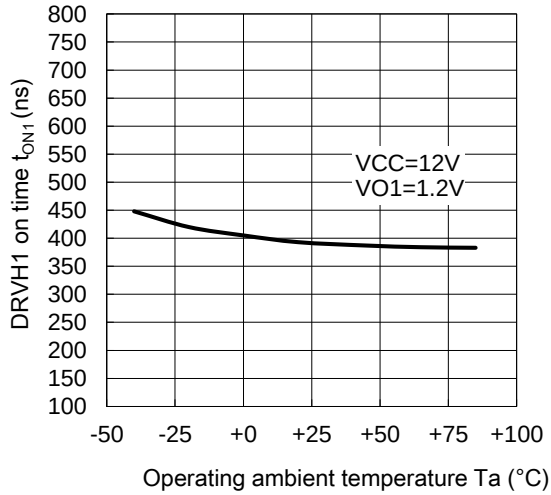
Error Comp. Threshold voltage (V_{TH2}) vs. Operating ambient temperature



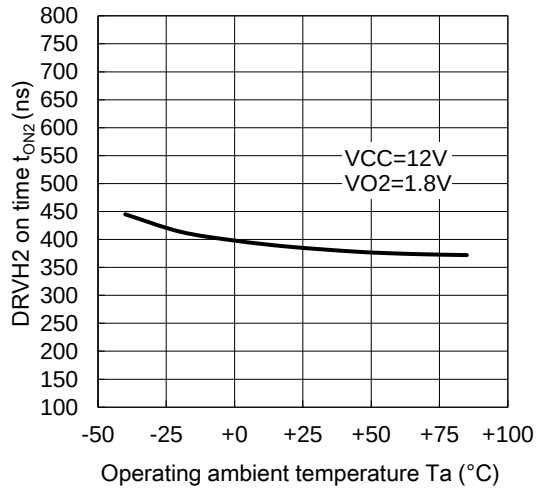
ILIM pin current vs. Operating ambient temperature



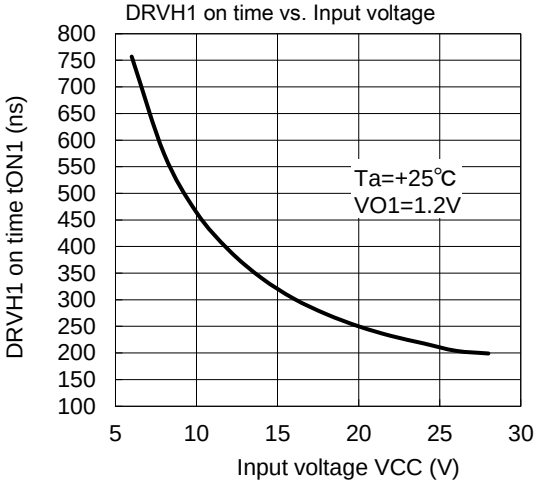
DRVH1 on time vs. Operating ambient temperature



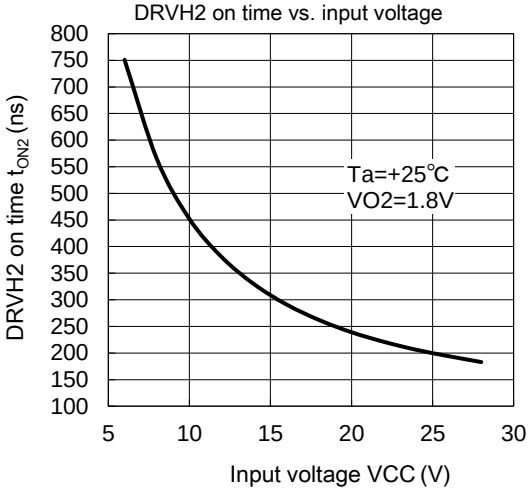
DRVH2 on time vs. Operating ambient temperature



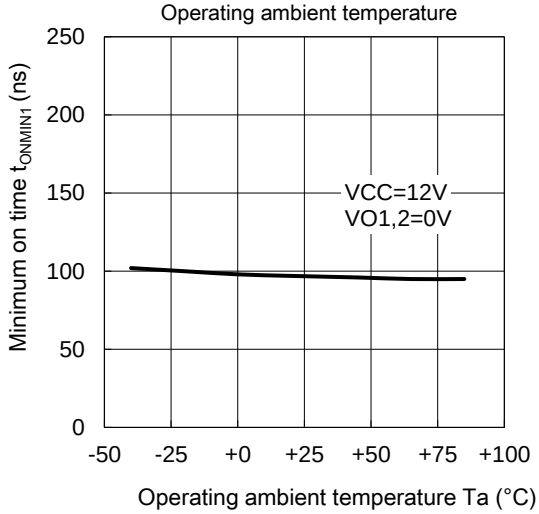
DRVH1 on time vs. Input voltage



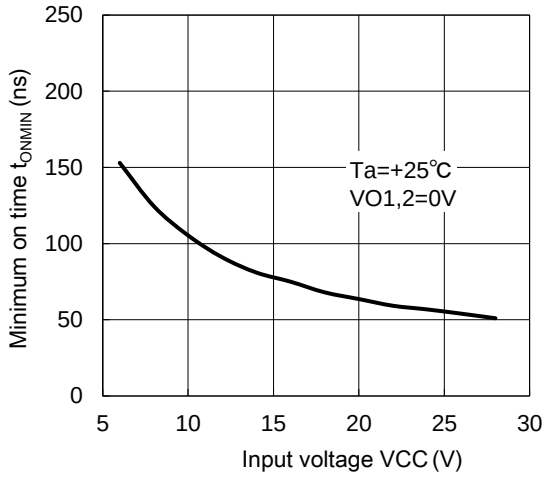
DRVH2 on time vs. input voltage



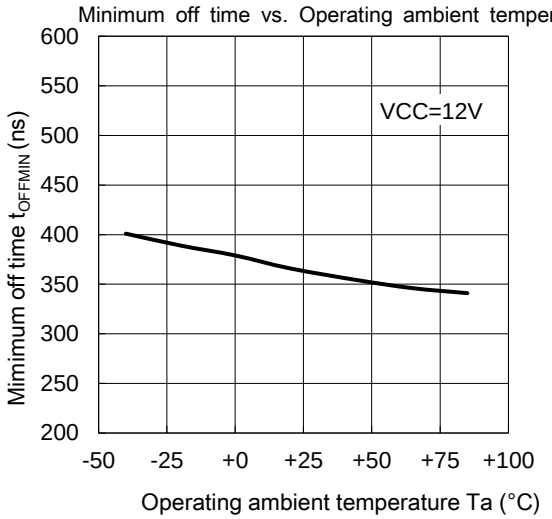
Minimum on time vs.
Operating ambient temperature



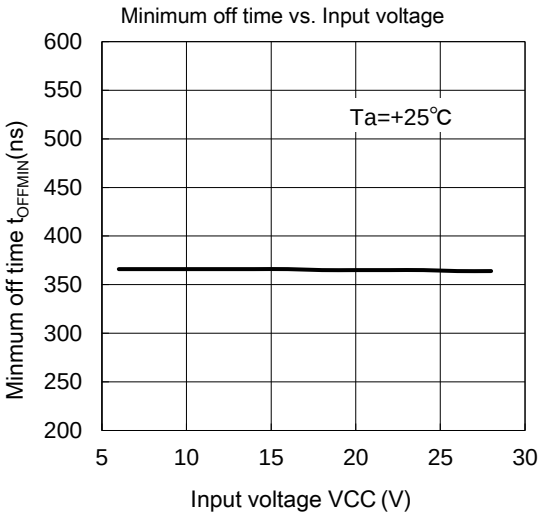
Minimum on time vs. Input voltage

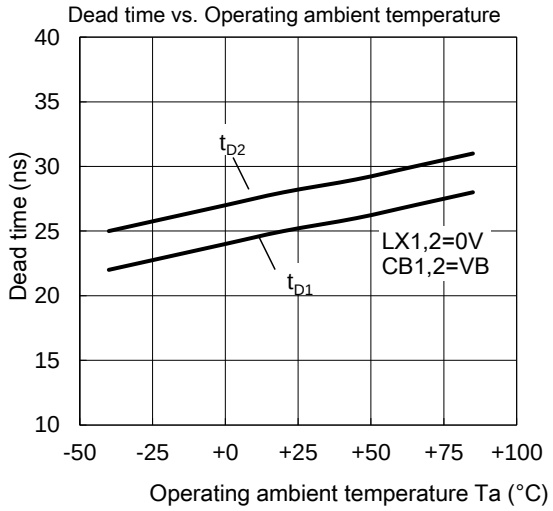


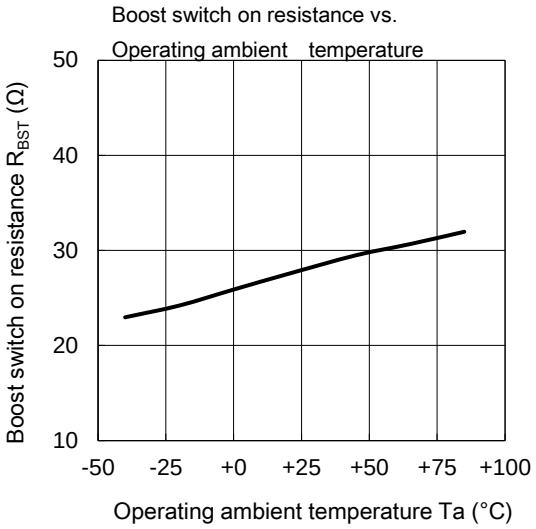
Minimum off time vs. Operating ambient temper



Minimum off time vs. Input voltage







t_{D1} : period from DRVL off to DRVH on

t_{D2} : period from DRVH off to DRVL on

8. Function Description

8.1 Bottom Detection Comparator System

The bottom detection comparator system for low output voltage ripple determines the ON time (t_{ON}) using the input voltage (V_{IN}) and output voltage (V_{OUT}) and holds the ON state for a specified period. During the OFF period, the reference voltage (INTREF) is compared with the feedback voltage (FB) using the error comparator (Error Comp.). When the feedback voltage (FB) is below the reference voltage (INTREF), RS-FF is set and the ON period starts again. Switching is repeated as described above. Error Comp. is used to compare the reference voltage (INTREF) with the feedback voltage (FB) to control the off time in order to stabilize the output voltage.

This system adds the inductor current slope detected during the synchronous rectification period (t_{OFF}) to the reference voltage (INTREF), and generates an output voltage slope in the IC during the OFF period, which is essential for the bottom detection comparator system. This enables the stable control operations under the low output voltage ripple conditions.

Figure 8-1. Circuit Diagram

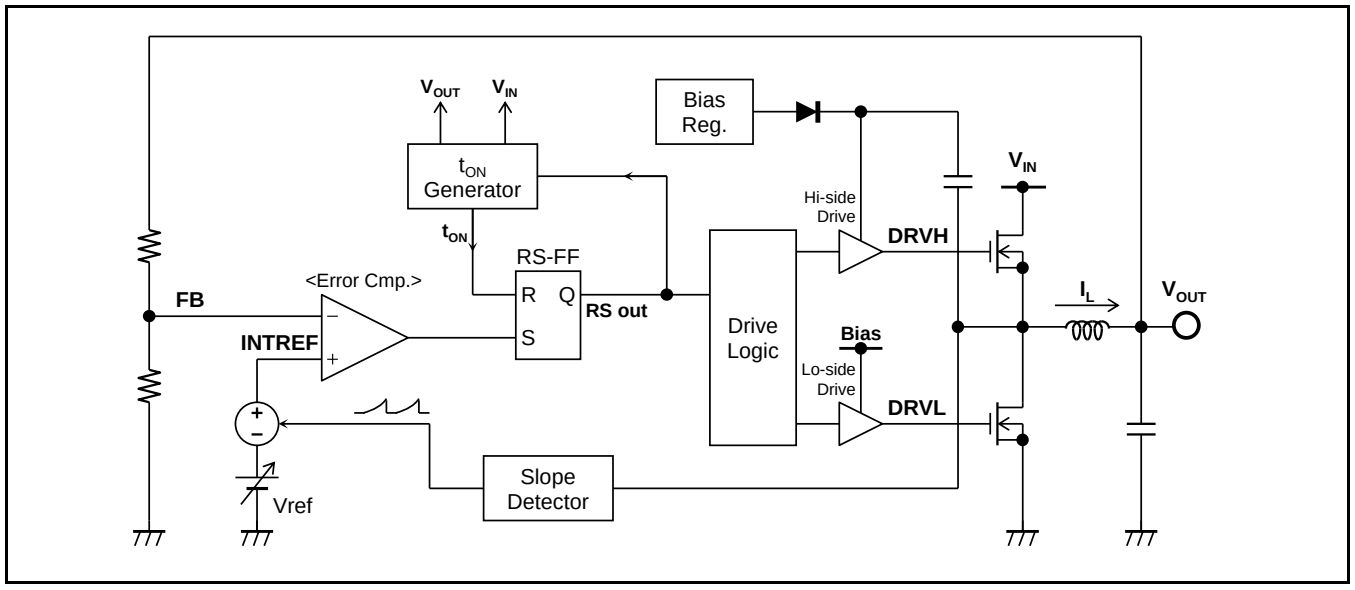
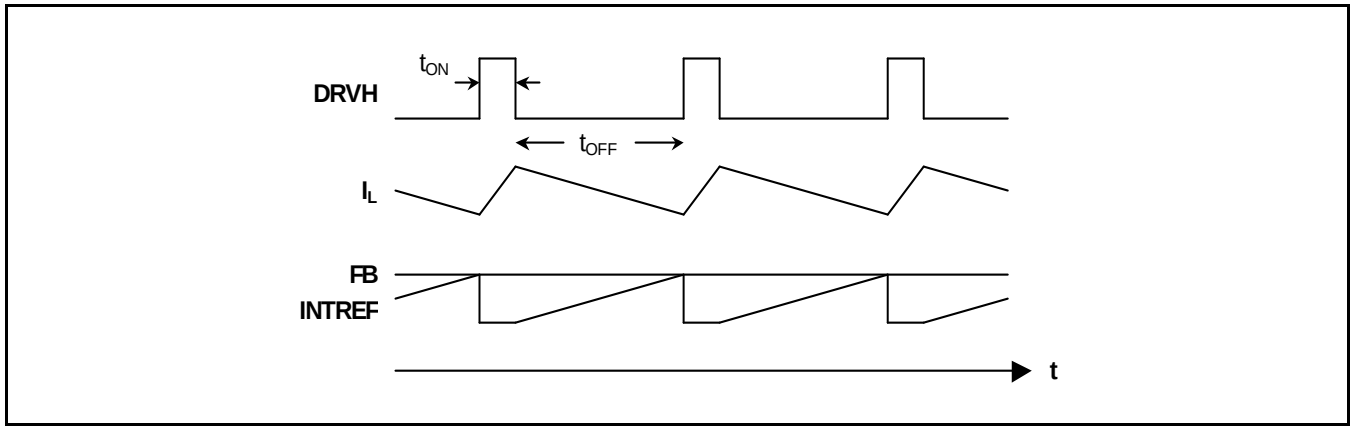


Figure 8-2. Bottom Detecting Operation



8.2 Bias Voltage Block [VB Reg., VREF Reg.]

VB Reg. generates 5.2V (typical) bias voltage from the VCC pin voltage for the control, output, and boost circuits. When either or both of the CTL1 or CTL2 pins (pins 3 and 10) are set to the “H” level, the system is restored from the standby state to supply the bias voltage from the VB pin (pin 19).

VREF Reg. generates a temperature compensating stable voltage of 4.55 V (typical) from the VREF pin (pin 18) which is used as the reference voltage in the IC and the bias power supply for the control circuit.

8.3 Under Voltage Lockout Protection Circuit Block (UVLO)

A transitional state or an instantaneous drop when the bias voltage (V_{VB}) for the control circuit starts will evoke malfunction of the IC and will cause system destruction or degradation. To avoid this sort of malfunction, the under voltage lockout protection detects a voltage drop in the VB pin (pin 19) and fixes the DRVH1 pin (pin 1), DRVH2 pin (pin 12), DRVL1 pin (pin 23), and DRVL2 pin (pin 14) to Level "L." The system recovers when the VB pin voltage exceeds the 4.2V threshold voltage (typical) of the under voltage lockout protection circuit.

8.4 Soft Start/Discharge Block (Soft Start, Discharge)

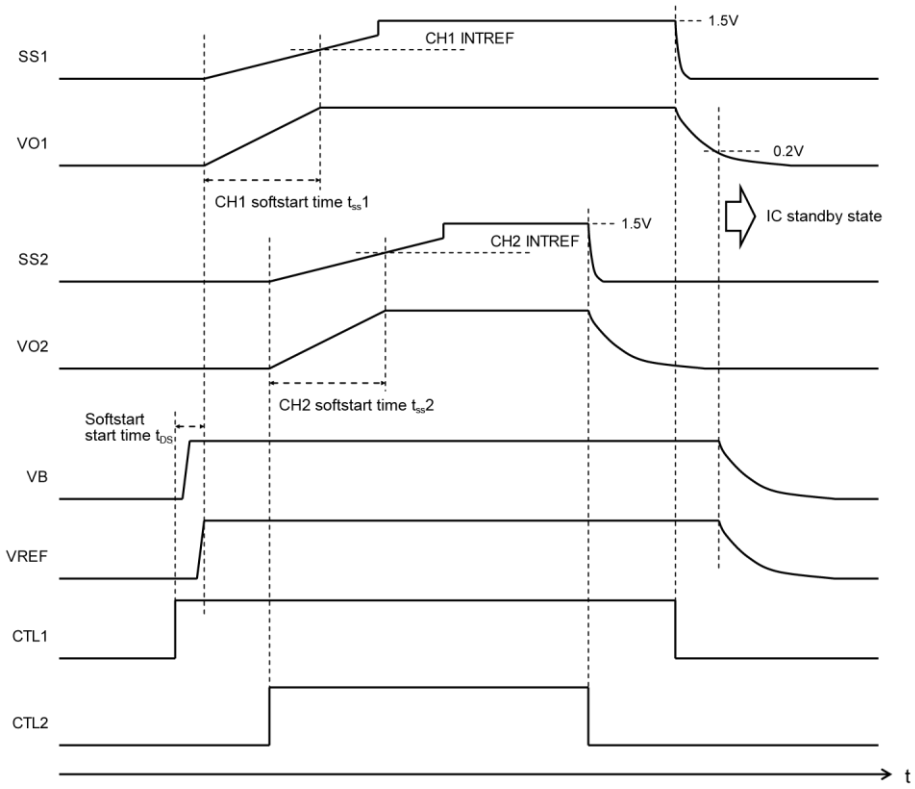
The soft start block is a circuit that prevents inrush current when powering on the IC.

When the CTL1 pin (pin 3) and CTL2 pin (pin 10) are set to Level "H," the reference voltage (SS1) for the CH1 error comparator and the reference voltage (SS2) for the CH2 error comparator start to increase in the soft start circuit built in to the IC. The reference voltages SS1 and SS2 increase linearly until the INTREF1 and INTREF2 voltages with the formula in Figure 10-3(tss1 and tss2). The system soft starts independent of the DC/DC convertor output load because the DC/DC convertor output increase with the same slope of the reference voltage.

From the time that the soft start commences until the initial switching commences, the low side FET stays OFF. The low side FET is allowed to come on after high side FET switching commences.

When the CTL1 pin (pin 3) and CTL2 pin (pin 10) are set to Level "L," the output capacitor discharges based on the FET(R_{ON}≈35Ω) for the discharge built in to the IC. When the VO1 pin (pin 4) and VO2 pin (pin 9) voltage becomes less than 0.2 V (typical) as a result of output capacitor discharge, the IC shuts down and transitions to standby. In addition, the discharge function operates both after under voltage protection circuit block (UVP Comp.) latch setting and after thermal shutdown protection circuit block (TSD) over temperature detection.

Figure 8-3. Example Timing Chart for Soft Start/Discharge



Channel	DAC0	DAC1	tss1
CH1	0V	0V	1.5 ms typ
	VB	0V	1.6 ms typ
	0V	VB	1.7 ms typ
	VB	VB	1.5 ms typ

Channel	DAC0	DAC1	tss2
CH2	-	-	1.5 ms typ

tss1,2 is calculated using the following formula.

$$tss1,2(ms) = tss(ms) \times \frac{V_{INTREF}}{0.735}$$

tss1,2: Soft start time of DC/DC converter CH1,2

tss: Soft start time (1.4 ms typical), which is specified at "6. Electrical Characteristics "

INTREF: Internal reference voltage (DC threshold) [V], which is referred at " V_{TH} in 6. Electrical Characteristics "

8.5 ON/OFF Time Generator Block (t_{ON} Generator)

The ON/OFF time generator block (t_{ON} Generator) has a built-in capacitor for timing setting and a resistor for timing setting and generates ON time which depends on input voltage and output voltage, and a minimum 380 ns (typical) OFF time.

The ON time is set from the voltage value for VCC pin (pin 20), input pin VO1 (pin 4) and the VO2 pin (pin 9) for the output voltage for each channel, using the following formula. To avoid beats from frequency discrepancies between both channels, the CH2 frequency is set to 1.5 times the CH1 frequency.

$$When\ \left(\frac{V_{VO1}}{V_{VCC}} \geq 0.035\right), t_{ON1}(ns) = \frac{V_{VO1}}{V_{VCC}} \times 4000\ ,\ f_{OSC1} \cong 250\ kHz$$

$$When\ \left(\frac{V_{VO2}}{V_{VCC}} \geq 0.052\right), t_{ON2}(ns) = \frac{V_{VO2}}{V_{VCC}} \times 2667,\ f_{OSC2} \cong 375\ kHz$$

The ON time is set so that it does not become less than the minimum 140 ns (typical). Therefore, when a soft start commences or when the input/output voltage ratio is small, the ON time operates at a minimum of 140 ns (typical).

$$When\ \left(\frac{V_{VO1}}{V_{VCC}} \leq 0.035\right), t_{ON1}(ns) = t_{ONMIN} = 140\ (typical)$$

$$When\ \left(\frac{V_{VO2}}{V_{VCC}} \leq 0.052\right), t_{ON2}(ns) = t_{ONMIN} = 140\ (typical)$$

8.6 Error Comparison Block (Error Comp.)

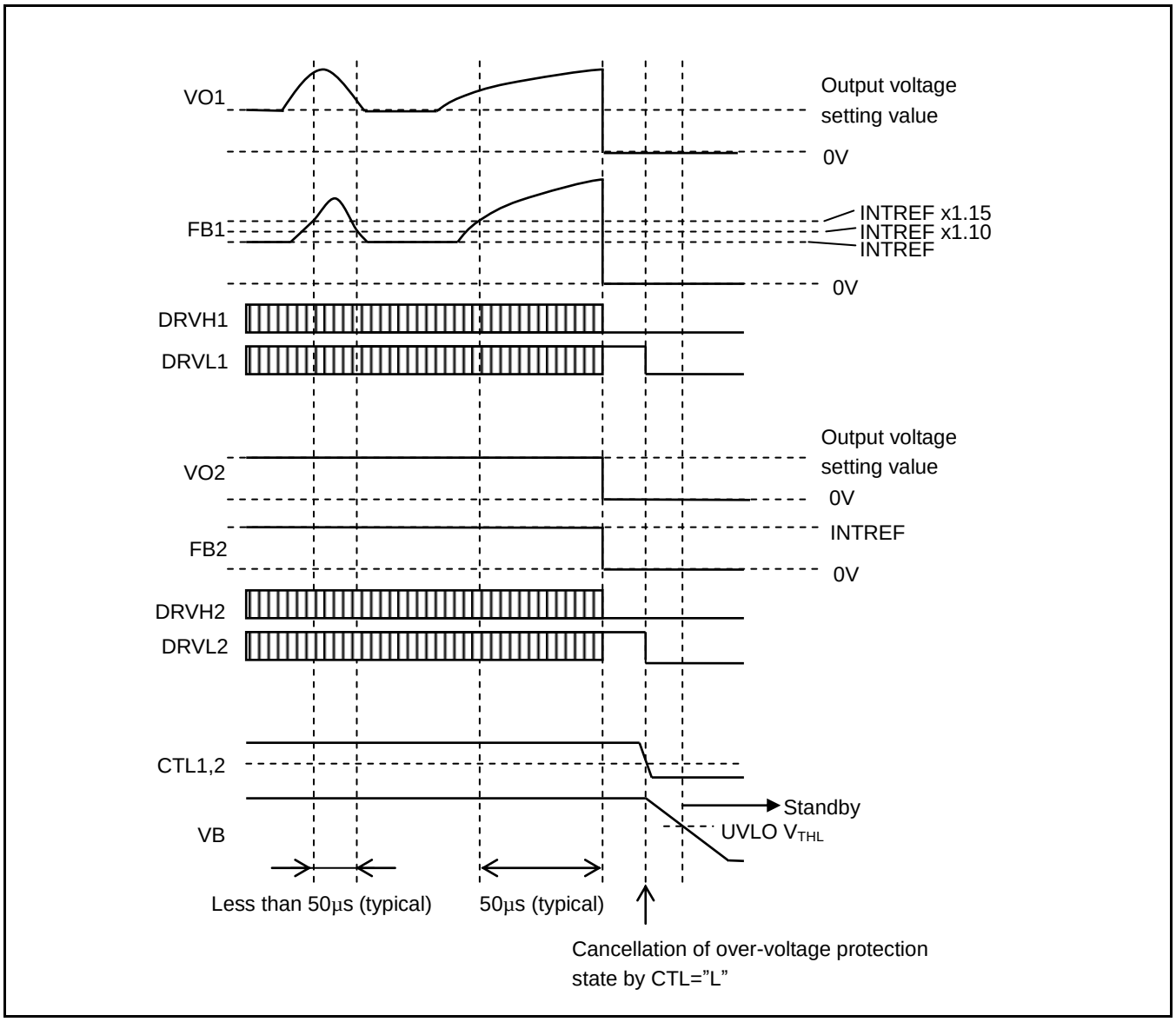
The error comparison block (Error Comp.) detects the bottom value of the output voltage ripple in the DC/DC converter.

You can set the output voltage flexibily(0.75V to 5.5V) by connecting an external output voltage setting resistor to FB1 (pin 5) and FB2 (pin 8).

8.7 Over Voltage Protection Circuit Block (OVP Comp.)

This function stops the output voltage when the DC/DC output voltage has increased, and protects devices connected to the output. This function compares the voltage that is 1.15 times (typical) the INTREF internal reference voltage with the feedback voltage that is input in the FB1 pin (pin 5) and the FB2 pin (pin 8). If the feedback voltage is found to be at least 50 μs (typical) higher, the RS latch is set, the DRVH1 pin (pin 1) and DRVH2 pin (pin 12) are set to Level "L", and the DRVL1 pin (pin 23) and DRVL2 pin (pin 14) are set to Level "H." The voltage output stops because these operations fix the high side FET to the off state and the low side FET to the on state for both channels of the DC/DC converter. Further, there is 5% (typical) hysteresis in the threshold for the over voltage protection operation to avoid malfunction of the over voltage protection function.

Figure 8-4. Example Timing Chart for the Over Voltage Protection Operation



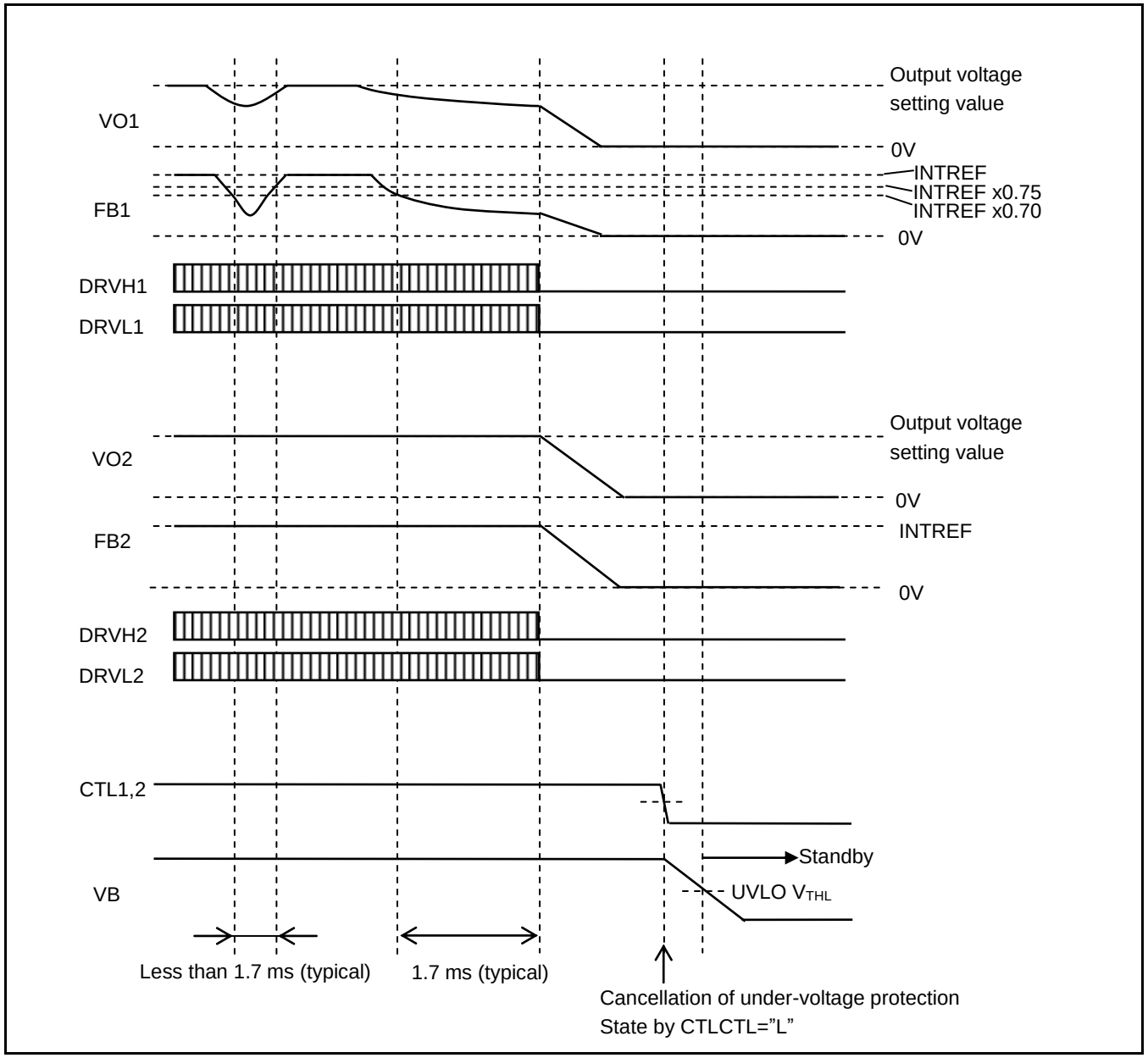
The over voltage protection state is released (the RS latch for over voltage protection is reset) under either of the following conditions.

- UVLO detection in the stop sequence after setting both the CTL1 pin (pin 3) and CTL2 pin (pin 10) to Level "L".
- UVLO detection in VCC power-off
- Thermal shutdown protection function (TSD) detection.

8.8 Under Voltage Protection Circuit Block (UVP Comp.)

This function stops the output voltage when the DC/DC output voltage has decreased, and protects devices connected to the output. This function compares the voltage that is 0.7 times (typical) the INTREF internal reference voltage with the feedback voltage that is input in the FB1 pin (pin 5) and the FB2 pin (pin 8). If the feedback voltage is found to be at least 1.7 ms (typical) lower, the RS latch is set, the DRVH1 pin (pin 1) and DRVH2 pin (pin 12) are set to Level "L", and the DRVL1 pin (pin 23) and DRVL2 pin (pin 14) are set to Level "L." In addition, when the latch is set for under voltage protection, the discharge function built in to the IC starts at the same time and voltage output stops for both channels. Further, there is 5% (typical) hysteresis in the threshold for the under voltage protection operation to avoid malfunction of the under voltage protection function.

Figure 8-5. Example Timing Chart for the Under Voltage Protection Operation



The under voltage protection state is released (the RS latch for under voltage protection is reset) under either of the following conditions.

■UVLO detection in the stop sequence after setting both the CTL1 pin (pin 3) and CTL2 pin (pin 10) to Level "L".

■UVLO detection in VCC power-off

■Thermal shutdown protection function (TSD) detection.

8.9 Thermal Shutdown Protection Block (TSD)

The thermal shutdown protection block (TSD) provides a function that prevents the IC from thermal damage. If the junction temperature of the thermal shutdown protection circuit reaches +150°C, the DRVH1 pin (pin 1) and DRVH2 pin (pin 12) are set to the “L” level, and the DRVL1 pin (pin 23) and DRVL2 pin (pin 14) are set to the “L” level, and switching stops. In addition, the discharge function that is built in to the IC runs, and voltage output for both channels stops. If the junction temperature drops to +125°C, the soft start is reactivated (restored automatically).

TSD detection is +150°C, but operations above the absolute maximum rating for the storage temperature (+125°C) are not guaranteed.

8.10 DAC Block (DAC)

You can change the reference voltage (INTREF1) for the CH1 error comparison block and the output voltage for the DC/DC converter by inputting an external 0V or VB pin voltage in the DAC0 pin (pin 7) and DAC1 pin (pin 17).

Table 8-1. Reference Voltage Settings

DAC0	DAC1	CH1 Reference Voltage (INTREF1)
0V	0V	0.802V typ
VB	0V	0.834V typ
0V	VB	0.867V typ
VB	VB	0.770V typ

8.11 Output Block (DRV1 and 2)

The output circuit is configured in CMOS format for both of the high side and the low side, and can drive an external Nch MOS FET.

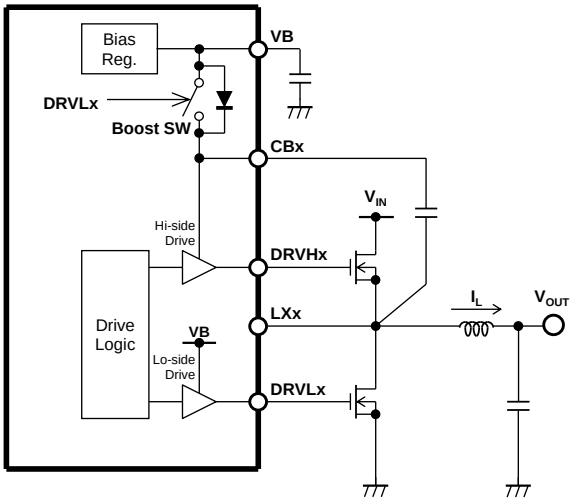
The output block for the high side FET supplies power from the built-in boost circuit, and the output block for the low side FET supplies power from the VB. This circuit prevents through-current by monitoring the gate voltages of the high side and low side FETs and controlling the timing of turning on one FET until the other FET is off. The sink ON resistance of the output circuit is a low 1Ω (typical), and the self turn on margin for the low side FET is improved.

8.12 Boost Circuit Block (CB1 and 2)

The boost circuit is needed high side FET in a case using Nch MOS FET.Efficiency improvement and/or reduction in parts cost can be expected of High side FET by using Nch MOSFET.

The boost circuit is formed a boost charge pump block which consists of the built-in switch for bootstraps and the condenser connected between CB pin and the LX pin. Then the condenser is charged through built-in switch from VB. The boosted power supply for gate drives of high side FET. The boost circuit has a built-in boost switch that eliminates the boost voltage (voltage between the CB pin and LX pin) loss of the forward voltage (Vf) that existed in older boost diodes. Therefore further efficiency improvement and reduction in parts cost can be expected more than a diode system.

Figure 8-6. Output Block and Boost Circuit Block



x: Each channel number

8.13 Over Current Detection Block (ILIM Comp.)

This function limits the output current when it has increased, and protects devices connected to the output. It compares the difference in voltage between the PGND1 pin (pin 22) and the LX1 pin (pin 24) and the ILIM1 pin (pin 21) voltage, and the difference in voltage between the PGND2 pin (pin 15) and LX2 pin (pin 13) and the ILIM2 pin (pin 16) voltage during the synchronous rectification period, and performs over current detection in every cycle.

The high side FET stays off until the difference in voltage between PGNDx and LXx is lower than the ILIMx pin voltage, and turns on after it becomes lower. This is how over current protection is performed. This protection operation drops the output voltage.

For the difference in voltage between PGNDx and LXx during the synchronous rectification period, the low side FET on resistance is sense resistance, and the inductor current is the sensed voltage waveform.

A 10 μA (typical) I_{ILIM} current is supplied from the ILIMx pin, so you can set any over current limit value by connecting resistance to the ILIMx pin. For the I_{ILIM} current, a temperature slope of 4200ppm/°C is set to compensate for the temperature dependence characteristics of the low side FET on resistance.

8.14 Control Block (CTL)

Turn CH1 on or off using the CTL1 pin (pin 3) and turn the CH2 on or off using the CTL2 pin (pin 10). Setting both CTL1 and 2 to Level "L" at the same time puts it in standby (the power supply current during standby is a maximum of 10 μA).

Table 8-2. Control Functions

CTL1	CTL2	DC/DC Converter (CH1)	DC/DC Converter (CH2)
L	L	OFF	OFF
H	L	ON	OFF
L	H	OFF	ON
H	H	ON	ON

8.15 Table of Protection Functions

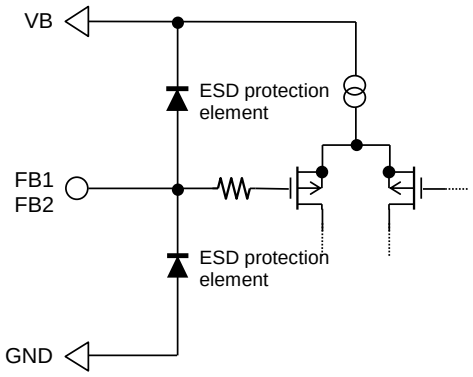
The following table shows the state of the DRVH1 and 2 pins (pins 1 and 12) and the DRVL1 and 2 pins (pins 23 and 14) when each protection function is in operation.

Table 8-3. Protection Functions

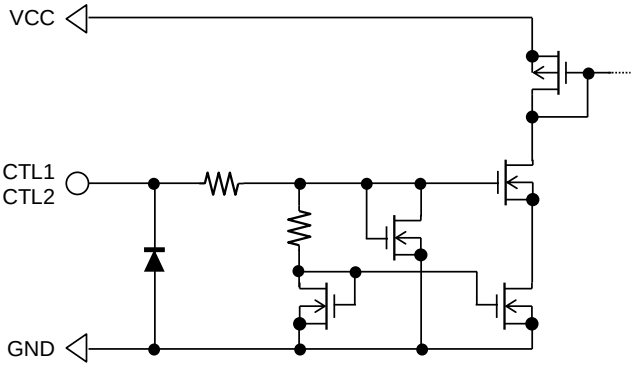
Protection function	Detection condition	Output of each pin during detection			DC/DC output drop state
		VB	DRVHx	DRVLx	
Under voltage lockout protection (UVLO)	V_{VB} < 3.6V	-	L	L	Natural electric discharge
Under voltage protection (UVP)	V_{FBx} < INTREFx × 0.7 V	5.2V	L	L	Electrical discharge by discharge function
Over voltage protection (OVP)	V_{FBx} > INTREFx × 1.15 V	5.2V	L	H	0V clamping
Over current protection (ILIM)	$V_{PGNDx} – V_{LXx} > V_{ILIMx}$	5.2V	switching	switching	Dropped by the set current value
Thermal shutdown protection (TSD)	Tj > +150°C	5.2V	L	L	Electrical discharge by discharge function
Control (CTL)	CTLx : H → L (VOx > 0.2V)	5.2V	L	L	Electrical discharge by discharge function

9. I/O Pin Equivalent Circuit Diagram

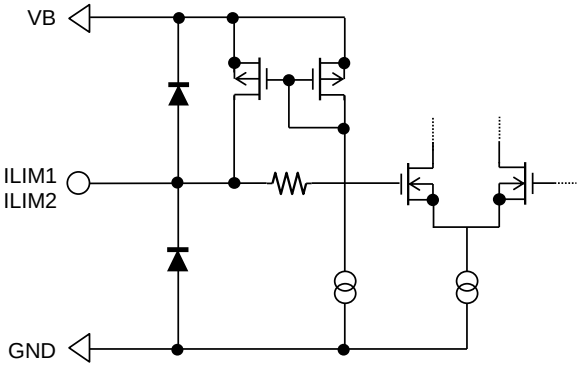
FB1, FB2 pins



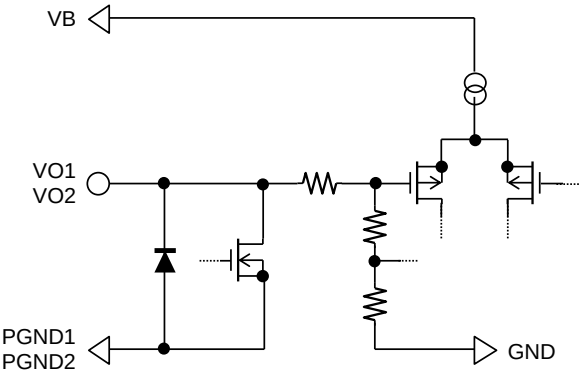
CTL1, CTL2 pins



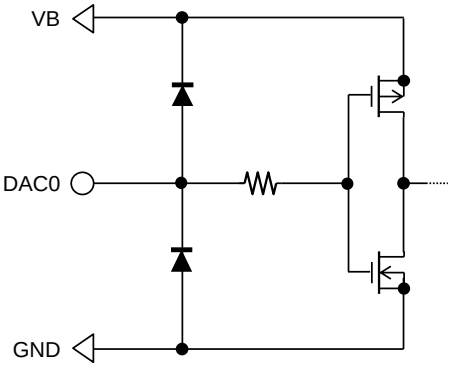
ILIM1, ILIM2 pins



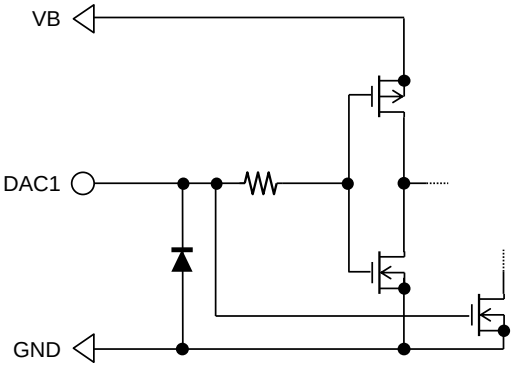
VO1, VO2 pins



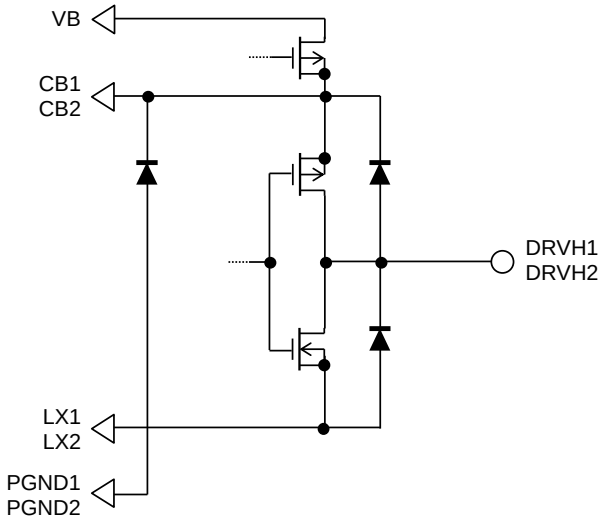
DAC0 pin



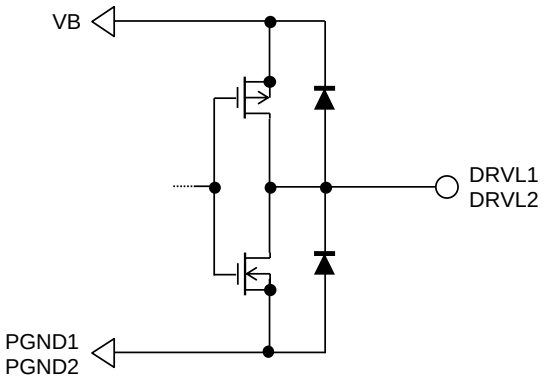
DAC1 pin



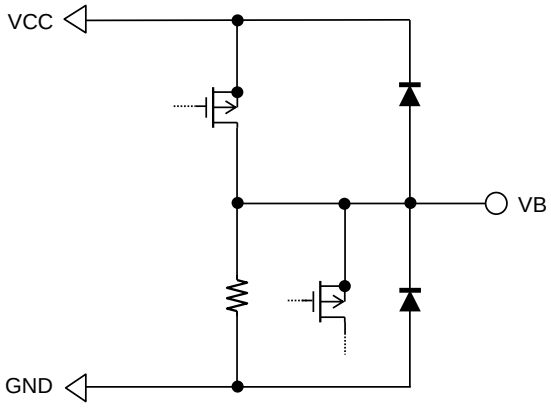
DRVH1, DRVH2, CB1, CB2, LX1, LX2 pins



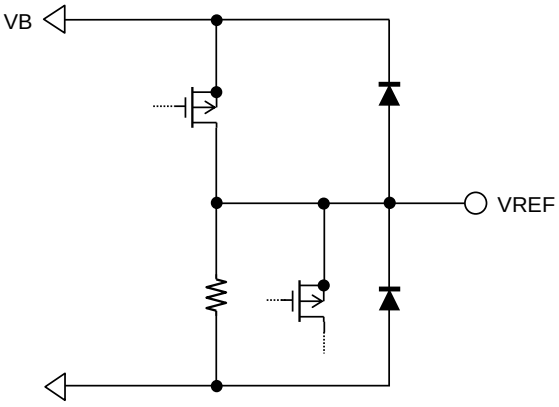
DRVL1, DRVL2 pins



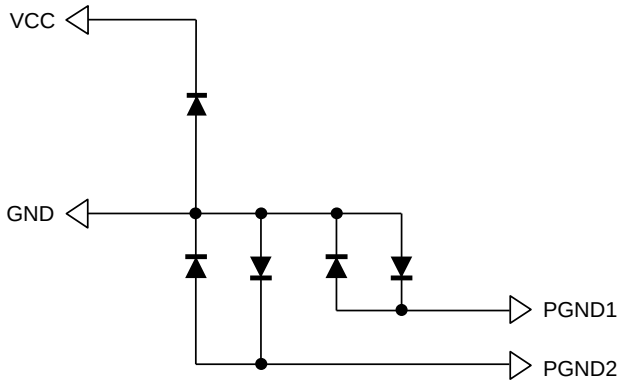
VB pin



VREF pin

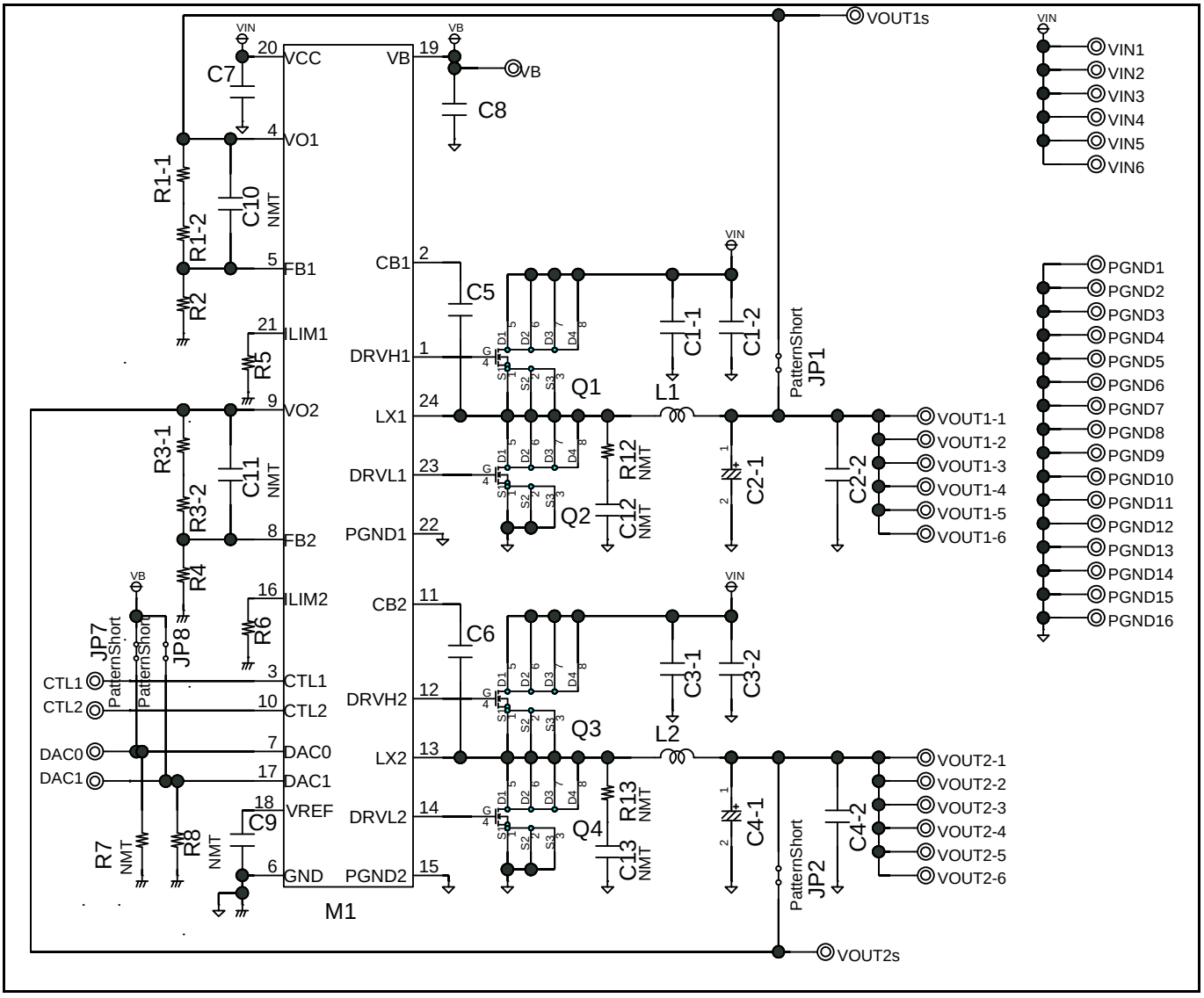


VCC, GND, PGND1, PGND2 pins



10. Example Application Circuit

Figure 10-1. Circuit Diagram



11. Part List

Table 11-1. Parts List

No.	Component	Item	Parts Number	Vendor	Value	Remarks
1	M1	PMIC	S6AP111A28GT1B000	CYPRESS	-	-
2	L1	Inductor	MPLC1040L4R7	KEMET	4.7µH	8A
3	L2	Inductor	MPLC1040L4R7	KEMET	4.7µH	8A
4	Q1	FET	FDMC8015L	FAIRCHILD	-	40V, 7A
5	Q2	FET	FDMC8327L	FAIRCHILD	-	40V, 12A
6	Q3	FET	FDMC8015L	FAIRCHILD	-	40V, 7A
7	Q4	FET	FDMC8327L	FAIRCHILD	-	40V, 12A
8	C1-1	Ceramic Capacitor	C3216X5R1V226M160AC	TDK	22µF	35V
9	C1-2	Ceramic Capacitor	C1608CH1H102J	TDK	0.001µF	50V
10	C2-1	Ceramic Capacitor	6TPE150MF	PANASONIC	150µF	6.3V
11	C2-2	Ceramic Capacitor	C1608CH1H102J	TDK	0.001µF	50V
12	C3-1	Ceramic Capacitor	C3216X5R1V226M160AC	TDK	22µF	35V
13	C3-2	Ceramic Capacitor	C1608CH1H102J	TDK	0.001µF	50V
14	C4-1	Ceramic Capacitor	6TPE150MF	PANASONIC	150µF	6.3V
15	C4-2	Ceramic Capacitor	C1608CH1H102J	TDK	0.001µF	50V
16	C5	Ceramic Capacitor	C1608X5R1H104K080AA	TDK	0.1µF	50V
17	C6	Ceramic Capacitor	C1608X5R1H104K080AA	TDK	0.1µF	50V
18	C7	Ceramic Capacitor	C1608X5R1H104K080AA	TDK	0.1µF	50V
19	C8	Ceramic Capacitor	C1608X5R1C225K	TDK	2.2µF	16V
20	C9	Ceramic Capacitor	C1608X5R1H105K080AB	TDK	1µF	50V
21	C10,C11,C12,C13	Ceramic Capacitor	C1608CH1H102J	TDK	0.001µF	NMT
22	R1-1	Chip Resistor	RR0816P-201-D	SUSUMU	0.2kΩ	-
23	R1-2	Chip Resistor	RR0816P-333-D	SUSUMU	33 kΩ	-
24	R2	Chip Resistor	RR0816P-103-D	SUSUMU	10 kΩ	-
25	R3-1	Chip Resistor	RR0816P-432-D	SUSUMU	4.3 kΩ	-
26	R3-2	Chip Resistor	RR0816P-513-D	SUSUMU	51 kΩ	-
27	R4	Chip Resistor	RR0816P-103-D	SUSUMU	10 kΩ	-
28	R5	Chip Resistor	RR0816P-103-D	SUSUMU	10 kΩ	-
29	R6	Chip Resistor	RR0816P-103-D	SUSUMU	10 kΩ	-
30	R7,R8	Chip Resistor	RR0816P-103-D	SUSUMU	10 kΩ	NMT
31	R12,R13	Chip Resistor	RK73H2ATTD10R0F	SUSUMU	10 Ω	NMT
32	JP1,JP2,JP7,JP8	Jumper	-	-	-	Pattern short
33	PGND, VOUT1, VOUT1a,VIN, CTL1, DAC0	Terminal	90131-0770	molex	-	2 × 10pin header
34	PGND, VOUT2, VOUT2a,VIN, CTL2, DAC1	Terminal	90131-0770	molex	-	2 × 10pin header

NMT: No mount.
These components are compliant with RoHS, and please ask each vendor for details if necessary.
CYPRESS : CYPRESS Semiconductor Corp.
KEMET : KEMET Electronics Corporation
FAIRCHILD : Fairchild Semiconductor Corp.
TDK : TDK Corporation
PANASONIC : Panasonic Corporation
SUSUMU : SUSUMU Co., Ltd.
molex : Molex Japan Co., Ltd.

12. Application Note

12.1 Setting Operating Conditions

Setting the Output Voltage

You can set the output voltage by adjusting the R1 and R2 resistance ratio. The output voltage is calculated using the following formula.

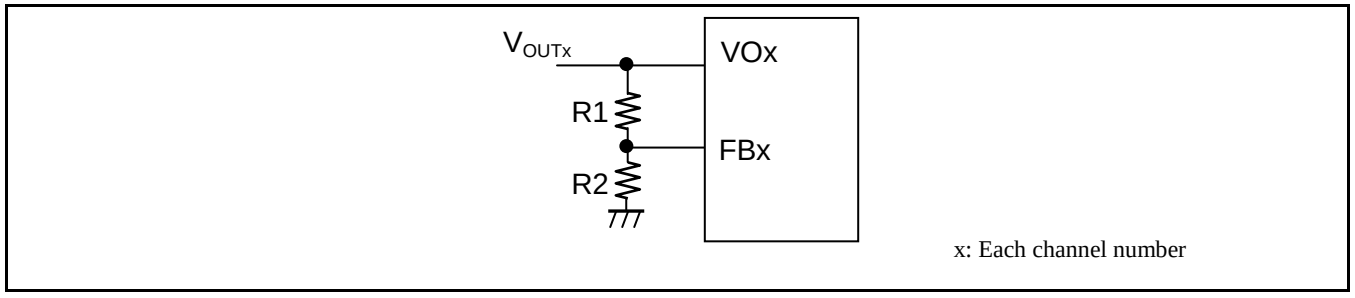
$$V_{OUT} = \frac{R1+R2}{R2} \times (INTREF - 0.0100 + 0.0184 \times \Delta I_L \times (1 - \frac{2.800 \times 10^{-7}}{t_{OFF}}) \times R_{ON\_Sync}) + \frac{\Delta V_{OUT}}{2}$$

$$\Delta V_{OUT} = ESR \times \Delta I_L \quad \Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN} \times f_{OSC}} \quad , \quad t_{OFF} = \frac{(V_{IN} - V_{OUT})}{f_{OSC} \times V_{IN}}$$

INTREF	: Internal reference voltage (DC threshold) [V]
V_{OUT}	: Output settings voltage [V]
V_{IN}	: Power supply voltage [V]
ΔV_{OUT}	: Output ripple voltage value [V]
t_{OFF}	: Off time [s]
R_{ON_Sync}	: ON resistance of low side FET [Ω]
ΔI_L	: Ripple current peak-to-peak value of inductor [A]
ESR	: Series resistance element of output capacitor [Ω]
L	: Inductor value [H]
f_{OSC}	: Switching frequency [Hz]

Select a total resistor value (R1+R2) of up to 100 kΩ for the setting output resistor.

Figure 12-1. FB Connection



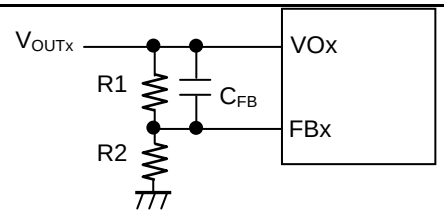
Connecting the Feedback Capacitor

The IC internally generates the output voltage slope during the OFF period to stabilize the switching frequency, but it is also effective to apply output ripple voltage to the FB pin. This is achieved by adding capacitors (C_{FB}) to the R1 in parallel. Applying a ripple voltage value to the FB terminals is more effective than high output voltage conditions that decrease it based on the R1 and R2 ratio. When selecting which capacitors to add, use the following formula.

$$C_{FB} \geq \frac{10 \times (R1+R2)}{2\pi \times f_{OSC} \times R1 \times R2}$$

C_{FB}	: Feedback capacitor capacitance [F]
R1,R2	: Output voltage setting resistance [Ω]
f_{OSC}	: Switching frequency [Hz]

Figure 12-2. FB Connection



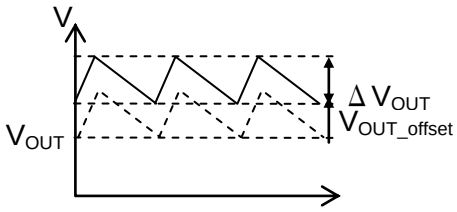
x: Each channel number

In addition, the output voltage will increase in response to the output ripple voltage when adding capacitors. Calculate the output voltage increase value V_{OUT}_offset using the following formula.

$$V_{OUT\_offset} = \frac{(V_{OUT} - INTREF) \times \Delta V_{OUT}}{2 \times INTREF}$$

INTREF : Internal reference voltage (DC threshold) [V]
V_{OUT}_offset : Output voltage increase value [V]
V_{OUT} : Output settings voltage value [V]
ΔV_{OUT} : Output ripple voltage value [V]

Figure 12-3. V_{OUT} Operation



To calculate the output voltage when factoring in the output voltage increase value, use the following formula.

$$V_{OUT} = \frac{R1+R2}{R2} \times INTREF + \frac{\Delta V_{OUT}}{2} + V_{OUT\_offset}$$

$$= \frac{R1+R2}{R2} \times (INTREF + \frac{\Delta V_{OUT}}{2})$$

V_{OUT} : Output settings voltage [V]
INTREF : Internal reference voltage (DC threshold)
ΔV_{OUT} : Output ripple voltage value [V]
V_{OUT_offset} : Output voltage increase value [V]

Maintaining a Difference between the Minimum Input and Output Voltage

Stable switching control is performed in this IC, so the minimum OFF time is set, but if the difference between the input and output is small, and the input voltage is less than the voltage value shown in the formula below, the output voltage is reduced. For this reason, you should maintain the difference between the minimum input voltages.

$$V_{IN\_MIN} = \frac{(V_{OUT} + I_{OUT\_MAX} \times (RDC + R_{ON\_Main})) \times V_{OUT}}{V_{OUT} - (V_{OUT} + I_{OUT\_MAX} \times (RDC + R_{ON\_Sync})) \times t_{OFFMINN} \times f_{OSC} \times 1.4}$$

V_{IN_MIN} : Input voltage [V]
V_{OUT} : Output settings voltage [V]
I_{OUT_MAX} : Maximum load current value [A]
R_{ON_Main} : High side FET ON resistance [Ω]
R_{ON_Sync} : ON resistance of low side FET [Ω]
RDC : Inductor direct current resistance [Ω]
f_{OSC} : Switching frequency setting value [Hz]
$t_{OFFMINN}$: Normal minimum OFF time (maximum value) [s]

Slope Voltage

To ensure a stable switching cycle, maintain a slope voltage of at least 15 mV.

Calculate the slope voltage using the following formula.

$$V_{Slope} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT} \times R_{ON\_Sync}}{L \times V_{IN} \times f_{OSC}}$$

V_{Slope} : Slope voltage [V]
V_{IN} : Power supply voltage [V]
V_{OUT} : Output settings voltage [V]
f_{OSC} : Switching frequency [Hz]
R_{ON_Sync} : ON resistance of low-side FET [Ω]
L : Inductor value [H]

Setting the Over Current Detection Value

The over current detection value can be set by adjusting the over current detection setting resistor that is connected to the ILIM pin.

Calculate the resistor value from the following formula.

$$R_{LIM} = \frac{R_{ON\_Sync} \times (I_{LIM} - \frac{\Delta I_L}{2})}{I_{LIM\_SOURCE}}$$

R_{LIM} : Over current detection value setting resistor [Ω]
I_{LIM} : Over current detection value [A]
I_{LIM_SOURCE} : ILIM pin source current [A]
ΔI_L : Ripple current peak-to-peak value of inductor [A]
R_{ON_Sync} : ON resistance of low side FET [Ω]

Figure 12-4. ILIM Connection

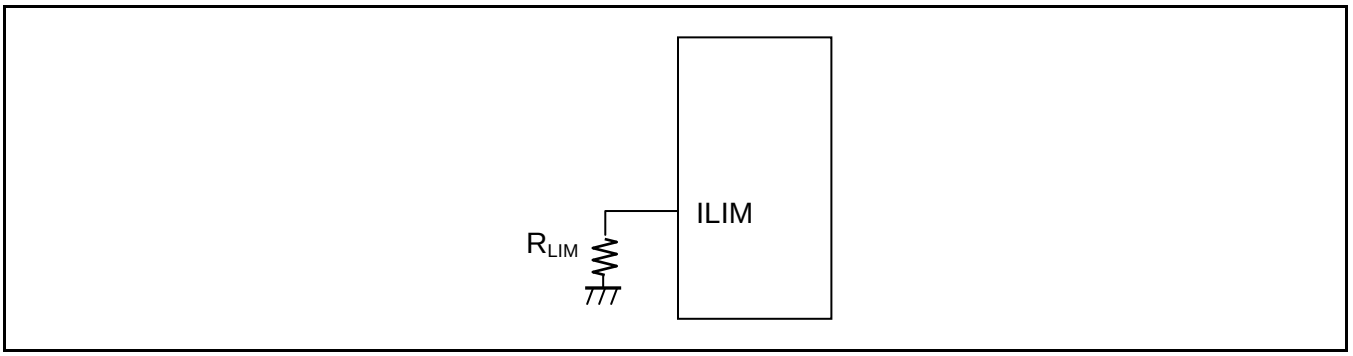
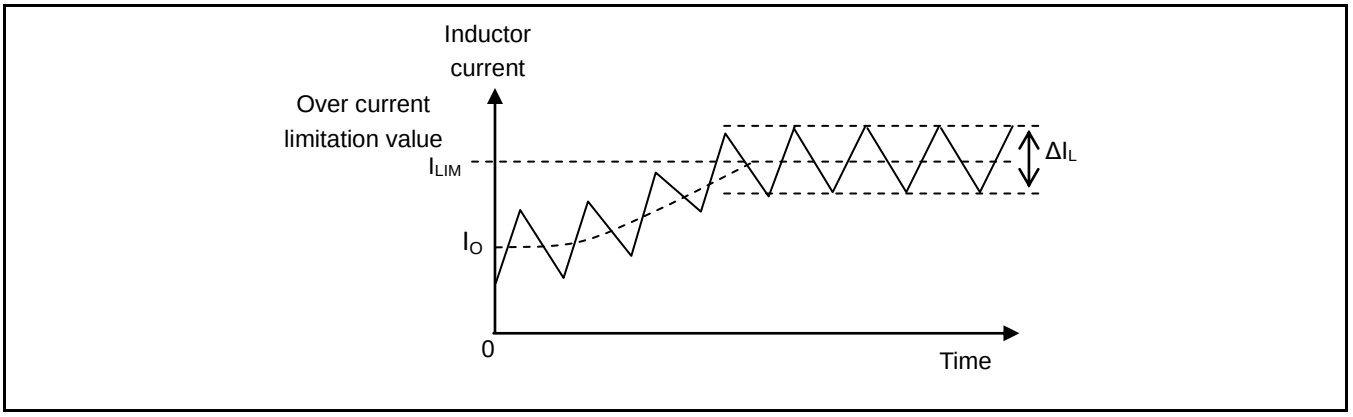


Figure 12-5. Over Current Operation



If the reduction in the inductance value for the inductor is large due to over current, the inductor ripple current increases and the current limitation value goes up, or else it is not restricted. If this happens, change to an inductor that has margin for DC current superimposition characteristics.

In addition, the over current detection value should provide plenty of margin for maximum load current.

Power Dissipation and Thermal Design

This is a high efficiency IC so power dissipation and thermal design do not need to be investigated in most cases, but they do need to be investigated when using the IC at a high power supply voltage, high oscillator frequency, high load, and high temperature. Calculate the internal IC loss from the following formula.

$$P_{IC} = V_{CC} \times (I_{CC} + Q_{G\_Total1} \times f_{OSC1} + Q_{G\_Total2} \times f_{OSC2})$$

P_{IC}	: IC internal loss [W]
V_{CC}	: Power supply voltage (V_{IN}) [V]
I_{CC}	: Power supply current [A] (1.8mA Max)
Q_{G_Total1}	: Total quantity of charge for the high-side FET and the low-side FET of each CH1 [C]
Q_{G_Total2}	: Total quantity of charge for the high-side FET and the low-side FET of each CH2 [C]
f_{OSC1}	: CH1 Switching frequency [Hz]
f_{OSC2}	: CH2 Switching frequency [Hz]

Calculate the junction temperature (Tj) from the following formula.

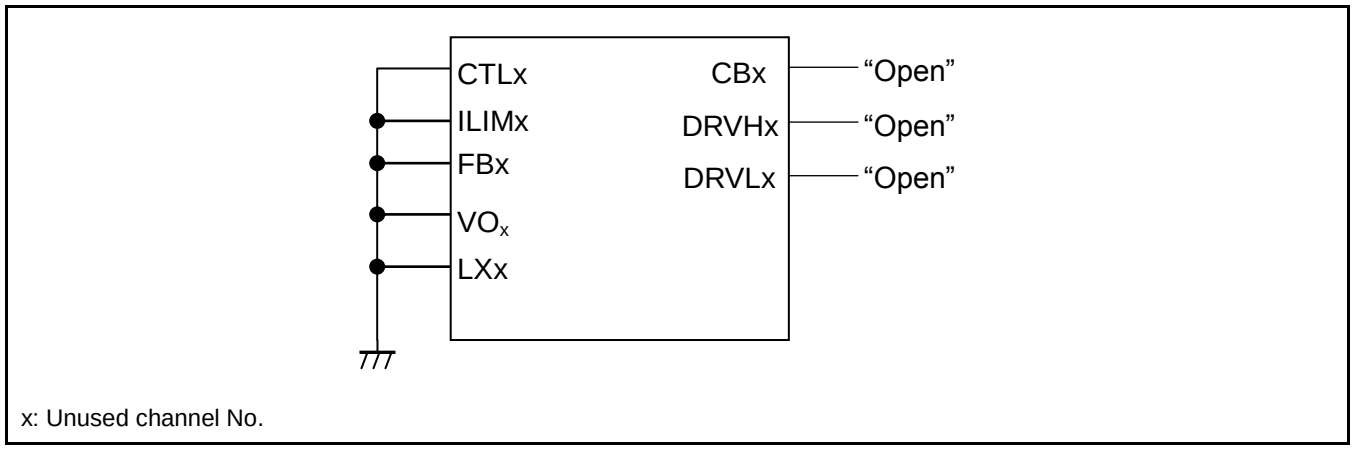
$$T_j = T_a + \theta_{ja} \times P_{IC}$$

T_j	: Junction temperature [°C] (+125°C Max)
T_a	: Ambient temperature [°C]
θ_{ja}	: TSSOP-24P package thermal resistance (75°C/W)
P_{IC}	: IC internal loss [W]

Pin Processing when Only Using a Single Channel

This IC is a 2ch DC/DC converter control IC, but you can also use it as a 1ch DC/DC converter using the following processing for pins from unused channels.

Figure 12-6. Pin Processing



x: Unused channel No.

12.2 Selecting Parts

Selection of smoothing inductor

The inductor value selects the value that the ripple current peak-to-peak value of the inductor is 50% or less of the maximum load current as a rough standard. Calculate the inductor value in this case by the following formula.

$$L \geq \frac{V_{IN} - V_{OUT}}{LOR \times I_{OUT\_MAX}} \times \frac{V_{OUT}}{V_{IN} \times f_{OSC}}$$

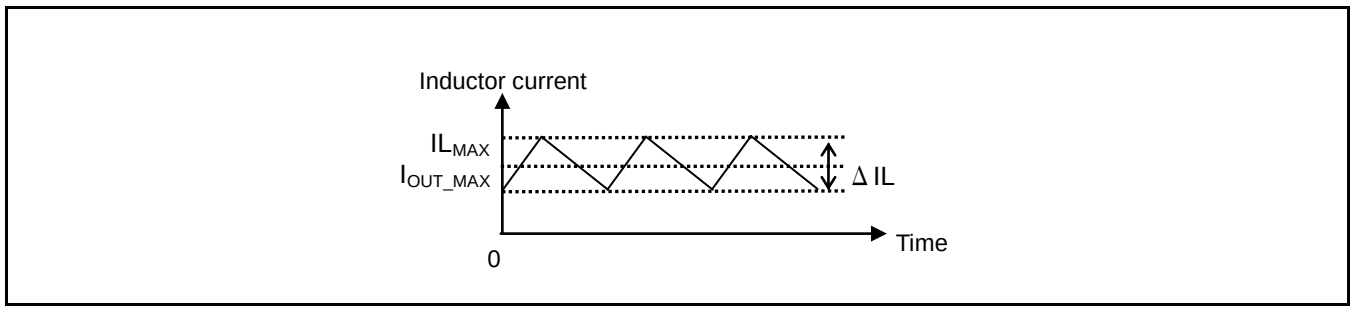
L	: Inductor value [H]
I_{out_max}	: Maximum load current [A]
LOR	: Ripple current peak-to-peak value of inductor/Maximum load current ratio (= 0.5)
V_{IN}	: Power supply voltage [V]
V_{OUT}	: Output setting voltage [V]
f_{OSC}	: Switching frequency [Hz]

It is necessary to calculate the maximum current value that flows to the inductor to judge whether the electric current that flows to the inductor is a rated value or less. Calculate the maximum current value of the inductor by the following formula.

$$IL_{MAX} \geq I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$

IL_{MAX}	: Maximum current value of inductor [A]
I_{OUT_MAX}	: Maximum load current [A]
ΔI_L	: Ripple current peak-to-peak value of inductor [A]
L	: Inductor value [H]
V_{IN}	: Power supply voltage [V]
V_{OUT}	: Output setting voltage [V]
f_{OSC}	: Switching frequency [Hz]

Figure 12-7. Maximum Output Current Setting



Selection of Switching FET

If selecting the high-side FET so that the value of the high-side FET conduction loss and the high-side FET switching loss is same, the loss is effectively decreased.

Confirm that the high-side FET loss is within the rating value.

$$P_{MainFET} = P_{RON\_Main} + P_{SW\_Main}$$

$P_{MainFET}$: High-side FET loss [W]
P_{RON_Main} : High-side FET conduction loss [W]
P_{SW_Main} : High-side FET switching loss [W]

High-side FET conduction loss

$$P_{RON\_Main} = I_{OUT\_MAX}{}^2 \times \frac{V_{OUT}}{V_{IN}} \times R_{ON\_Main}$$

P_{RON_Main} : High-side FET conduction loss [W]
I_{OUT_MAX} : Maximum load current [A]
V_{IN} : Power supply voltage [V]
V_{OUT} : Output voltage [V]
R_{ON_Main} : ON resistance of high-side FET [Ω]

The high-side FET switching loss can be calculated roughly by the following formula.

$$P_{SW\_Main} \approx 1.96 \times V_{IN} \times f_{OSC} \times I_{OUT\_MAX} \times Q_{SW}$$

P_{SW_Main} : Switching loss [W]
V_{IN} : Power supply voltage [V]
f_{OSC} : Switching frequency [Hz]
I_{OUT_MAX} : Maximum load current [A]
Q_{SW} : Amount of high-side FET gate switch electric charge [C]

Select the ON resistance of low-side FET from the range below.

$$R_{ON\_Sync} \le \frac{0.2}{(I_{LIM} - \frac{\Delta I_L}{2})}, \quad R_{ON\_Sync} \le \frac{0.1}{\Delta I_L}, \quad R_{ON\_Sync} \ge \frac{0.015}{\Delta I_L}$$

R_{ON_Sync} : ON resistance of low-side FET [Ω]
ΔI_L : Ripple current peak-to-peak value of inductor [A]
I_{LIM} : Over current detection value [A]

If the formula above has been already satisfied and then a low ON resistance FET as possible is used for the low-side FET, the loss is effectively decreased. Especially, it works dramatically in the low on duty mode.

The loss of the low-side FET can be calculated by the following formula.

$$P_{SyncFET} = P_{Ron\_Sync} = I_{OUT\_MAX}{}^{2} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{on\_Sync}$$

$P_{SyncFET}$: Low-side FET loss [W]
P_{Ron_Sync} : Low-side FET conduction loss [W]
I_{OUT_MAX} : Maximum load current [A]
V_{IN} : Power supply voltage [V]
V_{OUT} : Output voltage [V]
R_{ON_Sync} : ON resistance of low-side FET [Ω]

Turn-on and turn-off voltage of the low-side FET is generally small and the switching loss is small enough to ignore, so that is omitted here.

Especially, when turning on the high-side FET under the high power supply voltage condition, the rush-current might be generated by according to self-turn-on of the low-side FET. The parasitic capacitor value of the low-side FET needs to satisfy the following conditions.

$$V_{TH\_Sync} > \frac{C_{rss}}{C_{iss}} \times V_{IN}$$

V_{TH_Sync} : Threshold voltage of low-side FET [V]
C_{rss} : Parasitic feedback capacitance of low-side FET [F]
C_{iss} : Parasitic input capacitance of low-side FET [F]
V_{IN} : Power supply voltage [V]

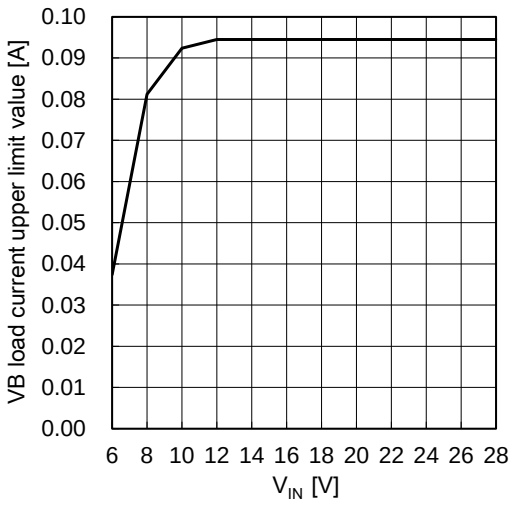
Also approaches of adding a capacitor close between the gate source pins of the low-side FET or adding resistor between the CB pin and the boost capacitor, and so on are effective as a countermeasure of the self-turn-on(adding resistor between the CB pin and the boost capacitor is also effective to adjust turn-on time of the high-side FET).

This device monitors the gate voltage of the switching FET and optimizes the dead time. If the dumping resistor is inserted among DRVH, DRVL and the switching FET gate to adjust turn-on and turn-off time of the switching FET, this function might malfunction. In this device, resistor should not be connected among the DRVH pin, the DRVL pin of IC and the switching FET gate, and should be connected by low impedance as possible.

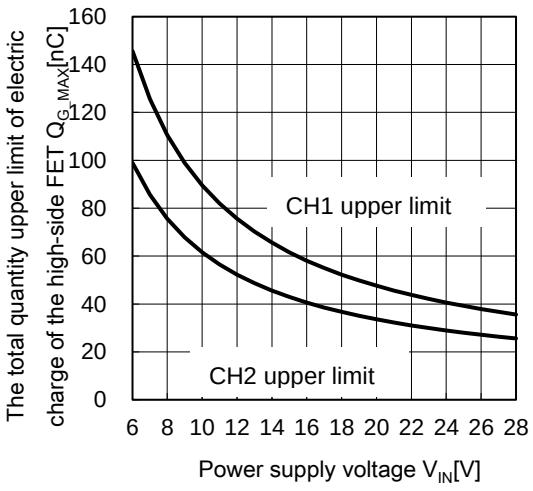
The gate drive power of the switching FET is supplied from LDO (VB) of IC inside. Select switching FET so that the total amount of the switching FET electric charge for 2 channels (QG_Total1, QG_Total2) satisfies the following formula.

$$I_{VB\_MAX} > Q_{G\_Total1} \times f_{OSC1} + Q_{G\_Total2} \times f_{OSC2}$$

I_{VB_MAX} : VB load current upper limit value (see the following graph) [A]
Q_{G_Total1} : Total quantity of charge for the high-side FET and the low-side FET of each CH1 [C]
Q_{G_Total2} : Total quantity of charge for the high-side FET and the low-side FET of each CH2 [C]
f_{OSC1} : CH1 Switching frequency [Hz]
f_{OSC2} : CH2 Switching frequency [Hz]



Moreover, select the total quantity of the high-side FET electric charge as a guide that does not exceed the total quantity of the high-side FET electric charge upper limit value shown below.



Whether the mean current value that flows to switching FET is a rated value or less of switching FET is judged. Each rating value for the switching FET can be calculated roughly by the following formula.

$$I_{D\_Main} > I_{OUT\_MAX} \times D \quad , \quad I_{D\_Sync} > I_{OUT\_MAX} \times (1-D)$$

I_{D_Main} : High-side FET drain current [A]
I_{D_Sync} : Low-side FET drain current [A]
I_{OUT_MAX} : Maximum load current [A]
D : On-duty

$$V_{DSS} > V_{IN}$$

V_{DSS} : Voltage between the high-side FET drain and source and the low-side FET drain and source [V]
V_{IN} : Power supply voltage [V]

Selection of fly-back diode

This device is improved by adding the fly-back diode when the conversion efficiency improvement or the suppression of the low-side FET fever is desired, although those are unnecessary to execute normally. The effect is achieved in the condition where the switching frequency is high or output voltage is lower. Select schottky barrier diode (SBD) that the forward current is as small as possible. In this DC/DC control IC, the period for the electric current flow into fly-back diode is limited to dead time period because the synchronous rectification system is adopted. (as for the dead time, see “Output Block” in “ELECTRICAL CHARACTERISTICS”). Each rating for the fly-back diode can be calculated by the following formula.

$$I_D \geq I_{OUT\_MAX} \times f_{OSC} \times (t_{D1} + t_{D2})$$

I_D : Forward current rating of SBD [A]
I_{OUT_MAX} : Maximum load current [A]
f_{OSC} : Switching frequency [Hz]
t_{D1} : Dead time period from DRVL off to DRVH on [s]
t_{D2} : Dead time period from DRVH off to DRVL on [s]

$$I_{FSM} \geq I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$

I_{FSM} : Peak forward surge current ratings of SBD [A]
I_{OUT_MAX} : Maximum load current [A]
ΔI_L : Ripple current peak-to-peak value of inductor [A]

$$V_{R\_Fly} > V_{IN}$$

V_{R_Fly} : Reverse voltage of fly-back diode direct current [V]
V_{IN} : Power supply voltage [V]

Selection of input capacitor

Select the input capacitor whose ESR is as small as possible. The ceramic capacitor is an ideal. Use the tantalum capacitor and the polymer capacitor of the low ESR when a mass capacitor is needed as the ceramic capacitor cannot support.

The ripple voltage is generated in the power supply voltage by the switching operation of DC/DC. Calculate the lower bound of input capacitor according to an allowable ripple voltage. Calculate the ripple voltage of the power supply from the following formula.

$$\Delta V_{IN} = \frac{I_{OUT\_MAX}}{C_{IN}} \times \frac{V_{OUT}}{V_{IN} \times f_{OSC}} + ESR \times (I_{OUT\_MAX} + \frac{\Delta I_L}{2})$$

ΔV_{IN} : Power supply ripple voltage peak-to-peak value [V]
I_{OUT_MAX} : Maximum load current value [A]
C_{IN} : Input capacitor value [F]
V_{IN} : Power supply voltage [V]
V_{OUT} : Output setting voltage [V]
f_{OSC} : Switching frequency [Hz]
ESR : Series resistance component of input capacitor [Ω]
ΔI_L : Ripple current peak-to-peak value of inductor [A]

Capacitor has frequency characteristic, the temperature characteristic, and the bias voltage characteristic, etc.The effective capacitor value might become extremely small depending on the use conditions. Note the effective capacitor value in the use conditions.

Calculate ratings of the input capacitor by the following formula:

$$V_{CIN} > V_{IN}$$

V_{CIN} : Withstand voltage of the input capacitor [V]
V_{IN} : Power supply voltage [V]

$$Irms \geq I_{OMAX} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

Irms : Allowable ripple current of input capacitor (effective value) [A]
I_{OMAX} : Maximum load current value [A]
V_{IN} : Power supply voltage [V]
V_{OUT} : Output setting voltage [V]

Selection of output capacitor

A certain level of ESR is required for stable operation of this IC. Use a tantalum capacitor or polymer capacitor as the output capacitor. If using a ceramic capacitor with low ESR, a resistor should be connected in series with it to increase ESR equivalently.

Calculate the output capacitor value by the following formula as a guide.

$$C_{OUT} \geq \frac{1}{4 \times f_{OSC} \times ESR}$$

C_{OUT} : Output capacitor value [F]
f_{OSC} : Switching frequency [Hz]
ESR : Series resistance of output capacitor [Ω]

Moreover, the output capacitor values are also derived from the allowable amount of overshoot and undershoot. The following formula is represented as the worst condition in which the shift time for a sudden load change is 0s. The output capacitor value allow a smaller amount than the value calculated by the following formula when a longer shift time.

$$C_{OUT} \geq \frac{\Delta I_{OUT}{}^2 \times L}{2 \times V_{OUT} \times \Delta V_{OUT\_OVER}}$$ …Overshoot condition

$$C_{OUT} \geq \frac{\Delta I_{OUT}{}^2 \times L \times (V_{OUT} + V_{IN} \times f_{OSC} \times t_{OFF\_MIN})}{2 \times V_{OUT} \times \Delta V_{OUT\_UNDER} \times (V_{IN} - V_{OUT} - V_{IN} \times f_{OSC} \times t_{OFF\_MIN})}$$

…Undershoot condition

C_{OUT} : Output capacitor value [F]
ΔV_{OUT_OVER} : Allowable amount of output voltage overshoot [V]
ΔV_{OUT_UNDER} : Allowable amount of output voltage undershoot [V]
ΔI_{OUT} : Current difference in sudden load change [A]
L : Inductor value [H]
V_{IN} : Power supply voltage [V]
V_{OUT} : Output setting voltage [V]
f_{OSC} : Switching frequency [Hz]
t_{OFF_MIN} : Minimum off time

The capacitor has frequency, operating temperature, and bias voltage characteristics, etc. Therefore, it must be noted that its effective capacitor value may be significantly smaller, depending on the use conditions.

$$V_{COUT} > V_{OUT}$$

V_{COUT} : Withstand voltage of the output capacitor [V]
V_{OUT} : Output voltage [V]

$$I_{RMS} \geq \frac{\Delta I_L}{2\sqrt{3}}$$

I_{RMS} : Allowable ripple current of output capacitor (effective value) [A]
ΔI_L : Ripple current peak-to-peak value of inductor [A]

When connecting resistance in series configuration while a ceramic capacitor is in use, the resistor rating is calculated by the following formula.

$$P_{ESR} > \frac{ESR \times \Delta I_L{}^2}{12}$$

P_{ESR} : Power dissipation of resistor [W]
ESR : Resistor value [Ω]
ΔI_L : Ripple current peak-to-peak value of inductor [A]

Selection of bootstrap capacitor

To drive the gate of high-side FET, the bootstrap capacitor must have enough stored charge. 0.1 µF is assumed to be standard, however, it is necessary to adjust it when the high-side FET Q_G is big. Consider the capacitor value calculated by the following formula as the lowest value for the bootstrap capacitor and select a thing anymore.

$$C_{BST} \geq 10 \times Q_G$$

C_{BST} : Bootstrap capacitor value [F]
Q_G : Total quantity of charge for the high-side FET gate [C]

Calculate ratings of the bootstrap capacitor by the following formula:

$$V_{CBST} > V_B$$

V_{CBST} : Withstand voltage of the bootstrap capacitor [V]
V_B : VB voltage [V]

VB pin capacitor

2.2 µF is assumed to be a standard, and when Q_G of switching FET used is large, it is necessary to adjust it. To suppress the ripple voltage by the switching FET gate drive, consider the capacitor value calculated by the following formula as the lowest value for VB capacitor and select a thing anymore.

$$C_{VB} \geq 50 \times (Q_{G\_Total1} + Q_{G\_Total2})$$

C_{VB} : VB pin capacitor value [F]
Q_{G_Total1} : Total quantity of charge for the high-side FET and the low-side FET of each CH1 [C]
Q_{G_Total2} : Total quantity of charge for the high-side FET and the low-side FET of each CH2 [C]

Calculate ratings of the VB pin capacitor by the following formula:

$$V_{CVB} > V_B$$

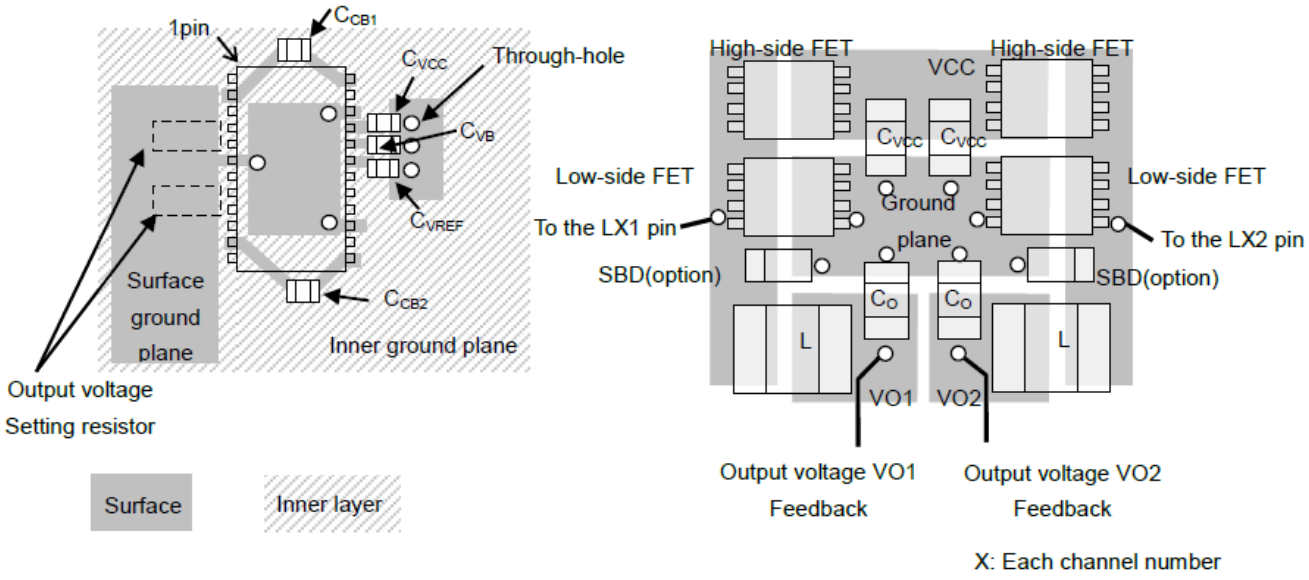
V_{CVB} : Withstand voltage of the VB pin capacitor [V]
V_B : VB voltage [V]

12.3 Layout

Consider the following points in your layout.

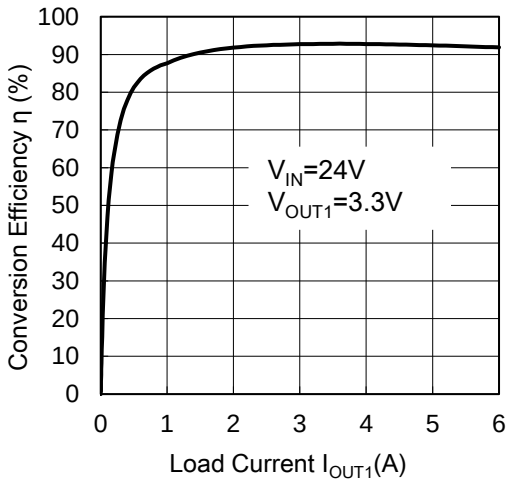
- Try to provide a ground plane on the IC mounting surface. Try not to pass the heavy current path through the ground of around IC.
- Try to connect the switching system parts on the surface and avoid connecting via the through-hole as much as possible.
- Provide through-holes close to GND pins for switching system parts, and connect them to the inner ground plane.
- Pay particular attention to the loop composed of the input capacitor (C_{VCC}), switching FET, and flyback diode (SBD), and make the current loop as small as possible.
- Place the bootstrap capacitor (C_{BOOT1}, C_{BOOT2}) as close as possible to the IC CBx and LXx pins.
- A large electric current will instantaneously flow in the net of the DRVHx and DRVLx pins connected to the switching FET gate. Make the wiring as short as possible and aim for a wire width of approximately 0.8 mm.
- Place the bypass capacitors (C_{VCC}, C_{VB}, C_{VREF}) that connect to the VCC, VB, and VREF as close to the pins as possible. In addition, connect the GND pin for the bypass capacitor to the inner ground plane through the nearest through-hole.
- In order to provide the IC with more accurate feedback on the ripple voltage that is generated by the output capacitor ESR, individually pull the feedback wires connected to the VOx pins of this IC from the closest possible output capacitor pins. The wires connected to the VOx and FBx pins are sensitive to noise. Try to keep these wires as far away from switching system parts as possible.
  In addition, place the output voltage setting resistors that are connected to these wires as close to the IC as possible. Make the FB pin wire as short as possible. In addition, for the inner layer right under the mounting location, provide a ground plane that has minimal ripple and spike noises, or provide a power plane if possible.

Switching system parts: Input capacitor (C_{VCC}), switching FET, flyback diode (SBD), inductor (L), output capacitor (C_O)

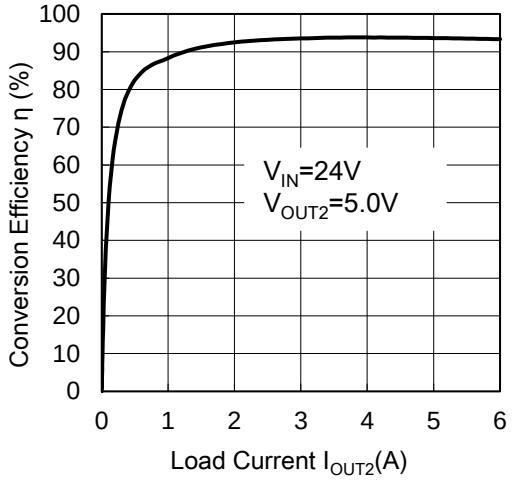


13. Reference Data

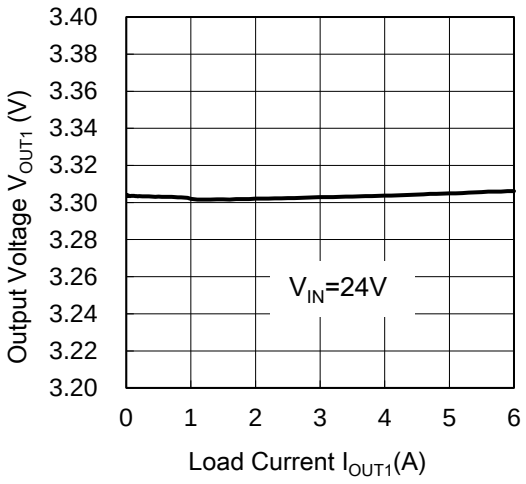
Conversion Efficiency vs. Load Current



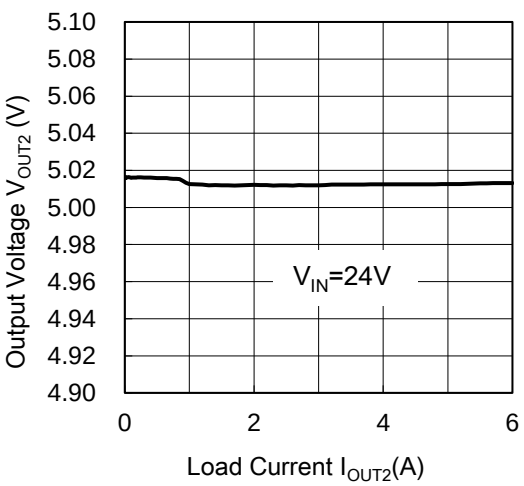
Conversion Efficiency vs. Load Current



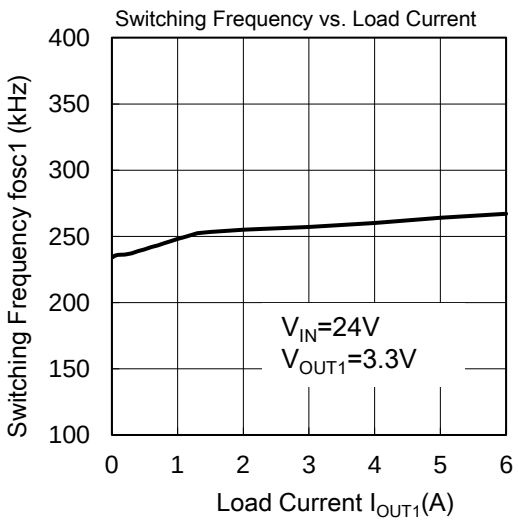
Output Voltage vs. Load Current



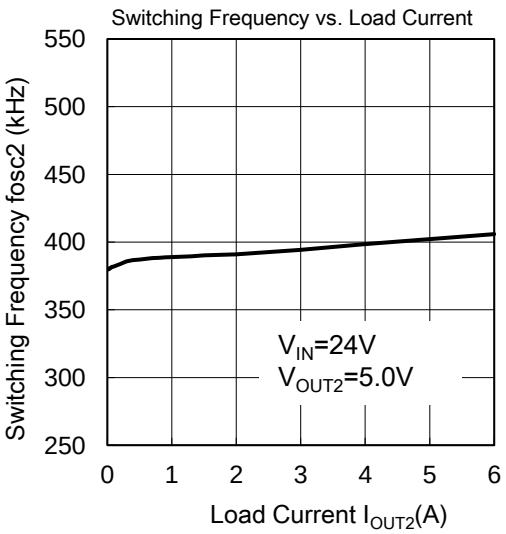
Output Voltage vs. Load Current



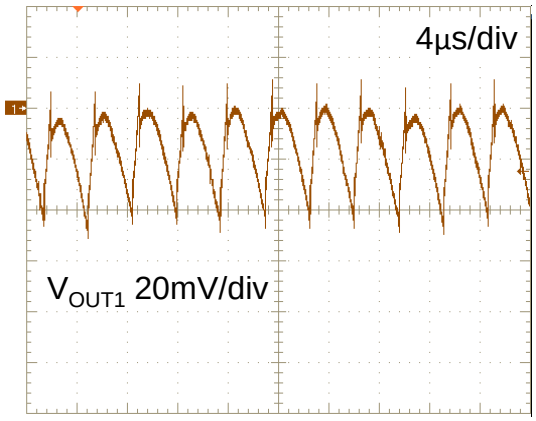
Switching Frequency vs. Load Current



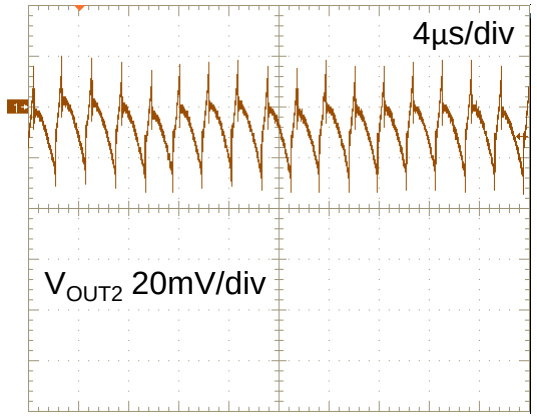
Switching Frequency vs. Load Current



Output Ripple Waveform

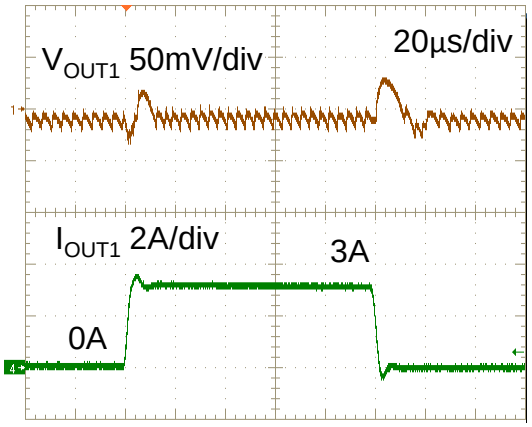


V_{IN}=24V, V_{OUT1}=3.3V, I_{OUT1}=6A

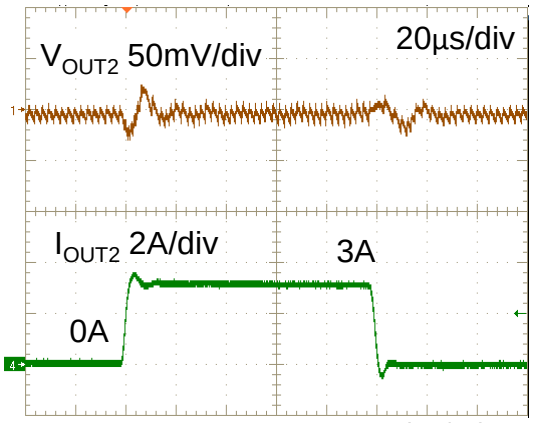


V_{IN}=24V, V_{OUT2}=5V, I_{OUT2}=6A

Load Sudden Change Waveform

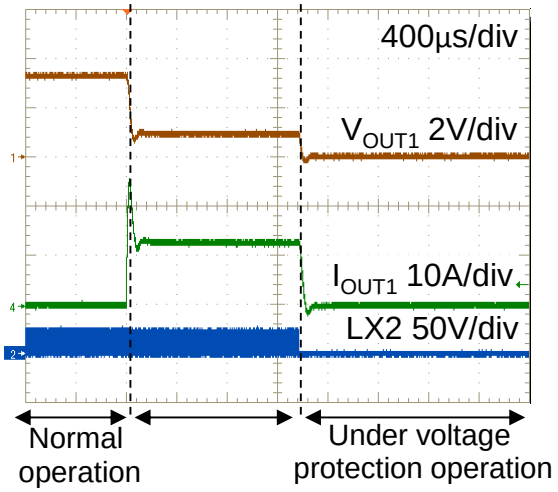


V_{IN}=24V, V_{OUT1}=3.3V, I_{OUT1}=0A↔3A(1A/µs)

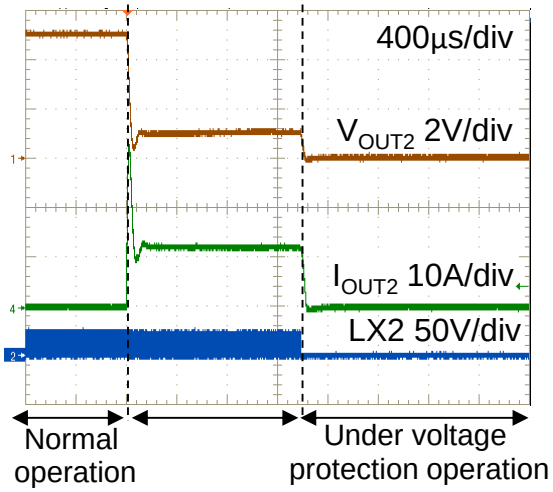


V_{IN}=24V, V_{OUT2}=5V, I_{OUT2}=0A↔3A(1A/µs)

Output Over Current Waveform

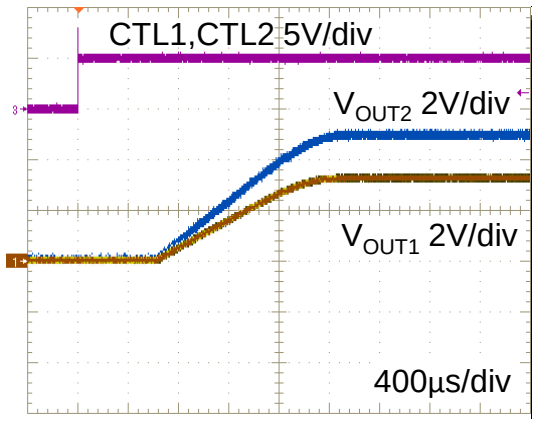


V_{IN}=24V, V_{OUT1}=3.3V

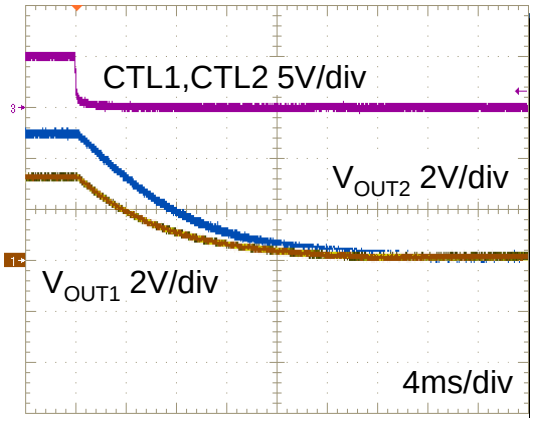


V_{IN}=24V, V_{OUT2}=5V

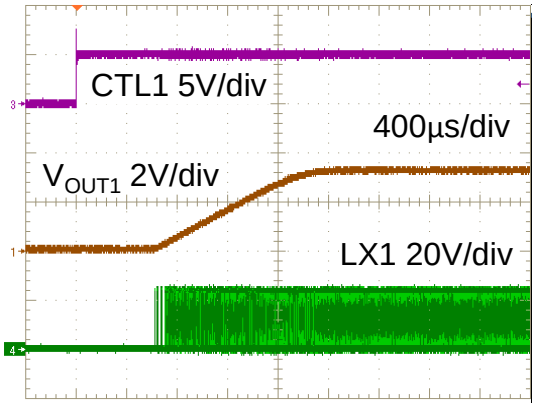
Startup, Shutdown Waveform



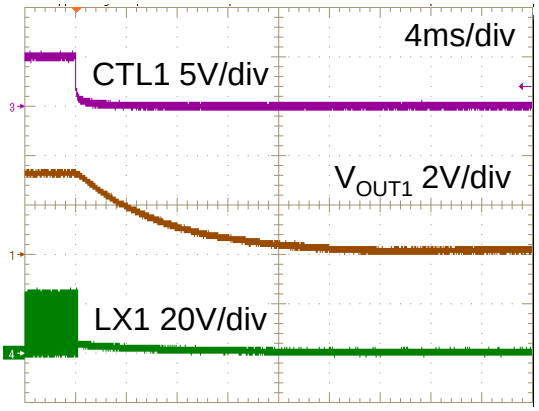
V_{IN}=24V, V_{OUT1}=3.3V, V_{OUT2}=5V, $I_{OUT1,2}$=0A



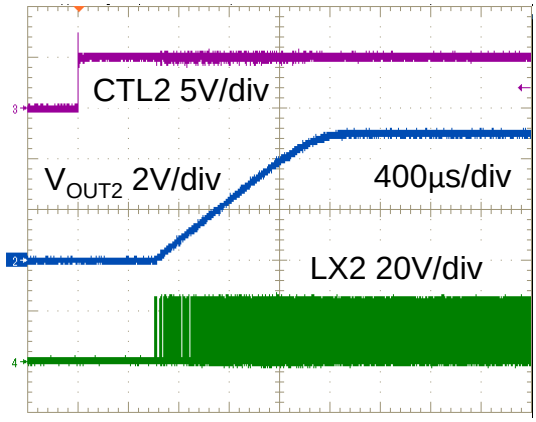
V_{IN}=24V, V_{OUT1}=3.3V, V_{OUT2}=5V, $I_{OUT1,2}$=0A



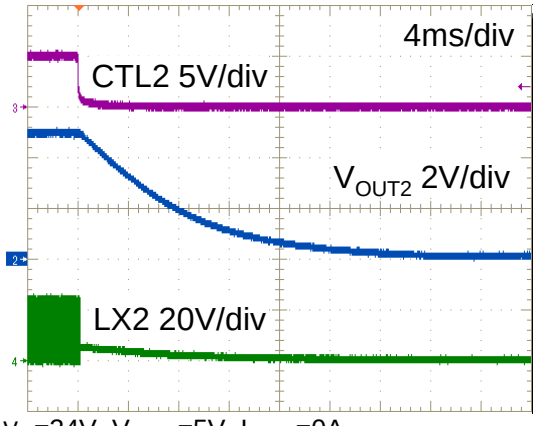
V_{IN}=24V, V_{OUT1}=3.3V, I_{OUT1}=0A



V_{IN}=24V, V_{OUT1}=3.3V, I_{OUT1}=0A



V_{IN}=24V, V_{OUT2}=5V, I_{OUT2}=0A



V_{IN}=24V, V_{OUT2}=5V, I_{OUT2}=0A

14. Usage Precaution

Printed circuit board ground lines should be set up with consideration for common impedance.

Take appropriate measures against static electricity.

- Containers for semiconductor materials should have anti−static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ in serial body and ground.

Do not apply negative voltages.

The use of negative voltages below −0.3 V may make the parasitic transistor activated to the LSI, and can cause malfunctions.

15. RoHS Compliance Information

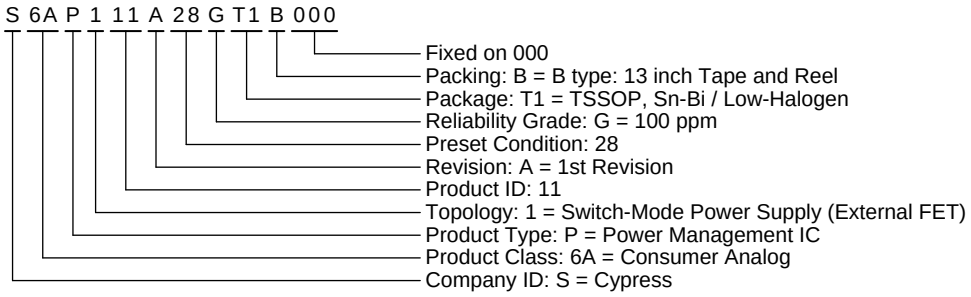
This product has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE).

16. Ordering Information

Part Number (MPN)	Package
S6AP111A28GT1B000	Plastic TSSOP (0.65 mm pitch), 24-pin (STI024)

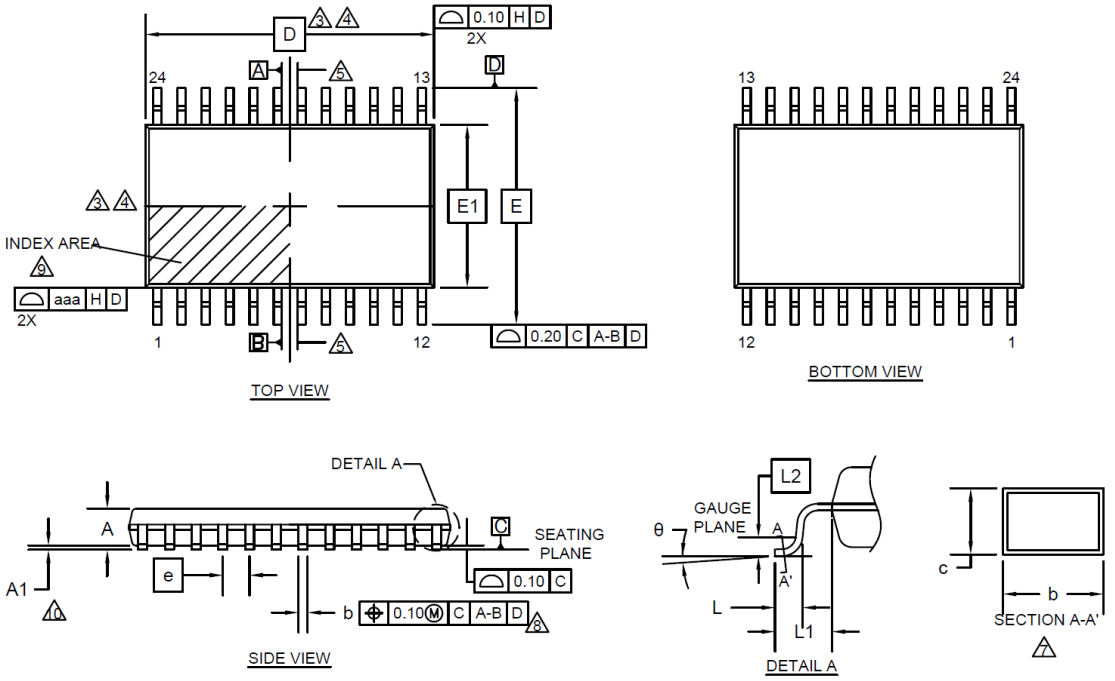
MPN: Marketing Part Number

Figure 16-1 Ordering Part Number Definitions



17. Package Dimensions

Package Code: STI024



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.20
A1	0.05	——	0.15
D	7.80 BSC		
E	6.40 BSC		
E1	4.40 BSC		
θ	0°	——	8°
c	0.10	——	0.19
b	0.20	0.22	0.29
L	0.45	0.60	0.75
L 1	1.00 REF		
L 2	0.25 BSC		
e	0.65 BSC		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A & B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. LF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
10. "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.

002-14046 Rev. **

18. Major Changes

Spansion Publication Number: S6AP111A28_DS405-00025

Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 1.0		
-	-	Preliminary → Full Production
16	10.5 ON/OFF Time Generator Block (t_{ON} Generator)	Description is changed : the CH2 ON time is set to 1/1.5 times the CH1 ON time → the CH2 frequency is set to 1.5 times the CH1 frequency
26,27	11.2 Layout	Description and picture is updated
Revision 2.0		
9	Absolute Maximum Ratings	VO1 and 2 added.
10	Recommended Operating Conditions	VO1 and 2 added.
11	Electrical Characteristics	Maximum specifications of minimum on time and minimum off time are added.
14 to 17	Typical Characteristics	Create new.
22	Function Description	Figure 11.4 modified.
23	Function Description	Figure 11.5 modified.
24	Function Description	Boost circuit Block (CB1 and 2) create new
27,28	I/O Pin Equivalent Circuit Diagram	Create new.
29	Example Application Circuit	Create new.
30,31	Part List	Create new.
37 to 44	Application Note	Selecting parts create new.

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: S6AP111A28 2ch DC/DC Converter IC with PWM Synchronous Rectification
Document Number: 002-08491

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	TAOA	08/31/2015	Migrated to Cypress and assigned document number 002-08491. No change to document contents or format.
*A	5135372	TAOA	02/16/2016	Updated to Cypress format.
*B	5641426	HIXT	02/24/2017	Updated Pin Assignment: Change the package name from FPT-24P-M10 to STI024 Added Usage Precaution Added RoHS Compliance Information Added Ordering Information Updated Package Dimensions: Updated to Cypress format
*C	5785669	MASG	06/26/2017	Adapted Cypress new logo.

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