PRELIMINARY

S6BP501A, S6BP502A

3ch DC/DC Converter IC for Automotive Cluster

S6BP501A/S6BP502A is a three channel output power management IC. This IC includes one high voltage buck DC/DC controller (DD3V), one buck DC/DC converter with built-in FETs (DD1V) and one boost DC/DC converter with built-in FETs (DD5V). Current mode architecture is used for fast load transient response. At no load, the input supply current is reduced to 15 µA (Typ). It is possible to provide stable output voltage under an automotive cold cranking condition until the input voltage falls to 2.5V. This IC is suitable for power supply solutions of automotive and Industrial applications. Each output voltage can be adjusted by external resistors. Both DD1V and DD5V support the switching frequencies up to 2.4 MHz to allow use of small size inductors, which can reduce a part mounting area. To decrease EMI, this IC equips a SYNC function that synchronizes to an external clock signal and a spread spectrum clock generator (SSCG). When not inputting an external clock, it operates by an internal clock. The SSCG is valid both internal clock and external clock. Moreover, this IC has power good (PG) monitors for each output and a thermal-warning indicator.

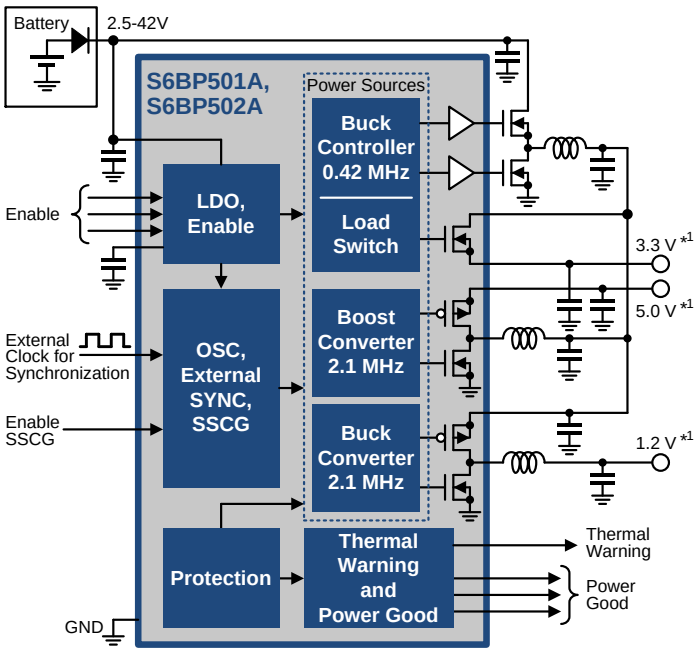
Features

- Wide input voltage range : 2.5V to 42V (DD3V)
- Adjustable output voltage with pairs of resistors
  - DD1V : 1.0V to 1.3V
  - DD3V : 3.2V to 3.4V
  - DD5V : 5.0V to 5.2V
- Switching frequency range (synchronizable to external clock by SYNC function)
  - DD1V, DD5V
    - Internal clock operation : 2.1 MHz (Typ)
    - External clock operation : 1.8 MHz to 2.4 MHz
  - DD3V (one-fifth-divided clock)
    - Internal clock operation : 420 kHz (Typ)
    - External clock operation : 360 kHz to 480 kHz
- Super-high efficiency by PFM operation (DD3V, DD5V : When fixing SYNC pin to a low level)
- Automatic PWM/PFM switching and fixed PWM operations are settable by SYNC pin (DD3V, DD5V)
- Operable on up to 100% duty (DD3V)
- Built-in phase compensators
- Built-in SSCG (spread spectrum clock generator)
- Synchronous rectification current mode architecture
- Shutdown current : 1 µA (Typ)
- Quiescent current : 15 µA (Typ)
- Load-independent soft-start
- Power good monitors for each output
  - OVD (over voltage detection)
  - UVD (under voltage detection)
- Enhanced protection functions
  - UVLO (under voltage lockout)
  - OVP (over voltage protection)
  - OCP (over current protection)
  - TSD (thermal shutdown)
  - TWI (thermal warning indicator)
- Wettable QFN-32 package : 5 mm × 5 mm
- AEC-Q100 compliant (Grade-2)

Applications

- Instrument cluster
- Automotive applications
- Industrial applications

Block Diagram



*1: Output voltages are finely adjustable with external resistive dividers

More Information

Cypress provides a wealth of data at www.cypress.com/pmic to help you to select the right PMIC device for your design, and to help you to quickly and effectively integrate the device into your design. Following is an abbreviated list for S6BP501A and S6BP502A:

- Overview: Automotive PMIC Portfolio, Automotive PMIC Roadmap
- Product Selector:
  - S6BP501A, S6BP502A: 3ch Automotive PMIC for Instrument Cluster
- Application Notes: Cypress offers S6BP501A and S6BP502A application notes. Recommended application notes for getting started with S6BP501A and S6BP502A are:
  - AN99435: Designing a Power Management System
  - AN201006: Thermal Considerations and Parameters
- Evaluation Kit Operation Manual:
  - S6SBP501A00VA1001, S6SBP502A00VA1001: Power block of automotive instrument cluster
- Related Products:
  - S6BP201A, S6BP202A, S6BP203A: 1ch Buck-Boost Automotive PMIC
  - S6BP401A: 6ch Automotive PMIC for ADAS

Contents

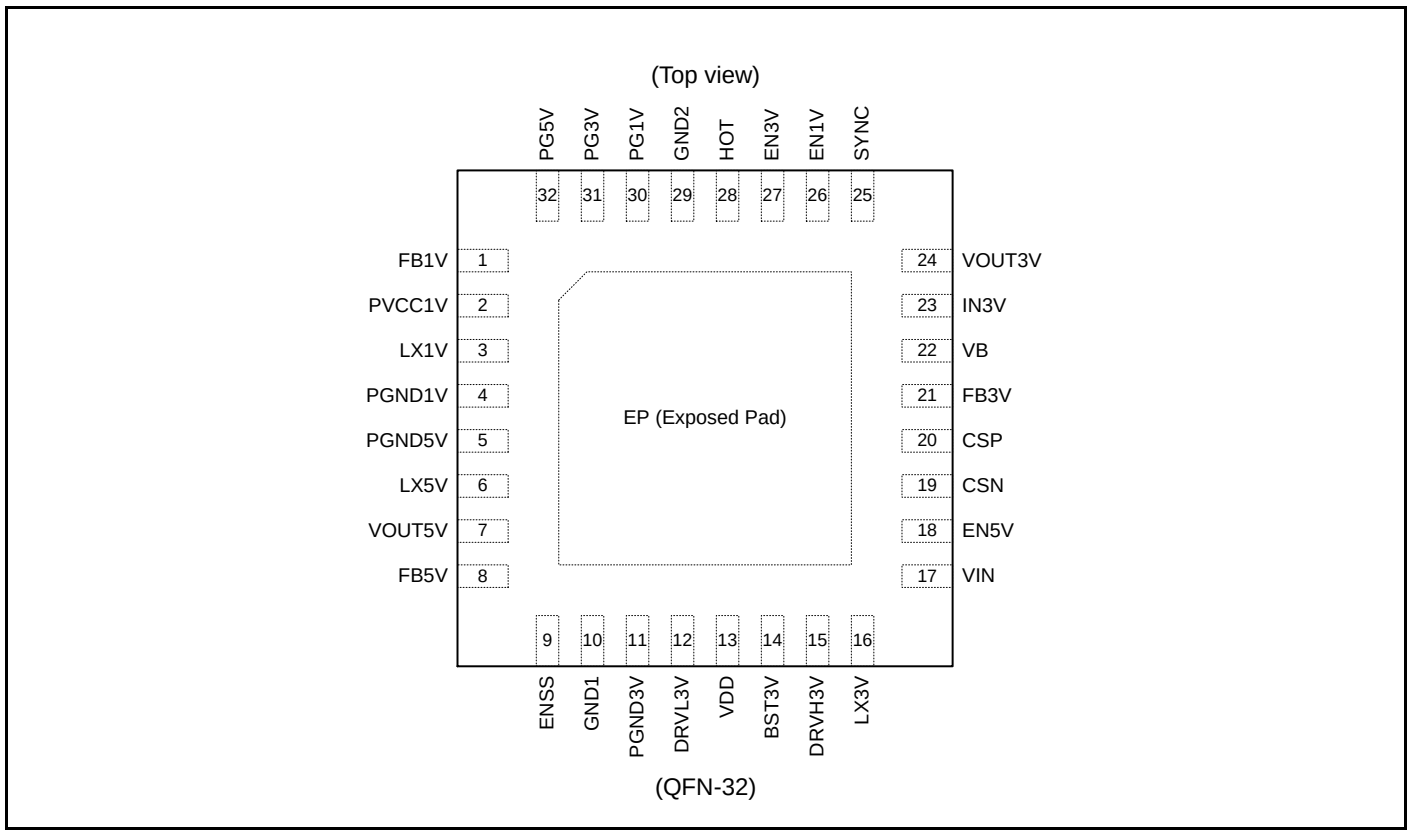
1. Product Lineup

To order a product, select an item from the product lineup blow. For information on the ordering part number, please see "13. Ordering Information".

Product Name		S6BP501A	S6BP502A
Pin count		32	
Power supply voltage range		2.5V to 42V	
Output voltage range	DD1V	1.0V to 1.3V	
	DD3V	3.2V to 3.4V	
	DD5V	5.0V to 5.2V	
Maximum output current	DD1V	1.4A	2.0A
	SW3V (*1)	1.6A	1.9A
	DD5V	1.3A	1.3A
Package		QFN-32 (VNG032)	

*1: Load switch for DD3V. Each value is the maximum output current via SW3V.

2. Pin Assignment

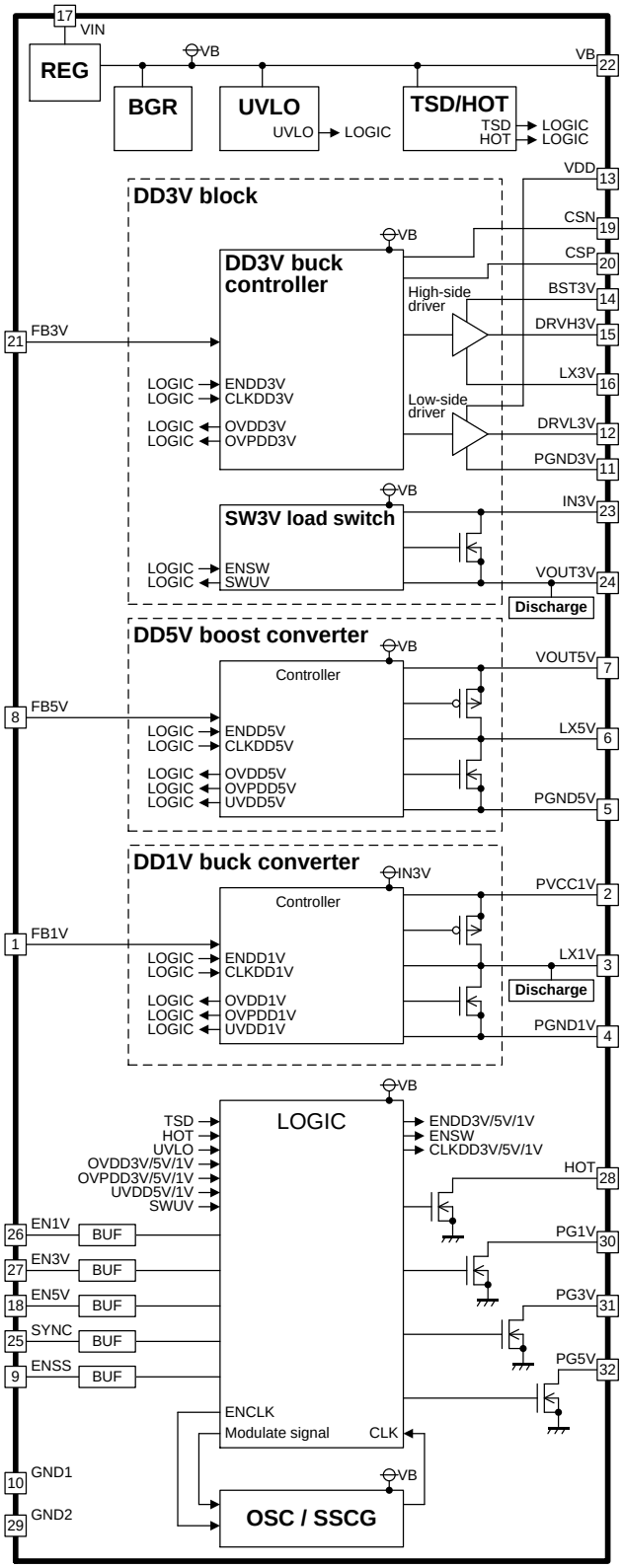


3. Pin Descriptions

Table 3-1 Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	FB1V	I	Feedback pin for DD1V output voltage
2	PVCC1V	−	Power supply pin for DD1V
3	LX1V	O	Inductor connection pin for DD1V
4	PGND1V	−	Power ground pin for DD1V
5	PGND5V	−	Power ground pin for DD5V
6	LX5V	O	Inductor connection pin for DD5V
7	VOUT5V	O	Voltage output pin for DD5V
8	FB5V	I	Feedback pin for DD5V output voltage
9	ENSS	I	Enable pin for SSCG (When not being used, connect this pin to ground pin. For the pin setting, see "Table 8-1 SSCG Pin Setting".)
10	GND1	−	Ground pin
11	PGND3V	−	Power ground for DD3V
12	DRVL3V	O	Low-side FET gate driver output pin for DD3V
13	VDD	I	Power supply pin for gate driver for DD3V
14	BST3V	I	Boost capacitor connection pin for DD3V
15	DRVH3V	O	High-side FET gate driver output pin for DD3V
16	LX3V	O	Inductor connection pin for DD3V
17	VIN	I	Power supply pin connecting battery
18	EN5V	I	Enable pin for DD3V and DD5V
19	CSN	I	Negative current sense pin
20	CSP	I	Positive current sense pin
21	FB3V	I	Feedback pin for DD3V output voltage
22	VB	O	Bias voltage output pin and power supply pin for logic Do NOT connect any loads to this pin
23	IN3V	I	Power supply pin for load switch (SW3V) and DD1V
24	VOUT3V	O	Voltage output pin for DD3V via load switch (SW3V)
25	SYNC	I	External clock input / SYNC function setting pin (For the pin setting, see "Table 8-2 SYNC Pin Setting".)
26	EN1V	I	Enable pin for DD1V
27	EN3V	I	Enable pin for SW3V load switch (SW3V)
28	HOT	O	Open drain type power good output pin for thermal warning indicator (When not being used, connect this pin to ground pin)
29	GND2	−	Ground pin
30	PG1V	O	Open drain type power good output pin for DD1V (When not being used, connect this pin to ground pin)
31	PG3V	O	Open drain type power good output pin for DD3V (When not being used, connect this pin to ground pin)
32	PG5V	O	Open drain type power good output pin for DD5V (When not being used, connect this pin to ground pin)

4. Architecture Block Diagram



5. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage (*1)	V_{VIN}	VIN pin	−0.3	+48	V
	V_{VB}	VB pin	−0.3	+6.9	V
	V_{VDD}	VDD pin	−0.3	+6.9	V
	V_{PVCC1V}	PVCC1V pin	−0.3	+6.9	V
	V_{IN3V}	IN3V pin	−0.3	+6.9	V
Pin voltage (*1)	V_{BST3V}	BST3V pin	−0.3	+48	V
	V_{CSN}	CSN pin	−0.3	V_{VB}	V
	V_{CSP}	CSP pin	−0.3	V_{VB}	V
	V_{FB1V}	FB1V pin	−0.3	V_{VB}	V
	V_{FB3V}	FB3V pin	−0.3	V_{VB}	V
	V_{FB5V}	FB5V pin	−0.3	+6.9	V
	V_{EN1V}	EN1V pin	−0.3	+6.9	V
	V_{EN3V}	EN3V pin	−0.3	+6.9	V
	V_{EN5V}	EN5V pin	−0.3	+48	V
	V_{PG1V}	PG1V pin	−0.3	+6.9	V
	V_{PG3V}	PG3V pin	−0.3	+6.9	V
	V_{PG5V}	PG5V pin	−0.3	+6.9	V
	V_{HOT}	HOT pin	−0.3	+6.9	V
	V_{ENSS}	ENSS pin	−0.3	V_{VB}	V
	V_{SYNC}	SYNC pin	−0.3	+6.9	V
LX voltage (*1)	V_{LX1V}	LX1V pin	−0.3	+6.9	V
	V_{LX3V}	LX3V pin	−0.3	+48	V
	V_{LX5V}	LX5V pin	−0.3	+6.9	V
Difference voltage	V_{BST3V_LX3V}	BST3V to LX3V	−0.3	+6.9	V
	V_{DRVH3V_LX3V}	DRVH3V to LX3V	−0.3	+6.9	V
	V_{DRVH3V_LX3V}	DRVL3V to PGND3V	−0.3	+6.9	V
	V_{LX5V_VOUT5V}	LX5V to VOUT5V	−0.3	+6.9	V
	V_{LX1_PVCC1V}	LX1 to PVCC1V	−0.3	+6.9	V
	V_{PGND1_GND}	PGND1V to GND1, PGND1V to GND2	−0.3	+0.3	V
	V_{PGND3_GND}	PGND3V to GND1, PGND3V to GND2	−0.3	+0.3	V
	V_{PGND5_GND}	PGND5V to GND1, PGND5V to GND2	−0.3	+0.3	V
	V_{VIN_EN5V}	VIN to EN5V	−0.3	+48	V
	V_{VB_INPUT}	VB to EN1V, VB to EN3V, VB to FB1V, VB to FB3V, VB to FB5V	−0.3	+6.9	V
Output current	I_{PG}	PG1V, PG3V, PG5V sink current	−3	0	mA
	I_{HOT}	HOT sink current	−3	0	mA
Power dissipation (*1)	P_D	Ta ≤ ±25°C	0	4280 (*2)	mW
Storage temperature	T_{STG}	−	−55	+150	°C

*1: PGND1V = PGND3V = PGND5V = GND1 = GND2 = 0V

*2: When the product is mounted on 76.2 mm × 114.3 mm, four-layer FR−4 board

Warning:

1. *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.*

6. Recommended Operating Conditions

Parameter	Symbol	Condition		Value			Unit
				Min	Typ	Max	
Power supply voltage (*1)	V_{VIN_START}	VIN pin	At initial start-up	+6.8	−	−	V
	V_{VIN}	VIN pin	After start-up	+4.5	+12	+42	V
			After start-up, Ta = 25°C	+3.7	+12	+42	V
			After start-up, Ta = 25°C, VOUT5V current = 1 mA, V_{EN1V} = V_{EN3V} = 0V	+2.5	+12	+42	V
	V_{VDD}	VDD pin		−	V_{VOUT5V}	−	V
	V_{PVCC1V}	PVCC1V pin		−	+3.3	−	V
	V_{IN3V}	IN3V pin		−	+3.3	−	V
Pin voltage (*1)	V_{EN1V}	EN1V pin		0	−	+5.5	V
	V_{EN3V}	EN3V pin		0	−	+5.5	V
	V_{EN5V}	EN5V pin		0	−	V_{VIN}	V
	V_{PG1V}	PG1V pin		0	−	+5.5	V
	V_{PG3V}	PG3V pin		0	−	+5.5	V
	V_{PG5V}	PG5V pin		0	−	+5.5	V
	V_{HOT}	HOT pin		0	−	+5.5	V
	V_{ENSS}	ENSS pin		0	−	V_{VB}	V
	V_{SYNC}	SYNC pin		0	−	+5.5	V
Input clock frequency	F_{SYNC}	SYNC pin		1.8	2.1	2.4	MHz
Input clock duty range	D_{SYNC}	SYNC pin		48	50	52	%
LX voltage (*1)	V_{LX5V}	LX5V pin		0	−	+5.5	V
DD1V output voltage (*1)	V_{VOUT1V}	Voltage of DD1V output capacitor		1.0	−	1.3	V
DD3V output voltage (*1)	V_{IN3V} (*2)	Voltage of DD3V output capacitor, IN3V pin		3.2	−	3.4	V
DD5V output voltage (*1)	V_{VOUT5V}	VOUT5V pin		5.0	−	5.2	V
BST capacitance	C_{BST}	BST3V to LX3V		0.068	0.1	0.47	µF
VB capacitance	C_{VB}	VB to GND		2.2	4.7	10	µF
Operating ambient temperature	Ta	−		−40	+25	+105	°C

*1: PGND1V = PGND3V = PGND5V = GND1 = GND2 = 0V

*2: V_{IN3V} is defined as DD3V output voltage, and V_{VOUT3V} (VOUT3V pin voltage) is defined as the DD3V output voltage via SW3V.

Warning:

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*
2. *Any use of semiconductor devices will be under their recommended operating condition.*
3. *Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.*
4. *No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.*

7. Electrical Characteristics

V_{VIN} = V_{EN5V} = 12V, V_{PVCC1V} = 3.3V, V_{VB} = V_{VDD} = V_{EN1V} = V_{EN3V} = 5.0V

(Unless specified otherwise, these are the electrical characteristics under the recommended operating environment.)

Parameter		Symbol	Condition		Value Min	Value Typ	Value Max	Unit
Supply current	Shutdown current	I_{SHDN}	VIN pin current, V_{VIN} = 12V, V_{EN1V} = V_{EN3V} = V_{EN5V} = 0V		–	1.0	–	µA
	Quiescent current	Iq	VIN pin current, V_{VIN} = 12V, V_{SYNC} = 0V, V_{EN1V} = V_{EN3V} = 0V, V_{EN5V} = 12V, All DC/DC converters with no load, External FET: NVTFS5826NL		–	15 (*1)	25 (*1)	µA
	VB supply current	I_{VB}	VB pin current, V_{VB} = 5V, V_{SYNC} = V_{VB}, V_{EN1V} = V_{EN3V} = 5V, V_{EN5V} = 12V, All DC/DC converters with no load		–	20	–	mA
UVLO block	IC operation start voltage	V_{UVLO_START}	VB pin, V_{VB} rising		4.3	4.4	4.5	V
	IC shutdown voltage	V_{UVLO_SHDN}	VB pin, V_{VB} falling		4.2	4.3	4.4	V
DD1V block	Feedback voltage	V_{FB1V}	FB1V pin		0.591 (−1.5%)	0.6	0.609 (+1.5%)	V
	Output regulation	–	DD1V output voltage (V_{VOUT1V}) , V_{PVCC1V} = V_{IN3V} = 3.3V, I_{VOUT1V} = 0 to 2.0A		−1.5 (*1)	–	+1.5 (*1)	%
	Over voltage protection (OVP) voltage	V_{OVPR_1V}	Monitoring V_{FB1V} rising		128.0	131.5	135.0	%
	Over voltage protection release voltage	V_{OVPF_1V}	–		–	–	0.94 (*1)	V
	High-side FET ON resistance	R_{ONH_1V}	I_{LX1V} = 50 mA (PVCC1V to LX1V)		–	130	–	mΩ
	Low-side FET ON resistance	R_{ONL_1V}	I_{LX1V} = −50 mA (LX1V to PGND1V)		–	100	–	mΩ
	FET leak current	I_{LEAK_1V}	V_{PVCC1V} = 5.0V, V_{EN1V} = 0V		–	–	3	µA
	Maximum output current	I_{OUTMAX_1V}	L = 1.5 µH	S6BP501A	1.4 (*1)	–	–	A
				S6BP502A	2.0 (*1)	–	–	A
	Over current protection current (LX peak current)	I_{LXPEAK_1V}	L = 1.5 µH	S6BP501A	1.75 (*1)	–	–	A
				S6BP502A	2.5 (*1)	–	–	A
	Discharge resistance	R_{DIS_1V}	LX1V pin		–	400	–	Ω
	Soft-start time	t_{SS_1V}	–		–	1.0	–	ms
DD3V block	Feedback voltage	V_{FB3V}	FB3V pin		0.8865 (−1.5%)	0.9	0.9135 (+1.5%)	V
	Output regulation	–	IN3V pin, V_{VIN} = 4.5V to 42V, I_{IN3V} = 0A to 5.1A		−1.25 (*1)	–	+1.25 (*1)	%
	PWM/PFM switching current	I_{PWMPFM_3V}	–		–	1000 (*1)	–	mA
	Over voltage protection (OVP) voltage	V_{OVPR_3V}	Monitoring V_{VOUT3V} rising		3.70	3.85	4.00	V
	Over voltage protection release voltage	V_{OVPF_3V}	–		–	–	0.94 (*1)	V
	Dead time	t_{DEAD_3V}	–		10	20	–	ns
	Maximum duty cycle	D_{MAX_3V}	V_{VIN} < V_{IN3V}		–	–	100	%
	Soft-start time	t_{SS_3V}	–		–	1.0	–	ms

V_{VIN} = V_{EN5V} = 12V, V_{PVCC1V} = 3.3V, V_{VB} = V_{VDD} = V_{EN1V} = V_{EN3V} = 5.0V
(Unless specified otherwise, these are the electrical characteristics under the recommended operating environment.)

Parameter			Symbol	Condition	Value			Unit
					Min	Typ	Max	
DD3V block	High-side output driver	ON resistance	R_{ONH_3V}	DRVH3V pin current = 10 mA, (BST3V to DRVH3V)	−	15	−	Ω
			R_{ONL_3V}	DRVH3V pin current = −50 mA, (DRVH3V to LX3V)	−	1	−	Ω
	Low-side output driver	ON resistance	R_{ONH_3V}	DRVL3V pin current = 50 mA, (PLX3V to DRVL3V)	−	1.5	−	Ω
			R_{ONL_3V}	DRVL3V pin current = −50 mA, (DRVL3V to LX3V)	−	0.75	−	Ω
	Boost switch	ON resistance	R_{ON_BSTSW}	I_{BST3V} = 10 mA	−	8	24	Ω
		Leak current	I_{R_BSTSW}	V_{BST3V} = 47V	−	−	2	µA
	Output current monitor	Over current limit	−	V_{CSP} − V_{CSN}	60	80	100	mV
		CSP input current	I_{CSP}	Fixed PWM operation	−	2	5	µA
		CSN input current	I_{CSN}	Fixed PWM operation	−	8	20	µA
	SW3V block	ON resistance	R_{ON_SW3V}	IN3V to VOUT3V current = 50 mA	−	−	100	mΩ
		Maximum output current	I_{LOAD_SW3V}	S6BP501A	1.6 (*1)	−	−	A
				S6BP502A	1.9 (*1)	−	−	A
		Leak current	I_{LEAK_SW3V}	V_{IN3V} = 3.3V, V_{EN3V} = 0V	−	−	3	µA
		Discharge resistance	R_{DIS_SW3V}	−	−	400	−	Ω
		Soft-start time	t_{SS_SW3V}	−	−	2.0	−	ms
DD5V block	Feedback voltage		V_{FB5V}	FB5V pin	1.182 (−1.5%)	1.2	1.218 (+1.5%)	V
	Output regulation		−	DD5V output voltage (V_{VOUT5V}), V_{IN3V} = 3.3V, I_{VOUT5V} = 0A to 1.3A	−3.0 (*1)	−	+3.0 (*1)	%
	PWM/PFM switching current		I_{PWMPFM_5V}	−	−	300 (*1)	−	mA
	Over voltage protection (OVP) voltage		V_{OVPR_5V}	Monitoring V_{VOUT5V} rising	5.6	5.8	6.0	V
	Over voltage protection release voltage		V_{OVPF_5V}	−	−	−	0.94 (*1)	V
	High-side FET ON resistance		R_{ONH_5V}	I_{LX5V} = 50 mA (VOUT5V to LX5V)	−	130	−	mΩ
	Low-side FET ON resistance		R_{ONL_5V}	I_{LX5V} = −50 mA (LX5V to PGND5V)	−	100	−	mΩ
	FET leak current		I_{LEAK_5V}	V_{VOUT5V} = 5.0V, V_{EN5V} = 0V	−	−	3	µA
	Maximum output current		I_{OUT_MAX5V}	L = 1.5 µH, S6BP501A	1.3 (*1)	−	−	A
				L = 1.5 µH, S6BP502A	1.3 (*1)	−	−	A
	Over current protection current (LX peak current)		I_{LX_PEAK5V}	L = 1.5 µH, S6BP501A	2.5 (*1)	−	−	A
				L = 1.5 µH, S6BP502A	2.5 (*1)	−	−	A
	Soft-start time		t_{SS_5V}	V_{VOUT5V} = 3.3V > 5.0V	−	0.5	−	ms

V_{VIN} = V_{EN5V} = 12V, V_{PVCC1V} = 3.3V, V_{VB} = V_{VDD} = V_{EN1V} = V_{EN3V} = 5.0V

(Unless specified otherwise, these are the electrical characteristics under the recommended operating environment.)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
EN1V pin	ON condition	V_{ON_EN1V}	−	2.0	−	−	V
	OFF condition	V_{OFF_EN1V}	−	−	−	0.4	V
	Input current	I_{ON_EN1V}	V_{EN1V} = 5.0V	−	50	−	µA
	Pull down resistance	R_{PULL_EN1V}	−	50	100	150	kΩ
EN3V pin	ON condition	V_{ON_EN3V}	−	2.0	−	−	V
	OFF condition	V_{OFF_EN3V}	−	−	−	0.4	V
	Input current	I_{ON_EN3V}	V_{EN3V} = 5.0V	−	50	−	µA
	Pull down resistance	R_{PULL_EN3V}	−	50	100	150	kΩ
EN5V pin	ON condition	V_{ON_EN5V}	−	2.5	−	−	V
	OFF condition	V_{OFF_EN5V}	−	−	−	0.2	V
	Input current	I_{ON_EN5V}	V_{EN5V} = 12.0V	−	1	3	µA
		I_{OFF_EN5V}	V_{EN5V} = 0V	−	0	−	µA
PG1V pin	Over voltage detection (OVD) voltage	V_{OVDR_PG1V}	Monitoring V_{FB1V} rising	105.0	106.5	108.0	%
	Over voltage detection release voltage	V_{OVDF_PG1V}	Monitoring V_{FB1V} falling	−	105.5	−	%
	Under voltage detection (UVD) voltage	V_{UVDF_PG1V}	Monitoring V_{FB1V} falling	92.5	94.0	95.5	%
	Under voltage detection release voltage	V_{UVDR_PG1V}	Monitoring V_{FB1V} rising	−	95.0	−	%
	Leak current	I_{LEAK_PG1V}	V_{PG5V} = 5.0V	−	−	1	µA
	Low level voltage	V_{LOW_PG1V}	I_{PG5V} = 3 mA	−	0.15	0.30	V
	Power-on reset time	t_{POR_PG1V}	V_{SYNC} = 0V	8	10	12	ms
PG3V pin	Over voltage detection (OVD) voltage	V_{OVDR_PG3V}	Monitoring V_{FB3V} rising	104.5	106.0	107.5	%
	Over voltage detection release voltage	V_{OVDF_PG3V}	Monitoring V_{FB3V} falling	−	105.0	−	%
	Under voltage detection (UVD) voltage	V_{UVDF_PG3V}	Monitoring V_{VOUT3V} falling	3.004	3.050	3.096	V
	Under voltage detection release voltage	V_{UVDR_PG3V}	Monitoring V_{VOUT3V} rising	−	3.080	−	V
	Leak current	I_{LEAK_PG3V}	V_{PG3V} = 5.0V	−	−	1	µA
	Low level voltage	V_{LOW_PG3V}	I_{PG3V} = 3 mA	−	0.15	0.30	V
	Power-on reset time	t_{POR_PG3V}	V_{SYNC} = 0V	8	10	12	ms
PG5V pin	Over voltage detection (OVD) voltage	V_{OVDR_PG5V}	Monitoring V_{FB5V} rising	106.0	108.0	110.0	%
	Over voltage detection release voltage	V_{OVDF_PG5V}	Monitoring V_{FB5V} falling	−	107.0	−	%
	Under voltage detection (UVD) voltage	V_{UVDF_PG5V}	Monitoring V_{FB5V} falling	90.0	92.0	94.0	%
	Under voltage detection release voltage	V_{UVDR_PG5V}	Monitoring V_{FB5V} rising	−	93.0	−	%
	Leak current	I_{LEAK_PG5V}	V_{PG5V} = 5.0V	−	−	1	µA
	Low level voltage	V_{LOW_PG5V}	I_{PG5V} = 3 mA	−	0.15	0.30	V
	Power-on reset time	t_{POR_PG5V}	V_{SYNC} = 0V	8	10	12	ms

V_{VIN} = V_{EN5V} = 12V, V_{PVCC1V} = 3.3V, V_{VB} = V_{VDD} = V_{EN1V} = V_{EN3V} = 5.0V

(Unless specified otherwise, these are the electrical characteristics under the recommended operating environment.)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
TSD block	Operation shutdown temperature	T_{TSDR}	Tj (*2) rising	−	+165 (*1)	−	°C
	Operation restart temperature	T_{TSDF}	Tj (*2) falling	−	+155 (*1)	−	°C
HOT pin	Thermal warning indicator temperature	T_{TWIR_HOT}	Tj (*2) rising	−	+140 (*1)	−	°C
	Thermal warning indicator release temperature	T_{TWIF_HOT}	Tj (*2) falling	−	+130 (*1)	−	°C
	Leak current	I_{LEAK_HOT}	V_{HOT} = 5.0V	−	−	1	µA
	Low level voltage	V_{LOW_HOT}	I_{PG} = 3 mA	−	0.15	0.30	V
OSC block	Switching frequency	F_{OSC1}	DD1V, DD5V, In internal clock operation	2.0	2.1	2.2	MHz
		F_{OSC2}	DD3V, F_{OSC2} = F_{OSC1} / 5, In internal clock operation	0.40	0.42	0.44	MHz
SYNC Pin/ SYNC block	High level voltage	V_{HIGH_SYNC}	In external clock input	2.0	−	−	V
	Low level voltage	V_{LOW_SYNC}	In external clock input	−	−	0.4	V
	Input current	I_{IN_SYNC}	V_{SYNC} = 5.0V	−	50	−	µA
	Pull down resistance	R_{PULL_SYNC}	−	50	100	150	kΩ
	Input frequency	F_{IN_SYNC}	In external clock input	1.8	−	2.4	MHz
	Switching frequency	F_{OSC1_SYNC}	DD1V, DD5V, F_{OSC1_SYNC} = F_{IN_SYNC}, In external clock operation	1.8	−	2.4	MHz
		F_{OSC2_SYNC}	DD3V, F_{OSC2_SYNC} = F_{IN_SYNC} / 5, In external clock operation	0.36	−	0.48	MHz
SSCG block	Modulation range	−	V_{ENSS} = V_{VB}	−	6 (*1)	−	%
	Modulation frequency	F_{MOD}	−	−	4	−	kHz
ENSS pin	ON condition	V_{ON_ENSS}	SSCG function ON	V_{VB} × 0.8	−	−	V
	OFF condition	V_{OFF_ENSS}	SSCG function OFF	−	−	V_{VB} × 0.2	V
	Input current	I_{ENSS}	−	−0.1	−	+0.1	µA

*1: The electrical characteristic is ensured by statistical characterization and indirect tests.

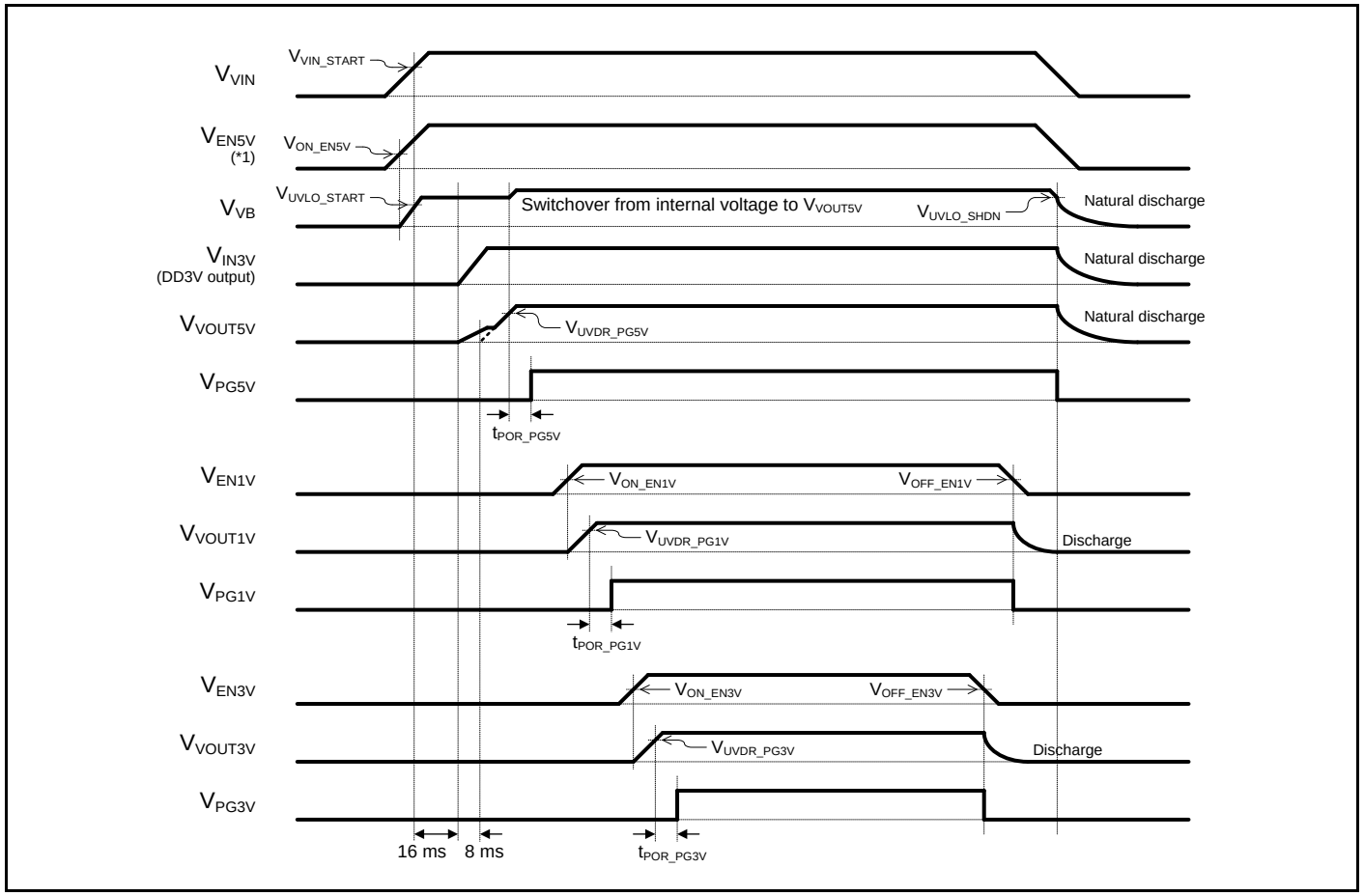
*2: Junction temperature

8. Functional Description

8.1 Operation Sequence

The operation sequence of this IC is described in this section.

Figure 8-1 Turn On and Turn Off Sequence



*1: When the V_{EN5V} drops to the V_{OFF_EN5V} while supplying a power to the VIN pin, the voltages, V_{PG1V}, V_{PG3V}, V_{PG5V} and V_{HOT}, are undefined.

8.2 Each Function Block

Each function block is described in this section.

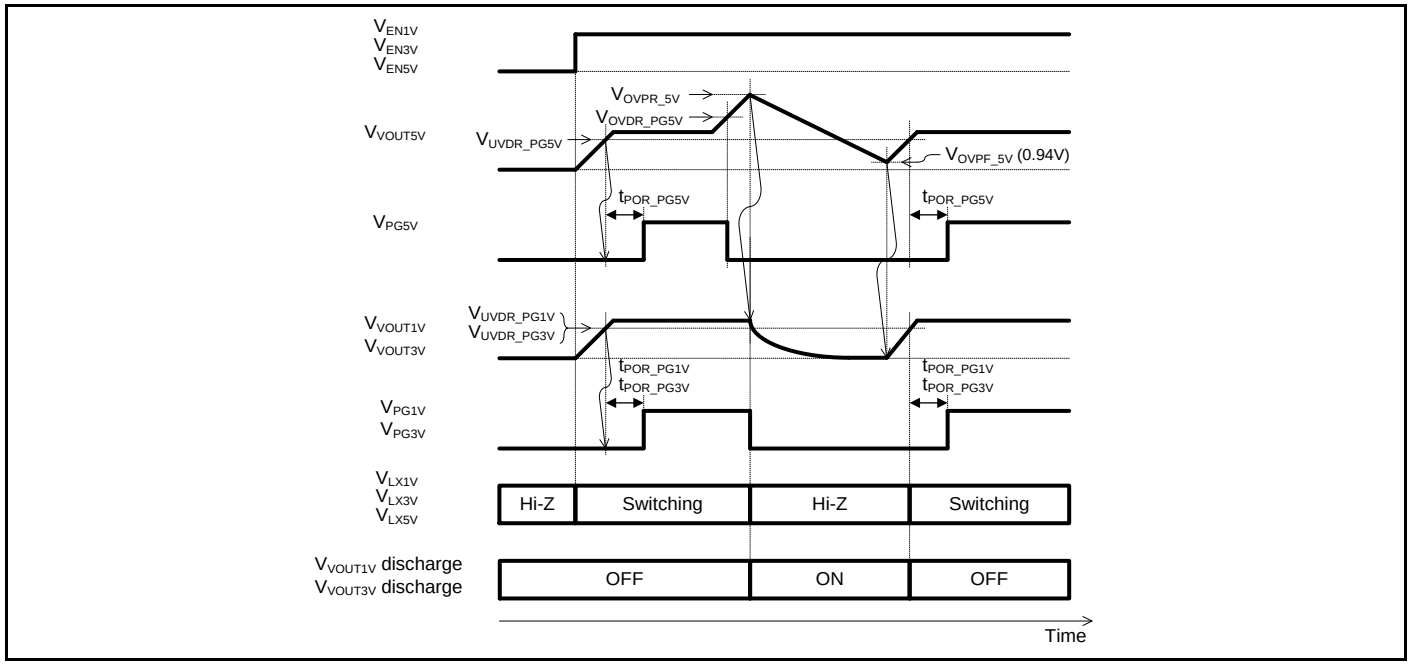
Under Voltage Lockout (UVLO)

This IC equips an UVLO function in order to prevent itself from operating unintentionally and from destructing or deteriorating its subsequent devices. The UVLO block monitors the VB voltage. Once VB unintentionally drops below the IC shutdown voltage (V_{UVLO_SHDN}), UVLO block prohibits the regulators and controllers switching FETs until VB becomes higher than the IC operation start voltage (V_{UVLO_START}).

Over Voltage Detection and Protection (OVD, OVP)

When an output voltage exceeds the over voltage detection (OVD) voltage, the corresponding PG is asserted the low level. In case any output voltage exceeds the over voltage protection (OVP) voltage, all output channels stop working to protect the connected devices. When all output voltage fall below the over voltage protection release voltage, this IC returns to the normal operation.

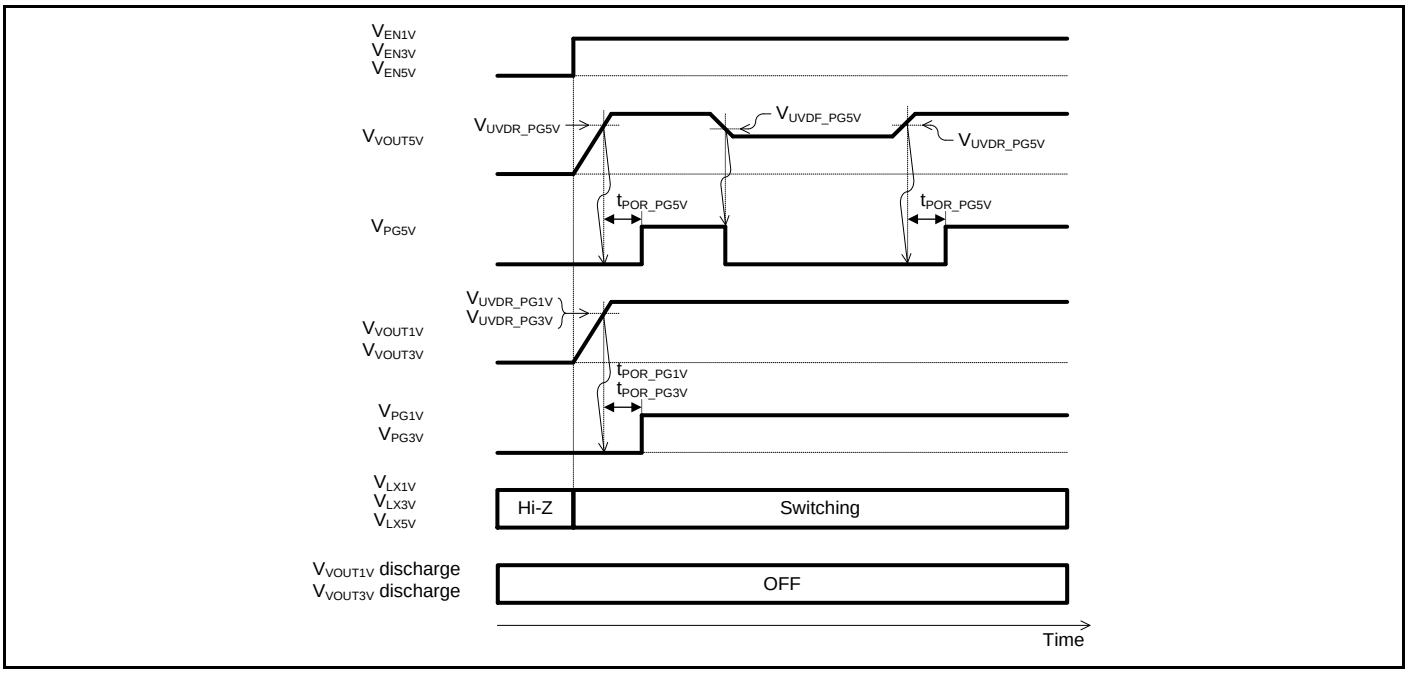
Figure 8-2 Over Voltage Detection and Over Voltage Protection Sequence



Under Voltage Detection (UVD)

When an output voltage falls below the under voltage detection (UVD) voltage, the corresponding PG pin is asserted the low level while the corresponding output channel keeps working. When the output voltage exceeds the under voltage detection release voltage, each PG will be recovered Hi-Z.

Figure 8-3 Under Voltage Detection Sequence



Over Current Protection (OCP)

In order to protect FETs from an excessive current, each output channel equips the OCP (over current protection) that sets current limits by monitoring the corresponding over current protection current (LX peak current).

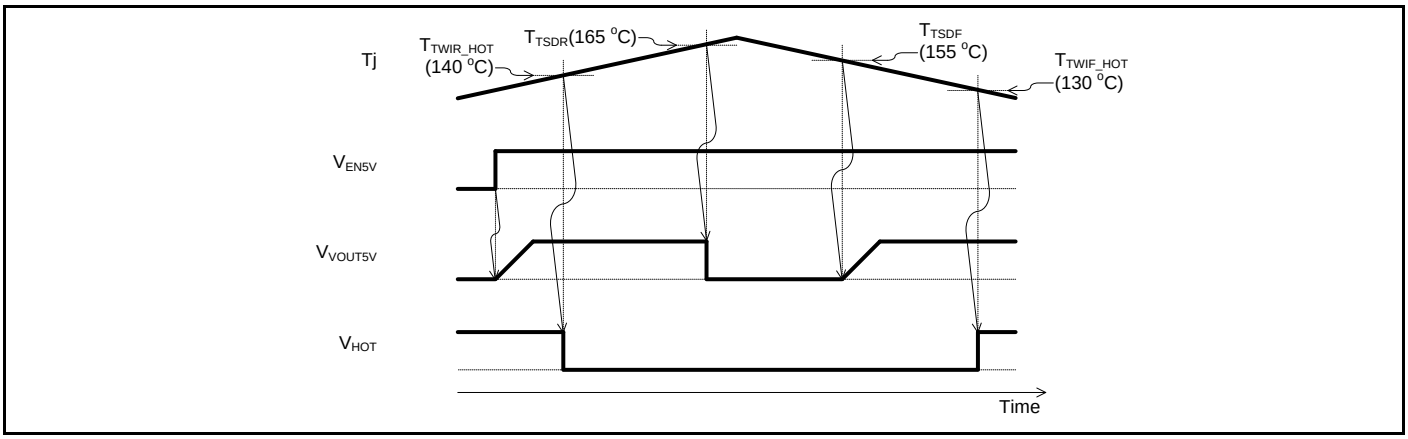
Thermal Shutdown (TSD)

The Thermal shutdown prevents this IC from a thermal destruction. If the junction temperature exceeds +165°C, all DC/DC converters stop working. When the junction temperature falls below +155°C, this IC returns to the normal operation.

Thermal Warning Indicator (HOT)

Prior to TSD, this IC is able to notice its subsequent devices that it is close to the limit temperature. The HOT pin is an open-drain output. If the junction temperature reaches +140°C, the HOT pin is asserted the low level. When the junction temperature falls below +130°C, the HOT pin will be recovered Hi-Z.

Figure 8-4 Thermal Shutdown and Thermal Warning Indicator Sequence



SSCG

This IC equips a SSCG (spread spectrum clock generator) function. When SSCG function turns on, it decreases EMI noise immediately. SSCG function modulates the clock signal by 0% to +6%, which clock signal can be sourced from the internal oscillator or an external clock source.

Table 8-1 SSCG Pin Setting

ENSS Pin Setting (*1)	SSCG Operation
L	SSCG function turns off. DD1V, DD3V and DD5V are provided with non-modulated clock
H	SSCG function turns on. DD1V, DD3V and DD5V are provided modulated.

*1: The H means $V_{ENSS} > V_{ON\_ENSS}$. The L means $V_{ENSS} < V_{OFF\_ENSS}$.

SYNC

This IC equips a SYNC function that is to synchronize with an external clock signal supplied from SYNC. Also, the switching between the automatic PWM/PFM switching operation or the fixed PWM operation is set by the SYNC pin. The Table 8-2 shows the state corresponding to each operation by the SYNC pin setting. Please refer to the Table 8-3 for the switching signals to be inputted to the SYNC pin and the availability. The switching frequency of the DD3V (F_{OSC2}) is a signal obtained by one-fifth dividing an internal clock or an inputted external clock.

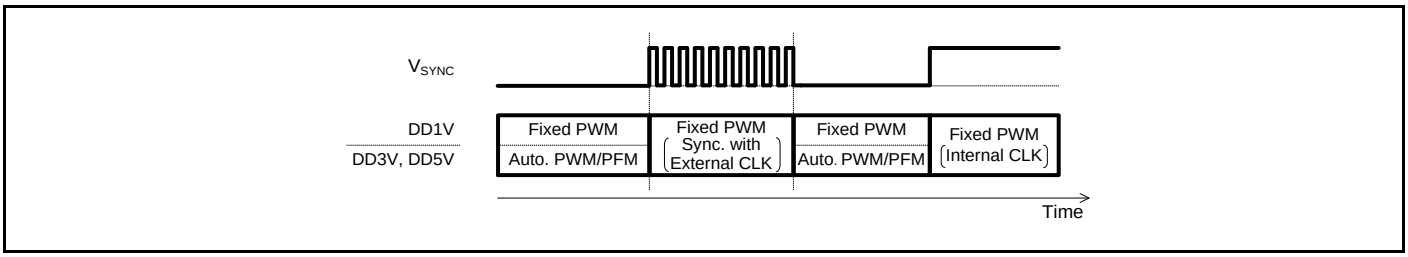
Table 8-2 SYNC Pin Setting

SYNC Pin Setting	DD1V Operation	DD3V Operation	DD5V Operation
L	Fixed PWM operation with internal clock	Automatic PWM/PFM switching operation with internal clock	Automatic PWM/PFM switching operation with internal clock
H	Fixed PWM operation with internal clock		
CLK	Fixed PWM operation synchronized with external clock		

Table 8-3 Switching signals to be inputted to the SYNC pin

Signals to be inputted to SYNC pin	Enable Pin Setting			Availability
	EN1V	EN3V	EN5V	
L ↔ CLK L ↔ H	L	L	H	Prohibited
	L or H	H	H	Available
	H	L or H	H	Available
H ↔ CLK	L or H	L or H	H	Available

Figure 8-5 SYNC Function Sequence



8.3 Output State and Protection Function Table

The following table shows the state of each output and each protection function.

Table 8-4 Output State and Protection Function Table

State	Enable Pin Setting (*1)			Output State (*2)				PG Pin Output (*3)			Remarks
	EN1V	EN3V	EN5V	DD1V	DD3V	SW3V	DD5V	PG1V	PG3V	PG5V	
DD1V, SW3V, DD5V are inactive	X	X	L	INA	INA	INA	INA	L	L	L	–
DD5V is active	L	L	H	INA	A	INA	A	L	L	Hi-Z	–
SW3V, DD5V are active	L	H	H	INA	A	A	A	L	Hi-Z	Hi-Z	–
DD1V, DD5V are active	H	L	H	A	A	INA	A	Hi-Z	L	Hi-Z	–
DD1V, SW3V, DD5V are active	H	H	H	A	A	A	A	Hi-Z	Hi-Z	Hi-Z	–
V_{VOUT1V} OVD	H	H	H	A	A	A	A	L	Hi-Z	Hi-Z	$V_{VOUT1V} > V_{OVDR\_PG1V}$
V_{VOUT3V} OVD	H	H	H	A	A	A	A	Hi-Z	L	Hi-Z	$V_{VOUT3V} > V_{OVDR\_PG3V}$
V_{VOUT5V} OVD	H	H	H	A	A	A	A	Hi-Z	Hi-Z	L	$V_{VOUT5V} > V_{OVDR\_PG5V}$
V_{VOUT1V} OVP	H	X	H	INA	INA	INA	INA	L	L	L	$V_{VOUT1V} > V_{OVPR\_1V}$
V_{VOUT3V} OVP	X	H	H	INA	INA	INA	INA	L	L	L	$V_{VOUT3V} > V_{OVPR\_3V}$
V_{VOUT5V} OVP	X	X	H	INA	INA	INA	INA	L	L	L	$V_{VOUT5V} > V_{OVPR\_5V}$
V_{VOUT1V} UVD	H	H	H	A	A	A	A	L	Hi-Z	Hi-Z	$V_{VOUT1V} < V_{UVDF\_PG5V}$
V_{VOUT3V} UVD	H	H	H	A	A	A	A	Hi-Z	L	Hi-Z	$V_{VOUT3V} < V_{UVDF\_PG3V}$
V_{VOUT5V} UVD	H	H	H	A	A	A	A	Hi-Z	Hi-Z	L	$V_{VOUT5V} < V_{UVDF\_PG5V}$
TSD	X	X	H	INA	INA	INA	INA	L	L	L	$Tj > T_{TSD}$

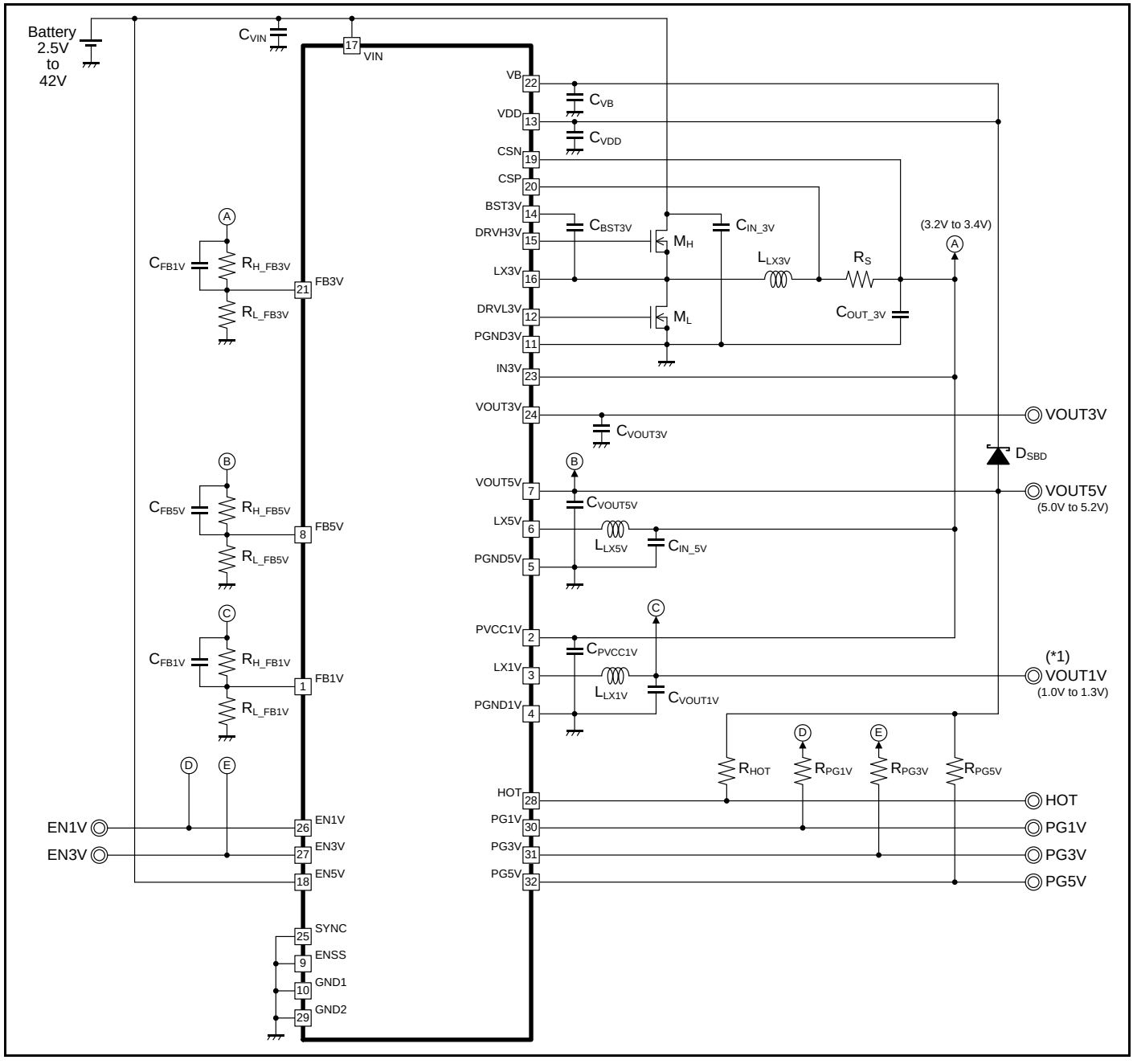
*1: The H means that each enable pin voltage is $V_{EN1V} > V_{ON\_EN1V}$, $V_{EN3V} > V_{ON\_EN3V}$, $V_{EN5V} > V_{ON\_EN5V}$.
The L means that each enable pin voltage is $V_{EN1V} < V_{OFF\_EN1V}$, $V_{EN3V} < V_{OFF\_EN3V}$, $V_{EN5V} < V_{OFF\_EN5V}$.
The X means that each enable pin voltage is the high level or the low level.

*2: The A means the active state. The INA means the inactive state.

*3: Each of the PG pins is formed as an open drain structure. In outputting the Hi-Z, the internal MOSFET is in the OFF state.

9. Application Circuit Example and Parts List

Figure 9-1 Application Circuit Example



*1: The VOUT1V is a pin name only for this circuit.

Table 9-1 Parts List

Block	Symbol	Item	Value	Part Number	Vendor	Size [mm]	Remarks
Common	C_{VIN}	Capacitor	0.1 µF	CGA3E2X7R1H104K080AA	TDK	1.6 × 0.8 × 0.8	X7R, Rated voltage: 50 V_{DC}
	C_{VB}	Capacitor	4.7 µF	CGA4J3X7R1C475K125AB	TDK	2.0 × 1.2 × 1.25	X7R, Rated voltage: 16 V_{DC}
	C_{VDD}	Capacitor	0.1 µF	CGA3E2X7R1E104K080AA	TDK	1.6 × 0.8 × 0.8	X7R, Rated voltage: 25 V_{DC}
	D_{SBD}	SBD	V_F: 0.5V	RB521S30T1G	ON	1.6 × 0.8 × 0.6	V_R: 30 V_{DC}, I_F: 200 mA, I_{FSM}: 1.0A
DD1V	R_{H_FB1V}	Resistor	270 kΩ (*1)	RK73H1JTTD2703F	KOA	1.6 × 0.8 × 0.45	Rated power: 0.1W
	R_{L_FB1V}	Resistor	270 kΩ (*1)	RK73H1JTTD2703F	KOA	1.6 × 0.8 × 0.45	Rated power: 0.1W
	C_{FB1V}	Capacitor	12 pF	CGA3E2C0G1H120J080AA	TDK	1.6 × 0.8 × 0.8	C0G, Rated voltage: 50 V_{DC}
	L_{LX1V}	Inductor	1.5 µH	CLF6045NI-1R5N-D	TDK	7.4 × 7.0 × 4.8	DCR: 13 mΩ, I_{DC_MAX}: 4.5A
	C_{PVCC1V}	Capacitor	4.7 µF	CGA4J3X7R1C475K125AB	TDK	2.0 × 1.2 × 1.25	X7R, Rated voltage: 16 V_{DC}
	C_{VOUT1V}	Capacitor	22 µF × 2	CGA6P1X7R1C226M250AC	TDK	3.2 × 2.5 × 2.5	X7R, Rated voltage: 16 V_{DC}
DD3V	R_{H_FB3V}	Resistor	200 kΩ (*2)	RK73H1JTTD2003F	KOA	1.6 × 0.8 × 0.45	Rated power: 0.1W
		Resistor	120 kΩ (*2)	RK73H1JTTD1203F	KOA	1.6 × 0.8 × 0.45	Rated power: 0.1W
	R_{L_FB3V}	Resistor	120 kΩ (*2)	RK73H1JTTD1203F	KOA	1.6 × 0.8 × 0.45	Rated power: 0.1W
	C_{FB3V}	Capacitor	–	–	–	–	Unnecessary for this circuit
	L_{LX3V}	Inductor	4.7 µH	CLF12577NIT-4R7N-D	TDK	12.8 × 12.5 × 8	DCR: 8.7 mΩ, I_{DC_MAX}: 9.6A
	C_{IN_3V}	Capacitor	10 µF	CGA9N3X7R1H106K230KB	TDK	5.7 × 5.0 × 2.3	X7R, Rated voltage: 50 V_{DC}
	C_{OUT_3V}	Capacitor	47 µF × 10	CGA9N3X7R1C476M230KB	TDK	5.7 × 5.0 × 2.4	X7R, Rated voltage: 16 V_{DC}
	M_H	N-ch MOSFET	R_{ON_MAX}: 32 mΩ	NVTFS5826NL	ON	3.3 × 3.3 × 0.75	V_{DS}: 60V, I_D: 10A
	M_L	N-ch MOSFET	R_{ON_MAX}: 32 mΩ	NVTFS5826NL	ON	3.3 × 3.3 × 0.75	V_{DS}: 60V, I_D: 10A
	C_{BST3V}	Capacitor	0.1 µF	CGA3E2X7R1H104K080AA	TDK	1.6 × 0.8 × 0.8	X7R, Rated voltage: 50 V_{DC}
	R_S	Resistor	10 mΩ	KRL2012-M-R010-F-T1	KOA	2.0 × 1.25 × 0.5	Rated power: 1W
SW3V	C_{VOUT3V}	Capacitor	22 µF	CGA6P1X7R1C226M250AC	TDK	3.2 × 1.6 × 1.6	X7R, Rated voltage: 16 V_{DC}
DD5V	R_{H_FB5V}	Resistor	2 MΩ (*3)	RK73H1JTTD2004F	KOA	1.6 × 0.8 × 0.45	Rated power: 0.1W
		Resistor	1.8 MΩ (*3)	RK73H1JTTD1804F	KOA	1.6 × 0.8 × 0.45	Rated power: 0.1W
	R_{L_FB5V}	Resistor	1.2 MΩ (*3)	RK73H1JTTD1204F	KOA	1.6 × 0.8 × 0.45	Rated power: 0.1W
	C_{FB5V}	Capacitor	3 pF	CGA3E2C0G1H030C080AA	TDK	1.6 × 0.8 × 0.8	C0G, Rated voltage: 50 V_{DC}
	L_{LX5V}	Inductor	1.5 µH	CLF6045NI-1R5N-D	TDK	7.4 × 7.0 × 4.8	DCR: 13 mΩ, I_{DC_MAX}: 4.5A
	C_{IN_5V}	Capacitor	4.7 µF	CGA4J3X7R1C475K125AB	TDK	2.0 × 1.2 × 1.25	X7R, Rated voltage: 16 V_{DC}
	C_{VOUT5V}	Capacitor	47 µF × 5	CGA9N3X7R1C476M230KB	TDK	5.7 × 5.0 × 2.4	X7R, Rated voltage: 16 V_{DC}
HOT/ PG pins	R_{HOT}	Resistor	100 kΩ	RK73H1JTTD1003F	KOA	1.6 × 0.8 × 0.45	Rated power: 0.1W
	R_{PG1V}	Resistor	100 kΩ	RK73H1JTTD1003F	KOA	1.6 × 0.8 × 0.45	Rated power: 0.1W
	R_{PG3V}	Resistor	100 kΩ	RK73H1JTTD1003F	KOA	1.6 × 0.8 × 0.45	Rated power: 0.1W
	R_{PG5V}	Resistor	100 kΩ	RK73H1JTTD1003F	KOA	1.6 × 0.8 × 0.45	Rated power: 0.1W

Capacitor: Ceramic capacitor, SBD: Schottky barrier diode
*1: V_{VOUT1V} setting ≈ 1.2V
*2: V_{IN3V} setting ≈ 3.3V
*3: V_{VOUT5V} setting ≈ 5.0V

TDK: TDK Corporation
KOA: KOA Corporation
ON: ON Semiconductor Corporation

Note:

- *The values of capacitors and resistors are subjects to consider according to a subsequent system. The values shown in the table are very dependable system whose current consumption varies dynamically from 0A to the full-load condition (maximum output current) in 10 µs.*

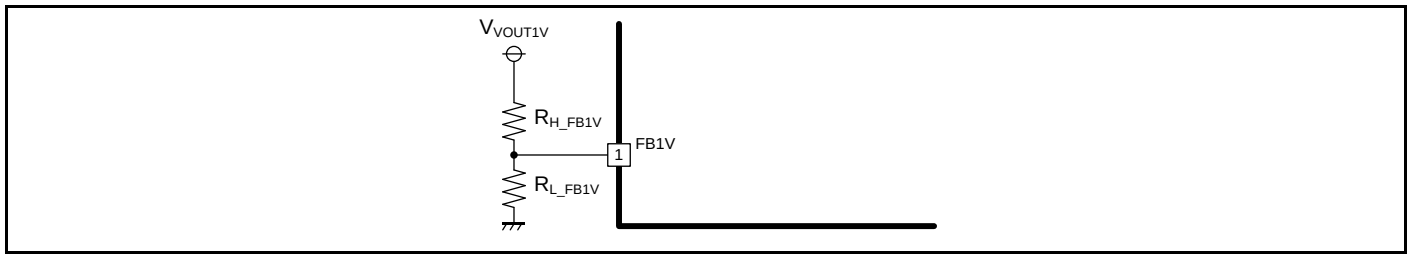
10. Application Note

10.1 Setting the Operation Conditions

DD1V Output Voltage

The DD1V output voltage (V_{VOUT1V}) of this IC can be adjusted by changing the external resistors connecting the FB1V pin.

Figure 10-1 DD1V Output Voltage Setting



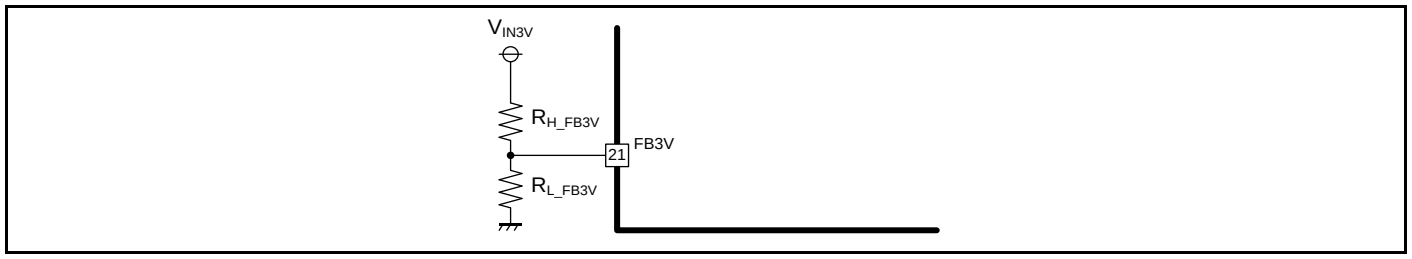
The DD1V output voltage (V_{VOUT1V}) can be calculated using the formula below.

$$V_{VOUT1V}\ [V] = \frac{R_{H\_FB1V} + R_{L\_FB1V}}{R_{L\_FB1V}} \times V_{FB1V}$$

DD3V Output Voltage

The DD3V output voltage (V_{IN3V}) of this IC can be adjusted by changing the external resistors connecting the FB3V pin.

Figure 10-2 DD3V Output Voltage Setting



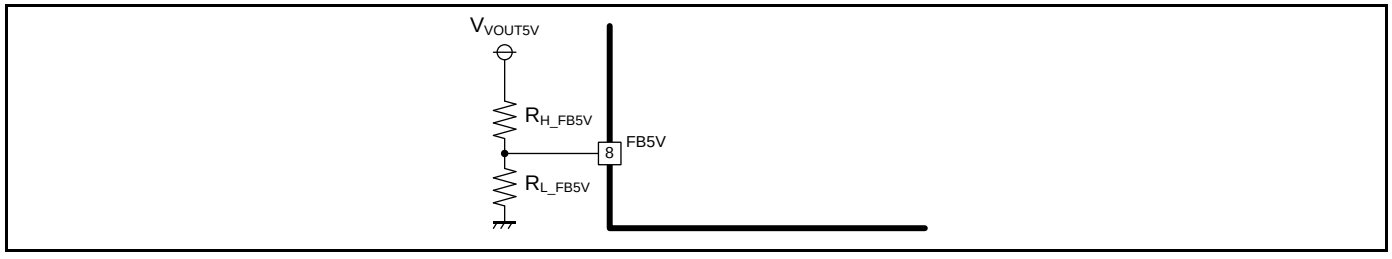
The DD3V output voltage (V_{IN3V}) can be calculated using the formula below.

$$V_{IN3V}\ [V] = \frac{R_{H\_FB3V} + R_{L\_FB3V}}{R_{L\_FB3V}} \times V_{FB3V}$$

DD5V Output Voltage

The DD5V output voltage (V_{VOUT5V}) of this IC can be adjusted by changing the external resistors connecting the FB5V pin.

Figure 10-3 DD5V Output Voltage Setting



The DD5V output voltage (V_{VOUT5V}) can be calculated using the formula below.

$$V_{VOUT5V}\ [V] = \frac{R_{H\_FB5V} + R_{L\_FB5V}}{R_{L\_FB5V}} \times V_{FB5V}$$

11. Usage Precaution

Printed circuit board ground lines should be set up with consideration for common impedance.

Take appropriate measures against static electricity.

- Containers for semiconductor materials should have anti−static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ in serial body and ground.

Do not apply negative voltages.

The use of negative voltages below −0.3 V may make the parasitic transistor activated to the LSI, and can cause malfunctions.

12. RoHS Compliance Information

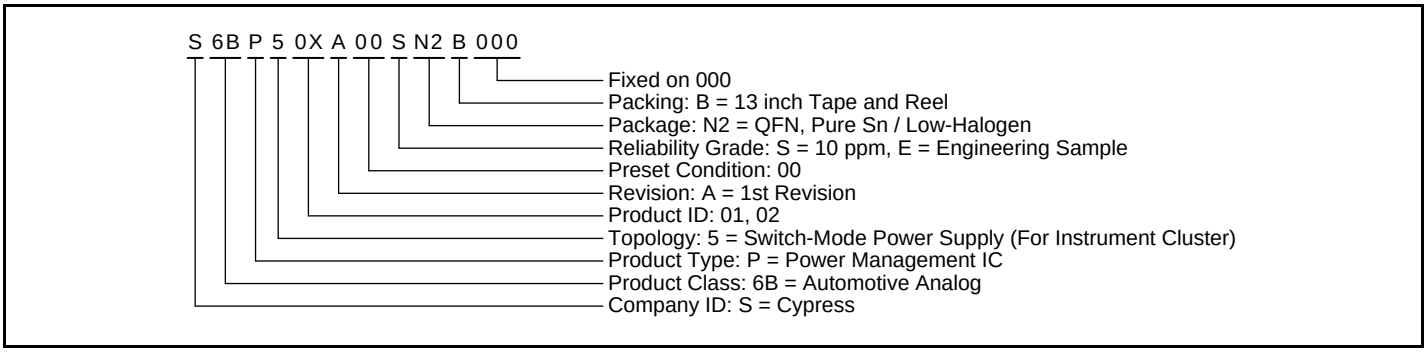
This product has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE).

13. Ordering Information

Part Number (MPN)	Package
S6BP501A00SN2B000 (*1)	Plastic, Wettable QFN (0.50 mm pitch), 32-pin (VNG032)
S6BP501A00EN2B000 (*2)	
S6BP502A00SN2B000 (*1)	
S6BP502A00EN2B000 (*2)	

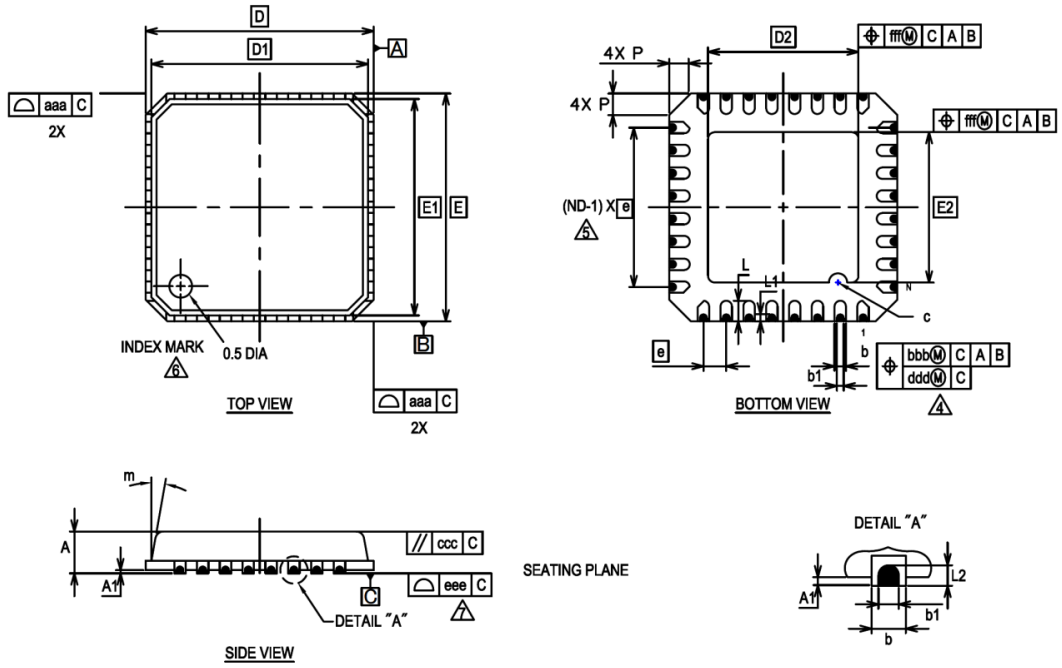
MPN: Marketing Part Number
*1: Commercial sample (CS)
*2: Engineering sample (ES)

Figure 13-1 Ordering Part Number Definitions



14. Package Dimensions

VNG032 : VERY THIN PLASTIC QUAD FLAT NO LEAD PACKAGES



SYMBOL	MILLIMETER			NOTE
	MIN.	NOM.	MAX.	
A	—	—	0.9	PROFILE
A1	0.00	—	0.05	
D		5.00 BSC.		
E		5.00 BSC.		
D1		4.75 BSC.		
E1		4.75 BSC.		
b	0.18	0.25	0.30	TERMINAL WIDTH
b1	0.10	0.15	0.20	DIMPLE WIDTH
D_2		3.30 BSC.		EXPOSED PAD SIZE
E_2		3.30 BSC.		EXPOSED PAD SIZE
e		0.50 BSC.		TERMINAL PITCH
L	0.35	0.45	0.55	TERMINAL LENGTH
L1	0.05	0.15	0.25	DIMPLE LENGTH
L2		0.09 REF.		DIMPLE HEIGHT
c		R0.20		PIN #1 ID
m	0	—	12°	
P	—	—	0.60	

N	32	TERMINAL COUNT
aaa	0.10	
bbb	0.10	
ccc	0.10	
ddd	0.05	
eee	0.08	
fff	0.10	

1. DIMENSIONING AND TOLERANCINC CONFORMS TO ASME Y14.5-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL. THE DIMENSION "b"SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
6. PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
7. UNILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Rev. A

Document History

Document Title: S6BP501A, S6BP502A 3ch DC/DC Converter IC for Automotive Cluster
Document Number: 002-03396

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4921966	HIXT	09/16/2015	New Spec.
*A	4998578	HIXT	11/02/2015	Added Errata.
*B	5107300	HIXT	01/26/2016	Updated the description for the pin name, IN3V in the Table 3-1. Updated the following Electrical Characteristics. I_{LEAK_1V}: Condition I_{LXPEAK_1V}: Min values t_{SS_3V}: Typ value R_{ONH_3V}: Typ value R_{ON_BSTSW}: Typ and Max values I_{R_BSTSW}: Condition and Max value I_{LOAD_SW3V}: Min values I_{LEAK_SW3V}: Condition t_{SS_SW3V}: Typ value I_{PWMPFM_5V}: Typ value I_{LEAK_5V}: Condition I_{LX_PEAK5V}: Typ value V_{OVDF_PG1V}: Typ value SSCG block (Modulation range): Typ value Updated the description and the Table 8-2 of the SYNC in the Section 8.2. Added the remarks for the DD5V output in the Table 8-3. Updated the following parts in the Table 9-1.. C_{VDD}: value, part number and remarks R_{H_FB3V}: value and part number R_{L_FB3V}: value and part number R_S: value Added “Development Support” Updated Errata.
*C	5198555	HIXT	05/16/2016	Added “AEC-Q100 compliant (Grade-2)” in Features. Updated Architecture Block Diagram. Deleted Errata item1, item2, item4, and item5 from Errata. Errata item3 in Errata is under confirmation with Rev.2 silicon.
*D	5325274	HIXT	09/09/2016	Added Block Diagram Added More Information Updated the values in Electrical Characteristics DD3V block: Boost switch R_{ONH_3V}: Condition (DRVH3V pin current = 50 mA → 10 mA), Typ value (8.5Ω → 15Ω) R_{ON_BSTSW}: Typ value (3Ω → 8Ω), Max value (10Ω → 24Ω) I_{R_BSTSW}: Max value (3 µA → 2 µA) Deleted “Development Support” Added Figure 13-1 Ordering Part Number Definitions Deleted Errata

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