EZ-PD™ CCG3PA Datasheet

USB Type-C Port Controller

General Description

EZ-PD™ CCG3PA is Cypress' highly integrated USB Type-C port controller that complies with the latest USB Type-C and PD standards and is targeted for PC power adapters, mobile chargers, car chargers, and power bank applications. In such applications, CCG3PA provides additional functionalities and BOM integration advantages. CCG3PA uses Cypress' proprietary M0S8 technology with a 32-bit Arm® Cortex®-M0 processor, 64-KB flash, a complete Type-C USB-PD transceiver, all termination resistors required for a Type-C port, an integrated feedback control circuitry for voltage (VBUS) regulation and system-level ESD protection. It is available in 24-pin QFN and 16-pin SOIC packages.

Features

Type-C Support and USB-PD Support

- Supports USB PD3.0 Version 1.1 Spec including Programmable Power Supply Mode
- Configurable resistors R_P and R_D
- Supports one USB Type-C port and one Type-A port

2x Legacy/Proprietary Charging Blocks

- Supports QC 4.0, Apple charging 2.4A, AFC, BC 1.2
- Integrates all required terminations on DP/DM lines

Integrated Voltage (VBUS) Regulation and Current Sense Amplifier

- Analog regulation of secondary side feedback node (direct feedback or opto coupler)
- Integrated shunt regulator function for VBUS control
- Constant current or constant voltage mode
- Supports low-side current sensing for constant current control

System-Level Fault Protection

- VBUS to CC Short Protection
- On-chip OVP, OCP, UVP, and SCP
- Supports OTP through integrated ADC circuit

32-bit MCU Subsystem

- Arm Cortex-M0 CPU
- 64-KB Flash
- 8-KB SRAM

Clocks and Oscillators

- Integrated oscillator eliminating the need for external clock

Power

- 3.0-V to 24.5-V operation (30-V tolerant)

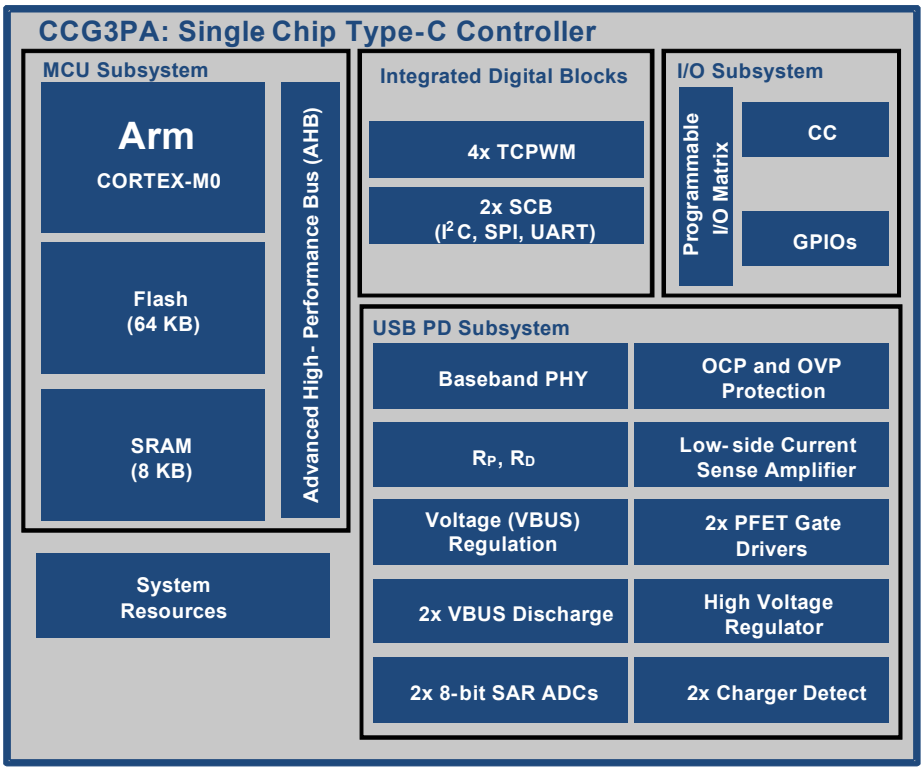
System-Level ESD Protection

- On CC, VBUS_C_MON_DISCHARGE, DP0, DM0, P2.2, and P2.3 pins
- ±8-kV Contact Discharge and ±15-kV Air Gap Discharge based on IEC61000-4-2 level 4C

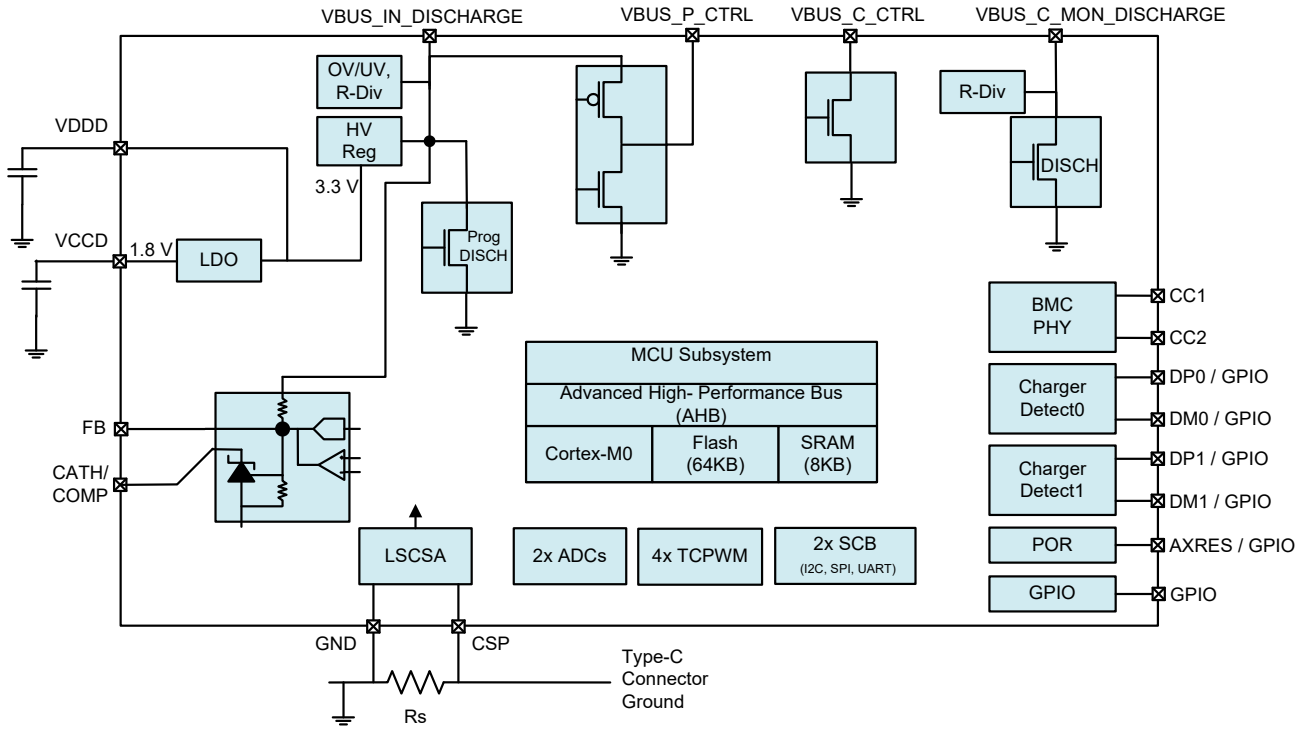
Packages

- 24-pin QFN and 16-pin SOIC
- Supports extended industrial temperature range (–40 °C to +105 °C)

Logic Block Diagram



Internal Block Diagram



Contents

Functional Overview

MCU Subsystem

CPU

The Cortex-M0 CPU in EZ-PD CCG3PA is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating.

The CPU also includes a serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for EZ-PD CCG3PA has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The EZ-PD CCG3PA device has a flash module with one bank of 64-KB flash, a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

USB-PD Subsystem (SS)

The USB-PD subsystem provides the interface to the Type-C USB port. This subsystem comprises a current sense amplifier, a high-voltage regulator, OVP, OCP, and supply switch blocks. This subsystem also includes all ESD required and supported on the Type-C port.

USB-PD Physical Layer

The USB-PD Physical Layer consists of a transmitter and receiver that communicate BMC-encoded data over the CC channel based on the PD 3.0 standard. All communication is half-duplex. The Physical Layer or PHY practices collision avoidance to minimize communication errors on the channel.

The USB-PD block includes all termination resistors (R_P and R_D) and their switches as required by the USB-PD spec. R_P and R_D resistors are required to implement connection detection, plug orientation detection, and for establishing USB DFP/UFP roles. The R_P resistor is implemented as a current source.

According to the USB Type-C spec, a Type-C controller such as CCG3PA must present certain termination resistors depending on its role in its unpowered state. The Sink role in a power bank application requires R_D resistors to be present on the CC pins whereas the DFP role, as in a power adapter, requires both CC lines to be open. To be flexible for such applications, CCG3PA includes the resistors required in the unpowered state on separate pads or pins. The dead battery R_D resistors are available on separate pads. The dead battery R_D is implemented as a bond option on parts for Power Bank applications. In these parts, each CC pin is bonded out together with its corresponding dead battery R_D resistor. On part numbers for the DFP application, the CC pins are not bonded with the dead battery R_D.

ADC

The ADC is a low-footprint 8-bit SAR ADC that is available for general-purpose A-D conversion applications in the chip. This ADC can be accessed from all GPIOs and the DP/DM pins through an on-chip analog mux. CCG3PA contains two instances of the ADC. The voltage reference for the ADCs is generated either from the VDDD supply or from internal bandgap. When sensing the GPIO pin voltage with an ADC, the pin voltage cannot exceed the VDDIO supply value.

Charger Detection

The two charger detection blocks connected to the two pairs of DP/DM pins allow CCG3PA to detect conventional battery chargers conforming to BC 1.2, and the following proprietary charger specifications: Apple, Qualcomm's QuickCharge 4.0, and Samsung AFC.

VBUS Overcurrent and Overvoltage Protection

The CCG3PA chip has an integrated hardware block for VBUS overvoltage protection (OVP)/overcurrent protection (OCP) with configurable thresholds and response times on the Type C port.

VBUS Short Protection

CCG3PA provides four VBUS short protection pins: CC1, CC2, P2.2, and P2.3. These pins are protected from accidental shorts to high-voltage VBUS. Accidental shorts may occur because the CC1 and CC2 pins are placed next to the VBUS pins in the USB Type-C connector. A Power Delivery controller without the high-voltage VBUS short protection will be damaged in the event of accidental shorts. When the protection circuit is triggered, CCG3PA can handle up to 17 V forever and between 17 V to 22 VDC for 1000 hours on the OVT pins. When a VBUS short event occurs on the CC pins, a temporary high-ringing voltage is observed due to the RLC elements in the USB Type-C cable. Without CCG3PA connected, this ringing voltage can be twice (44 V) the maximum VBUS voltage (21.5 V). However, when CCG3PA is connected, it is capable of clamping temporary high-ringing voltage and protecting the CC pin using IEC ESD protection diodes.

Low-side Current Sense Amplifier (CSA)

The CCG3PA chip also has an integrated low-side current sense amplifier that is capable of detecting current in the order of 100 mA across a 5 mΩ external resistor. It also supports constant current mode of operation in power adapter application as a provider.

PFET Gate Drivers on VBUS Path

CCG3PA has two integrated PFET gate drivers to drive external PFETs on the VBUS provider and consumer path. The VBUS_P_CTRL gate driver has an active pull-up, and thus can drive high, low or High-Z.

The VBUS_C_CTRL gate driver can drive only low or high-Z, thus requiring an external pull-up. These pins are VBUS voltage-tolerant.

VBUS Discharge FETs

CCG3PA also has two integrated VBUS discharge FETs used to discharge VBUS to meet the USB-PD specification timing on a detach condition. VBUS Discharge FET on the provider side can be used to accelerate the ramp down of VBUS to default 5V on the secondary side.

Voltage (VBUS) Regulation

CCG3PA contains an integrated feedback control circuitry (for AC/DC applications) for secondary side control with analog regulation of the feedback/cathode pins to achieve the appropriate voltage on VBUS pin as per the negotiated contract with the peer device over Type-C.

Integrated Digital Blocks

Serial Communication Blocks (SCB)

EZ-PD CCG3PA has two SCBs, which can be configured to implement an I^2C, SPI, or UART interface. The hardware I^2C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as master or slave.

In the I^2C mode, the SCB blocks are capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I^2C that creates a mailbox address range in the memory of EZ-PD CCG3PA and effectively reduce I^2C communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripherals are compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/Os are implemented with GPIO in open-drain modes.

The I^2C port on the SCB blocks of EZ-PD CCG3PA are not completely compliant with the I^2C spec in the following aspects:

- The GPIO cells for SCB 1's I^2C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

Timer/Counter/PWM Block (TCPWM)

EZ-PD CCG3PA has four TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals.

I/O Subsystem

EZ-PD CCG3PA has up to 12 GPIOs of which, some of them can be re-purposed to support functions of SCB (I^2C, UART, SPI). GPIO pins P0.0 and P0.1 are overvoltage-tolerant (OVT) (upto 7V).

The GPIO block implements the following:

- Seven drive strength modes:
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Port pins P1.0 and P1.1 can be configured to indicate Fault for OCP/SCP/OVP/UVP conditions. Any two fault conditions can be mapped to two GPIOs or all the four faults can be OR'ed to indicate over one GPIO.

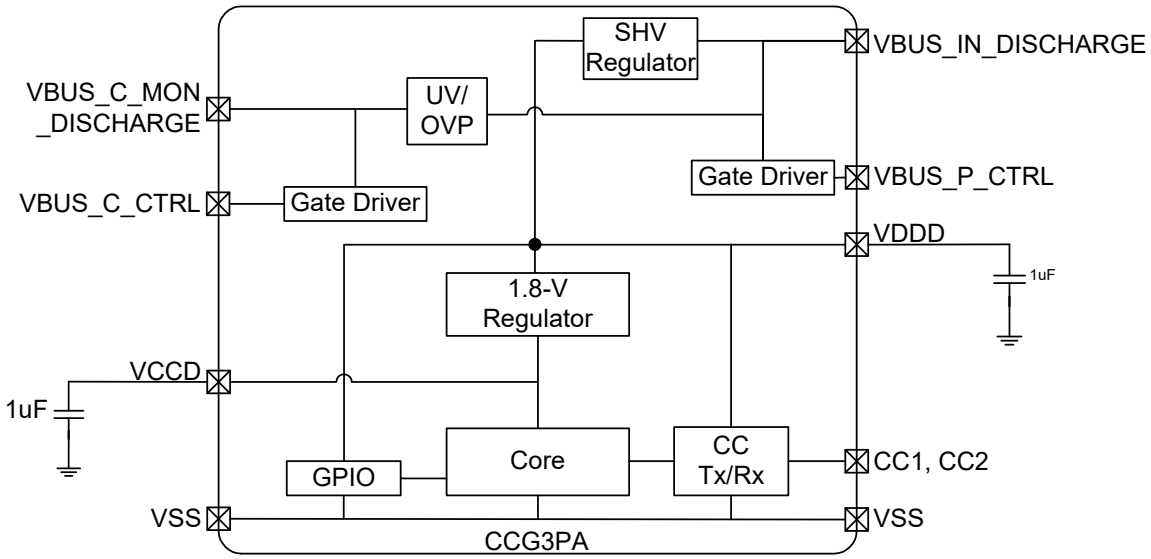
Power Systems Overview

CCG3PA can operate from two possible external supply sources: VBUS_IN_DISCHARGE (3.0 V–24.5 V) or VDDD (2.7 V–5.5 V). When powered through VBUS_IN_DISCHARGE, the internal regulator generates VDDD of 3.3 V for chip operation. The regulated supply, VDDD, is either used directly inside some analog blocks or further regulated down to VCCD (1.8 V), which powers majority of the core using the regulators. CCG3PA has three different power modes: Active, Sleep, and Deep Sleep. Transitions between these power modes are managed by the power system. When powered through the VBUS_IN_DISCHARGE pin, VDDD cannot be used to power external devices and should be connected to a 1-µF capacitor for the regulator stability only. These pins are not supported as power supplies. Refer to the application diagrams for capacitor connections.

Table 1. CCG3PA Power Modes

Mode	Description
Power-On Reset (POR)	Power is valid and an internal reset source is asserted or SleepController is sequencing the system out of reset.
ACTIVE	Power is valid and CPU is executing instructions.
SLEEP	Power is valid and CPU is not executing instructions. All logic that is not operating is clock gated to save power.
DEEP SLEEP	Main regulator and most blocks are shut off. DeepSleep regulator powers logic, but only low-frequency clock is available.

Figure 1. Power System Requirement Block Diagram



Pinouts

Table 2. CCG3PA Pin Descriptions

24-Pin QFN	16-Pin SOIC	Pin Name	Description
1	–	P1.0	Port 1 pin 0: GPIO/UART_1_CTS/I2C_SDA_1[1] / TCPWM_line_0[2], Programmable SCP/OCP/OVP/UVP Fault indication
2	–	P1.1	Port 1 pin 1: GPIO/UART_1_RTS/I2C_SCL_1[1] / TCPWM_line_1[3], Programmable SCP/OCP/OVP/UVP Fault indication
3	5	VBUS_P_CTRL	Provider (PMOS) FET control (30-V Tolerant) 0: Path ON 1: Path OFF
4	–	VBUS_C_CTRL	VBUS Consumer (PMOS) FET Control (30-V Tolerant) 0: Path ON Z: Path OFF
5	–	DP1/P1.2	USB D+/Port 1 pin 2: GPIO/UART_1_TX1/AFC/QC/BC 1.2/Apple Charging/No IEC
6	–	DM1/P1.3	USB D-/Port 1 pin 3: GPIO/UART_1_RX1/AFC/QC/BC 1.2/Apple Charging/No IEC
7	6	SWD_DAT_0/P0.0	Port 0 pin 0: GPIO/OVT/I2C_SDA_0/TCPWM_line_0/UART_0_CTS
8	7	SWD_CLK_0/P0.1	Port 0 pin 1: GPIO/OVT/I2C_SCL_0/TCPWM_line_1/UART_0_RTS
9	8	AXRES/P2.0	Port 2 pin 0: GPIO/Alternate XRES[4]/TCPWM_line_0//UART_0_TX0
10	–	P2.1	Port 2 pin 1: GPIO/TCPWM_line_1//UART_0_RX0
11	9	VBUS_C_MON_DIS-CHARGE	Type C VBUS Monitor with Internal Discharge FET
12	–	P2.2	Port 2 pin 2: GPIO with Open drain with pull-up assist. Configurable as GPIO_20VT/I2C_SDA_1/IEC. Tolerant to temporary short to VBUS pin..
13	–	P2.3	Port 2 pin 3: GPIO with Open drain with pull-up assist. Configurable as GPIO_20VT/I2C_SCL_1/IEC. Tolerant to temporary short to VBUS pin.
14	10	CC2	Communication Channel 2 with Dead-battery Rd Bonding Option/IEC. Tolerant to temporary short to VBUS pin.
15	11	CC1	Communication Channel 1 with Dead-battery Rd Bonding Option/IEC. Tolerant to temporary short to VBUS pin.
16	12	DM0/P3.1	USB D-/Port 3 pin 1: GPIO/UART_1_RX0/AFC/QC/BC 1.2/Apple Charging/IEC
17	13	DP0/P3.0	USB D+/Port 3 pin 0: GPIO/UART_1_TX0/AFC/QC/BC 1.2/Apple Charging/IEC
18	14	VBUS_IN_DIS CHARGE	VBUS Power IN (3.0 V–24.5 V) with Internal Discharge FET
19	16	CSP	CS +: Current sense input
20	1	FB	Voltage regulation feedback pin
21	2	CATH/COMP	Cathode of voltage regulation and compensation for other applications
22	15	GND	Ground
23	3	VDDD	Power Input: 2.7 V–5.5 V
24	4	VCCD	1.8-V Core Voltage pin (not intended for use as a power source)
–	–	EPAD	Ground

Note
1. Out of the two SCB blocks (SCB0 and SCB1), while the SCB0's I2C functionality is mapped out to the P0.0/P0.1 GPIO pins, the I2C functionality of SCB1 provides flexibility to have it mapped either on P1.0/P1.1 OR P2.2/P2.3 GPIO pins.
2. TCPWM_line_0 can be mapped to port pins P1.0, P0.0, P2.0 or P2.2.
3. TCPWM_line_1 can be mapped to port pins P1.1, P0.1, P2.1 or P2.3.
4. AXRES pin will be internally pulled up during the Power On I/O initialization time (see Table 6 for more details).
5. See Table 9 and Table 10 for specifications related to these pins.

Table 3. GPIO Ports, Pins and Their Functionality

Port	24-QFN	16-SOIC	SCB Function			TCPWM	Fault Indicator	Protection Capability		USB Charging Signal				IEC4
Pin	Pin#	Pin#	UART	SPI	I2C			VBUS Short	OVT	AFC	QC	BC1.2	Apple	
P0.0	7	6	UART_0_CTS	SPI_1_MOSI	I2C_0_SDA	TCPWM_line_0:0	–	–	Yes	–	–	–	–	–
P0.1	8	7	UART_0_RTS	SPI_1_MISO	I2C_0_SCL	TCPWM_line_1:0	–	–	Yes	–	–	–	–	–
P1.0	1		UART_1_CTS	SPI_0_SEL	I2C_1_SDA:1	TCPWM_line_2:1	Yes	–	–	–	–	–	–	–
P1.1	2		UART_1_RTS	SPI_0_MISO	I2C_1_SCL:1	TCPWM_line_3:1	Yes	–	–	–	–	–	–	–
P1.2	5		UART_1_TX1	SPI_0_MOSI	–	–	–	–	–	D+	D+	D+	D+	–
P1.3	6		UART_1_RX1	SPI_0_CLK	–	–	–	–	–	D-	D-	D-	D-	–
P2.0	9	8	UART_0_TX0	SPI_1_SEL	–	TCPWM_line_2:0	–	–	–	–	–	–	–	–
P2.1	10		UART_0_RX0	SPI_1_CLK	–	TCPWM_line_3:0	–	–	–	–	–	–	–	–
P2.2	12		UART_0_TX1	–	I2C_1_SDA:0	TCPWM_line_0:1	–	Yes	–	–	–	–	–	Yes
P2.3	13		UART_0_RX1	–	I2C_1_SCL:0	TCPWM_line_1:1	–	Yes	–	–	–	–	–	Yes
P3.0	17	13	UART_1_TX0	–	–	–	–	–	–	D+	D+	D+	D+	Yes
P3.1	16	12	UART_1_RX0	–	–	–	–	–	–	D-	D-	D-	D-	Yes

Figure 2. Pinout of 24-QFN Package (Top View)

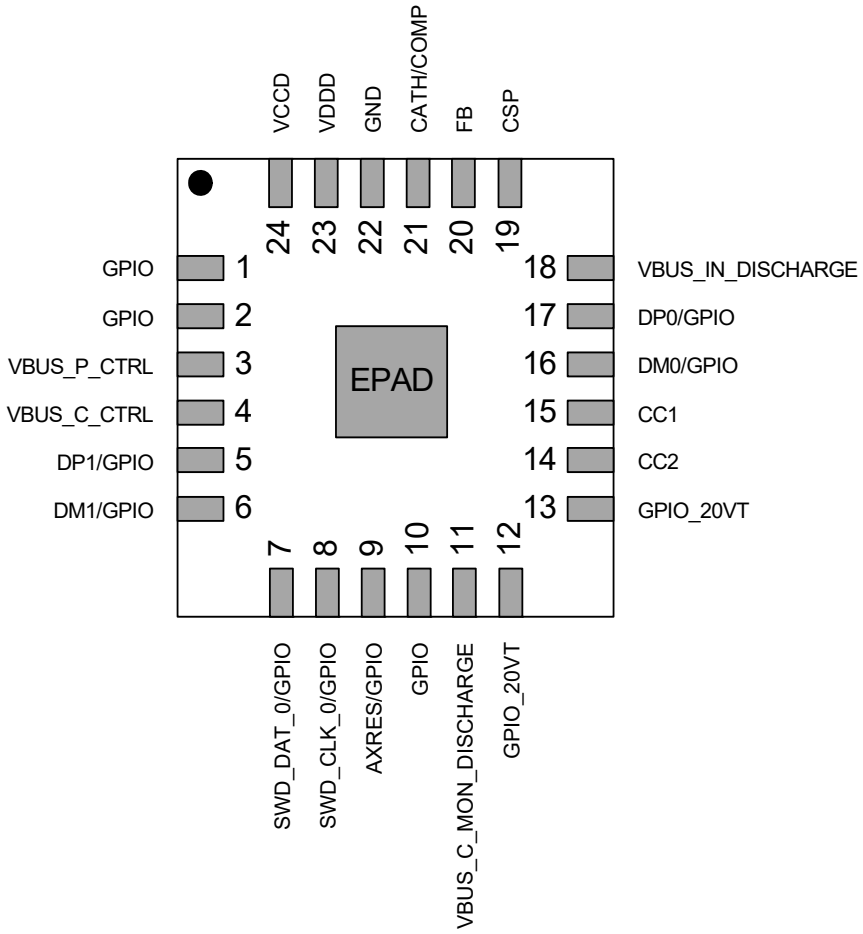
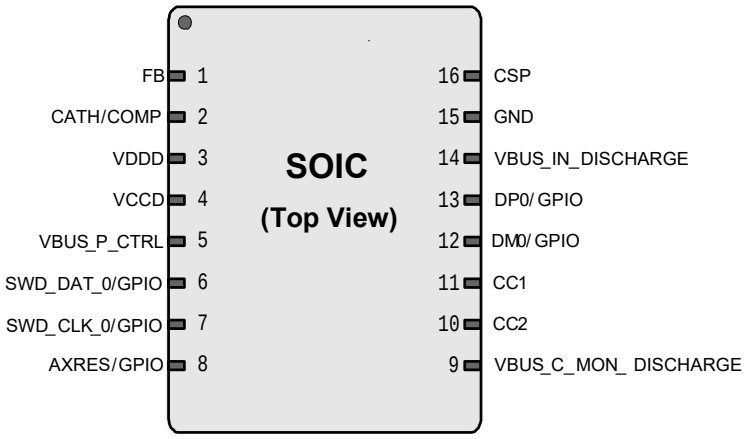


Figure 3. Pinout of 16-SOIC Package (Top View)



CCG3PA Programming and Bootloading

There are two ways to program application firmware into a CCG3PA device:

1. Programming the device flash over SWD Interface

2. Application firmware update over CC interface

Generally, the CCG3PA devices are programmed over SWD interface only during development or during the manufacturing process of the end product. Once the end product is manufactured, the CCG3PA device's application firmware can be updated via the CC bootloader interface.

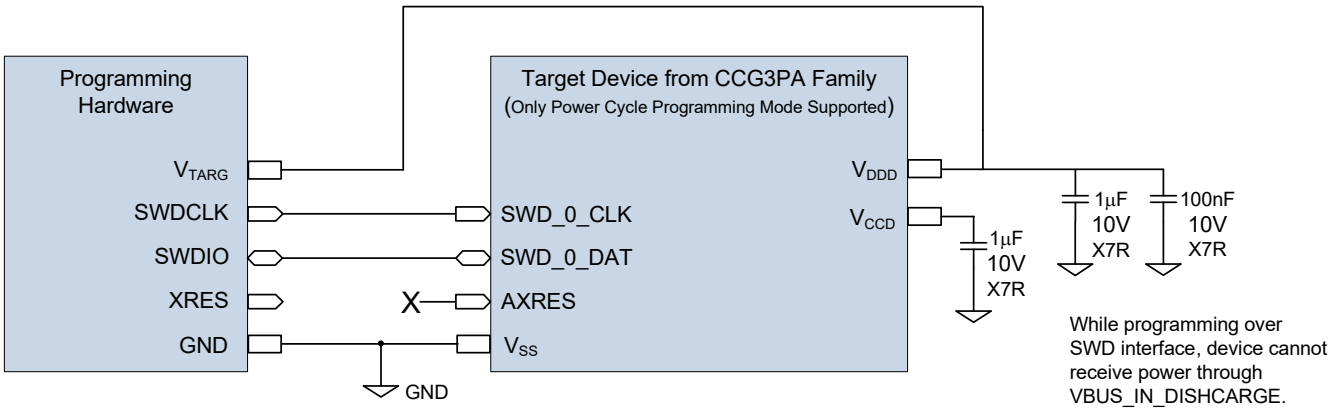
Programming the Device Flash over SWD Interface

CCG3PA family of devices can be programmed using the SWD interface. Cypress provides a programming kit (CY8CKIT-002 MiniProg3 Kit) called MiniProg3 and PSoC Programmer Software which can be used to program the flash as well as debug firmware. The flash is programmed by downloading the information from a hex file. This hex file is a binary file generated as an output of building the firmware project in PSoC Creator Software. Click here for more information on how to use the MiniProg3 programmer. There are many third party programmers that support mass programming in a manufacturing environment.

As shown in the block diagram in Figure 4, the SWD_0_DAT and SWD_0_CLK pins are connected to the host programmer's SWDIO (data) and SWDCLK (clock) pins respectively. During SWD programming, the CCG3PA device has to be powered by the host programmer by connecting its VTARG (power supply to the target device) to VDDD pin of CCG3PA device. While programming over SWD interface, the CCG3PA device cannot receive power through VBUS_IN_DISCHARGE.

The CCG3PA device family does not have the XRES pin. Due to that, the XRES line from the host programmer remains unconnected, and hence programming using Reset Mode is not supported. In other words, CCG3PA devices are supported by Power Cycle programming mode only since XRES line is not used. Contact Cypress for further details on CYPD3XXX Programming Specifications.

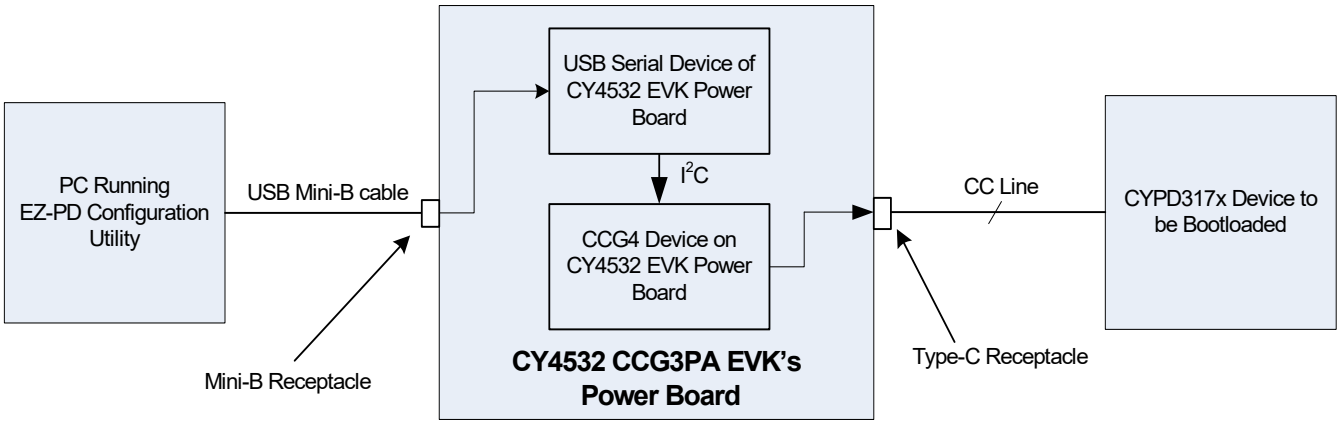
Figure 4. Connecting the Programmer to CYPD317x Device



Application Firmware Update over CC Interface

For bootloading CCG3PA applications, the CY4532 CCG3PA EVK can be used to send programming and configuration data as Cypress specific Vendor Defined Messages (VDMs) over the CC line. The CY4532 CCG3PA EVK's Power Board is connected to the system containing CCG3PA device on one end and a Windows PC running the EZ-PD™ Configuration Utility as shown in Figure 5 on the other end to bootload the CCG3PA device.

Figure 5. Application Firmware Update over CC Interface



Application Firmware (FW) update feature over CC interface is intended for use during development and manufacturing. Cypress strongly recommends customers to use the EZ-PD Configuration Utility to turn off the Application FW Update over CC interface in the firmware that is updated into CCG3PA's flash before mass production. This prevents unauthorized firmware from being updated over CC-interface in the field. Refer to the knowledge base article KBA230192 on how to configure this in EZ-PD Configuration Utility.

If you desire to retain the Application Firmware update over CC interface feature post-production for on-field firmware updates, contact Cypress Sales for further guidelines.

Application Diagrams

Figure 6 and Figure 7 show the application diagrams of CCG3PA-based Power Adapter with Opto-Coupler Feedback control using 16-pin SOIC and 24-pin QFN parts respectively. In an opto-feedback power adapter, CCG3PA implements a shunt regulator and the feedback to the primary controller is through an opto-coupler. The current drawn through the CATH path is proportional to the potential difference between FB pin and the internal bandgap reference voltage. At default 5-V VBUS, the FB pin will be held at the voltage set by the bandgap reference voltage using internal VBUS resistor dividers.

If VBUS needs to be changed from default 5 V, using internal IDACs and an error amplifier, CCG3PA draws a proportional current through the CATH pin. This in turn gets coupled to the primary controller through the opto-coupler.

Figure 6. CCG3PA Based Power Adapter Application Diagram with Opto Coupler Feedback Control (16-pin SOIC Device)

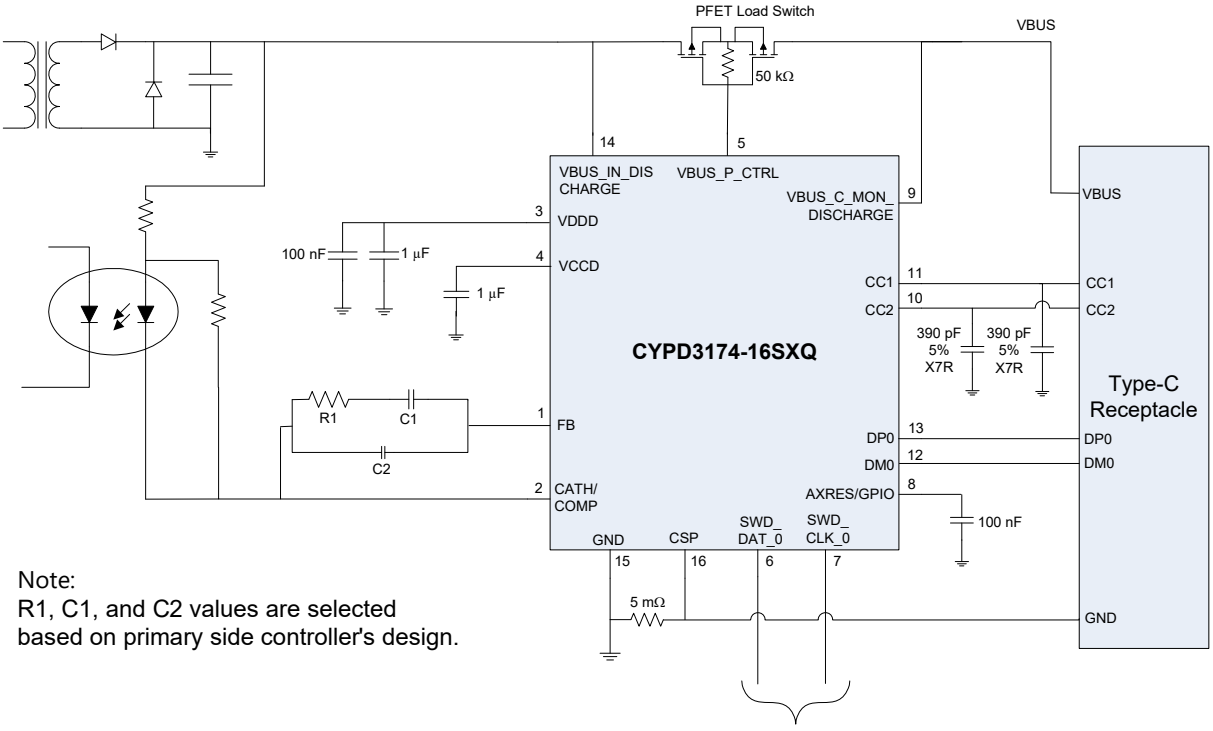
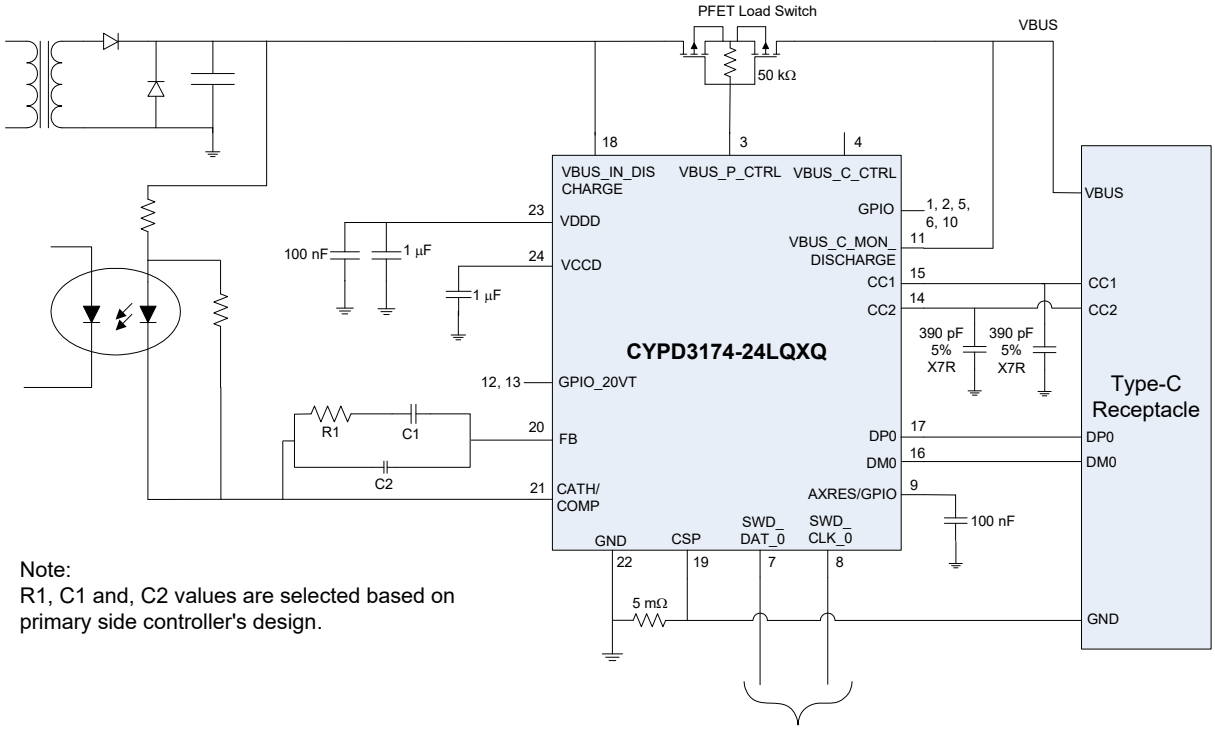


Figure 7. CCG3PA Based Power Adapter Application Diagram with Opto Coupler Feedback Control (24-pin QFN Device)



Note:
R1, C1 and, C2 values are selected based on primary side controller's design.

Figure 8 shows the application diagram of CCG3PA based power adapter with Direct Feedback control. In this application, VBUS is maintained at a constant voltage. The default value of VBUS upon power up (which is usually at 5 V) is set up by choosing the appropriate resistor divider that will set the FB node at a voltage expected by the secondary controller.

Feedback node is regulated using internal IDACs. Whenever a change in VBUS voltage is needed, CCG3PA will either source or sink a proportional current at feedback node, based on the amount of voltage change needed.

Figure 8. CCG3PA Based Power Adapter Application Diagram with Direct Feedback Control

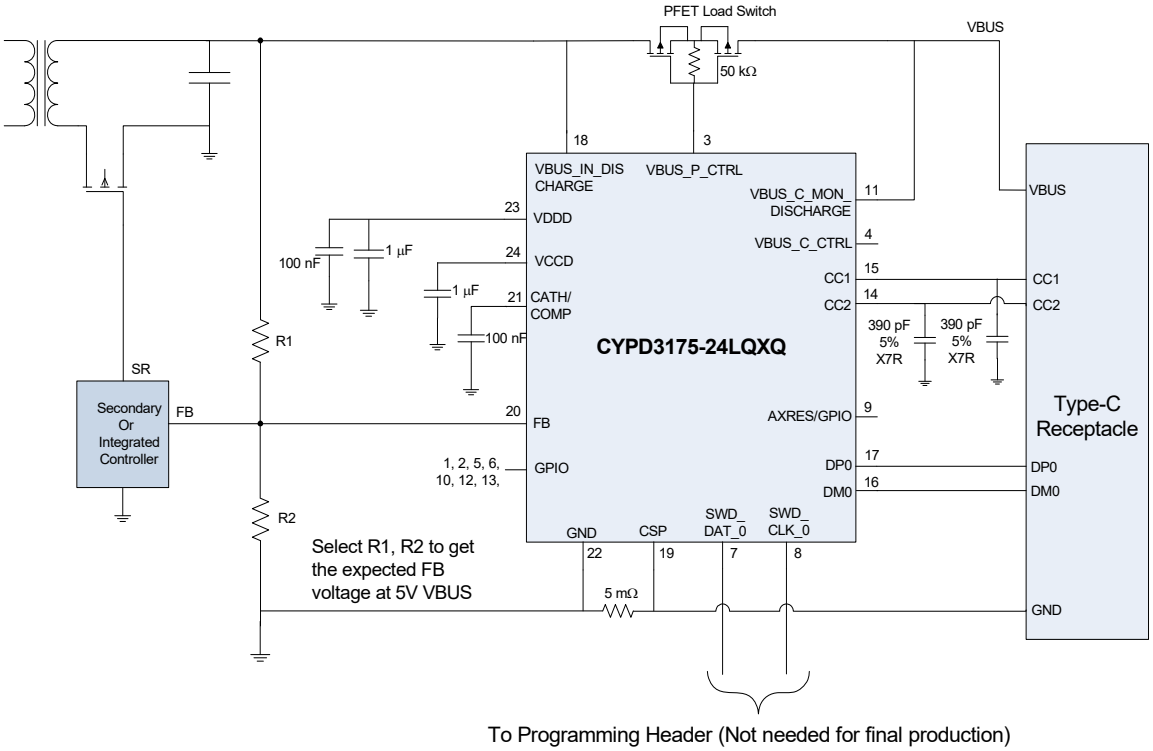


Figure 9 shows the application diagram of a CCG3PA based power adapter application with direct feedback control for two port car charger. The car charger application can charge portable devices connected to the Type-C and Type-A port simultaneously. The Type-C port supports USBPD 3.0 QC 4.0, Apple Charging 2.4A, and AFC. The Type-A port supports QC 3.0, Apple Charging and AFC.

Figure 9. CCG3PA Based Power Adapter Application with Direct Feedback Control for Two Port Car Charger

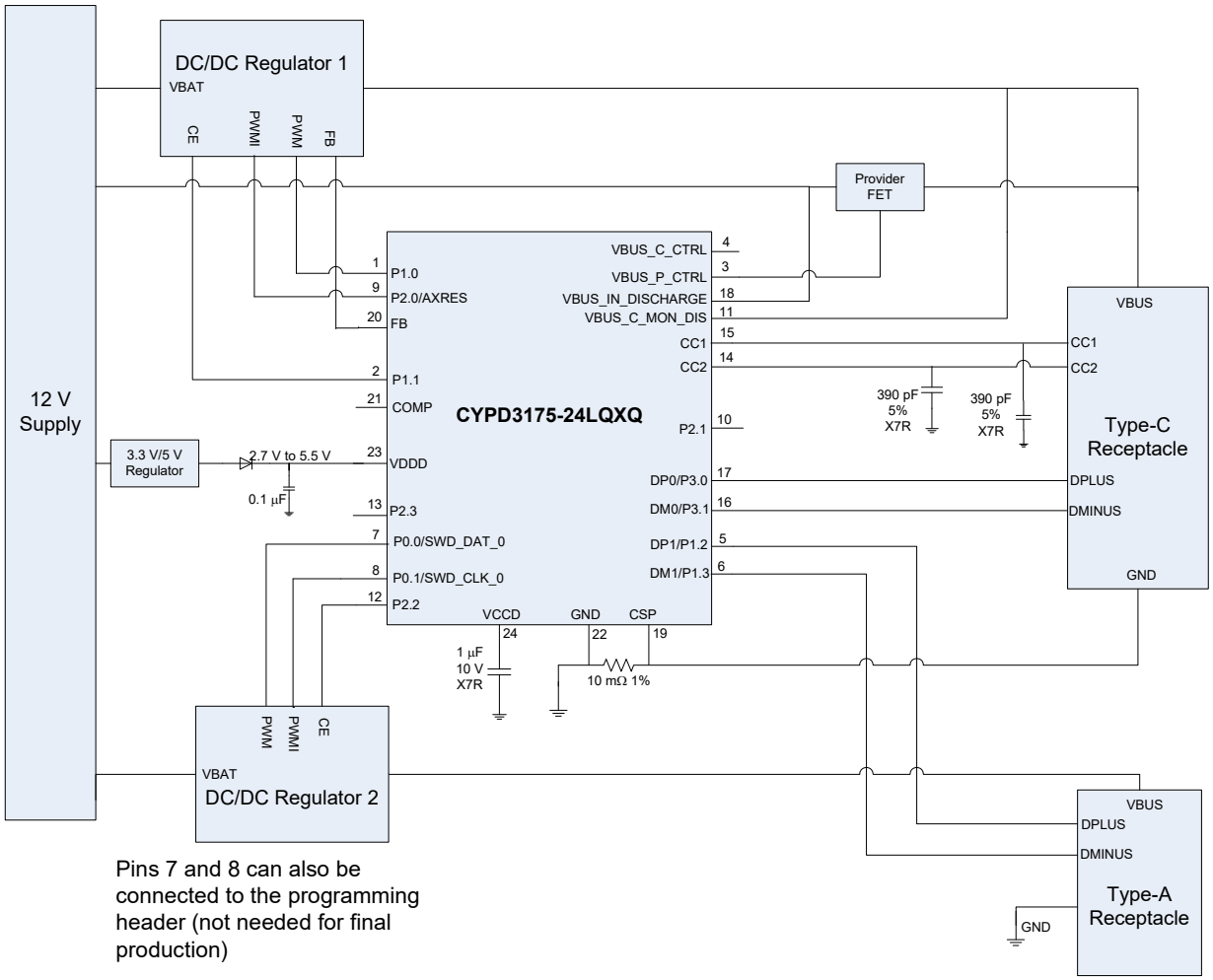
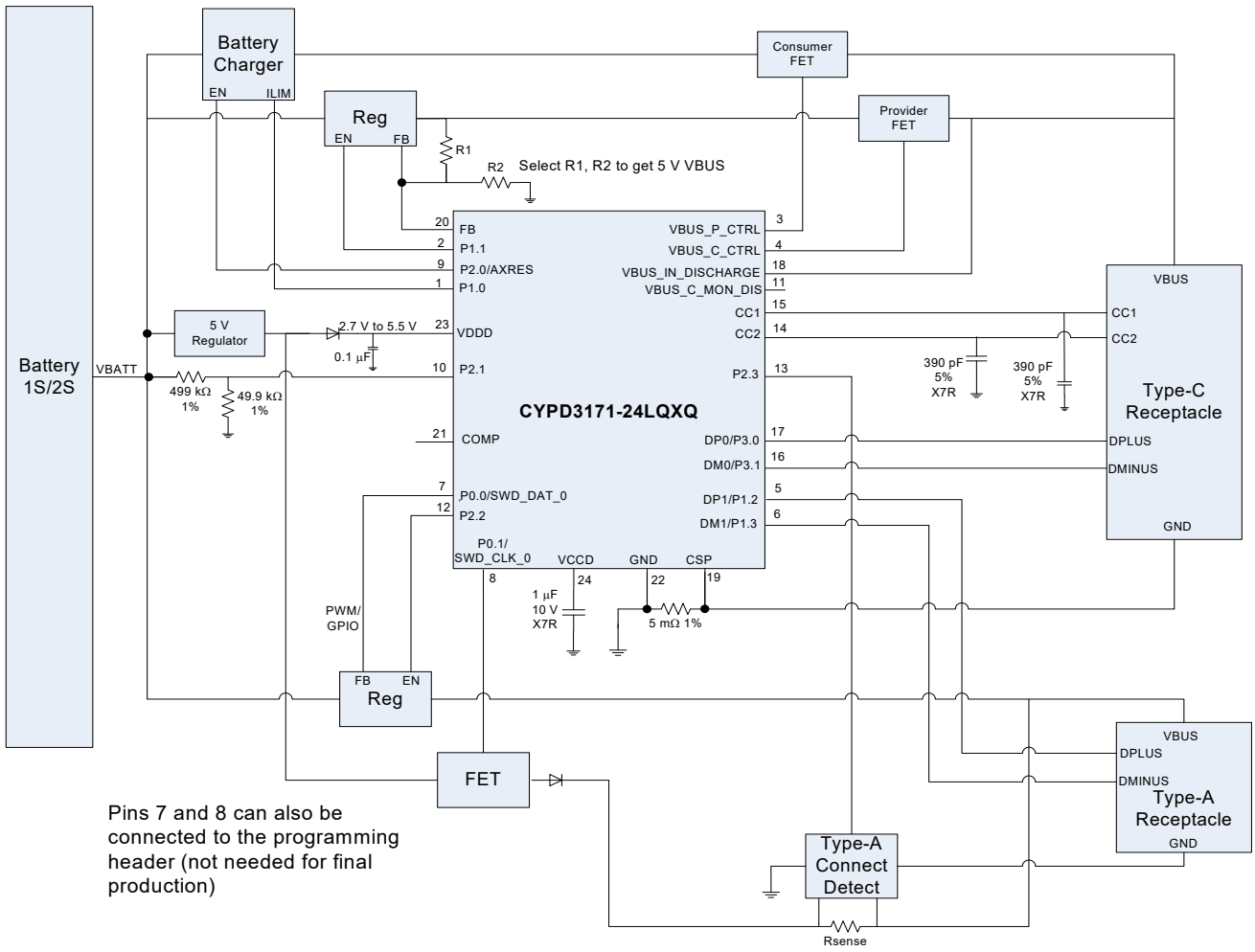


Figure 10 shows the application diagram of a CCG3PA based power bank application. It shows dual port power bank implementation using CCG3PA device. The power bank application can charge portable devices connected to the Type-C and Type-A port simultaneously. The Type-C port can be configured to support USBPD 3.0 QC 4.0, Apple Charging 2.4A, and AFC. The Type-A port can be configured to support QC3.0, Apple Charging, and AFC.

The battery can be charged from Type-C and USBPD power adapters or BC1.2 power adapters.

Figure 10. CCG3PA Power Bank Application Diagram



Electrical Specifications

Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{BUS_MAX}	Max supply voltage relative to V_{SS} on VBUS_IN_DISCHARGE and VBUS_C_MON_DISCHARGE pins	–	–	30	V	Absolute max
V_{DDD_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	
$V_{CC\_PIN\_ABS}$	Max voltage on CC1, CC2 pins and port pins P2.2 and P2.3 for applicable devices	–	–	22[6]	V	
V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DDD} +0.5	V	
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
$I_{GPIO\_injection}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5	mA	Absolute max, current injected per pin
$V_{GPIO\_OVT\_ABS}$	OVT GPIO voltage	–0.5	–	6	V	Applicable to port pins P0.0 and P0.1
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch-up	–100	–	100	mA	–
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	–	–	V	Contact discharge on CC1, CC2, VBUS, P2.2 and P2.3 pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	–	–	V	Air discharge for DPLUS, DMINUS, CC1, CC2, VBUS, P2.2 and P2.3 pins

Note
6. As per USB PD specification, maximum allowed VBUS = 21.5V.

Device-Level Specifications

All specifications are valid for –40 °C ≤ T_A ≤ 105 °C and T_J ≤ 120 °C, except where noted.

Table 5. DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PWR#2	V_{DDD}	Power Supply Input Voltage	2.7	–	5.5	V	Sink mode, –40 °C ≤ T_A ≤ 105 °C.
SID.PWR#2_A	V_{DDD}	Power Supply Input Voltage	3.0	–	5.5	V	Source mode, –40 °C ≤ T_A ≤ 105 °C.
SID.PWR#3	V_{BUS_IN}	Power Supply Input Voltage	3.0	–	24.5	V	–40 °C ≤ T_A ≤ 105 °C.
SID.PWR#5	V_{CCD}	Output Voltage for core Logic	–	1.8	–	V	–
SID.PWR#13	C_{exc}	Power supply decoupling capacitor for V_{DDD}	0.8	1	–	µF	X5R ceramic or better
SID.PWR#14	C_{exv}	Power supply decoupling capacitor for VBUS_IN_DISH-CARGE	–	0.1	–	µF	X5R ceramic or better
Active Mode. Typical values measured at V_{DDD} = 5.0V or V_{BUS} = 5.0 V and T_A = 25 °C.							
SID.PWR#8	I_{DD_A}	Supply current from V_{BUS} or V_{DDD}	–	10	–	mA	V_{DDD} = 5 V OR V_{BUS} = 5 V, T_A = 25 °C. CC1/CC2 in Tx or Rx, no I/O sourcing current, 2 SCBs at 1 Mbps, EA/ADC/CSA/UVOV ON, CPU at 24 MHz.
Sleep Mode. Typical values measured at V_{DD} = 3.3 V and T_A = 25 °C.							
SID25A	I_{DD_S}	CC, I^2C, WDT wakeup on. IMO at 24 MHz.	–	3	–	mA	V_{DDD} = 3.3 V, T_A = 25 °C, All blocks except CPU are on, CC IO on, EA/ADC/CSA/UVOV On.
Deep Sleep Mode. Typical values measured at T_A = 25 °C.							
SID_PA_DS_UA	$I_{DD\_PA\_DS\_UA}$	V_{BUS} = 4.5 to 5.5 V. CC Attach, I^2C, WDT Wakeup on	–	100	–	µA	Power Adapter/Charger application Power Source = V_{BUS} = 5 V, T_A = 25 °C, Type-C Not Attached. CC Attach, I^2C and WDT enabled for Wakeup.
SID_PA_DS_A	$I_{DD\_PA\_DS\_A}$	V_{BUS} = 3.0 to 24.5 V. CC, I^2C, WDT Wakeup on	–	500	–	µA	Power Adapter/Charger application VBUS = 24.5 V, T_A = 25 °C, Part is in deep sleep. Attached, CC I/O on, ADC/CSA/UVOV On
SID_PB_DS_UA	$I_{DD\_PB\_DS\_UA}$	V_{DDD} = 3.0 to 5.5 V. CC Attach, I^2C, WDT Wakeup on	–	100	–	µA	Power Bank application Power Source = V_{DDD} = 5 V, T_A = 25 °C, Type-C Not Attached. CC Attach, I^2C and WDT enabled for Wakeup.
SID_P-B_DS_A_SRC	$I_{DD\_P-B\_DS\_A\_SRC}$	V_{DDD} = 3.0 to 5.5 V. CC, I^2C, WDT Wakeup on	–	500	–	µA	Power Bank Source application V_{DDD} = 5 V, T_A= 25 °C, Part is in deep sleep. Attached, CC I/O on, ADC/CSA/UVOV On.
SID_P-B_DS_A_SNK	$I_{DD\_P-B\_DS\_A\_SNK}$	V_{BUS} 4.0 to 24.5 V. CC, I^2C, WDT Wakeup on	–	500	–	µA	Power Bank Sink application V_{BUS} = 24.5 V, T_A = 25 °C, Part is in deep sleep. Attached, CC I/O on, ADC/CSA/UVOV On

Table 6. AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#4	F_{CPU}	CPU input frequency	DC	–	48	MHz	All V_{DDD}
SID.PWR#17	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	–
SID.PWR#18	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	35	µs	–
SYS.FES#1	$T_{\_PWR\_RDY}$	Power-up to “Ready to accept I^2C/CC command”	–	5	25	ms	–
SID.PWR#18A	$T_{POR\_HIZ\_T}$	Power-on I/O Initialization Time	–	3	–	ms	–

I/O

Table 7. I/O DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.GIO#37	V_{IH_CMOS}	Input voltage HIGH threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID.GIO#38	V_{IL_CMOS}	Input voltage LOW threshold	–	–	0.3 × V_{DDD}	V	CMOS input
SID.GIO#39	$V_{IH\_VDDD2.7-}$	LVTTL input, V_{DDD} < 2.7 V	0.7× V_{DDD}	–	–	V	–
SID.GIO#40	$V_{IL\_VDDD2.7-}$	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 × V_{DDD}	V	–
SID.GIO#41	$V_{IH\_VDDD2.7+}$	LVTTL input, $V_{DDD} \geq$ 2.7 V	2.0	–	–	V	–
SID.GIO#42	$V_{IL\_VDDD2.7+}$	LVTTL input, $V_{DDD} \geq$ 2.7 V	–	–	0.8	V	–
SID.GIO#33	V_{OH_3V}	Output voltage HIGH level	V_{DDD} –0.6	–	–	V	I_{OH} = 4 mA at 3-V V_{DDD}
SID.GIO#36	V_{OL_3V}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 10 mA at 3-V V_{DDD}
SID.GIO#5	R_{PU}	Pull-up resistor value	3.5	5.6	8.5	kΩ	+25 °C T_A, all V_{DDD}
SID.GIO#6	R_{PD}	Pull-down resistor value	3.5	5.6	8.5	kΩ	+25 °C T_A, all V_{DDD}
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25 °C T_A, 3-V V_{DDD}
SID.GIO#17	C_{PIN_A}	Max pin capacitance	–	–	22	pF	Capacitance on DP0, DM0, DP1, DMI pins. Guaranteed by characterization.
SID.GIO#17A	C_{PIN}	Max pin capacitance	–	3	7	pF	–40°C to +85°C T_A, All V_{DDD}, all other I/O_S. Guaranteed by characterization.
SID.GIO#43	V_{HYSTTL}	Input hysteresis, LVTTL V_{DDD} > 2.7 V	15	40	–	mV	Guaranteed by characterization.
SID.GIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–	mV	V_{DDD} < 4.5 V. Guaranteed by characterization.
SID69	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	Guaranteed by design.
SID.GIO#45	I_{TOT_GPIO}	Maximum total sink chip current	–	–	85	mA	Guaranteed by design.
OVT							
SID.GIO#46	I_{IHS}	Input current when Pad > V_{DDD} for OVT inputs	–	–	10.00	µA	Per I^2C specification

Table 8. I/O AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID70	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{load} = 25 pF
SID71	T_{FALLF}	Fall time in Fast Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{load} = 25 pF

Table 9. GPIO_20VT DC Specifications (Applicable to port pins P2.2 and P2.3 only)

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID.GPIO_20VT#4	GPIO_20VT_I_LU	GPIO_20VT Latch up current limits	–140	–	140	mA	Max / min current in to any input or output, pin-to-pin, pin-to-supply
SID.GPIO_20VT#5	GPIO_20VT_RPU	GPIO_20VT Pull-up resistor value	1	–	25	kΩ	+25 °C T_A, 1.4 V to GPIO_20VT_Voh(min)
SID.GPIO_20VT#6	GPIO_20VT_RPD	GPIO_20VT Pull-down resistor value	2.5	–	20	kΩ	+25°C T_A, 1.4-V to V_{DDD}
SID.GPIO_20VT#16	GPIO_20VT_IIL	GPIO_20VT Input leakage current (absolute value)	–	–	2	nA	+25°C T_A, 3-V V_{DDD}
SID.GPIO_20VT#17	GPIO_20VT_CPIN	GPIO_20VT pin capacitance	15	–	25	pF	–40 °C to +85 °C T_A, All V_{DDD}, F = 1 MHz
SID.GPIO_20VT#36	GPIO_20VT_Vol	GPIO_20VT Output Voltage low level.	–	–	0.4	V	I_{OL} = 2 mA
SID.GPIO_20VT#41	GPIO_20VT_Vih_LVTTL	GPIO_20VT LVTTL Input Voltage high level.	2	–	–	V	$V_{DDD} \geq 2.7$ V
SID.GPIO_20VT#42	GPIO_20VT_Vil_LVTTL	GPIO_20VT LVTTL Input Voltage low level.	–	–	0.8	V	$V_{DDD} \geq 2.7$ V
SID.GPIO_20VT#43	GPIO_20VT_Vhysttl	GPIO_20VT Input hysteresis LVTTL	15	40	–	mV	$V_{DDD} \geq 2.7$ V
SID.GPIO_20VT#69	GPIO_20VT_IDIODE	GPIO_20VT Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	

Table 10. GPIO_20VT AC Specifications (Applicable to port pins P2.2 and P2.3 only)

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID.GPIO_20VT#70	GPIO_20VT_TriseF	GPIO_20VT Rise time in Fast Strong Mode	1	–	45	ns	All V_{DDD}, C_{load} = 25 pF
SID.GPIO_20VT#71	GPIO_20VT_TfallF	GPIO_20VT Fall time in Fast Strong Mode	2	–	15	ns	All V_{DDD}, C_{load} = 25 pF

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for GPIO Pins

Table 11. PWM AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS. Maximum = 48 MHz.
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between quadrature-phase inputs

I^2C

Table 12. Fixed I^2C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	100	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135	µA	–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	310	µA	–
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	1.4	–	µA	–

Table 13. Fixed I^2C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

Table 14. Fixed UART DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I_{UART1}	Block current consumption at 100 kbps	–	–	20	µA	–
SID161	I_{UART2}	Block current consumption at 1000 kbps	–	–	312	µA	–

Table 15. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

Table 16. Fixed SPI DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	I_{SPI1}	Block current consumption at 1 Mb/s	–	–	360	µA	–
SID164	I_{SPI2}	Block current consumption at 4 Mb/s	–	–	560	µA	–
SID165	I_{SPI3}	Block current consumption at 8 Mb/s	–	–	600	µA	–

Table 17. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	F_{SPI}	SPI Operating frequency (Master; 6X oversampling)	–	–	8	MHz	–

Table 18. Fixed SPI Master Mode AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID167	T_{DMO}	MOSI Valid after SClock driving edge	–	–	15	ns	–
SID168	T_{DSI}	MISO Valid before SClock capturing edge	20	–	–	ns	Full clock, late MISO sampling
SID169	T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to slave capturing edge

Table 19. Fixed SPI Slave Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID170	T_{DMI}	MOSI Valid before Sclock capturing edge	40	–	–	ns	–
SID171	T_{DSO}	MISO Valid after Sclock driving edge	–	–	$42 + 3 \times T_{CPU}$	ns	$T_{CPU} = 1/F_{CPU}$
SID171A	T_{DSO_EXT}	MISO Valid after Sclock driving edge in Ext Clk mode	–	–	48	ns	–
SID172	T_{HSO}	Previous MISO data hold time	0	–	–	ns	–
SID172A	$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	100	–	–	ns	–

System Resources

Power-on-Reset (POR) with Brown Out SWD Interface

Table 20. Imprecise Power On Reset (PRES) (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	$V_{RISEIPOR}$	Power-on Reset (POR) rising trip voltage	0.80	–	1.50	V	–
SID186	$V_{FALLIPOR}$	POR falling trip voltage	0.70	–	1.4	V	–

Table 21. Precise Power On Reset (POR)

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	$V_{FALLPPOR}$	Brown-out Detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	–
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1	–	1.5	V	–

Table 22. SWD Interface Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.SWD#1	F_SWDCLK1	3.3V ≤ VDDD ≤ 5.5V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#2	F_SWDCLK2	2.7V ≤ VDDD ≤ 3.3V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#3	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID.SWD#4	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID.SWD#5	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.50 × T	ns	–
SID.SWD#6	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	–

Internal Main Oscillator

Table 23. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	–

Table 24. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 24, 36, and 48 MHz (trimmed)	–	–	±2	%	–
SID226	$T_{STARTIMO}$	IMO start-up time	–	–	7	µs	Guaranteed by characterization.
SID228	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	Guaranteed by characterization.
SID.CLK#1	F_{IMO}	IMO frequency	24	36	48	MHz	Only 3 frequencies supported: 24 MHz, 36 MHz, and 48 MHz.

Internal Low-Speed Oscillator Power Down

Table 25. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO1}	I_{LO} operating current	–	0.3	1.05	µA	–
SID233	$I_{ILOLEAK}$	I_{LO} leakage current	–	2	15	nA	–

Table 26. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO1}$	I_{LO} start-up time	–	–	2	ms	Guaranteed by Characterization
SID238	$T_{ILODUTY}$	I_{LO} duty cycle	40	50	60	%	Guaranteed by Characterization
SID.CLK#5	F_{ILO}	I_{LO} frequency	20	40	80	kHz	–

Table 27. PD DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PD.1	Rp_std	DFP CC termination for default USB Power	64	80	96	µA	–
SID.PD.2	Rp_1.5A	DFP CC termination for 1.5A power	166	180	194.4	µA	–
SID.PD.3	Rp_3.0A	DFP CC termination for 3.0A power	304	330	356.4	µA	–
SID.PD.4	Rd	UFP CC termination	4.59	5.1	5.61	kΩ	–
SID.PD.5	Rd_DB	UFP (Power Bank) Dead Battery CC Termination on CC1 and CC2	4.08	5.1	6.12	kΩ	All supplies forced to 0V and 1.32 V applied at CC1 or CC2
SID.PD.6	$V_{gndoffset}$	Ground offset tolerated by BMC receiver	–500	–	500	mV	Relative to the remote BMC transmitter.

Table 28. LS-CSA Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.LSCSA.1	Cin_inp	CSP Input capacitance	7	–	10	pF	Guaranteed by characterization
SID.LSCSA.2	Csa_Acc1	CSA accuracy 5 mV < Vsense < 10 mV	–15	–	15	%	Active Mode
SID.LSCSA.3	Csa_Acc2	CSA accuracy 10 mV < Vsense < 15 mV	–10	–	10	%	
SID.LSCSA.4	Csa_Acc3	CSA accuracy 15 mV < Vsense < 20 mV	–6	–	6	%	
SID.LSCSA.5	Csa_Acc4	CSA accuracy 20 mV < Vsense < 30 mV	–5	–	5	%	
SID.LSCSA.6	Csa_Acc5	CSA accuracy 30 mV < Vsense < 50 mV	–4	–	4	%	
SID.LSCSA.7	Csa_Acc6	CSA accuracy 50 mV < Vsense	–4	–	4	%	
SID.LSCSA.8	Csa_SCP_Acc1	CSA SCP 80 mV	–16.5	–	30	%	
SID.LSCSA.9	Csa_SCP_Acc2	CSA SCP 100 mV	–13.4	–	24	%	
SID.LSCSA.10	Csa_SCP_Acc3	CSA SCP 150 mV	–9.4	–	16	%	
SID.LSCSA.11	Csa_SCP_Acc4	CSA SCP 200 mV	–7.5	–	12	%	
SID.LSCSA.12	Av	Nominal Gain values supported: 5, 10, 20, 35, 50, 75, 125, 150	5	–	150	V/V	–
SID.LSCSA.24	Av1_E_Trim	Gain Error	–3	–	3	%	Guaranteed by characterization
SID.LSCSA.31	Av_E_SCP	Gain Error of SCP stage	–3.5	–	3.5	%	Guaranteed by characterization

Table 29. LS-CSA AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.LSCSA.AC.1	T_{OCP_GPIO}	Delay from OCP threshold trip to output GPIO toggle	–	–	20	µs	Available on P1.0 or P1.1
SID.LSCSA.AC.2	T_{OCP_Gate}	Delay from OCP threshold trip to external PFET Power Gate Turn off	–	–	50	µs	–
SID.LSCSA.AC.3	T_{SCP_GPIO}	Delay from SCP threshold trip to output GPIO toggle	–	–	15	µs	Available on P1.0 or P1.1
SID.LSCSA.AC.4	T_{SCP_Gate}	Delay from SCP threshold trip to external PFET Power Gate Turn off	–	–	50	µs	–
SID.LSCSA.AC.5	T_{SR_GPIO}	Delay from SR threshold trip to output GPIO toggle	–	–	20	µs	Available on P1.0 or P1.1

Table 30. UV/OV Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.UVOV.1	V_{THOV1}	Overvoltage Threshold Accuracy, 4.0 V to 11.0 V	–3	–	3	%	Active Mode
SID.UVOV.2	V_{THOV2}	Overvoltage Threshold Accuracy, 11 V to 27.4 V	–3.2	–	3.2	%	
SID.UVOV.3	V_{THUV1}	Undervoltage Threshold Accuracy, 2.7 V to 3.3 V	-4	–	4	%	
SID.UVOV.4	V_{THUV2}	Undervoltage Threshold Accuracy, 3.3 V to 4.0 V	–3.5	–	3.5	%	
SID.UVOV.5	V_{THUV3}	Undervoltage Threshold Accuracy, 4.0 V to 11.0 V	–3	–	3	%	
SID.UVOV.6	V_{THUV4}	Undervoltage Threshold Accuracy, 11.0 V to 22.0 V	–2.9	–	2.9	%	

Table 31. UV/OV AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.UVOV.AC.1	T_{OV_GPIO}	Delay from UV threshold trip to output GPIO toggle	–	–	20	µs	Available on P1.0 or P1.1
SID.UVOV.AC.2	T_{OV_GATE}	Delay from UV threshold trip to external PFET power gate turn off	–	–	50	µs	–
SID.UVOV.AC.3	T_{UV_GPIO}	Delay from UV threshold trip to output GPIO toggle	–	–	20	µs	Available on P1.0 or P1.1

Gate Driver Specifications

Table 32. Gate Driver DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.GD.1	R_{PD}	Pull-down resistance	–	–	3	kΩ	Applicable on VBUS_P_CTRL and VBUS_C_CTRL to turn ON external PFET.
SID.GD.2	R_{PU}	Pull-up resistance	–	–	4	kΩ	Applicable on VBUS_P_CTRL to turn OFF external PFET
SID.GD.3	I_{PD0}	Pull-down current sink at drive strength of 1	25	–	75	µA	I-mode (current mode) pull down at 5 V. Applicable on VBUS_P_CTRL and VBUS_C_CTRL to turn ON external PFET
SID.GD.4	I_{PD1}	Pull-down current sink at drive strength of 2	50	–	150	µA	
SID.GD.5	I_{PD2}	Pull-down current sink at drive strength of 4	140	–	300	µA	
SID.GD.6	I_{PD3}	Pull-down current sink at drive strength of 8	280	–	580	µA	
SID.GD.7	I_{PD4}	Pull-down current sink at drive strength of 16	560	–	1200	µA	
SID.GD.8	I_{PD5}	Pull-down current sink at drive strength of 32	1120	–	2300	µA	
SID.GD.9	I_leak_p1	Pin leakage on VBUS_P_CTRL	–	0.003	–	µA	+25 °C T_J, 5-V V_{DDD}, 20-V V_{BUS}
SID.GD.10	I_leak_c1	Pin leakage on VBUS_C_CTRL	–	0.003	–	µA	+25 °C T_J, 5-V V_{DDD}, 20-V V_{BU}
SID.GD.11	I_leak_p2	Pin leakage on VBUS_P_CTRL	–	–	2	µA	+85 °C T_J, 5-V V_{DDD}, 20-V V_{BU}
SID.GD.12	I_leak_c2	Pin leakage on VBUS_C_CTRL	–	–	2	µA	+85 °C T_J, 5-V V_{DDD}, 20-V V_{BU}
SID.GD.13	I_leak_p3	Pin leakage on VBUS_P_CTRL	–	–	7	µA	+125 °C T_J, 5-V V_{DDD}, 20-V V_{BU}
SID.GD.14	I_leak_c3	Pin leakage on VBUS_C_CTRL	–	–	7	µA	+125 °C T_J, 5-V V_{DDD}, 20-V V_{BU}

Table 33. Gate Driver AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.GD.15	T_{PD1}	Pull down delay on VBUS_C_CTRL	–	–	2	µs	Cload = 2 nF, Delay to VBUS –1.5 V from initiation of falling edge, VBUS = 5 V to 20 V, 50 KΩ tied between VBUS_C_CTRL and VBUS
SID.GD.16	$T_{r\_discharge}$	Discharge rate of output node on VBUS_C_CTRL	–	–	5	V/µs	80% to 20%, 50 KΩ tied between VBUS_C_CTRL and VBUS, Cload = 2 nF, Vinitial = 24 V
SID.GD.17	T_{PD2}	Pull down delay on VBUS_P_CTRL	–	–	2	µs	Cload = 2 nF, Delay to VBUS –1.5 V from initiation of falling edge, V_{BUS} = 5 V to 20 V, 50 KΩ tied between VBUS_C_CTRL and VBUS
SID.GD.18	T_{PU}	Pull up delay on VBUS_P_CTRL	–	–	18	µs	Cload = 2 nF, Delay to VBUS–1.5 V from initiation of falling edge, VBUS = 5 V to 20 V, 50 KΩ tied between VBUS_C_CTRL and VBUS
SID.GD.19	SR_{PU}	Output slew rate on VBUS_P_CTRL	–	–	5	V/µs	Cload = 2 nF, 20% to 80% of VBUS_P_CTRL range
SID.GD.20	SR_{PD}	Output slew rate on VBUS_P_CTRL	–	–	5	V/µs	Cload = 2 nF, 80% to 20% of VBUS_P_CTRL range

Table 34. VBUS Discharge Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID.VBUS.DISC.6	I1	20-V NMOS ON current for DS = 1	0.15	–	1	mA	Measured at 0.5 V
SID.VBUS.DISC.7	I2	20-V NMOS ON current for DS = 2	0.4	–	2	mA	
SID.VBUS.DISC.8	I4	20-V NMOS ON current for DS = 4	0.9	–	4	mA	
SID.VBUS.DISC.9	I8	20-V NMOS ON current for DS = 8	2	–	8	mA	
SID.VBUS.DISC.10	I16	20-V NMOS ON current for DS = 16	4	–	10	mA	
SID.VBUS.DISC.11	VBUS_Stop_Error	Error percentage of final V_{BUS} value from setting	–	–	10	%	When V_{BUS} is discharged to 5 V. Guaranteed by Characterization.

Table 35. Voltage (VBUS) Regulation DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID.DC.VR.1	$V_{\_IN\_3}$	V(pad_in) at 3-V target	2.85	3	3.15	V	Active mode shunt regulator at 3 V with bandgap
SID.DC.VR.2	$V_{\_IN\_5}$	V(pad_in) at 5-V target	4.75	5	5.25	V	Active mode shunt regulator at 5 V
SID.DC.VR.3	$V_{\_IN\_9}$	V(pad_in) at 9-V target	8.55	9	9.45	V	Active mode shunt regulator at 9 V
SID.DC.VR.4	$V_{\_IN\_15}$	V(pad_in) at 15-V target	14.25	15	15.75	V	Active mode shunt regulator at 15 V
SID.DC.VR.5	$V_{\_IN\_20}$	V(pad_in) at 20-V target	19	20	21	V	Active mode shunt regulator at 20 V
SID.DC.VR.6	$V_{\_IN\_3\_DS}$	V(pad_in) at 3-V target	2.7	3	3.3	V	Deep Sleep mode shunt regulator at 3 V with bandgap
SID.DC.VR.7	$V_{\_IN\_5\_DS}$	V(pad_in) at 5-V target	4.5	5	5.5	V	Deep Sleep mode shunt regulator at 5 V
SID.DC.VR.8	$V_{\_IN\_9\_DS}$	V(pad_in) at 9-V target	8.1	9	9.1	V	Deep Sleep mode shunt regulator at 9 V
SID.DC.VR.9	$V_{\_IN\_15\_DS}$	V(pad_in) at 15-V target	13.5	15	16.5	V	Deep Sleep mode shunt regulator at 15 V
SID.DC.VR.10	$V_{\_IN\_20\_DS}$	V(pad_in) at 20-V target	18	20	22	V	Deep Sleep mode shunt regulator at 20 V
SID.DC.VR.11	I_{KA_OFF}	Off-state cathode current	–	–	10	µA	–
SID.DC.VR.12	I_{KA_ON}	Current through cathode pin	–	–	10	mA	–

Table 36. VBUS Short Protection Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.VSP.1	V_SHORT_TRIGGER	Short-to-VBUS system-side clamping voltage on the CC/P2.2/P2.3 pins	–	9	–	V	Guaranteed by Characterization.

Table 37. VBUS DC Regulator Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.VREG.2	VBUS_-DETECT	VBUS detect threshold voltage	1.08	–	2.62	V	–

Table 38. VBUS AC Regulator Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.VREG.3	T_{start}	Total startup time for the regulator supply outputs	–	–	200	µs	Guaranteed by Characterization.

Analog to Digital Converter

Table 39. ADC DC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	–2.5	–	2.5	LSB	Reference voltage generated from VDDD
SID.ADC.2A	INL	Integral non-linearity	–1.5	–	1.5	LSB	Reference voltage generated from bandgap
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5	LSB	Reference voltage generated from VDDD
SID.ADC.3A	DNL	Differential non-linearity	–1.5	–	1.5	LSB	Reference voltage generated from bandgap
SID.ADC.4	Gain Error	Gain error	–1.5	–	1.5	LSB	–
SID.ADC.6	V_{REF_ADC2}	ADC reference voltage when generated from band gap.	1.96	2.0	2.04	V	Reference voltage generated from bandgap

Table 40. ADC AC Specifications (Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.ADC.7	SLEW_Max	Rate of change of sampled voltage signal	–	–	3	V/ms	–

Memory

Table 41. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.MEM#3	FLASH_ERASE	Row erase time	–	–	15.5	ms	–40 °C ≤ T_A ≤ 85 °C, all V_{DDD}
SID.MEM#4	FLASH_WRITE	Row (Block) write time (erase and program)	–	–	20	ms	–40 °C ≤ T_A ≤ 85 °C, all V_{DDD}
SID.MEM#8	FLASH_ROW_PGM	Row program time after erase	–	–	7	ms	25 °C ≤ T_A ≤ 55 °C, all V_{DDD}
SID178	$T_{BULKERASE}$	Bulk erase time (32 KB)	–	–	35	ms	–
SID180	$T_{DEVPROG}$	Total device program time	–	–	7.5	s	–
SID182	F_{RET1}	Flash retention, T_A ≤ 55 °C, 100K P/E cycles	20	–	–	years	–
SID182A	F_{RET2}	Flash retention, T_A ≤ 85 °C, 10K P/E cycles	10	–	–	years	–
SID182B	F_{RET3}	Flash retention, T_A ≤ 105 °C, 10K P/E cycles	3	–	–	years	–

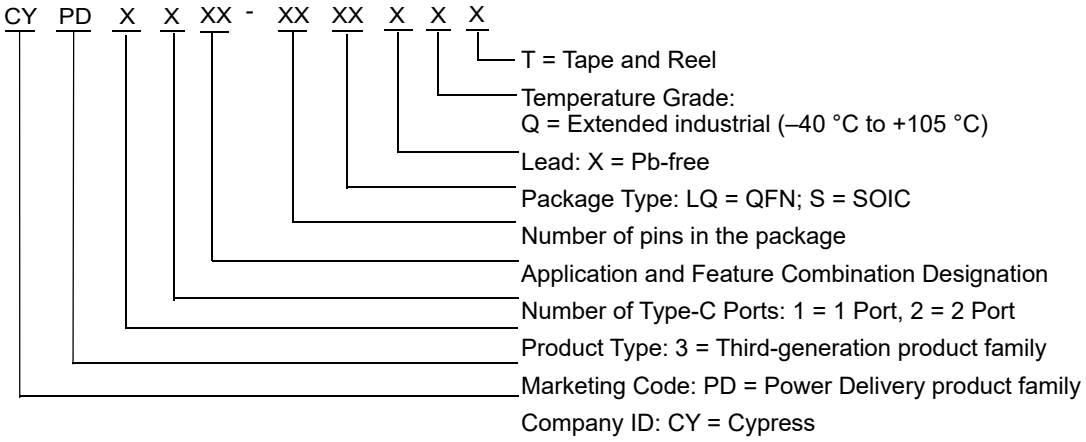
Ordering Information

Table 42 lists the EZ-PD CCG3PA part numbers and features.

Table 42. CCGPA Ordering Information

MPN	Application	Termination Resistor	Role	Bootloader[7]	Package Type	Si ID
CYPD3171-24LQXQ	Power Bank	R_P, R_D, R_{D-DB}	DRP	UFP CC Bootloader	24-Pin QFN	2003
CYPD3174-16SXQ	Power Adapter based on Opto Coupler Feedback	R_P	DFP	DFP CC with Opto Coupler Feedback Bootloader	16-Pin SOIC	2001
CYPD3174-24LQXQ	Power Adapter based on Opto Coupler Feedback	R_P	DFP	DFP CC with Opto Coupler Feedback Bootloader	24-Pin QFN	2000
CYPD3175-24LQXQ	Power Adapter based on Direct Feedback	R_P	DFP	DFP CC with Direct Feedback Bootloader	24-Pin QFN	2002

Ordering Code Definitions



Note
7. It is assumed that VBUS is at 5V by default. Bootloader execution is not responsible for controlling the generation of 5V VBUS.

Packaging

Table 43. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	Extended Industrial	-40	25	105	°C
T_J	Operating junction temperature	Extended Industrial	-40	25	120	°C
T_{JA}	Package θ_{JA} (24-QFN)	–	–	–	19.98	°C/W
T_{JC}	Package θ_{JC} (24-QFN)	–	–	–	4.78	°C/W
T_{JA}	Package θ_{JA} (16-SOIC)	–	–	–	84	°C/W
T_{JC}	Package θ_{JC} (16-SOIC)	–	–	–	33.9	°C/W

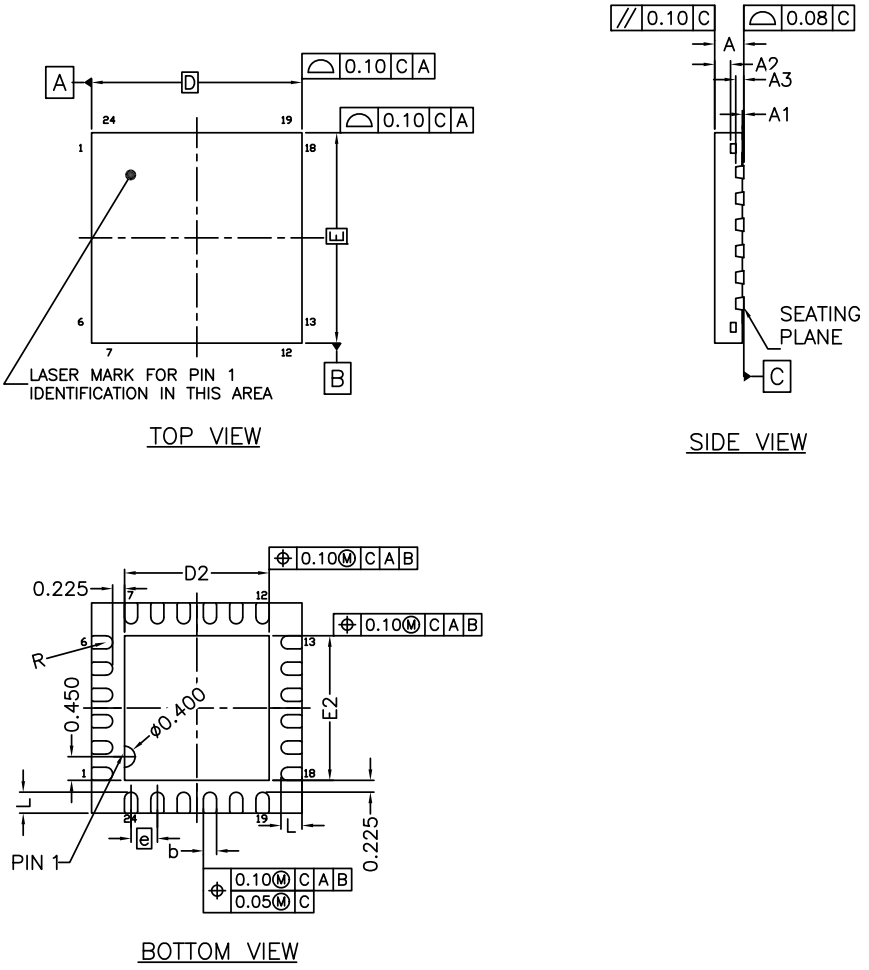
Table 44. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time within 5°C of Peak Temperature
24-pin QFN	260°C	30 seconds
16-pin SOIC	260°C	30 seconds

Table 45. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
24-pin QFN	MSL3
16-pin SOIC	MSL3

Figure 11. 24-pin QFN Package Outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	0.60
A_1	0.00	—	0.05
A_2	—	0.40	0.425
A_3	0.152 REF		
b	0.18	0.25	0.30
D	4.00 BSC		
D_2	2.65	2.75	2.85
E	4.00 BSC		
E_2	2.65	2.75	2.85
L	0.30	0.40	0.50
e	0.50 BSC		
R	0.09	—	—

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. PACKAGE WARPAGE MAX 0.08 mm.
7. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY TO TERMINALS.
9. JEDEC SPECIFICATION NO. REF: N.A.

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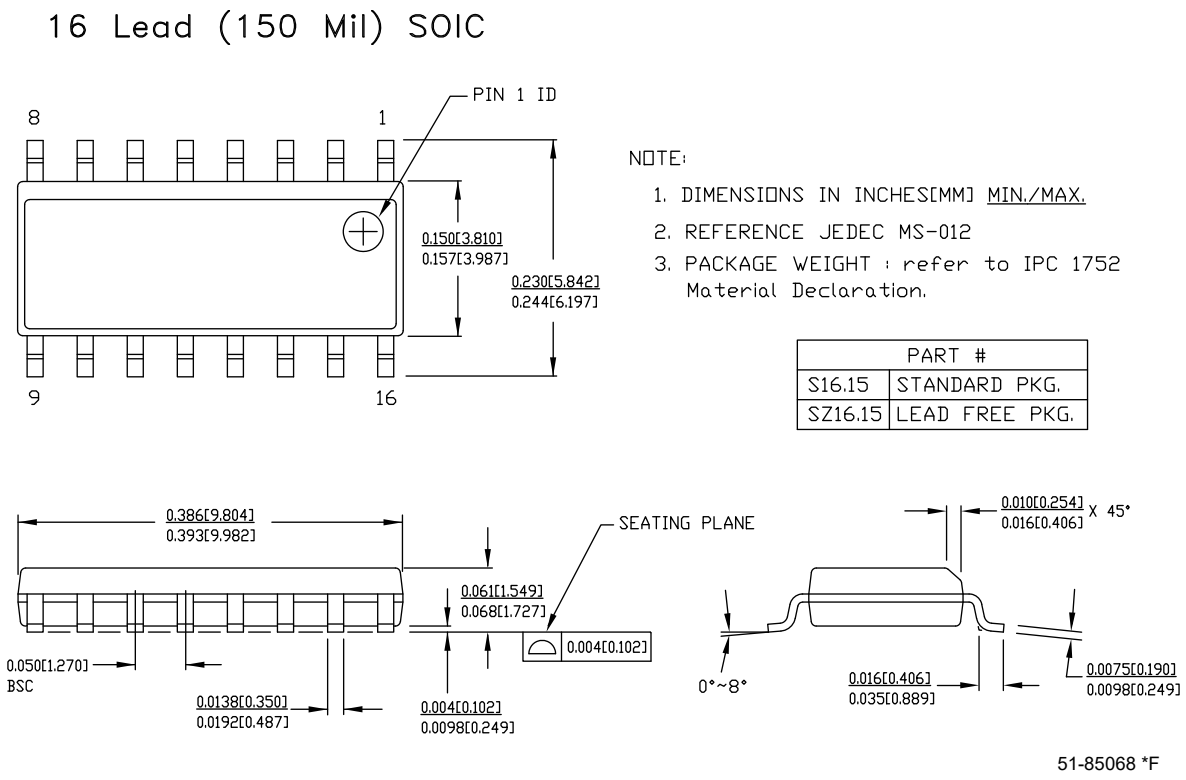
Figure 12. 16-pin SOIC Package Outline



Acronyms

Table 46. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
AES	advanced encryption standard
API	application programming interface
Arm®	advanced RISC machine, a CPU architecture
CC	configuration channel
CCG3	Cable Controller Generation 3
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
EEPROM	electrically erasable programmable read-only memory
EMCA	electronically marked cable assembly, a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FS	full-speed
GPIO	general-purpose input/output
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
LDO	low-dropout regulator
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller
opamp	operational amplifier

Table 46. Acronyms Used in this Document *(continued)*

Acronym	Description
OCP	overcurrent protection
OTP	over temperature protection
OVP	overvoltage protection
OVT	overvoltage tolerant
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCL	I^2C serial clock
SCP	short circuit protection
SDA	I^2C serial data
S/H	sample and hold
SHA	secure hash algorithm
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USBIO	USB input/output, CCG2 pins used to connect to a USB port
UVP	undervoltage protection
XRES	external reset I/O pin

Document Conventions

Units of Measure

Table 47. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	mega samples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Document History Page

Document Title: EZ-PD™ CCG3PA Datasheet, USB Type-C Port Controller Document Number: 002-16951			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	5473667	10/13/2016	New datasheet
*A	5544333	12/13/2016	Changed datasheet status to Preliminary. Updated Features. Updated Logic Block Diagram. Updated Functional Overview Updated Figure 2, Figure 3, Figure 6, Figure 8, Figure 9, and Figure 10. Updated Pinouts. Updated Table 4 with VCC_PIN_ABS and VSBU_PIN_ABS parameters. Added Q-temp parts in Table 42.
*B	5583660	01/18/2017	Updated EZ-PD™ CCG3PA Datasheet, USB Type-C Port Controller, Features, I/O Subsystem, CPU, Charger Detection, and Ordering Information. Updated Table 2 and Table 4. Updated Figure 6 through Figure 10. Updated Sales page.
*C	5665676	03/22/2017	Updated Figure 2, Figure 6, Figure 8, Figure 10, Table 1,Table 2, Table 4, Table 42, Features, Logic Block Diagram, Functional Overview, Power Systems Overview, Ordering Code Definitions, Acronyms. Added Internal Block Diagram. Added Table 5 through Table 41 in Device-Level Specifications. Updated compliance with USB spec in Sales, Solutions, and Legal Information. Updated Cypress logo.
*D	5738854	05/19/2017	Added Application Diagram description before Figure 6, Figure 8, Figure 9, and Figure 10. Added Figure 1. Added CCG3PA Programming and Bootloading section. Added Document History Page section. Added Table 3. Updated Figure 3, Figure 4, Figure 6, Figure 8, Figure 9, and Figure 10. Updated Table 2, Table 4, Table 5, and Table 42. Updated Figure 11 (spec 002-16934 Rev. ** to *A) in Packaging. Updated Cypress logo, Sales page, and Copyright information.
*E	5984670	12/06/2017	Removed Preliminary document status. Updated System-Level Fault Protection, Power, and System-Level ESD Protection. Updated Internal Block Diagram Updated Figure 2. Table 2: Updated Pins 12 and 13. Added Note 5. Updated Figure 6. Added Figure 7. Table 4: Updated max value for $V_{CC\_PIN\_ABS}$ Table 5: Removed SID_DS and updated typ value for SID_PB_DS_UA. Table 7: Added new SID.GIO#17 spec and changed SID.GIO#17 to SID.GIO#17A. Added Table 9 and Table 10. Table 12: Updated max value for SID149. Table 22; Added “Guaranteed by Characterization” Table 24: Updated Conditions for SID226 and SID228. Updated typ value and conditions for SID.CLK#1. Table 26: Updated Conditions for SID234 and SID238. Table 28: Updated min, typ, and max values for SID.LSCSA.1,SID.LSCSA.7, and SID.LSCSA.24 Updated Conditions for SID.GIO#17A, SID.GIO#43, SID.GIO#44, SID.GIO#45, and SID69. Table 31: Added “Guaranteed by Characterization” Table 32: Added SID.GD.9, SID.GD.10, SID.GD.11, SID.GD.12, SID.GD.13, SID.GD.14. Changed description of spec IDs SID.GD.1 to SID.GD.8. Table 33: Renumbered all spec IDs starting from SID.GD.15 to SID.GD.20. Modified max values of SID.GD.15, SID.GD.17 and SID.GD.18. Modified Details/Conditions of all parameters. Table 34: Removed spec IDs SID.VBUS.DISC.1 to SID.VBUS.DISC5. Renumbered SID.VBUS.DISC6 to SID.VBUS.DISC11. Added new spec IDs SID.VBUS.DISC6 to SID.VBUS.DISC10.

Document Title: EZ-PD™ CCG3PA Datasheet, USB Type-C Port Controller Document Number: 002-16951			
*E (contd)	5984670	12/06/2017	Table 35: Added V_IN_3 and V_IN3_DS parameters and renumbered spec IDs from SID.DC.VR.1 to SID.DC.VR.12. Added Table 36. Table 39: Updated min and max values for SID.ADC.4. Table 42: Added new MPN CYPD3174-24LQXQ. Modified "Application" column of CYPD3174-16SXQ and CYPD3175-24LQXQ MPNs. Removed Errata. Added Table 43, Table 44 and Table 45 to Packaging section.
*F	6079226	03/02/2018	Added “The voltage reference for the ADCs is generated either from the VDDD supply or from internal bandgap. When sensing the GPIO pin voltage with an ADC, the pin voltage cannot exceed the VDDIO supply value” to ADC section. Table 2: Updated the Descripion “GPIO with Open drain with pull-up assist. Configurable as GPIO_20VT/I2C_SDA_1/IEC. Tolerant to temporary short to VBUS pin” for Pins P2.2 and P2.3. Table 7: Removed SBU1, SBU2 reference in Details/Conditions for Spec ID SID.GIO#17. Table 32: Moved “0.003” to Typ column for the Spec ID SID.GD.9 and SID.GD.10. Table 12: Updated typical and max values for II2C4 parameter. Table 9: Removed GPIO_20VT_Voh parameter. Table 28: Updated max values of Csa_SCP_Acc parameters. Table 39: Updated the Description of Spec ID SID.ADC.6 as “ADC reference voltage when generated from band gap.”. Removed SID.ADC.5 parameter and added SID.ADC.2A and SID.ADC.3A parameters. Updated Details/Conditions of SID.ADC.2 and SID.ADC3 parameters. Table 35: Added units (V) to SID.DC.VR.3, SID.DC.VR.4 and SID.DC.VR.5 parameters. Updated VBUS Short Protection and I/O Subsystem sections. Updated Table 3 with information on Fault Indicator and VBUS Short Protection Capability. Updated Application Diagrams section.
*G	6864135	04/20/2020	Updated Application Firmware Update over CC Interface section. Added reference to KBA230192. Updated 24-pin QFN Package Outline (002-16934 *A to *C). Updated 16-pin SOIC Package Outline (51-85068 *E to *F). Updated Sales, Solutions, and Legal Information and Copyright year.

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