RMS POWER DETECTOR DC - 3.9 GHz

RoHS EARTH FRIENDLY

Typical Applications

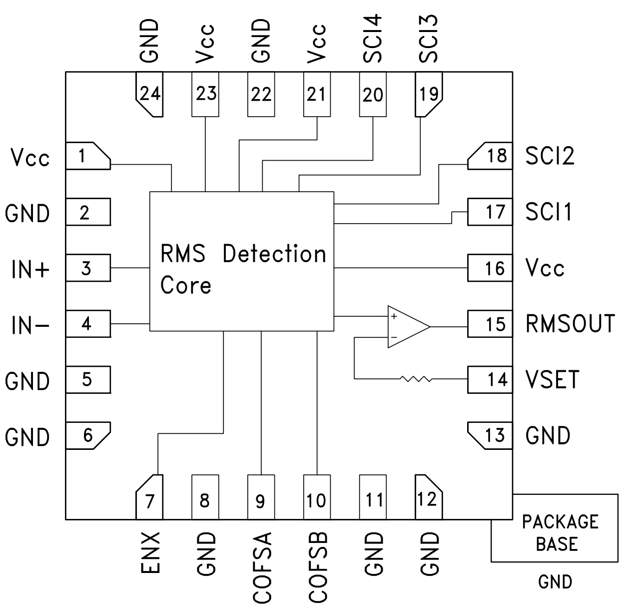
The HMC1010LP4E is ideal for:

- Log –> Root-Mean-Square (RMS) Conversion
- Received Signal Strength Indication (RSSI)
- Transmitter Signal Strength Indication (TSSI)
- RF Power Amplifier Efficiency Control
- Receiver Automatic Gain Control
- Transmitter Power Control

Features

±1 dB Detection Accuracy to 3.9 GHz
Input Dynamic Range: -50 dBm to +10 dBm
RF Signal Wave shape & Crest Factor Independent
Digitally Programmable Integration Bandwidth
+5V Operation from -40°C to +85°C
Excellent Temperature Stability
Power-Down Mode
24 Lead 4x4mm SMT Package: 16mm²

Functional Diagram



General Description

The HMC1010LP4E Power Detector is designed for RF power measurement, and control applications for frequencies up to 3.9 GHz. The detector provides an accurate RMS representation of any RF/IF input signal. The output is a temperature compensated monotonic, representation of real signal power, measured with an input sensing range of 60 dB.

The HMC1010LP4E is ideally suited to those wide bandwidth, wide dynamic range applications, requiring repeatable measurement of real signal power, especially where RF/IF wave shape and/or crest factor change with time.

The integration bandwidth of the HMC1010LP4E is digitally programmable with the use of input pins SCI1-4 with a range of more than 4 decades. This allows the user to dynamically set the operation bandwidth providing the capability of handling different types of modulations on the same platform.

The HMC1010LP4E features an internal OP-AMP at output stage, which provides for slope & intercept adjustments and enables controller application.

Electrical Specifications, T_A = +25 °C, Vcc = 5V

Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Dynamic Range (±1dB Error) [2]								
Input Frequency	100	900	1900	2200	2700	3500	3900	MHz
Differential Input Configuration [1]	59	64	62	62	59	49	45	dB
Deviation vs Temperature: (Over full temperature range -40 °C to 85 °C). Deviation is measured from reference, which is the same WCDMA input at 25 °C.								
[1] Differential Input Interface with 1:1 Balun Transformer (over full input frequency range)						1		dB
[2] With WCDMA 4 Carrier (TM1-64 DPCH)								

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HMC1010* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- HMC1010LP4E Evaluation Board

DOCUMENTATION

Data Sheet

- HMC1010 Data Sheet

REFERENCE MATERIALS

Quality Documentation

- Package/Assembly Qualification Test Report: LP4, LP4B, LP4C, LP4K (QTR: 2013-00487 REV: 04)
- Semiconductor Qualification Test Report: BiCMOS-A (QTR: 2013-00235)

DESIGN RESOURCES

- HMC1010 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all HMC1010 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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Submit a technical question or find your regional support number.

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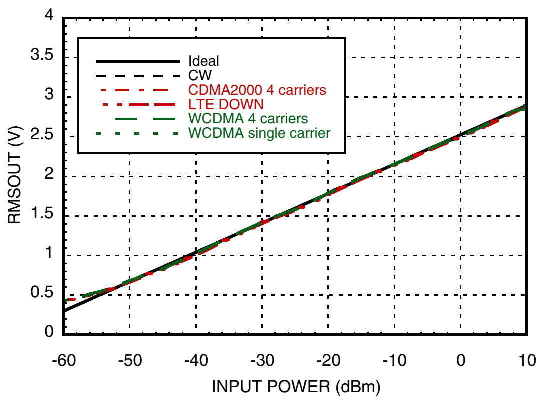
Electrical Specifications II,

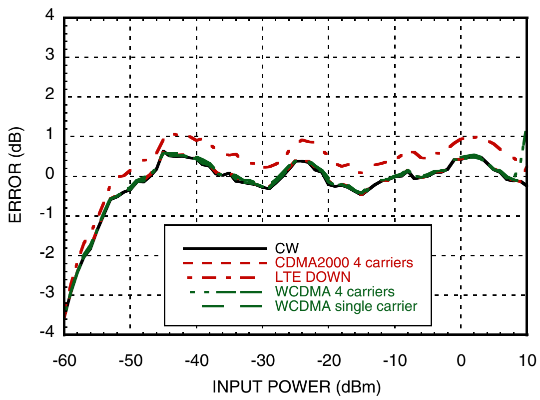
T_A = +25 °C, Vcc = 5V, Sci4 = Sci1 = 0V, Sci3 = Sci2 = 5V, Unless Otherwise Noted

Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Input Frequency	100	900	1900	2200	2700	3500	3900	MHz
Modulation Deviation (Output deviation from reference, which is measured with CW input at equivalent input signal power)								
WCDMA 4 Carrier (TM1-64 DPCH) at +25 °C	0.1	0.1	0.1	0.1	0.1	0.2	0.2	dB
WCDMA 4 Carrier (TM1-64 DPCH) at +85 °C	0.1	0.1	0.1	0.1	0.1	0.1	0.2	dB
WCDMA 4 Carrier (TM1-64 DPCH) at -40 °C	0.1	0.1	0.1	0.1	0.1	0.1	0.2	dB
Logarithmic Slope and Intercept [1]								
Logarithmic Slope	36.4	36.6	37.3	37.8	39	43.3	47.7	mV/dB
Logarithmic Intercept	-70.1	-69.1	-67.6	-66.3	-63.1	-55	-51	dBm
Max. Input Power at ±1dB Error	4	10	10	10	6	5	4	dBm
Min. Input Power at ±1dB Error	-55	-54	-52	-52	-49	-44	-41	dBm
[1] With WCDMA 4 Carrier (TM1-64 DPCH)								

RMSOUT vs. Pin with Different Modulations @ 1900 MHz [1]



RMSOUT Error vs. Pin with Different Modulations @ 1900 MHz [1]



[1] Data was taken at Sci4=Sci1=0V, Sci3=Sci2=5V, shortest integration time is for SCI=0000, allowed longest integration time is for SCI=1100

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Electrical Specifications III,

T_A = +25 °C, Vcc = 5V, Sci4 = Sci1 = 0V, Sci3 = Sci2 = 5V, Unless Otherwise Noted

Parameter	Conditions	Min	Typ.	Max	Units
Differential Input Configuration					
Input Network Return Loss	up to 2.5 GHz [1]		> 10		dB
Input Resistance between IN+ and IN-	Between pins 3 and 4		150		Ω
Input Voltage Range	$V_{DIFFIN} = V_{IN+} - V_{IN-}$			1.6	V
RMSOUT Output					
Output Voltage Range			0.4 to 2.9		V
Source/Sink Current Compliance	RMSOUT held at VCC/2		8 / -0.524		mA
Output Slew Rate (rise / fall)	Sci4=Sci3=Sci2=Sci1=0V, Cofs=1nF		17.92 / 1.41		10^6 V/s
VSET Input (Negative Feedback Terminal)					
Input Voltage Range	For control applications with nominal slope/intercept settings		0.4 to 2.9		V
Input Resistance			5		MΩ
SCI1-4 Inputs, ENX Logic Input (Power Down Control)					
Input High Voltage		0.7xVcc			V
Input Low Voltage				0.3xVcc	V
Input High Current				1	μA
Input Low Current				1	μA
Input Capacitance			0.5		pF
Power Supply					
Supply Voltage		4.5	5	5.5	V
Supply Current with no input power	40 mA typical at -40 °C, 54.5 mA typical at 85 °C		47.5		mA
Supply Current with Pin = 0 dBm	42 mA typical at -40 °C, 57 mA typical at 85 °C		50		mA
Standby Mode Supply Current			5		mA

[1] Performance of differential input configuration is limited by the balun. Baluns used is M/A-COM ETC1-1-13 specified over 4.5 to 3000 MHz

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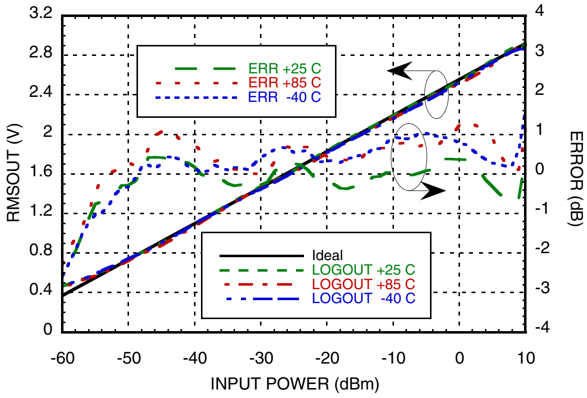
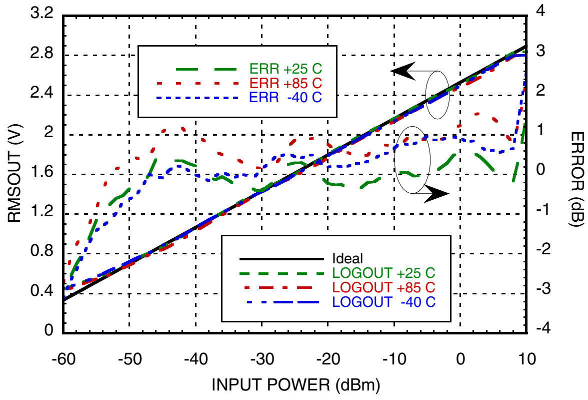
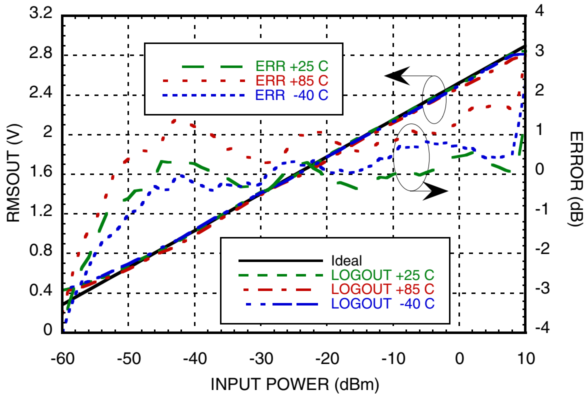
RMSOUT & Error vs. Pin @ 100 MHz [1][2]



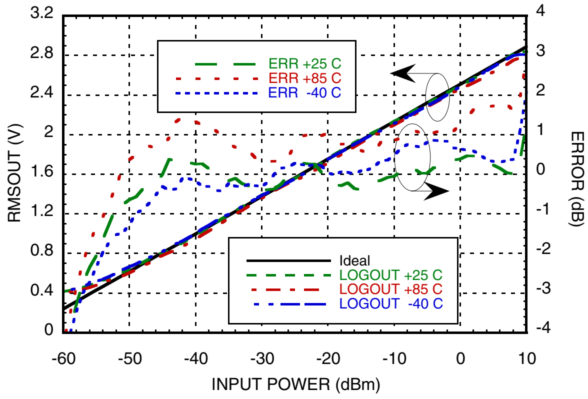
RMSOUT & Error vs. Pin @ 900 MHz [1][2]



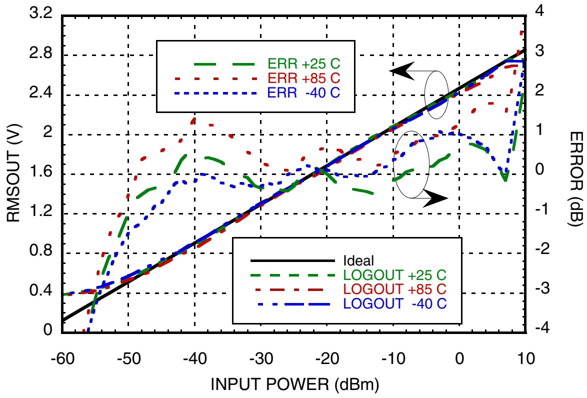
RMSOUT & Error vs. Pin @ 1900 MHz [1][2]



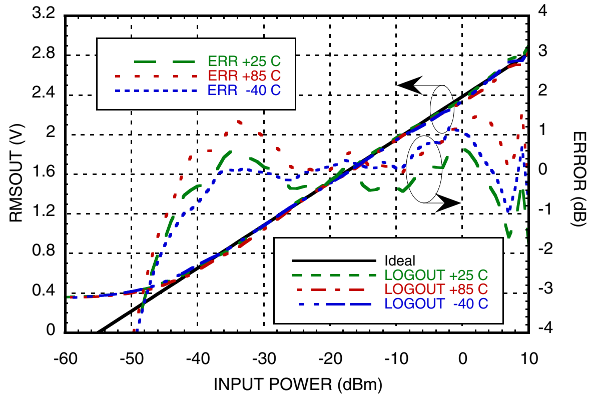
RMSOUT & Error vs. Pin @ 2200 MHz [1][2]



RMSOUT & Error vs. Pin @ 2700 MHz [1][2]



RMSOUT & Error vs. Pin @ 3500 MHz [1][2]



[1] Data was taken at Sci4=Sci1=0V, Sci3=Sci2=5V, shortest integration time is for SCI=0000, allowed longest integration time is for SCI=1100

[2] WCDMA 4 carriers input waveform

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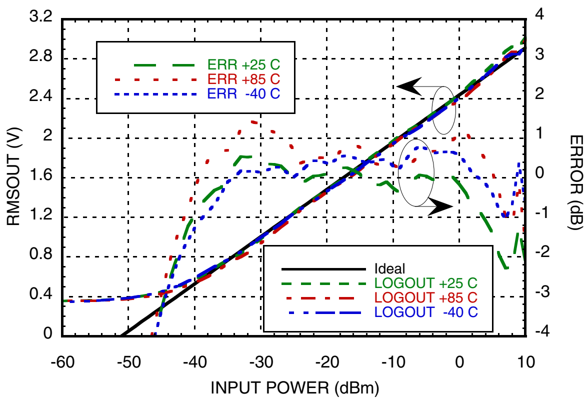
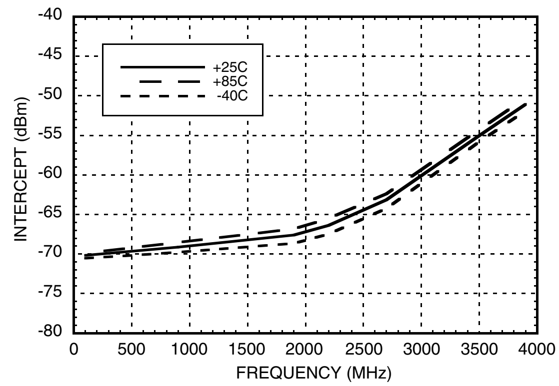
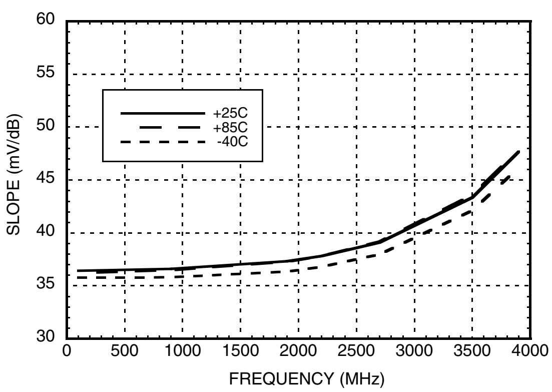
RMSOUT & Error vs. Pin @ 3900 MHz [1][2]



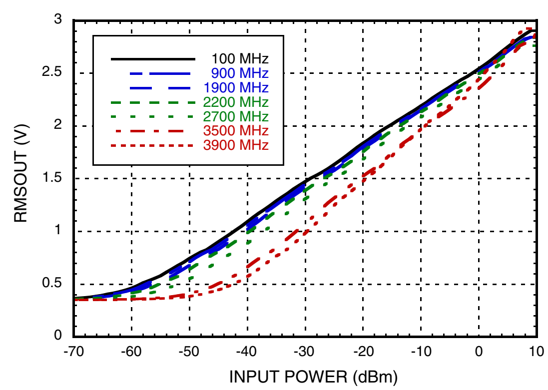
Intercept vs. Frequency [1][2]



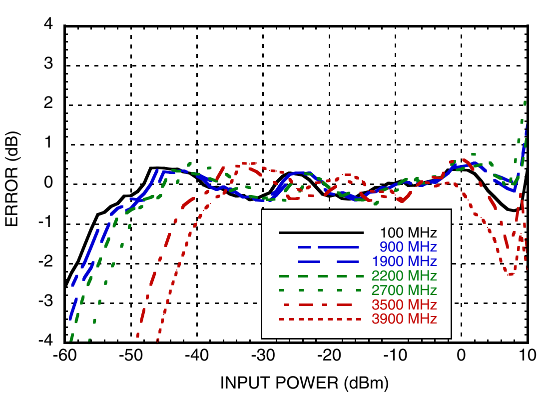
Slope vs. Frequency [1][2]



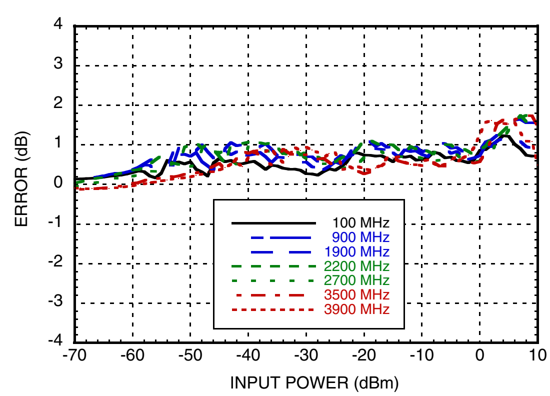
RMSOUT vs. Pin with WCDMA 4 Carrier @ +25 °C [1]



RMSOUT Error vs. Pin with WCDMA 4 Carrier @ +25 °C [1]



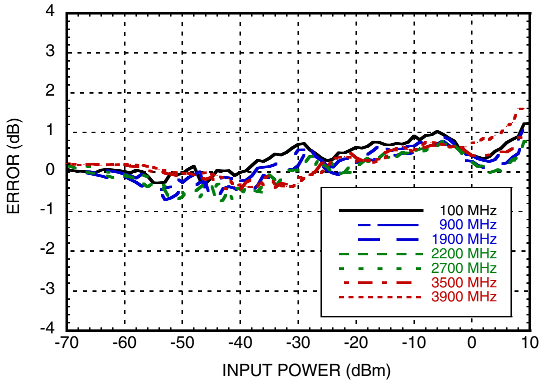
RMSOUT Error vs. Pin with WCDMA 4 Carrier @ +85 °C wrt +25 °C Response [1]



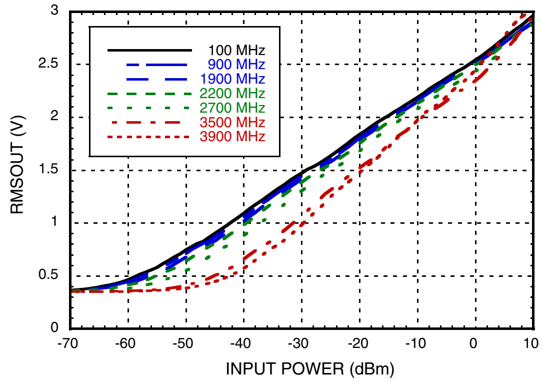
[1] Data was taken at Sci4=Sci1=0V, Sci3=Sci2=5V, shortest integration time is for SCI=0000, allowed longest integration time is for SCI=1100

[2] WCDMA 4 carriers input waveform

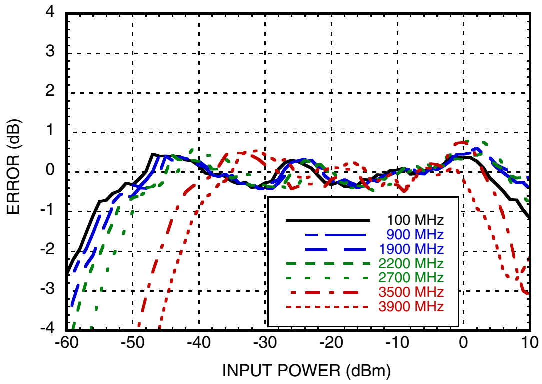
RMSOUT Error vs. Pin with WCDMA 4 Carrier @ -40 °C wrt +25 °C Response [1]



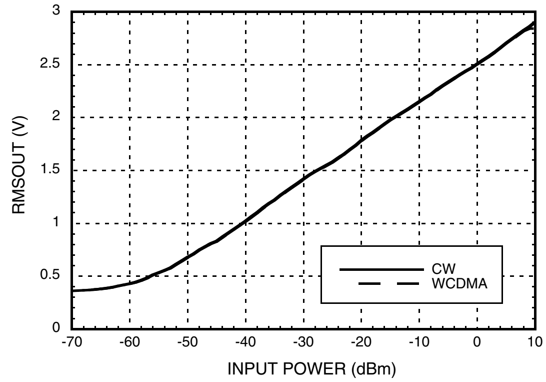
RMSOUT vs. Pin with CW @ +25 °C [1]



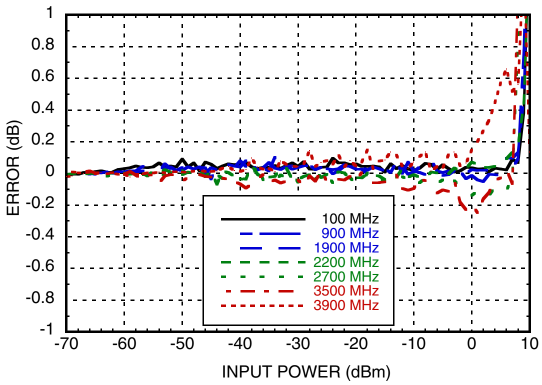
RMSOUT Error vs. Pin with CW @ +25 °C [1]



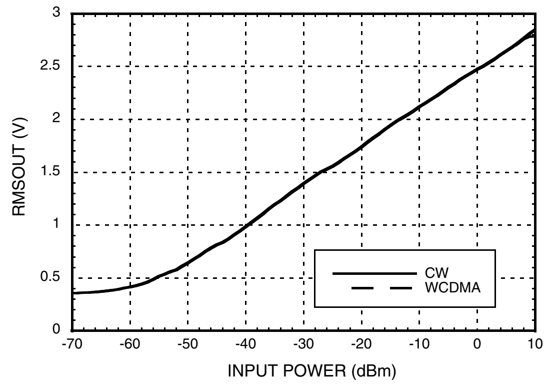
RMSOUT vs. Pin w/ CW & WCDMA 4 Carrier (TM1-64 DPCH) @ 1900 MHz & +25 °C [1]



Reading Error for WCDMA 4 Carrier wrt CW Response @ +25 °C [1]



RMSOUT vs. Pin w/ CW & WCDMA 4 Carrier (TM1-64 DPCH) @ 1900 MHz & +85 °C [1]



[1] Data was taken at Sci4=Sci1=0V, Sci3=Sci2=5V, shortest integration time is for SCI=0000, allowed longest integration time is for SCI=1100

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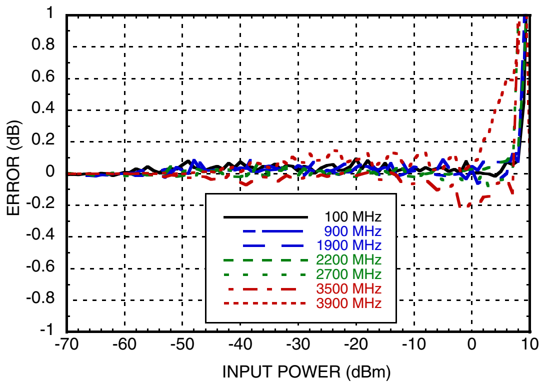
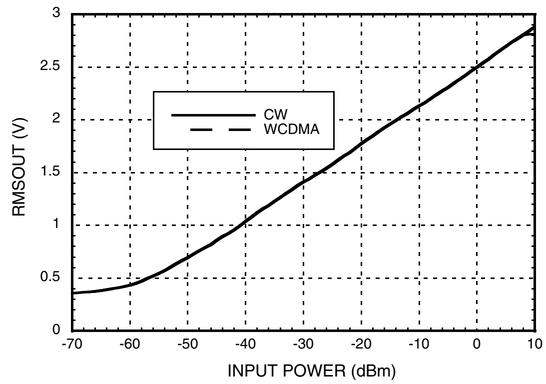
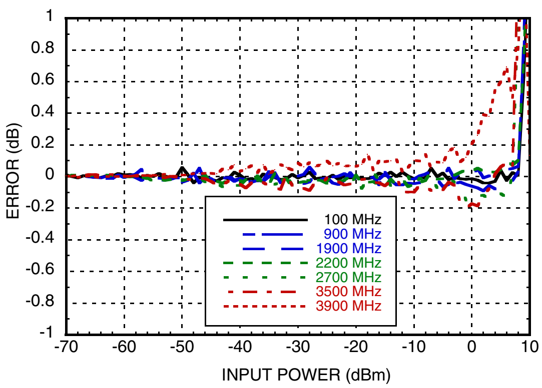
Reading Error for WCDMA 4 Carrier wrt CW Response @ +85 °C [1]



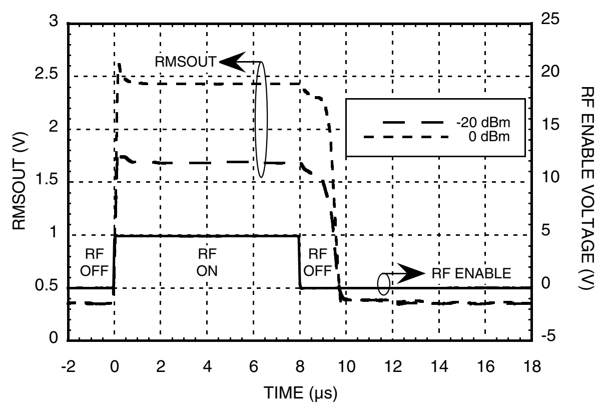
RMSOUT vs. Pin w/ CW & WCDMA 4 Carrier (TM1-64 DPCH) @ 1900 MHz & -40 °C [1]



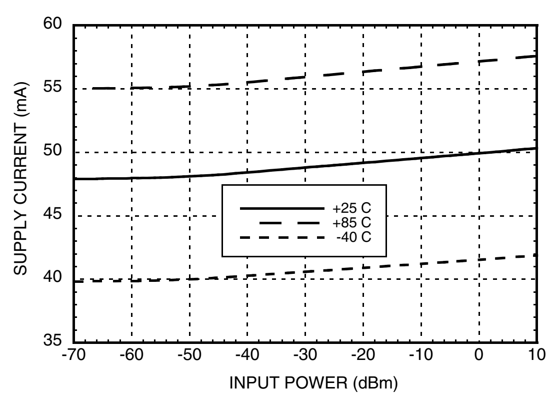
Reading Error for WCDMA 4 Carrier wrt CW Response @ -40 °C [1]



Output Response with SCI = 0000 @ 1900 MHz

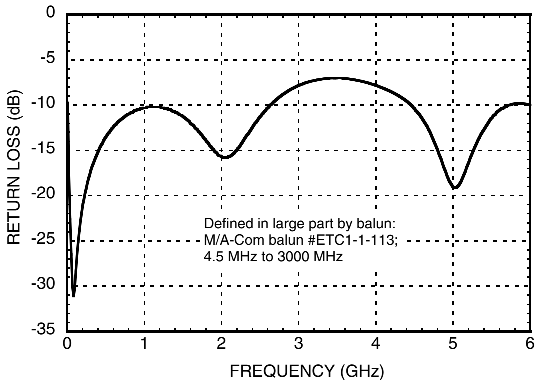


Typical Supply Current vs. Pin, Vcc = 5V

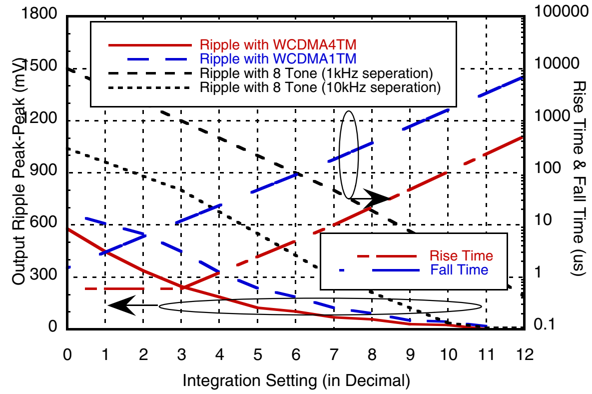


[1] Data was taken at Sci4=Sci1=0V, Sci3=Sci2=5V, shortest integration time is for SCI=0000, allowed longest integration time is for SCI=1100

Input Return Loss vs. Frequency



Output Ripple & Rise/Fall Time vs. Integration Setting [Sci4,Sci3,Sci2,Sci1] in Decimal



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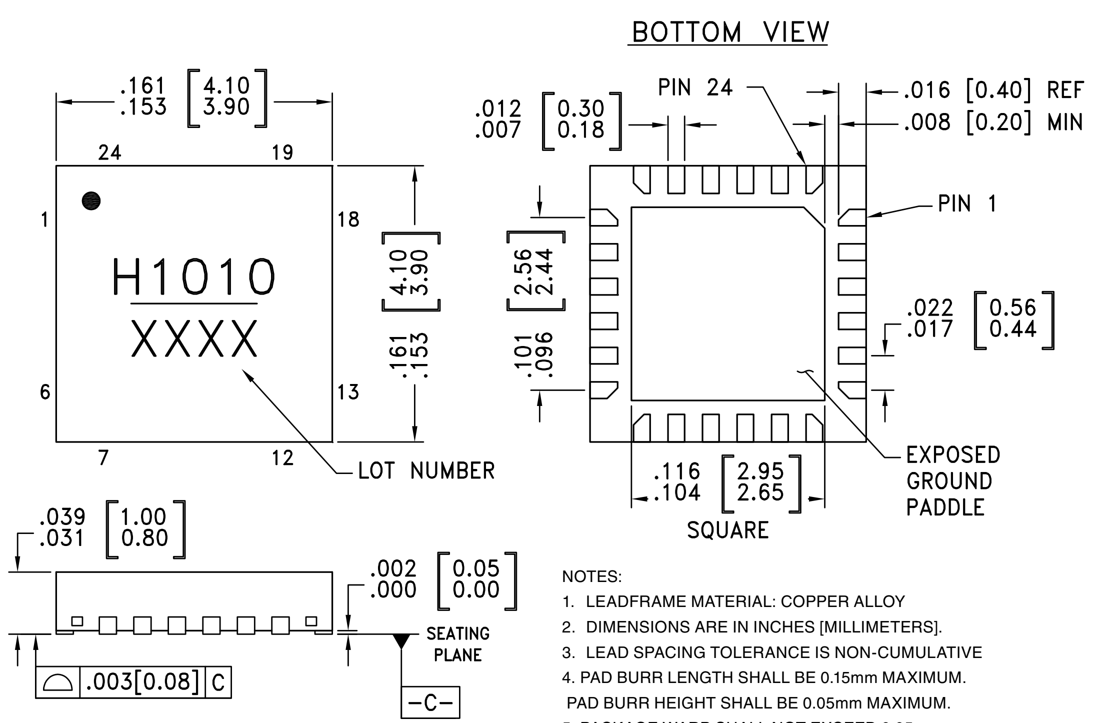
Absolute Maximum Ratings

Supply Voltage (Vcc)	5.6V
RF Input Power	16 dBm
Differential Input Voltage	1.6 Vp-p
Channel / Junction Temperature	125 °C
Continuous Pdiss (T = 85°C) (Derate 34.87 mW/°C above 85°C)	1.39 W
Thermal Resistance (R_{th}) (junction to ground paddle)	28.68 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1B

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



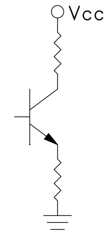
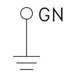
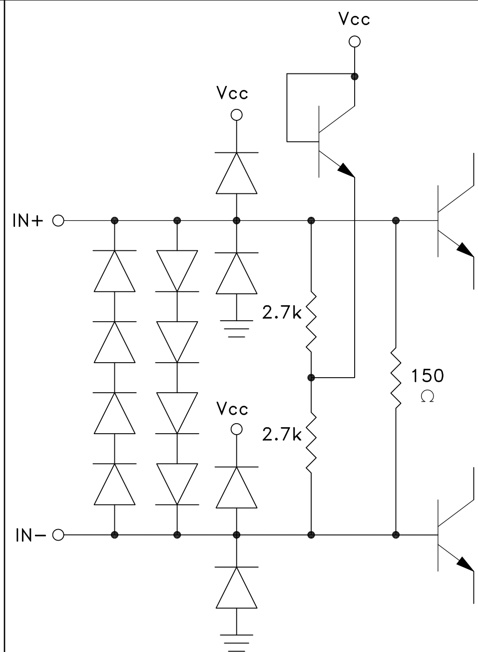
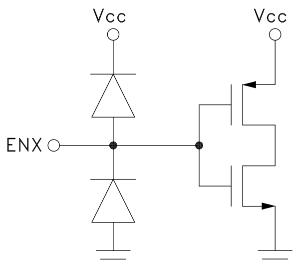
NOTES:
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HMC APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC1010LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H1010 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 16, 21, 23	Vcc	Power Supply. Connect supply voltage to these pins with appropriate filtering.	
2, 5, 6, 8, 11 - 13, 22, 24 Package Base	GND	Package bottom has an exposed metal paddle that must be connected to RF/DC ground.	
3, 4	IN+, IN-	RF input pins. Connect RF to IN+ and IN- through a 1:1 balun	
7	ENX	Disable pin. Connect to GND for normal operation. Applying voltage V>0.8xVcc will initiate power saving mode	

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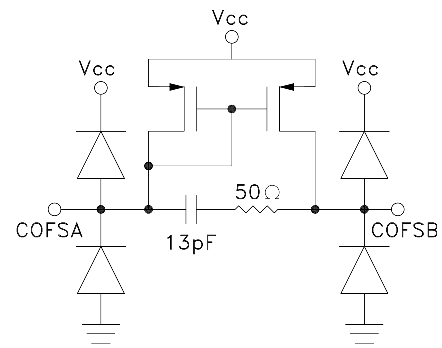
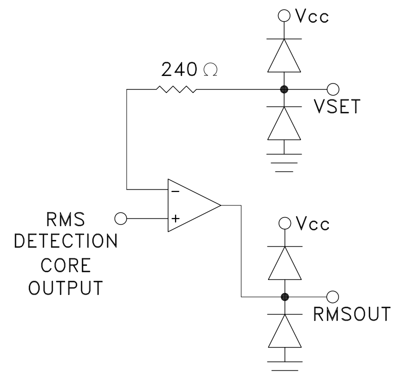
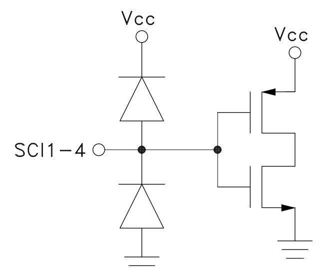
Pin Descriptions (Continued)

Pin Number	Function	Description	Interface Schematic
9, 10	COFSA, COFSB	High pass filter capacitor input. Connect a capacitor between COFSA and COFSB to determine 3 dB point of input signal high-pass filter.	
14	VSET	Setpoint input for controller mode. Allows change of output slope resulting in output power leveling.	
15	RMSOUT	Logarithmic output that provides an indication of mean square input power.	
17 - 20	SCI1 - SCI4	Digitally Programmable Integration Bandwidth Control. Input pins that control the internal integration time constant for RMS calculation. SCI4 is the most significant bit. Set V>0.8xVcc to enable and V<0.2xVcc to disable (active high). Shortest integration time is for SCI=0000, allowed longest integration time is for SCI=1100 (1101, 1110 and 1111 SCI settings are forbidden states). Each step changes the integration time by 1 octave.	

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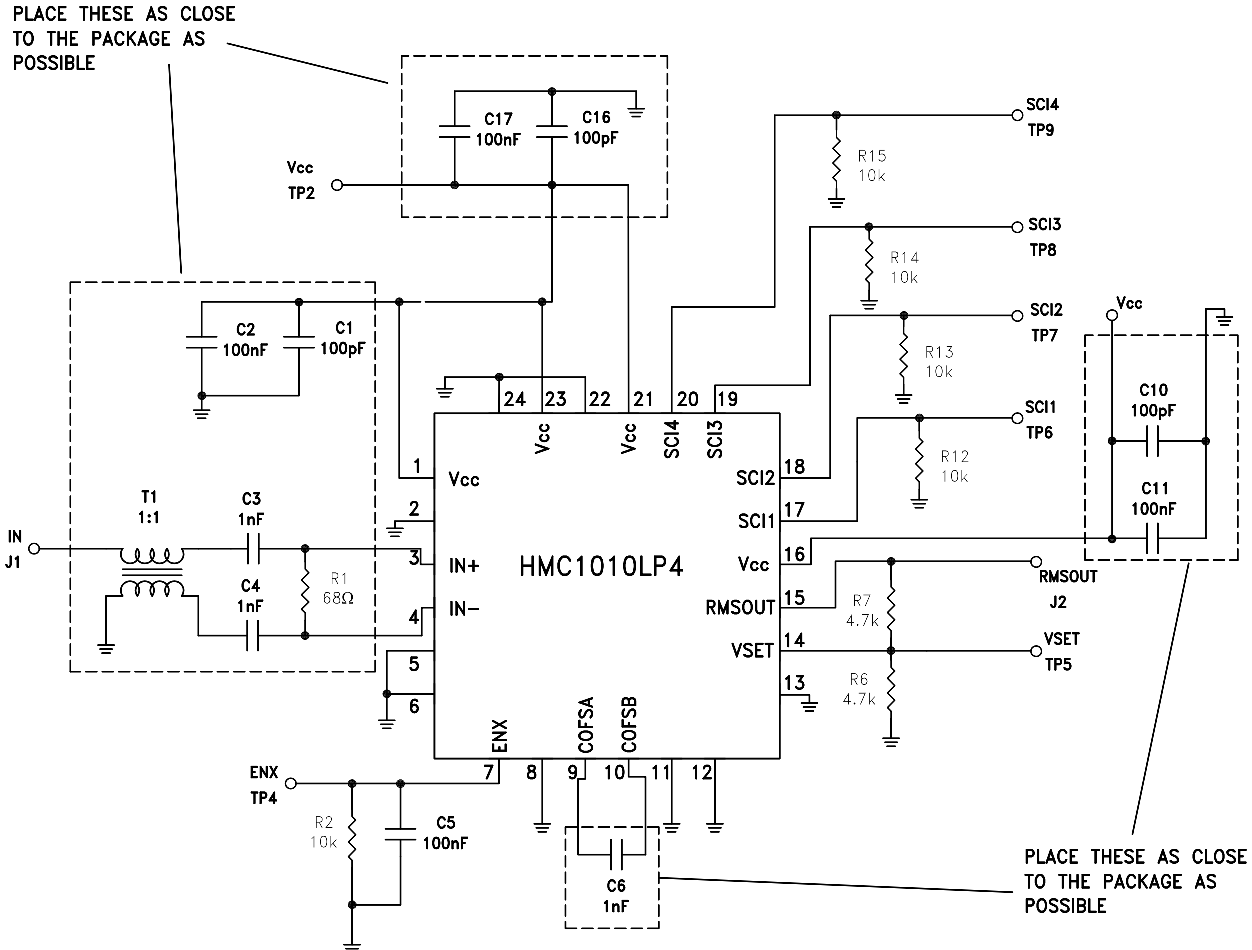
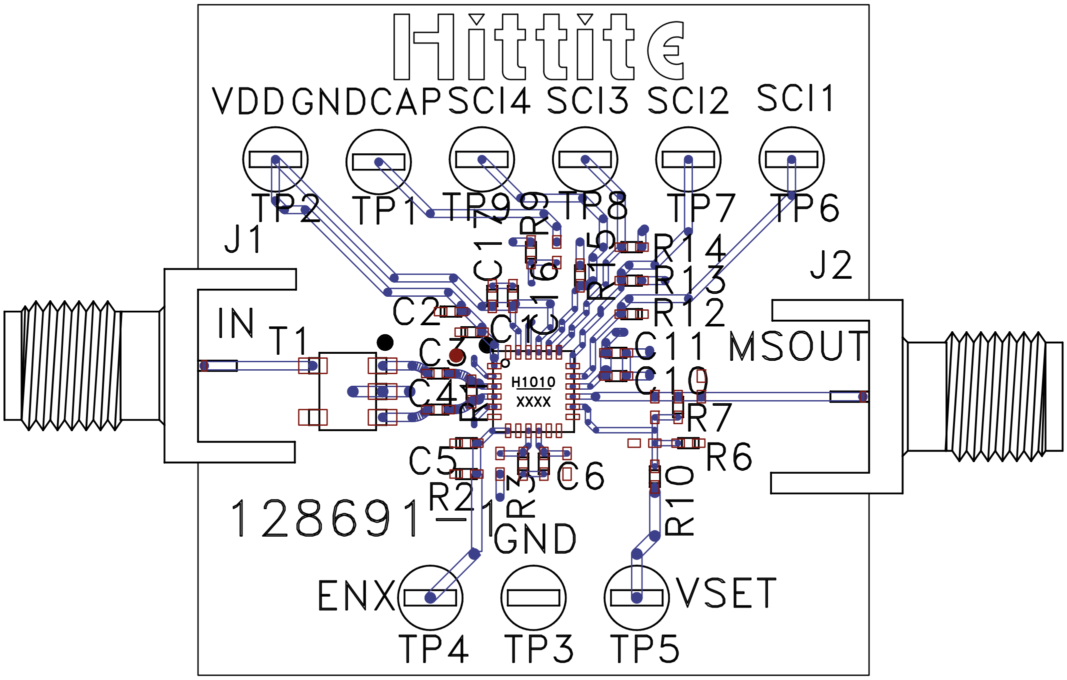
Application Circuit - Differential Configuration



Evaluation PCB - Differential Configuration



List of Materials for Evaluation PCB 128694 [1]

Item	Description
J1, J2	PC Mount SMA Connector
TP1 - TP9	DC Pin
C1, C10, C16	100 pF Capacitor, 0402 Pkg.
C3, C4, C6	1000 pF Capacitor, 0402 Pkg.
C2, C5, C11, C17	100 nF Capacitor, 0402 Pkg.
R1	68 Ohm Resistor, 0402 Pkg.
R2, R12 - R15	10 k Resistor, 0402 Pkg.
R3, R9, R10	0 Ohm Resistor, 0402 Pkg.
R6, R7	4.7 k Resistor, 0402 Pkg.
T1	1:1 Balun, M/A-COM ETC1-1-13
U1	HMC1010LP4E RMS Power Detector
PCB [2]	128691 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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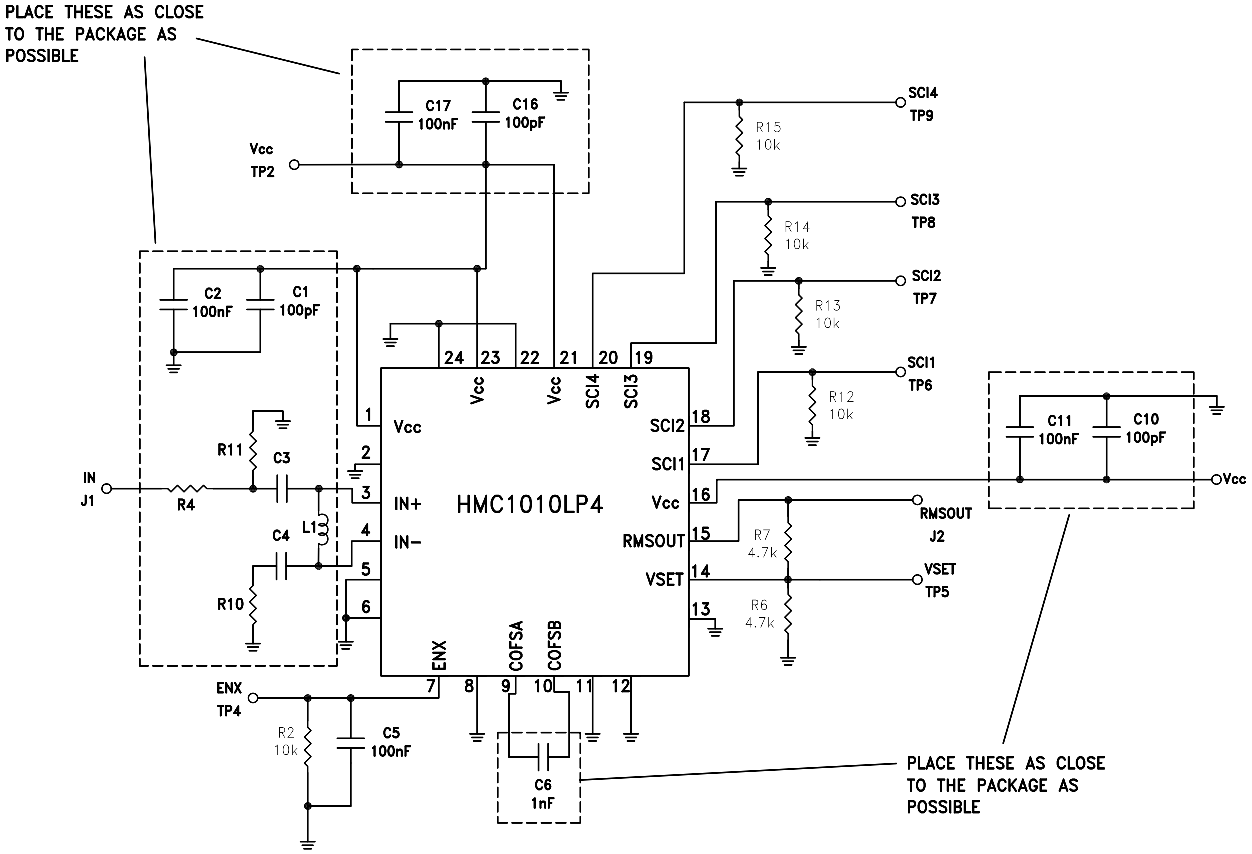
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D*

Application Circuit - Single-Ended Configuration, 900 MHz Tune



Note: For the values of C3, C4, R4, R10, R11, L1, refer to Single-Ended Input Interface in Application Information

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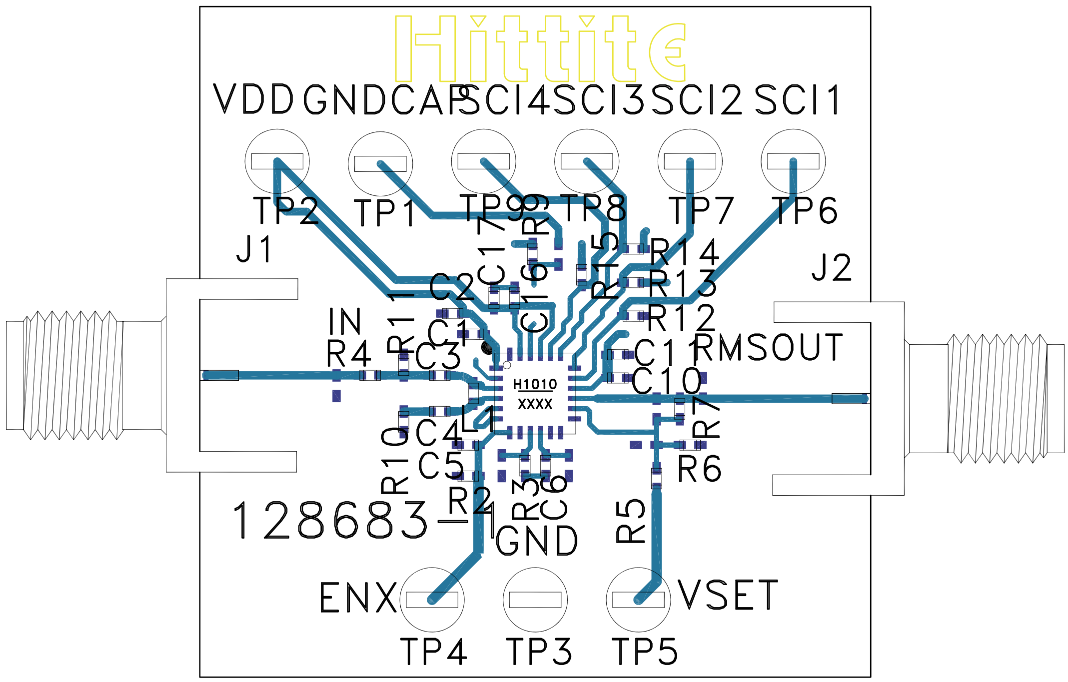
Evaluation PCB - Single-Ended Configuration, 900 MHz Tune



List of Materials for Evaluation PCB 130436 [1]

Item	Description
J1, J2	SMA Connector
TP1 - TP9	DC Pin
C1, C3, C10, C16	100 pF Capacitor, 0402 Pkg.
C2, C5, C11, C17	100 nF Capacitor, 0402 Pkg.
C4	5.6 pF Capacitor, 0402 Pkg.
C6	1000 pF Capacitor, 0402 Pkg.
R2, R12 - R15	10 k Resistor, 0402 Pkg.
R3, R5, R9, R10	0 Ohm Resistor, 0402 Pkg.
R4	27 Ohm Resistor, 0402 Pkg.
R6, R7	4.7 k Resistor, 0402 Pkg.
R11	82 Ohm Resistor, 0402 Pkg.
L1	6.8 nH Inductor, 0402 Pkg.
U1	HMC1010LP4E RMS Power Detector
PCB [3]	128683 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Board is configured with single-ended interface suitable for input signal frequencies at 900 MHz. Refer to section on tuning single-ended interface in application information for operating with signals at other frequencies.

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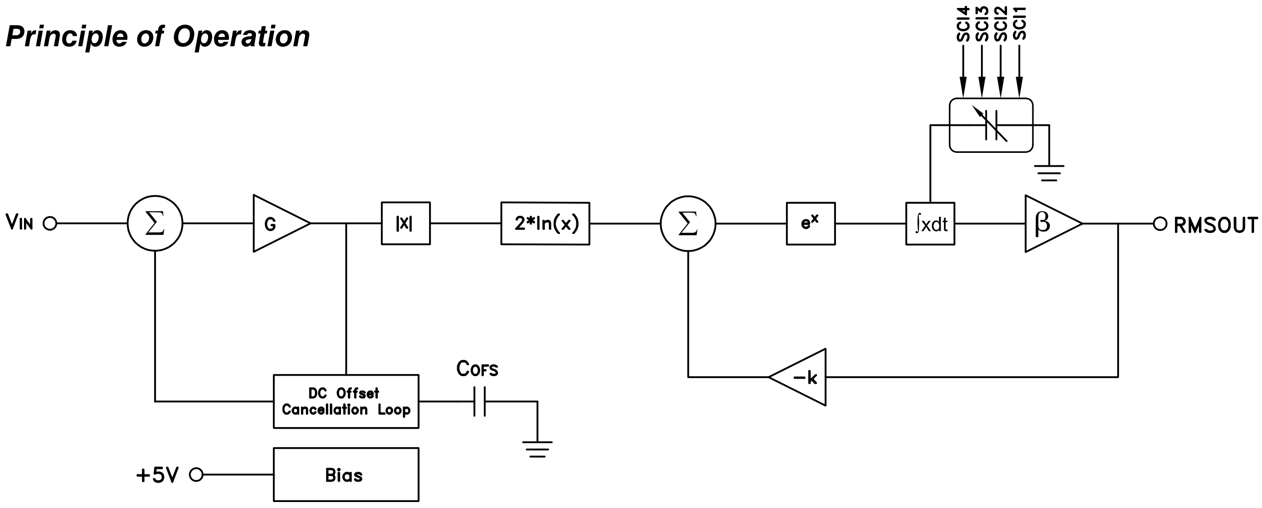
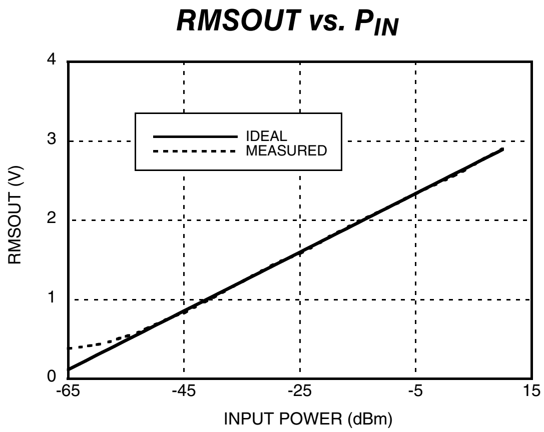
Application Information

Principle of Operation



$$RMSOUT = \frac{1}{k}\ln\left(\beta k G^2 \int V_{IN}^{\,2} dt\right)$$

P_{IN} = RMSOUT / [log-slope] + [log-intercept], dBm



Monolithic true-RMS detectors are in-effect analog calculators, calculating the RMS value of the input signal, unlike other types of power detectors which are designed to respond to the RF signal envelope. At the core of an RMS detector is a full-wave rectifier, log/antilog circuit, and an integrator. The RMS output signal is directly proportional to the logarithm of the time-average of V_{IN}^2. The bias block also contains temperature compensation circuits which stabilize output accuracy over the entire operating temperature range. The DC offset cancellation circuit actively cancels internal offsets so that even very small input signals can be measured accurately.

Configuration For The Typical Application

The RF input can be connected in differential configuration, or single-ended configuration: see “RF Input Interface” section for details on input configuration.

The RMS output signal is typically connected to VSET, through a resistive network providing a Pin -> RMSOUT transfer characteristic slope of 36.6mV/dBm (at 900 MHz), however the RMS output can be re-scaled to “magnify” a specific portion of the input sensing range, and to fully utilize the dynamic range of the RMS output. Refer to the section under the “log-slope and intercept” heading for details.

Due to part-to-part variations in log-slope and log-intercept, a system-level calibration is recommended to satisfy absolute accuracy requirements: refer to the “System Calibration” section for more details.

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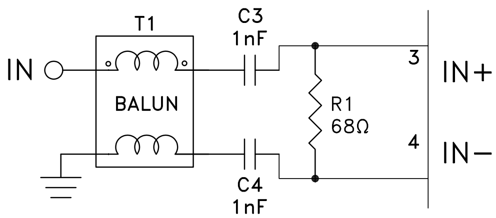
RF Input Interface

The IN+ and IN- pins are differential RF inputs, which can be externally configured with differential or single-ended input. Power match components are placed at these input terminals, along with DC blocking capacitors. The coupling capacitor values also set the lower spectral boundary of the input signal bandwidth.

Differential (Diff) Input Interface:



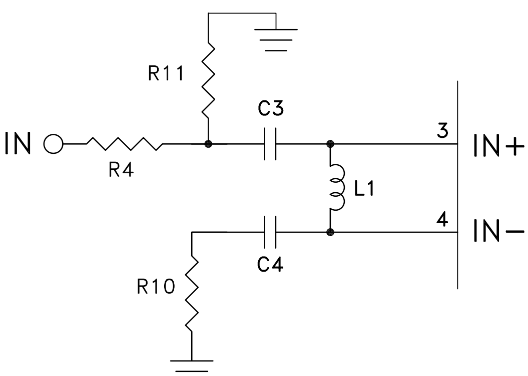
The value of R1 depends on the balun used; if the balun is 50Ω on both sides of the SE-Diff conversion, then

R1 = (150 * RM)/ (150 - RM) Ω, where

RM = the desired power match impedance in ohms

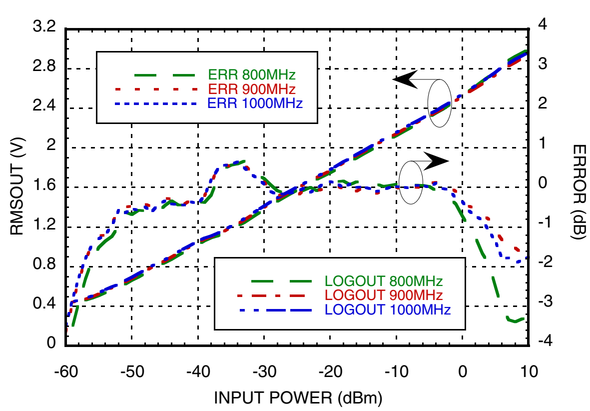
For RM = 50Ω, R1 = 75Ω ≈ 68Ω

Single-Ended (SE) Input Interface:



Tuned SE-interface for signal frequency = 900 MHz
Use R4 = 27Ω, R11 = 82Ω, C3 = 100 pF, L1=6.8nH, C4=5.6pF, R10 = 0Ω. Refer to application circuit for single-ended configuration on page 11-14.

RMSOUT & Error vs. Pin Using Tuned SE-Interface: 900 ± 100 MHz [1]



[1] CW input waveform.

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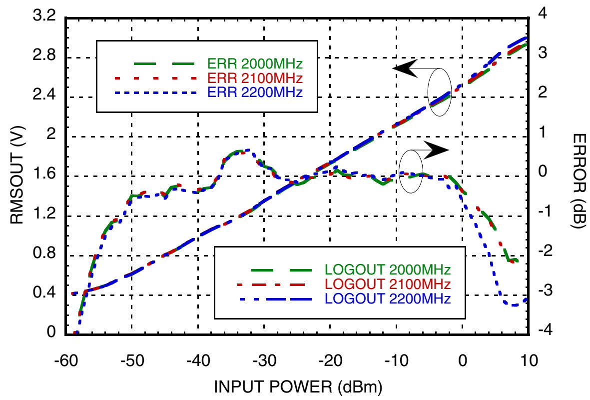
Tuned SE-interface for signal frequency = 2100 MHz
Use R4 = 27Ω, R11 = 82Ω, C3 = 100 pF, L1=2.4nH, C4=2pF, R10 = 0Ω. Refer to application circuit for single-ended configuration on page 11-14.

RMSOUT & Error vs. Pin Using Tuned SE-Interface: 2100 ± 100 MHz [1]



Please contact Hittite Customer Support for single-ended tuning for other signal frequencies.
A DC bias (Vcc-1.2V) is present on the IN+ and IN- pins, and should not be overridden

RMS Output Interface and Transient Response

The HMC1010LP4 features digital input pins (SCI1-SCI4) that control the internal integration time constant. Output transient response is determined by the digital integration controls, and output load conditions.

Shortest integration time is for SCI=0000, allowed longest integration time is for SCI=1100 (1101, 1110 and 1111 SCI settings are forbidden states).

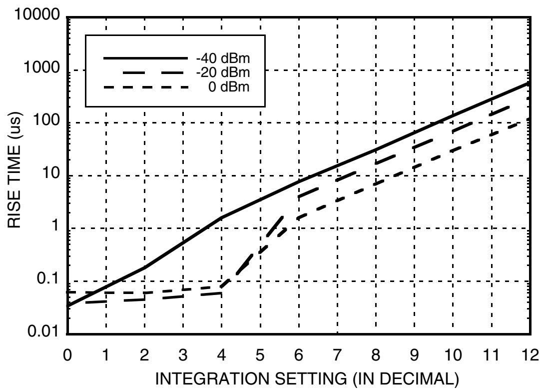
Using larger values of SCI will narrow the operating bandwidth of the integrator, resulting in a longer averaging time-interval and a more filtered output signal; however it will also slow the power detector's transient response. A larger SCI value favors output accuracy over speed. For the fastest possible transient settling times set SCI to 0000. This configuration will operate the integrator at its widest possible bandwidth, resulting in short averaging time-interval and an output signal with little filtering. Most applications will choose a SCI setting that maintains balance between speed and accuracy. Furthermore, error performance over modulation bandwidth is dependent on the SCI setting. For example modulations with relatively low frequency components and high crest factors may require higher SCI (integration) settings.

Table 1: Transient Response vs. SCI Setting[2]:

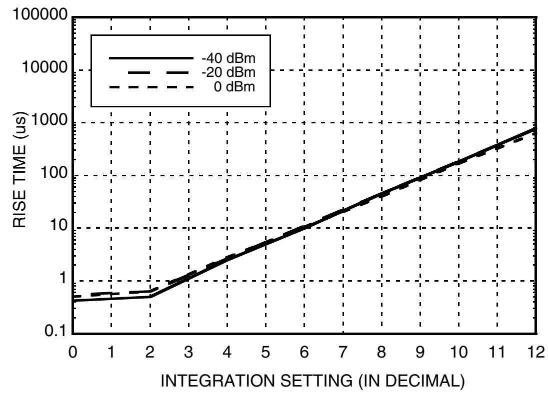
	RMSOUT Rise-Time 10% -> 90% (µs)			RMSOUT Rise Settling Time (µs)[3]			RMSOUT Fall-time 100% -> 10% (µs)		
SCI4,3,2,1	Pin = 0 dBm	Pin = -20 dBm	Pin = -40 dBm	Pin = 0 dBm	Pin = -20 dBm	Pin = -40 dBm	Pin = 0 dBm	Pin = -20 dBm	Pin = -40 dBm
0000	0.062	0.038	0.034	0.504	0.546	0.422	1.73	1.73	1.79
0010	0.06	0.045	0.18	0.63	0.63	0.495	5.55	5.55	5.85
0100	0.08	0.06	1.6	2.8	2.65	2.5	22.4	22.3	23.6
0110	1.6	4	7.7	10.5	11	10	93.5	91	96
1000	7	17	31	40	45	45	378	372	386
1010	30	70	138	170	184	182	1510	1510	1590
1100	120	300	580	630	770	780	6400	6400	6600

[1] CW input waveform.
[2] Input signal is 1900 MHz CW-tone switched on and off
[3] Measured from RF switching edge to 1dB (input referred) settling of RMSOUT.

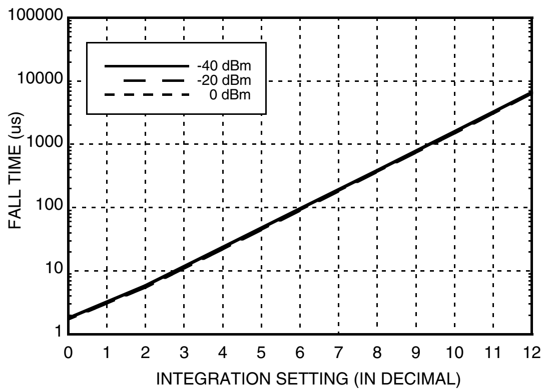
**Rise Time[1] vs.
SCI Setting over Input Power**



**Rise Settling Time [2] vs.
SCI Setting over Input Power**



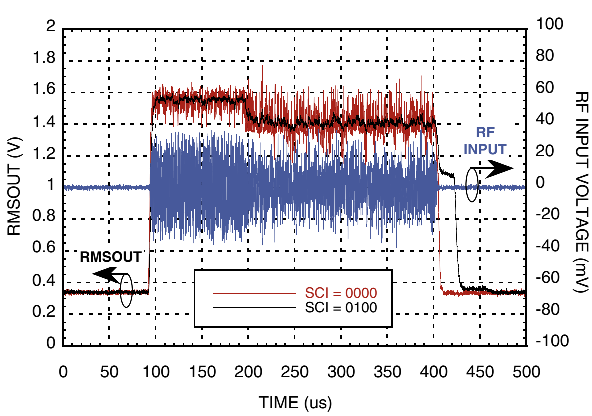
**Fall Time[3] vs.
SCI Setting over Input Power**



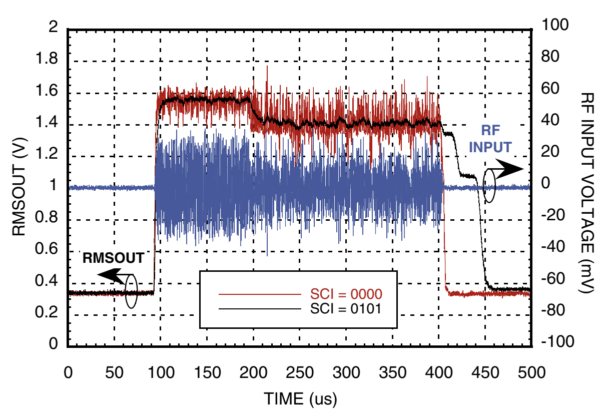
For increased load drive capability, consider a buffer amplifier on the RMS output. Using an integrating amplifier on the RMS output allows for an alternative treatment for faster settling times. An external amplifier optimized for transient settling can also provide additional RMS filtering, when operating HMC1010LP4E with a lower SCI value.

Following figures show how the peak-to-peak ripple decreases with higher SCI settings along with the RF pulse response over different modulations.

**Residual Ripple for 2.6 GHz WiMAX OFDM
Advanced 802.16 @ SCI = 0100**

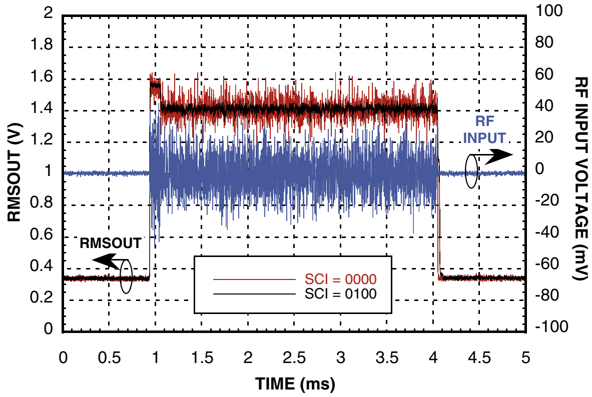


**Residual Ripple for 2.6 GHz WiMAX OFDM
Advanced 802.16 @ SCI = 0101**

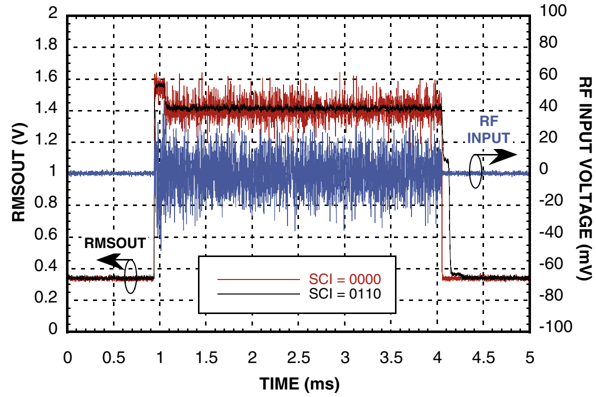


[1] Measured from 10% to 90%
[2] Measured from RF switching edge to 1dB (input referred) settling of RMSOUT.
[3] Measured from 100% to 10%

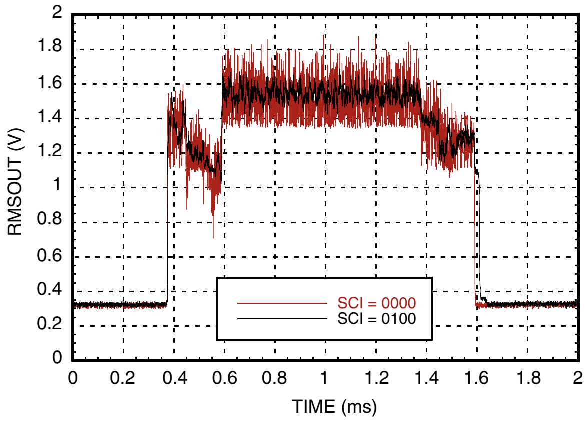
Residual Ripple for 2.6 GHz WiBRO @ SCI = 0100



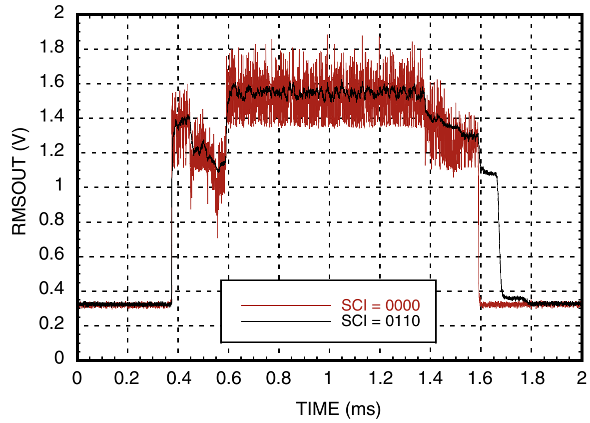
Residual Ripple for 2.6 GHz WiBRO @ SCI = 0110



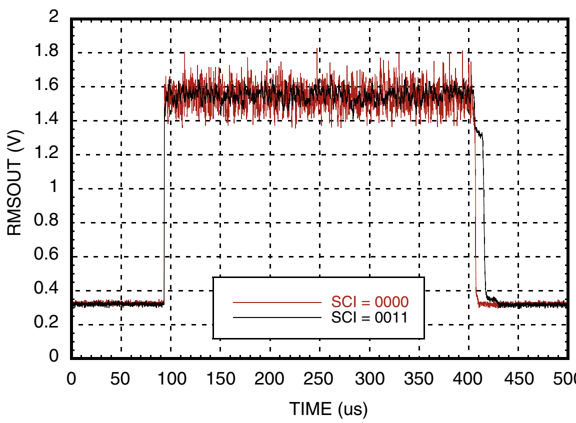
Residual Ripple for 2.6 GHz LTE Downlink @ SCI = 0100



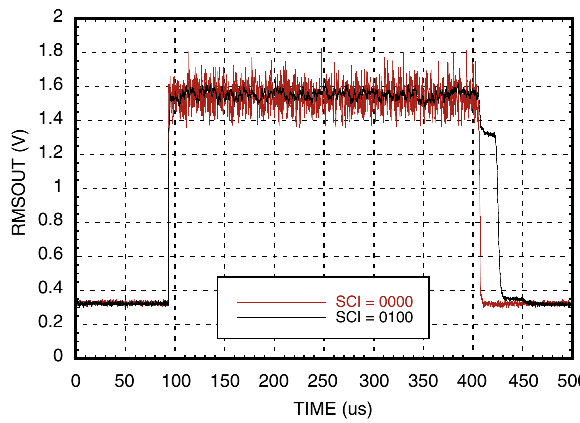
Residual Ripple for 2.6 GHz LTE Downlink @ SCI = 0110



Residual Ripple for 2.6 GHz WCDMA @ SCI = 0011



Residual Ripple for 2.6 GHz WCDMA @ SCI = 0100



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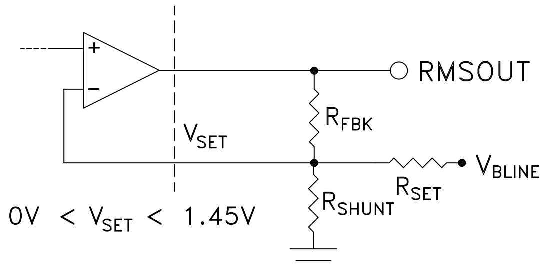
LOG-Slope and Intercept

The HMC1010LP4 provides for an adjustment of output scale with the use of an integrated operational amplifier. Logslope and intercept can be adjusted to “magnify” a specific portion of the input sensing range, and to fully utilize the dynamic range of the RMS output.

A log-slope of 37.3 mV/dB (@1900 MHz) is set by connecting RMS Output to VSET through resistor network for ß = 1 (see application schematic).

The log-slope is adjusted by applying the appropriate resistors on the RMS and VSET pins. Log-intercept is adjusted by applying a DC voltage to the VSET pin.



Optimized slope = ß * log-slope

Optimized intercept = log-intercept – (R_{FBK} /R_{SET}) * VBLINE

$$\beta = \frac{R_{FBK}}{R_{FBK} \,//\, R_{SHUNT} \,//\, R_{SET}}$$

When R_{FBK}=0 to set RMSOUT=VSET, then ß=1/2

If RSET is not populated, then ß = ½ * (RFBK/ (RFBK // RSHUNT)) and intercept is at nominal value.

Example: The logarithmic slope can be simply increased by choosing appropriate RFBK and RSHUNT values while not populating the RSET resistor on the evaluation board to keep the intercept at nominal value.

Setting RFBK =4.7KΩ and RSHUNT = 2.2KΩ results in an optimized slope of:

Optimized Slope = ß * log_slope = 1.57* 37.3mV / dB

Optimized Slope = 58 mV / dB

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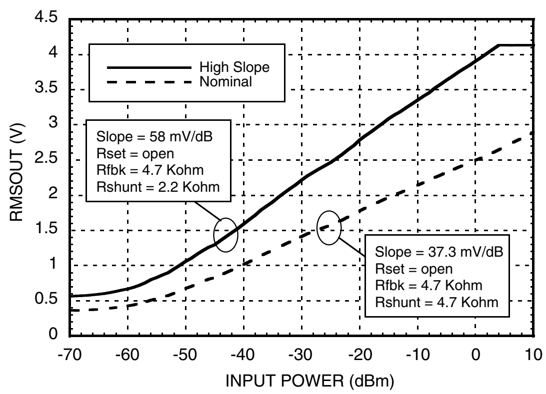
Slope Adjustment



Example: The logarithmic intercept can also be adjusted by choosing appropriate RFBK, RSHUNT, and RSET values.

Setting RFBK = 4.7KΩ, RSHUNT =2.2KΩ, and RSET = 24KΩ results in an optimized slope of:

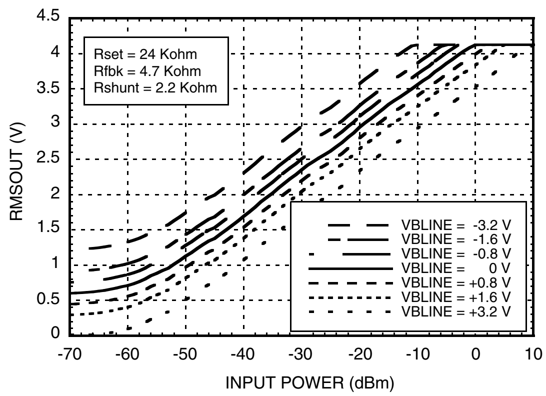
Optimized Slope = ß * log_slope = 1.67 * 37.3 mV / dB

Optimized Slope = 62 mV / dB

Optimized Intercept = log_intercept –(RFBK/RSET)*VBLINE

Optimized Intercept = log_intercept - 0.196 * VBLINE

Intercept Adjustment



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DC Offset Compensation Loop

Internal DC offsets, which are input signal dependant, require continuous cancellation. Offset cancellation is a critical function needed for maintenance of measurement accuracy and sensitivity. The DC offset cancellation loop performs this function, and its response is largely defined by the capacitance (COFS) connected between COFSA, COFSB pins.

COFS sets the loop bandwidth of the DC offset compensations. Higher COFS values are required for measuring lower RF frequencies. The optimal loop bandwidth setting will allow internal offsets to be cancelled at a minimally acceptable speed.

DC Offset Cancellation Loop $\approx \frac{1}{\pi(5000)(C_{OFS}+20\times10^{12})}$ Bandwidth , Hz

For example: loop bandwidth for DC cancellation with COFS = 1nF, bandwidth is ~62 kHz

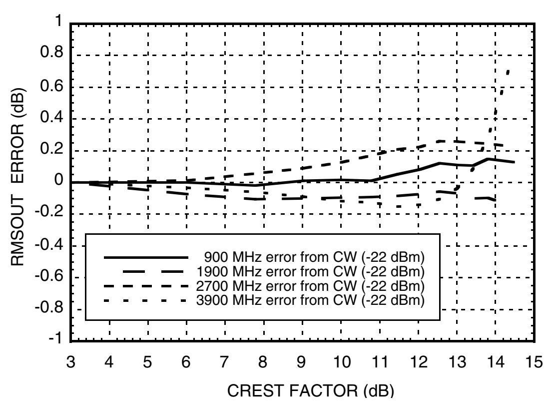
Standby Mode

The ENX can be used to force the power detector into a low-power standby mode. As ENX is deactivated, power is restored to all of the circuits. There is no memory of previous conditions. Coming-out of stand-by, internal integration and COFS capacitors will require recharging, so if large SCI values have been chosen, the wake-up time will be lengthened.

Modulation Performance – Crest factor performance

The HMC1010LP4E can detect modulated signals with very high crest factors accurately.
For example, up to 2.7 GHz, a modulated RF signal with a crest factor of 15 dB can be detected with 0.2 dB error.

**RMSOUT Error vs.
Crest Factor over Frequency**



System Calibration

Due to part-to-part variations in log-slope and log-intercept, a system-level calibration is recommended to satisfy absolute accuracy requirements. When performing this calibration, choose at least two test points: near the top end and bottom-end of the measurement range. It is best to measure the calibration points in the regions (of frequency and amplitude) where accuracy is most important. Derive the log-slope and log-intercept, and store them in non-volatile memory.

For example if the following two calibration points were measured at 2.2 GHz:

With RMSOUT = 2.321V at Pin= -5 dBm,
and RMSOUT = 0.809V at Pin= -45 dBm
slope calibration constant = SCC
SCC = (-45+5)/(0.809-2.321) = 26.45 dB/V
intercept calibration constant = ICC
ICC = Pin – SCC*RMSOUT = -5 – 26.45 * 2.321 = -66.39 dBm

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Now performing a power measurement at -25 dBm:

RMSOUT measures 1.559V
[Measured Pin] = [Measured RMSOUT]*SCC + ICC
[Measured Pin] = 1.559*26.45 – 66.39 = -25.155 dBm
An error of only 0.155 dB

Factory system calibration measurements should be made using an input signal representative of the application. If the power detector will operate over a wide range of frequencies, choose a central frequency for calibration.

Layout Considerations

- Mount RF input coupling capacitors close to the IN+ and IN- pins.
- Solder the heat slug on the package underside to a grounded island which can draw heat away from the die with low thermal impedance. The grounded island should be at RF ground potential.
- Connect power detector ground to the RF ground plane, and mount the supply decoupling capacitors close to the supply pins.

Definitions

- Log-slope: slope of P_{IN} –> RMSOUT transfer characteristic. In units of mV/dB
- Log-intercept: x-axis intercept of P_{IN} –> RMSOUT transfer characteristic. In units of dBm.
- RMS Output Error: The difference between the measured P_{IN} and actual P_{IN} using a line of best fit.
  [measured_P_{IN}] = [measured_ RMSOUT] / [best-fit-slope] + [best-fit-intercept], dBm
- Input Dynamic Range: the range of average input power for which there is a corresponding RMS output voltage with “RMS Output Error” falling within a specific error tolerance.
- Crest Factor: Peak power to average power ratio for time-varying signals.

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