600mA Main/Camera LED Controller

FEATURES

- **Multimode Charge Pump Provides Up to 94% Efficiency (1x, 1.5x, 2x)**
- **Up to 600mA Total Output Current**
- **LTC3209-1: 8 Current Sources Available as 6×25mA MAIN, 1×400mA CAM and 1×15mA AUX**
- **LTC3209-2: 8 Current Sources Available as 5×25mA MAIN, 2×200mA CAM and 1×15mA AUX**
- **LED On/Off and Brightness Level Programmable Using 2-Wire I²C™ Interface**
- Automatic Charge Pump Mode Switching or Fixed Mode for Power Supply Generation
- Low Noise Constant Frequency Operation*
- Internal Soft-Start Limits Inrush Current During Start-up and Mode Switching
- Short Circuit/Thermal/Open-Shorted LED Protection
- 256 Brightness States for MAIN Display
- 16 Brightness States for CAM Display
- 4 Brightness States for AUX Display
- 20-Lead (4mm × 4mm) QFN Package

APPLICATIONS

- Video/Camera Phones with QVGA+ Displays

DESCRIPTION

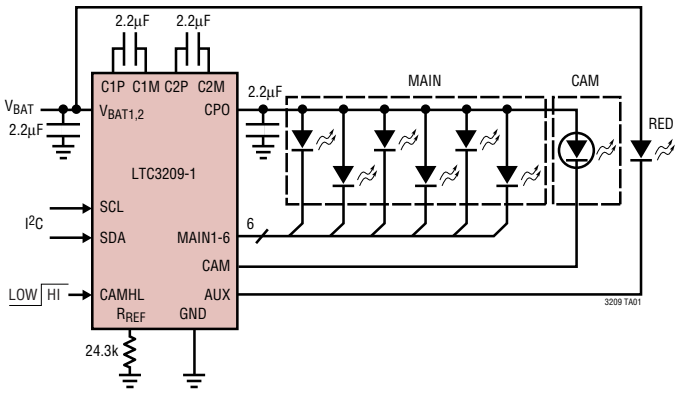
The LTC®3209-1/LTC3209-2 are highly integrated multidisplay LED controllers. These parts contain a high efficiency, low noise charge pump to provide power to MAIN, CAM and AUX LED displays. The LTC3209-1/LTC3209-2 require only four small ceramic capacitors and one current set resistor to form a complete LED power supply and current controller.

The maximum display currents are set by a single external resistor. Current for each LED is controlled by a precision internal current source. Dimming and On/Off for all displays is achieved via the I²C serial interface. 256 states are available for the MAIN display. Sixteen states are available for the CAM display and four states are available for the AUX display.

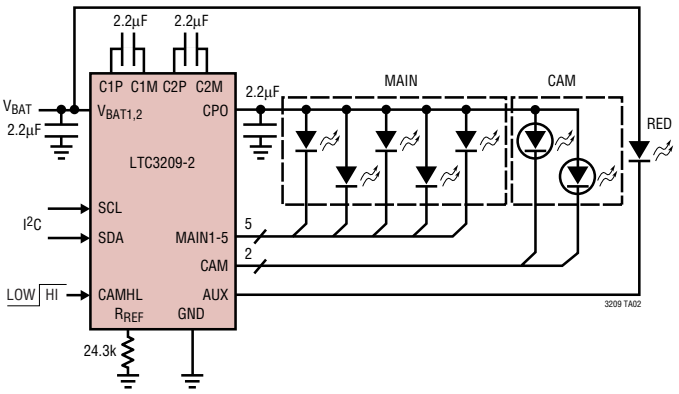
The charge pump optimizes efficiency based on the voltage across the LED current sources. The part powers up in 1x mode and will automatically switch to boost mode whenever any enabled MAIN or CAM LED current source begins to enter dropout. The first dropout switches the part into 1.5x mode and a subsequent dropout switches the part into 2x mode. The part resets to 1x mode whenever a data bit is updated via the I²C port. The parts are available in a 4mm × 4mm 20-lead QFN package.

TYPICAL APPLICATION

LTC3209-1 6 MAIN/1 CAM Operation



LTC3209-2 5 MAIN/2 CAM Operation

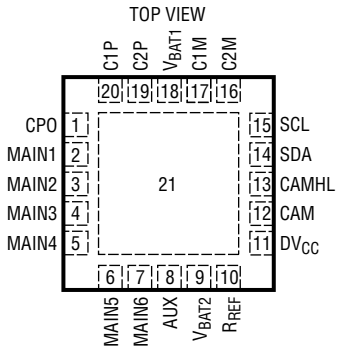


ABSOLUTE MAXIMUM RATINGS

(Note 1)

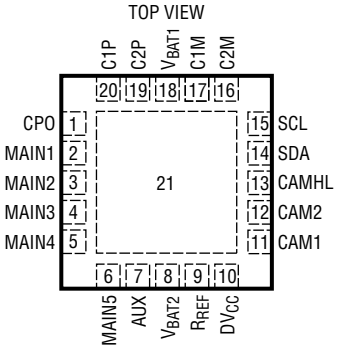
V_{BAT}, DV_{CC}, CPO to GND ..... –0.3 to 6V
SDA, SCL, CAMHL ..... –0.3V to (DV_{CC} + 0.3V)
I_{CPO} (Note 4) 700mA
$I_{MAIN1-6}$ (Note 5) 31mA
I_{AUX} (Note 5) 30mA
I_{CAM1-2} (Note 5) 250mA
I_{CAM} (Note 5) 500mA
CPO, R_{REF} Short-Circuit Duration ..... Indefinite
Operating Temperature Range (Note 2) .. –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C

PACKAGE/ORDER INFORMATION



UF PACKAGE
20-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 40°C/W
EXPOSED PAD IS GND (PIN 21), MUST BE SOLDERED TO PCB



UF PACKAGE
20-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 40°C/W
EXPOSED PAD IS GND (PIN 21), MUST BE SOLDERED TO PCB

ORDER PART NUMBER	UF PART MARKING	ORDER PART NUMBER	UF PART MARKING
LTC3209EUF-1	32091	LTC3209EUF-2	32092

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. $V_{BAT1,2}$ = 3.6V, DV_{CC} = 3V, R_{REF} = 24.3k, C1 = C2 = C3 = C4 = 2.2µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{BAT} Operating Voltage		●	2.9		4.5	V
I_{VBAT} Operating Current	I_{CPO} = 0, 1x Mode, LED Disabled I_{CPO} = 0, 1.5x Mode I_{CPO} = 0, 2x Mode			0.4 2.7 4.5		mA mA mA
V_{BAT} UVLO Threshold				1.5		V
DV_{CC} Operating Voltage		●	1.5		4.5	V
DV_{CC} Operating Current	DV_{CC} = 1.8V, Serial Port Idle	●			1	µA
DV_{CC} UVLO Threshold				1		V
V_{BAT} Shutdown Current	DV_{CC} = 3V	●		3	7	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. $V_{BAT1,2}$ = 3.6V, DV_{CC} = 3V, R_{REF} = 24.3k, C1 = C2 = C3 = C4 = 2.2µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
White LED Current (MAIN1-6), 8-Bit Linear DAC						
Full-Scale LED Current	MAIN = 1V	●	25	28	31	mA
Minimum (1LSB) LED Current	MAIN = 1V			110		µA
LED Current Matching	Any Two MAIN Outputs at 50% FS			1		%
LED Dropout Voltage	Mode Switch Threshold, I_{MAINx} = FS			180		mV
White LED Current (CAM), LTC3209-1, 4-Bit Linear DAC						
Full-Scale LED Current	CAM = 1V	●	360	400	440	mA
Minimum (1LSB) LED Current	CAM = 1V			26.8		mA
LED Dropout Voltage	Mode Switch Threshold, I_{CAM} = FS			400		mV
White LED Current (CAM1-2), LTC3209-2, 4-Bit Linear DAC						
Full-Scale LED Current	CAM = 1V	●	180	200	220	mA
Minimum (1LSB) LED Current	CAM = 1V			13.3		mA
LED Current Matching	CAM1-2 at 50% FS			1		%
LED Dropout Voltage	Mode Switch Threshold, I_{CAM} = FS			400		mV
AUX LED Current, 2-Bit Linear DAC						
Full-Scale LED Current	AUX = 1V	●	12.5	13.75	15	mA
Minimum (1LSB) LED Current	AUX = 1V			4.4		mA
V_{OL}	I_{AUX} = 1mA; C0, C1 = High			18		mV
Charge Pump (CPO)						
1x Mode Output Impedance				0.5		Ω
1.5x Mode Output Impedance	V_{BAT} = 3V, V_{CPO} = 4.2V (Note 3)			2.7		Ω
2x Mode Output Impedance	V_{BAT} = 3V, V_{CPO} = 4.8V (Note 3)			3.2		Ω
CPO Voltage Regulation	1.5x Mode, I_{CPO} = 2mA 2x Mode, I_{CPO} = 2mA			4.6 5.1		V V
CLOCK Frequency				0.85		MHz
SDA, SCL, CAMHL						
V_{IL} (Low Level Input Voltage)		●			0.3 • DV_{CC}	V
V_{IH} (High Level Input Voltage)		●	0.7 • DV_{CC}			V
V_{OL}, Digital Output Low (SDA)	I_{PULLUP} = 3mA	●		0.16	0.4	V
I_{IH}	SDA, SCL, CAMHL = DV_{CC}	●	–1		1	µA
I_{IL}	SDA, SCL, CAMHL = 0V	●	–1		1	µA
Serial Port Timing (Notes 6, 7)						
t_{SCL}	Clock Operating Frequency				400	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition		1.3			µs
$t_{HD,STA}$	Hold Time After (Repeated) Start Condition		0.6			µs
$t_{SU,STA}$	Repeated Start Condition Setup Time		0.6			µs
$t_{SU,STO}$	Stop Condition Setup Time		0.6			µs
$t_{HD,DAT(OUT)}$	Data Hold Time		0		900	ns
$t_{HD,DAT(IN)}$	Input Data Hold Time		0			ns
$t_{SU,DAT}$	Data Setup Time		100			ns
t_{LOW}	Clock Low Period		1.3			µs
t_{HIGH}	Clock High Period		0.6			µs
t_f	Clock Data Fall Time		20		300	ns
t_r	Clock Data Rise Time		20		300	ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. $V_{BAT1,2}$ = 3.6V, DV_{CC} = 3V, R_{REF} = 24.3k, C1 = C2 = C3 = C4 = 2.2µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SP}	Spike Suppression Time		50			ns
R_{REF}						
VR_{REF}	R_{REF} = 24.3k	●	1.20	1.23	1.26	V
RR_{REF}	Reference Resistor Range		20		30	kΩ

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3209-1/LTC3209-2 are guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C ambient operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: 1.5x mode output impedance is defined as $(1.5V_{BAT} – V_{CPO})/I_{OUT}$. 2x mode output impedance is defined as $(2V_{BAT} – V_{CPO})/I_{OUT}$.

Note 4: Based on long term current density limitations. Assumes an operating duty cycle of ≤ 10% under absolute maximum conditions for duration less than 10 seconds. Max Charge Pump current for continuous operation is 300mA.

Note 5: Based on long term current density limitations.

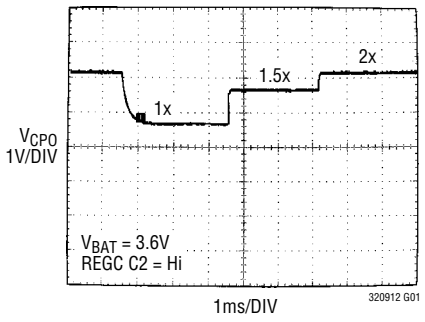
Note 6: All values are referrenced to V_{IH} and V_{IL} levels.

Note 7: Guaranteed by design.

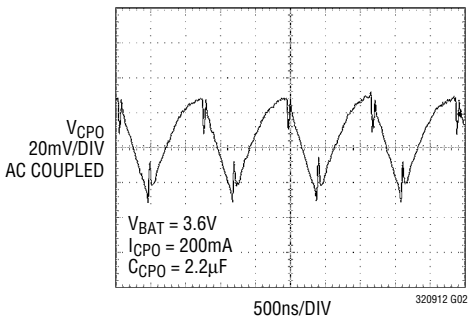
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C unless otherwise noted

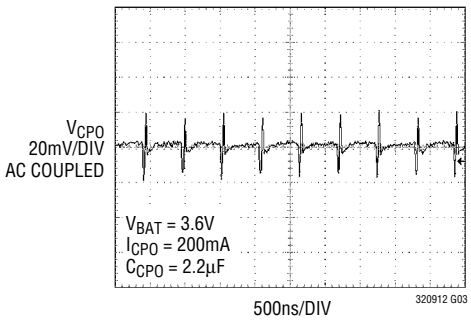
Mode Switch Fast Dropout Times



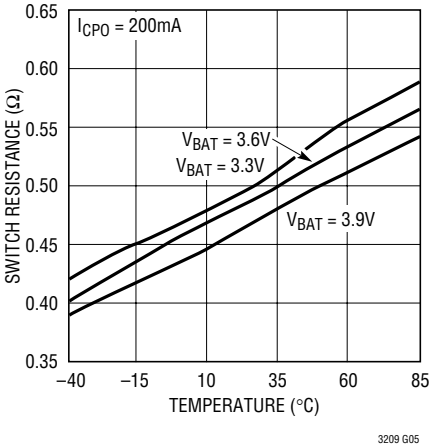
1.5x Mode CPO Ripple



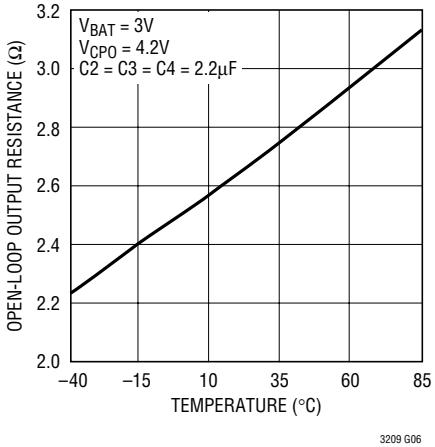
2x Mode CPO Ripple



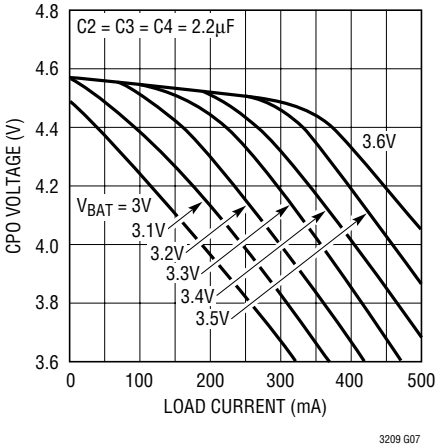
1x Mode Switch Resistance vs Temperature



1.5x Mode Charge Pump Open-Loop Output Resistance vs Temperature $(1.5V_{BAT}–V_{CPO})/I_{CPO}$

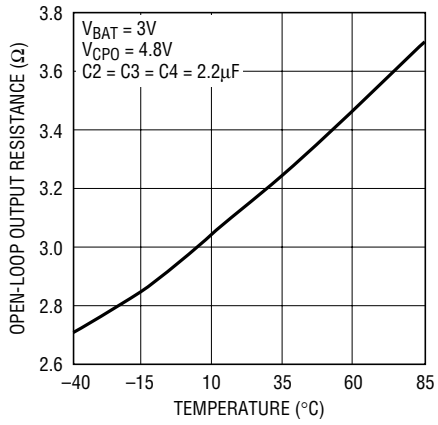


1.5x Mode CPO Voltage vs Load Current



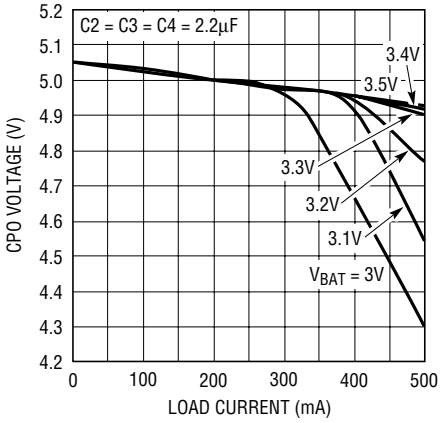
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted

2x Mode Charge Pump Open-Loop Output Resistance vs Temperature $(2V_{BAT}–V_{CPO})/I_{CPO}$



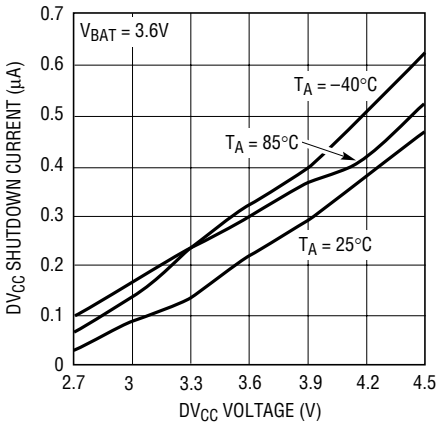
3209 G08

2x Mode CPO Voltage vs Load Current



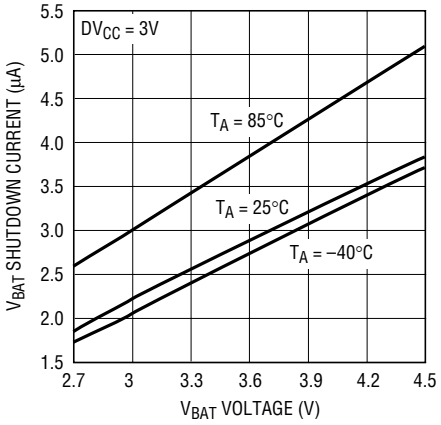
3209 G09

DV_{CC} Shutdown Current vs DV_{CC} Voltage



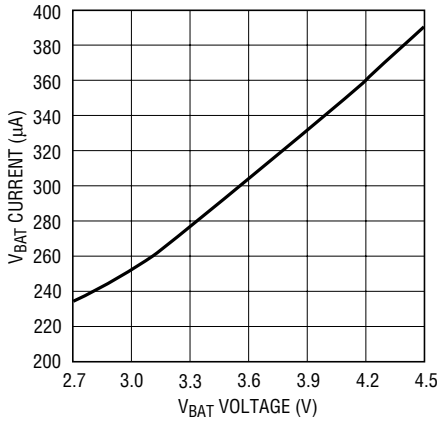
3209 G11

V_{BAT} Shutdown Current vs V_{BAT} Voltage



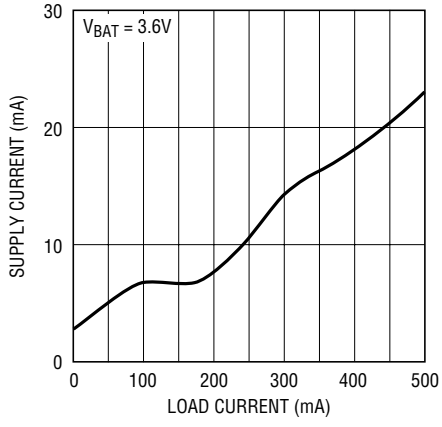
3209 G12

1x Mode No Load V_{BAT} Current vs V_{BAT} Voltage



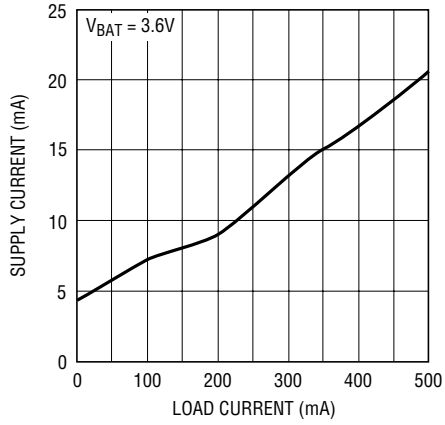
3209 G13

1.5x Mode Supply Current vs I_{CPO} $(I_{VBAT}–1.5I_{CPO})$



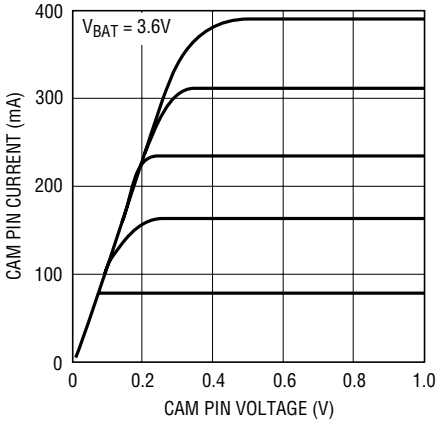
3209 G14

2x Mode Supply Current vs I_{CPO} $(I_{VBAT}–2I_{CPO})$



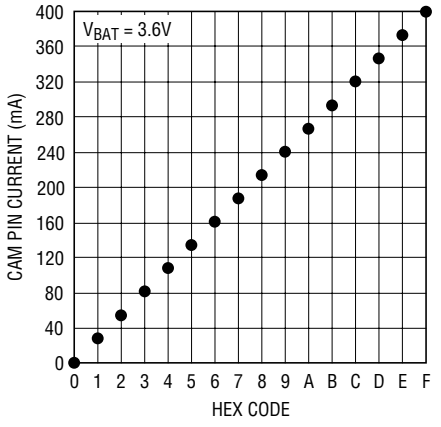
3209 G15

LTC3209-1 CAM Pin Current vs CAM Pin Voltage



3209 G22

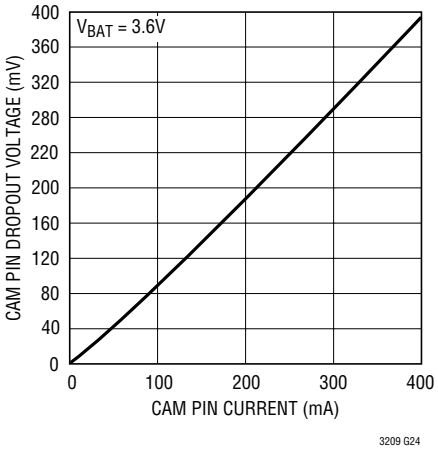
LTC3209-1 CAM Pin Current vs Input Code



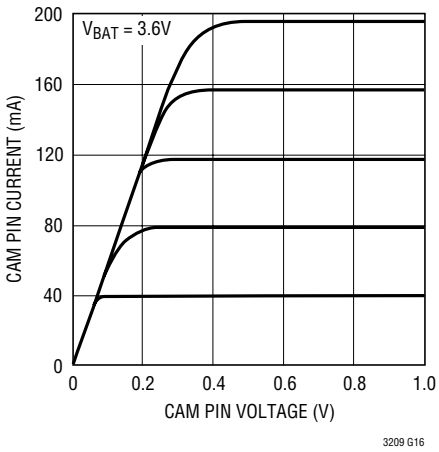
3209 G23

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted

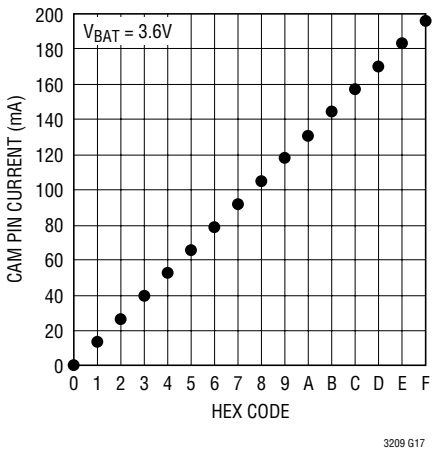
LTC3209-1 CAM Pin Dropout Voltage vs CAM Pin Current



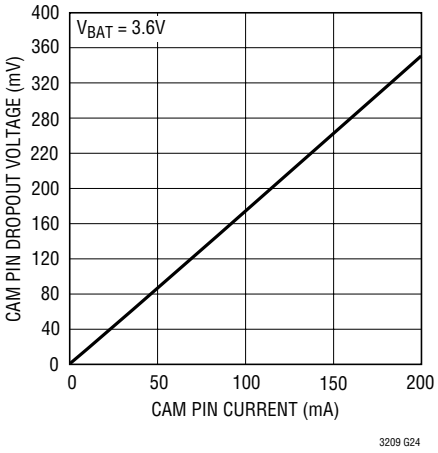
LTC3209-2 CAM Pin Current vs CAM Pin Voltage



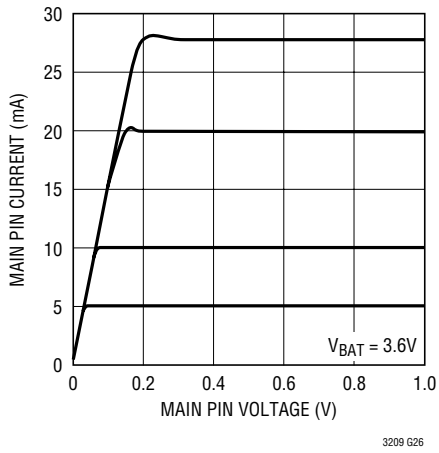
LTC3209-2 CAM Pin Current vs Input Code



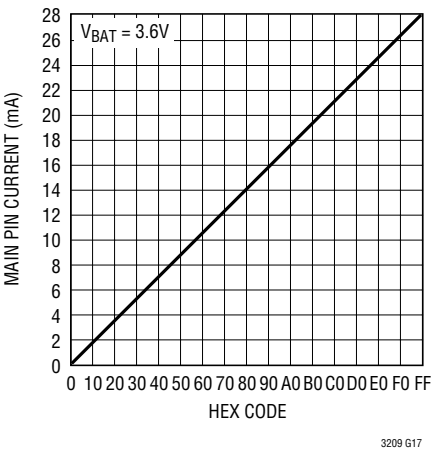
LTC3209-2 CAM Pin Dropout Voltage vs CAM Pin Current



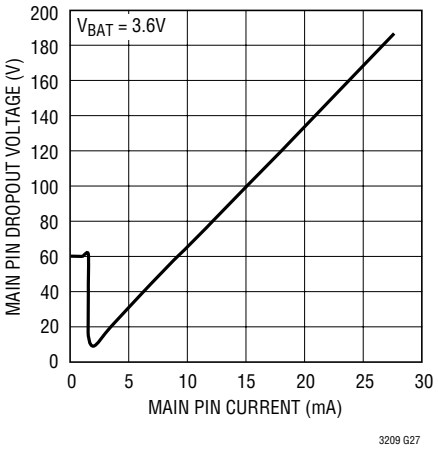
MAIN Pin Current vs MAIN Pin Voltage



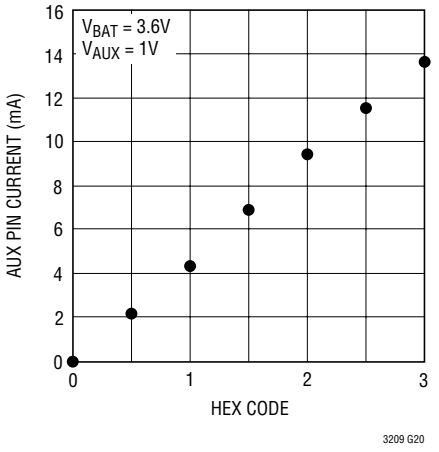
MAIN Pin Current vs Input Code



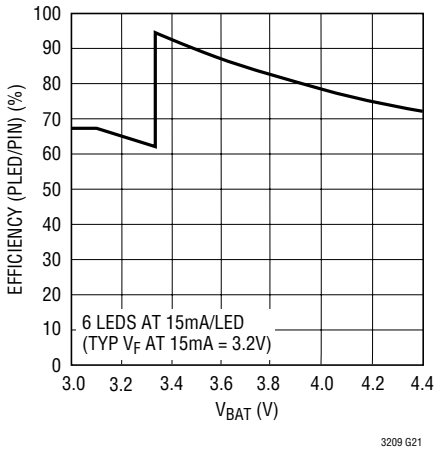
MAIN Pin Dropout Voltage vs MAIN Pin Current



AUX Pin Current vs Input Code



6-LED MAIN Display Efficiency vs V_{BAT}



PIN FUNCTIONS (LTC3209-1/LTC3209-2)

CPO (Pin 1/Pin 1): Output of the Charge Pump Used to Power LEDs. A 2.2µF X5R or X7R ceramic capacitor should be connected to ground.

MAIN1-6 (Pins 2, 3, 4, 5, 6, 7, LTC3209-1): Current Source Outputs for the MAIN Display White LEDs. The LEDs on the MAIN display can be set from 0mA to 28mA in 256 steps via software control and internal 8-bit linear DAC. Each output can be disabled externally by connecting the output to CPO. Setting data in REGA to 0 disables all MAIN outputs.

MAIN1-5 (Pins 2, 3, 4, 5, 6, LTC3209-2): Current Source Outputs for the MAIN Display White LEDs. The LEDs on the MAIN display can be set from 0mA to 28mA in 256 steps via software control and internal 8-bit linear DAC. Each output can be disabled externally by connecting the output to CPO. Setting data in REGA to 0 disables all MAIN outputs.

AUX (Pin 8/Pin 7): Current Source Output for the AUX Display LED. The LED current source can be set from 0mA to 13.75mA in 4 steps via software control and internal 2-bit DAC. AUX does not have dropout sensing and cannot be disabled by connecting to CPO. This pin can also be used as an I^2C controlled general purpose output.

$V_{BAT2,1}$ (Pins 9, 18/Pins 8, 18): Supply Voltage for the Entire Device. Two separate pins are used to isolate the charge pump from the analog sections to reduce noise. Both pins must be connected together externally and bypassed with a single 2.2µF low ESR ceramic capacitor close to V_{BAT1}. V_{BAT2} may require a 0.1µF capacitor.

R_{REF} (Pin 10/Pin 9): This pin controls the maximum amount of LED current for all displays. The R_{REF} voltage is 1.23V. An external 24.3k resistor to ground sets the reference currents for all display DACs and support circuits for nominal MAIN full-scale current of 28mA and total CAM full-scale current of 400mA. The value for R_{REF} is limited to a range of 20k to 30k.

DV_{CC} (Pin 11/Pin 10): Supply Voltage for All Digital I/O Lines. This pin sets the logic reference level of the LTC3209-1/LTC3209-2. Decouple DV_{CC} to GND with a 0.1µF capacitor. A UVLO circuit on the DV_{CC} pin forces all registers to all 0s whenever DV_{CC} is below the UVLO threshold.

CAM1-2 (Pins 11, 12, LTC3209-2): Current Source Outputs for the CAM1 and CAM2 Display White LEDs. The LEDs on the two CAM displays can each be set from 0mA to 200mA in 16 steps via software control and internal 4-bit linear DAC. Two 4-bit registers are available. One is used to program the high camera current and the second the low camera current. These registers can be selected via the serial port or the CAMHL pin. Each output can be disabled by connecting the output to CPO. Setting data in REGB to 0 disables both CAM outputs. (See Applications Information).

CAM (Pin 12, LTC3209-1): Current Source Output for the CAM Display White LED. The LED on the CAM display can be set from 0mA to 400mA in 16 steps via software control and internal 4-bit linear DAC. Two 4-bit registers are available. One is used to program the high camera current and the second the low camera current. These registers can be selected via the serial port or the CAMHL pin. Each output can be disabled by connecting the output to CPO. Setting data in REGB to 0 disables the CAM output. (See Applications Information).

CAMHL (Pin 13/Pin 13): This pin selects CAM high current register when asserted high and CAM low current register when low. The high to low transition automatically resets the charge pump mode to 1x.

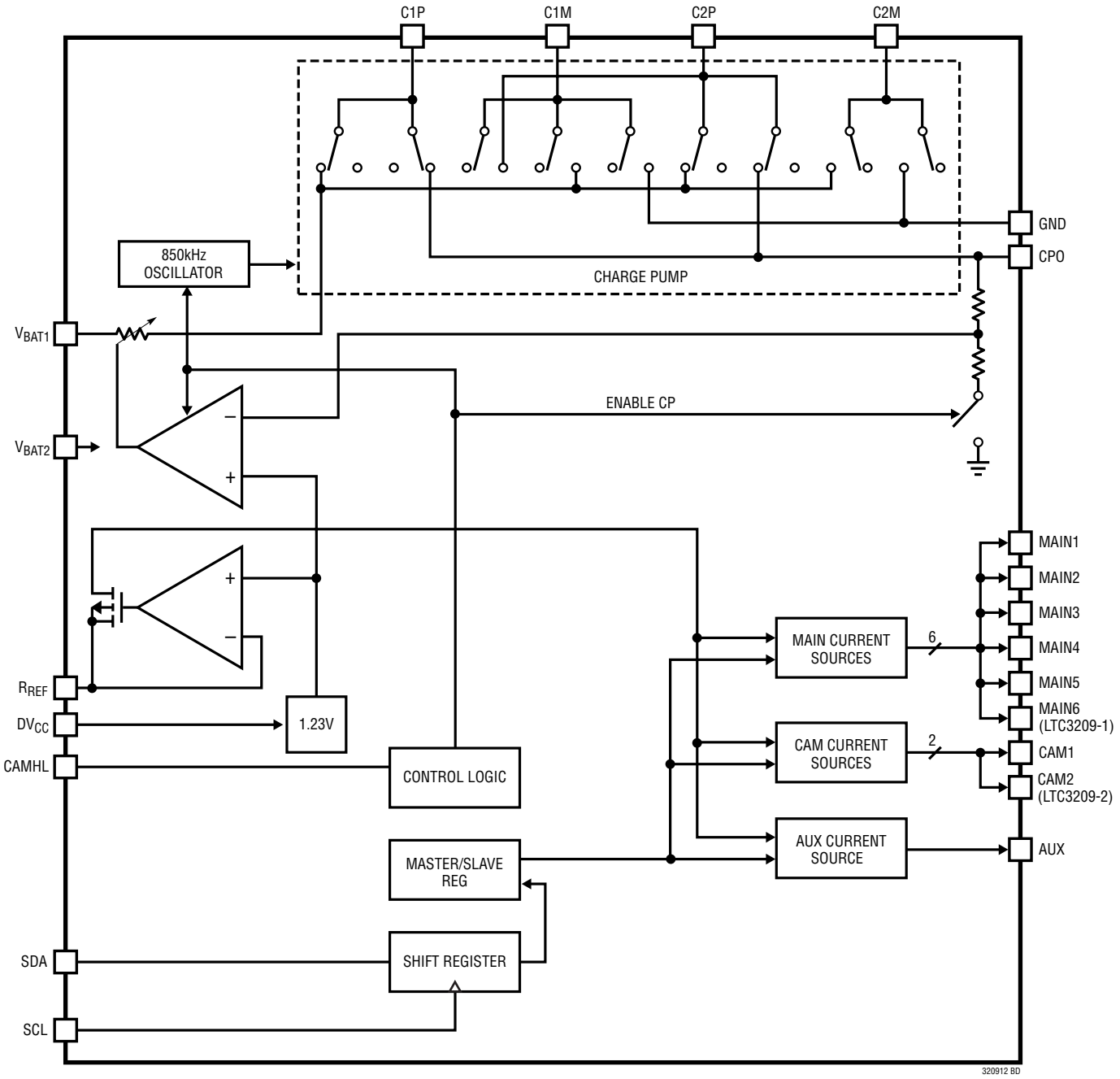
SDA (Pin 14/Pin 14): I^2C Data Input for the Serial Port. Serial data is shifted in one bit per clock to control the LTC3209-1/LTC3209-2. The logic level is referenced to DV_{CC}.

SCL (Pin 15/Pin 15): I^2C Clock Input. The logic level for SCL is referenced to DV_{CC}.

C1P, C2P, C1M, C2M (Pins 20, 19, 17, 16/Pins 20, 19, 17, 16): Charge Pump Flying Capacitor Pins. A 2.2µF X7R or X5R ceramic capacitor should be connected from C1P to C1M and C2P to C2M.

Exposed Pad (Pin 21/Pin 21): System Ground. Connect Exposed Pad to PCB ground plane.

BLOCK DIAGRAM



OPERATION

The LTC3209-1 has 6 MAIN outputs, 1 CAM output and 1 AUX output. The LTC3209-2 has 5 MAIN outputs, 2 CAM outputs and 1 AUX output.

Power Management

The LTC3209-1/LTC3209-2 use a switched capacitor charge pump to boost CPO to as much as 2 times the input voltage up to 5.1V. The part starts up in 1x mode. In this mode, V_{BAT} is connected directly to CPO. This mode provides maximum efficiency and minimum noise. The LTC3209-1/LTC3209-2 will remain in 1x mode until a MAIN or CAM LED current source drops out. Dropout occurs when a current source voltage becomes too low for the programmed current to be supplied. When dropout is detected, the LTC3209-1/LTC3209-2 will switch into 1.5x mode. The CPO voltage will then start to increase and will attempt to reach 1.5x V_{BAT} up to 4.6V. Any subsequent dropout will cause the part to enter the 2x mode. The CPO voltage will attempt to reach 2x V_{BAT} up to 5.1V. The part will be reset to 1x mode whenever a DAC data bit is updated via the I^2C port or on the falling edge of the CAMHL signal.

A 2-phase nonoverlapping clock activates the charge pump switches. In the 2x mode the flying capacitors are charged on alternate clock phases from V_{BAT} to minimize input current ripple and CPO voltage ripple. In 1.5x mode the flying capacitors are charged in series during the first clock phase and stacked in parallel on V_{BAT} during the second phase. This sequence of charging and discharging the flying capacitors continues at a constant frequency of 850kHz.

The currents delivered by the LED current sources are controlled by an associated DAC. Each DAC is programmed via the I^2C port.

Soft-Start

Initially, when the part is in shutdown, a weak switch connects V_{BAT1} to CPO. This allows V_{BAT1} to slowly charge the CPO output capacitor and prevent large charging currents to occur.

The LTC3209-1/LTC3209-2 also employs a soft-start feature on its charge pump to prevent excessive inrush current and supply droop when switching into the step-up modes. The current available to the CPO pin is increased linearly over a typical period of 125µs. Soft-start occurs at the start of both 1.5x and 2x mode changes.

Charge Pump Strength

When the LTC3209-1/LTC3209-2 operate in either 1.5x mode or 2x mode, the charge pump can be modeled as a Thevenin-equivalent circuit to determine the amount of current available from the effective input voltage and effective open-loop output resistance, R_{OL} (Figure 1).

R_{OL} is dependent on a number of factors including the switching term, $1/(2f_{OSC} \bullet C_{FLY})$, internal switch resistances and the nonoverlap period of the switching circuit. However, for a given R_{OL}, the amount of current available will be directly proportional to the advantage voltage of $1.5V_{BAT}$ - CPO for 1.5x mode and $2V_{BAT}$ - CPO for 2x mode.

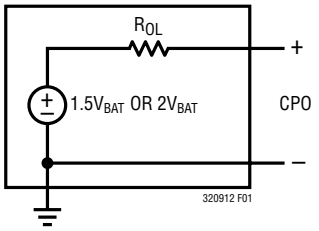


Figure 1. Charge Pump Thevenin Equivalent Open-Loop Circuit

OPERATION

Consider the example of driving white LEDs from a 3.1V supply. If the LED forward voltage is 3.8V and the current sources require 100mV, the advantage voltage for 1.5x mode is 3.1V • 1.5 – 3.8V – 0.1V or 750mV. Notice that if the input voltage is raised to 3.2V, the advantage voltage jumps to 900mV—a 20% improvement in available strength.

From Figure 1, for 1.5x mode the available current is given by:

$$I_{OUT} = \frac{1.5V_{BAT} - V_{CPO}}{R_{OL}}$$

For 2x mode, the available current is given by:

$$I_{OUT} = \frac{2V_{BAT} - V_{CPO}}{R_{OL}}$$

Notice that the advantage voltage in this case is 3.1V • 2 – 3.8V – 0.1V = 2.3V. R_{OL} is higher in 2x mode but a significant overall increase in available current is achieved.

Typical values of R_{OL} as a function of temperature are shown in Figures 2 and 3.

Shutdown Current

Shutdown occurs when all the current source data bits have been written to zero or when DV_{CC} is below the DV_{CC} UVLO threshold.

Although the LTC3209-1/LTC3209-2 is designed to have very low shutdown current, it will draw about 3µA from V_{BAT} when in shutdown. Internal logic ensures that the LTC3209-1/LTC3209-2 is in shutdown when DV_{CC} is grounded. Note, however that all of the logic signals that are referenced to DV_{CC} (SCL, SDA, CAMHL) will need to be at DV_{CC} or below (i.e., ground) to avoid violation of the absolute maximum specifications on these pins.

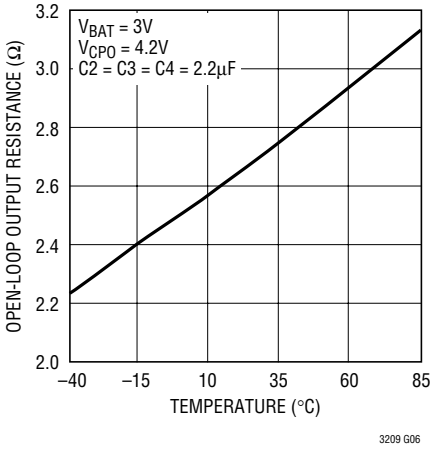


Figure 2. Typical 1.5x R_{OL} vs Temperature

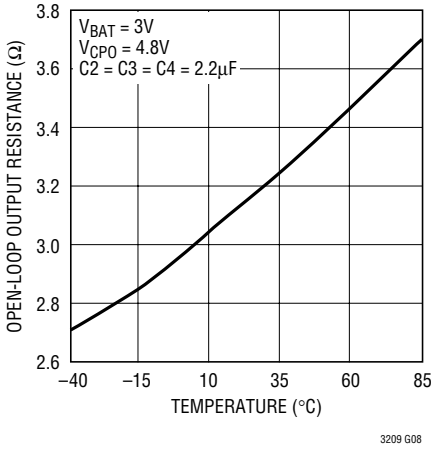


Figure 3. Typical 2x R_{OL} vs Temperature

OPERATION

Serial Port

The microcontroller compatible I^{2}C serial port provides all of the command and control inputs for the LTC3209-1/ LTC3209-2. Data on the SDA input is loaded on the rising edge of SCL. D7 is loaded first and D0 last. There are three data registers and one address register. Once all address bits have been clocked into the address register acknowledge occurs. After the data registers have been written a load pulse is created after the stop bit. The load pulse transfers all of the data held in the data registers to the DAC registers. At this point the LED current will be changed to the new settings. The serial port uses static logic registers so there is no minimum speed at which it can be operated.

MAIN Current Sources

LTC3209-1

There are six MAIN current sources. These current sources have an 8-bit linear DAC for current control. For R_{REF} = 24.3k, the output current range is 0mA to 28mA in 256 steps.

The current sources are disabled when a block receives an all zero data word. The supply current for that block is reduced to zero. In addition unused LED outputs can be connected to CPO to turn off the current source output and reduce the operating current to typically 10µA.

LTC3209-2

There are five MAIN current sources. These current sources have an 8-bit linear DAC for current control. For R_{REF} = 24.3k, the output current range is 0mA to 28mA in 256 steps.

The current sources are disabled when a block receives an all zero data word. The supply current for that block is reduced to zero. In addition unused LED outputs can be connected to CPO to turn off the current source output and reduce the operating current to typically 10µA.

Camera Current Sources

LTC3209-1

There is one CAM current source. This current source has a 4-bit linear DAC for current control. The output current range is 0mA to 400mA in 16 steps (R_{REF} = 24.3k).

The current source is disabled when the block receives an all zero data word. The supply current for the block is reduced to zero. In addition, the LED output can be connected to CPO to turn off the current source output and reduce operating current to typically 10µA. This pin cannot be allowed to float if unused since dropout will be erroneously detected.

LTC3209-2

There are two CAM current sources. These current sources have a 4-bit linear DAC for current control. The output current range of each current source is 0mA to 200mA in 16 steps (R_{REF} = 24.3k).

The current sources are disabled when the block receives an all zero data word. The supply current for the block is reduced to zero. In addition unused LED outputs can be connected to CPO to turn off the current source output and reduce the operating current to typically 10µA. These pins cannot be allowed to float if unused since dropout will be erroneously detected.

Auxiliary Current Source

There is one AUX current source. This current source has a 2-bit Linear DAC for current control. The output current range is 0mA to 13.75mA in 4 steps (OFF, 33%, 67%, 100%). The AUX output does not have dropout detection and cannot be disabled when connected to CPO.

The current source is disabled when the block receives an all zero data word and the supply current for the block is reduced to zero. This output can also be used as an I^{2}C controlled digital open-drain general purpose output.

OPERATION

CAMHL

The CAMHL pin quickly selects the camera high register for flash applications without reaccessing the I^2C port. When low the CAM current range will be controlled by the camera low 4-bit register. When CAMHL is asserted high the current range will be set by the camera high 4-bit register. The dropout delay is reduced from 150ms to 2ms when CAMHL is asserted high so that the charge pump can quickly change modes if required. When CAMHL is asserted from high to low the charge pump mode is reset to 1x.

Thermal Protection

The LTC3209-1/LTC3209-2 have built-in overtemperature protection. At internal die temperatures of around 150°C thermal shutdown will occur. This will disable all of the current sources and charge pump until the die has cooled by about 15°C. This thermal cycling will continue until the fault has been corrected.

R_{REF} Current Set Resistor

The current set resistor is connected between the R_{REF} pin and ground. This resistor sets the full-scale current for all three displays (MAIN, CAM and AUX) according to the following equations:

$$MAIN = \frac{1.23V}{R_{REF}} \bullet 550$$

$$CAM = \frac{1.23V}{R_{REF}} \bullet 7900 \quad \text{(LTC3209-1)}$$

$$CAM = \frac{1.23V}{R_{REF}} \bullet 3950 \quad \text{(LTC3209-2)}$$

$$AUX = \frac{1.23V}{R_{REF}} \bullet 272$$

A 24.3k, 1% resistor provides full-scale currents of 28mA for the MAIN; 400mA (total) current for CAM and 13.75mA for AUX current sources.

This input is protected against shorts to ground or low value resistors <10k. When a fault is detected the reference current amplifier is current limited. In addition the current source outputs and charge pump are disabled.

Mode Switching

The LTC3209-1/LTC3209-2 will automatically switch from 1x mode to 1.5x mode and subsequently to 2x mode whenever a dropout condition is detected at an LED pin. Dropout occurs when a current source voltage becomes too low for the programmed current to be supplied. When switching modes the mode change will not occur unless dropout has existed for 150ms. This delay will allow the LEDs to warm up and achieve the final LED forward voltage value. The dropout delay can be reduced to 2ms by programming the Drop2ms bit C2 in the REGC register or when the CAMHL pin is switched high when controlling the CAM LEDs.

The mode will automatically switch back to 1x whenever a data bit is updated via the I^2C port or when CAMHL switches from high to low. If the part is forced into either 1.5x mode or 2x mode to operate as a fixed voltage power supply over I^2C, no mode switching will occur until an I^2C update is given.

OPERATION

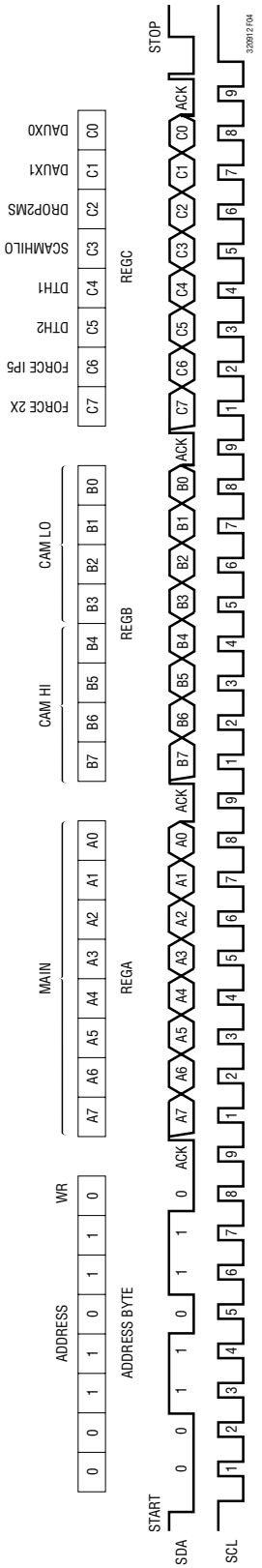


Figure 4. Bit Assignments

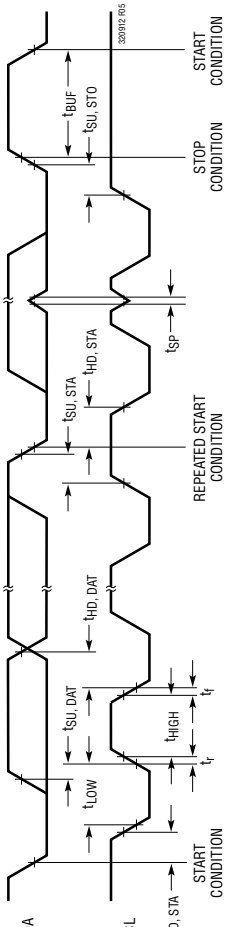


Figure 5. Timing Parameters

OPERATION

REGA, MAIN LED 8-Bit DAC Data

MSB							LSB
A7	A6	A5	A4	A3	A2	A1	A0
MAIN D7	MAIN D6	MAIN D5	MAIN D4	MAIN D3	MAIN D2	MAIN D1	MAIN D0

REGB, CAMERA LED 4-Bit High and 4-Bit Low DAC Data

MSB	HIGH BITS		LSB	MSB	LOW BITS		LSB
B7	B6	B5	B4	B3	B2	B1	B0
CAM D3	CAM D2	CAM D1	CAM D0	CAM D3	CAM D2	CAM D1	CAM D0

REGC, AUX Data and Option Byte

MSB							LSB
C7	C6	C5	C4	C3	C2	C1	C0
Force2x	Force1p5	Dth2	Dth1	Scamhilo	Drop2ms	DAUX1	DAUX0

DAUX0		AUX DAC Data (LSB)
DAUX1		AUX DAC Data (MSB)
Drop2ms	1 0	Changes Dropout Time from 150ms to 2ms Dropout Time is 150ms Unless CAMHL is Enabled and High
Scamhilo	1 0	Selects CAM High Register, Disables CAMHL Pin Selects CAM Low Register, Enables CAMHL Pin
Dth1	0	Must Always be 0 (Test Mode)
Dth2	0	Must Always be 0 (Test Mode)
Force1p5	1 0	Forces Charge Pump into 1.5x Mode, CPO Regulates at 4.6V Enables Mode Logic to Control Mode Changes Based on Dropout Signal
Force2x	1 0	Forces Charge Pump into 2x Mode, Overrides Force1p5 Signal, CPO Regulates at 5.1V Enables Mode Logic to Control Mode Changes Based on Dropout Signal

I²C Interface

The LTC3209-1/LTC3209-2 communicates with a host (master) using the standard I²C 2-wire interface. The Timing Diagram (Figure 5) shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 SMBus accelerator, are required on these lines.

The LTC3209-1/LTC3209-2 is a receive-only (slave) device.

Bus Speed

The I²C port is designed to be operated at speeds of up to 400kHz. It has built-in timing delays to ensure correct operation when addressed from an I²C compliant master device. It also contains input filters designed to suppress glitches should the bus become corrupted.

OPERATION

START and STOP Conditions

A bus-master signals the beginning of a communication to a slave device by transmitting a START condition.

A START condition is generated by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for communication with another I^2C device.

Byte Format

Each byte sent to the LTC3209-1/LTC3209-2 must be 8 bits long followed by an extra clock cycle for the Acknowledge bit to be returned by the LTC3209-1/LTC3209-2. The data should be sent to the LTC3209-1/LTC3209-2 most significant bit (MSB) first.

Acknowledge

The Acknowledge signal is used for handshaking between the master and the slave. An Acknowledge (active low) generated by the slave (LTC3209-1/LTC3209-2) lets the master know that the latest byte of information was received. The Acknowledge related clock pulse is generated by the master. The master releases the SDA line (high) during the Acknowledge clock cycle. The slave-receiver must pull down the SDA line during the Acknowledge clock pulse so that it remains a stable low during the high period of this clock pulse.

Slave Address

The LTC3209-1/LTC3209-2 responds to only one 7-bit address which has been factory programmed to 0011011. The eighth bit of the address byte (R/W) must be 0 for the LTC3209-1/LTC3209-2 to recognize the address since it is a write only device. This effectively forces the address to be 8 bits long where the least significant bit of the address is 0. If the correct seven bit address is given but the R/W bit is 1, the LTC3209-1/LTC3209-2 will not respond.

Bus Write Operation

The master initiates communication with the LTC3209-1/LTC3209-2 with a START condition and a 7-bit address followed by the Write Bit R/W = 0. If the address matches that of the LTC3209-1/LTC3209-2, the part returns an Acknowledge. The master should then deliver the most significant data byte. Again the LTC3209-1/LTC3209-2 acknowledges and cycle is repeated two more times for a total of one address byte and three data bytes. Each data byte is transferred to an internal holding latch upon the return of an Acknowledge. After all three data bytes have been transferred to the LTC3209-1/LTC3209-2, the master may terminate the communication with a STOP condition. Alternatively, a REPEAT-START condition can be initiated by the master and another chip on the I^2C bus can be addressed. This cycle can continue indefinitely and the LTC3209-1/LTC3209-2 will remember the last input of valid data that it received. Once all chips on the bus have been addressed and sent valid data, a global STOP condition can be sent and the LTC3209-1/LTC3209-2 will update all registers with the data that it had received.

In certain circumstances the data on the I^2C bus may become corrupted. In these cases the LTC3209-1/LTC3209-2 responds appropriately by preserving only the last set of complete data that it has received. For example, assume the LTC3209-1/LTC3209-2 has been successfully addressed and is receiving data when a STOP condition mistakenly occurs. The LTC3209-1/LTC3209-2 will ignore this STOP condition and will not respond until a new START condition, correct address, new set of data and STOP condition are transmitted.

Likewise, if the LTC3209-1/LTC3209-2 was previously addressed and sent valid data but not updated with a STOP, it will respond to any STOP that appears on the bus with only one exception, independent of the number of REPEAT-STARTs that have occurred. If a REPEAT-START is given and the LTC3209-1/LTC3209-2 successfully acknowledges its address, it will not respond to a STOP until all bytes of the new data have been received and acknowledged.

APPLICATIONS INFORMATION

V_{BAT}, CPO Capacitor Selection

The style and value of the capacitors used with the LTC3209-1/LTC3209-2 determine several important parameters such as regulator control loop stability, output ripple, charge pump strength and minimum start-up time.

To reduce noise and ripple, it is recommended that low equivalent series resistance (ESR) ceramic capacitors are used for both CV_{BAT} and C_{CPO}. Tantalum and aluminum capacitors are not recommended due to high ESR.

The value of C_{CPO} directly controls the amount of output ripple for a given load current. Increasing the size of C_{CPO} will reduce output ripple at the expense of higher start-up current. The peak-to-peak output ripple of the 1.5x mode is approximately given by the expression:

$$V_{RIPPLE(P-P)} = \frac{I_{OUT}}{3f_{OSC} \bullet C_{CPO}}$$

Where f_{OSC} is the LTC3209-1/LTC3209-2 oscillator frequency or typically 850kHz and C_{CPO} is the output storage capacitor.

The output ripple in 2x mode is very small due to the fact that load current is supplied on both cycles of the clock.

Both style and value of the output capacitor can significantly affect the stability of the LTC3209-1/LTC3209-2. As shown in the Block Diagram, the LTC3209-1/LTC3209-2 use a control loop to adjust the strength of the charge pump to match the required output current. The error signal of the loop is stored directly on the output capacitor. The output capacitor also serves as the dominant pole for the control loop. To prevent ringing or instability, it is important for the output capacitor to maintain at least 1µF of capacitance over all conditions.

In addition, excessive output capacitor ESR will tend to degrade the loop stability. If the output capacitor has 160mΩ or more of ESR, the closed-loop frequency response will cease to roll off in a simple one-pole fashion and poor load transient response or instability may occur. Multilayer ceramic chip capacitors typically have exceptional ESR performance. MLCCs combined with a tight board layout will result in very good stability. As the value of C_{CPO} controls the amount of output ripple, the value of CV_{BAT} controls the amount of ripple present at the input pin (V_{BAT}). The LTC3209-1/LTC3209-2 input current will be relatively constant while the charge pump is either in the input charging phase or the output charging phase but will drop to zero during the clock nonoverlap times. Since the nonoverlap time is small (~25ns), these missing "notches" will result in only a small perturbation on the input power supply line. Note that a higher ESR capacitor such as tantalum will have higher input noise due to the higher ESR. Therefore, ceramic capacitors are recommended for low ESR. Input noise can be further reduced by powering the LTC3209-1/LTC3209-2 through a very small series inductor as shown in Figure 6. A 10nH inductor will reject the fast current notches, thereby presenting a nearly constant current load to the input power supply. For economy, the 10nH inductor can be fabricated on the PC board with about 1cm (0.4") of PC board trace.

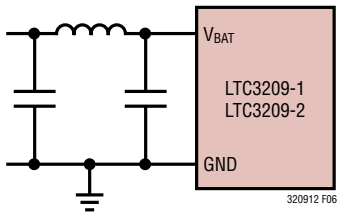


Figure 6. 10nH Inductor Used for Input Noise Reduction (Approximately 1cm of Board Trace)

Flying Capacitor Selection

Warning: Polarized capacitors such as tantalum or aluminum should never be used for the flying capacitors since their voltage can reverse upon start-up of the LTC3209-1/LTC3209-2. Ceramic capacitors should always be used for the flying capacitors.

The flying capacitors control the strength of the charge pump. In order to achieve the rated output current it is necessary to have at least 1.6µF of capacitance for each of the flying capacitors. Capacitors of different materials lose their capacitance with higher temperature and voltage at different rates. For example, a ceramic capacitor made of X7R material will retain most of its capacitance from –40°C to 85°C whereas a Z5U or Y5V style capacitor will

APPLICATIONS INFORMATION

lose considerable capacitance over that range. Z5U and Y5V capacitors may also have a very poor voltage coefficient causing them to lose 60% or more of their capacitance when the rated voltage is applied. Therefore, when comparing different capacitors, it is often more appropriate to compare the amount of achievable capacitance for a given case size rather than comparing the specified capacitance value. For example, over rated voltage and temperature conditions, a 1µF, 10V, Y5V ceramic capacitor in a 0603 case may not provide any more capacitance than a 0.22µF, 10V, X7R available in the same case. The capacitor manufacturer's data sheet should be consulted to determine what value of capacitor is needed to ensure minimum capacitances at all temperatures and voltages.

Table 1 shows a list of ceramic capacitor manufacturers and how to contact them:

Table 1. Recommended Capacitor Vendors

AVX	www.avxcorp.com
Kemet	www.kemet.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay	www.vishay.com

Layout Considerations and Noise

Due to the high switching frequency and the transient currents produced by the LTC3209-1/LTC3209-2, careful board layout is necessary. A true ground plane and short connections to all capacitors will improve performance and ensure proper regulation under all conditions.

The flying capacitor pins C1P, C2P, C1M and C2M will have high edge rate waveforms. The large dv/dt on these pins can couple energy capacitively to adjacent PCB runs. Magnetic fields can also be generated if the flying capacitors are not close to the LTC3209-1/LTC3209-2 (i.e., the loop area is large). To decouple capacitive energy transfer, a Faraday shield may be used. This is a grounded PCB trace between the sensitive node and the LTC3209-1/LTC3209-2 pins. For a high quality AC ground, it should be returned to a solid ground plane that extends all the way to the LTC3209-1/LTC3209-2.

The following guidelines should be followed when designing a PCB layout for the LTC3209.

- The Exposed Pad should be soldered to a large copper plane that is connected to a solid, low impedance ground plane using plated, through-hole vias for proper heat sinking and noise protection.
- Input and output capacitors (C1 and C4) must be placed close to the part.
- The flying capacitors (C2 and C3) must be placed close to the part. The traces running from the pins to the capacitor pads should be as wide as possible.
- V_{BAT}, CPO traces must be made wide to minimize inductance and handle the high currents.
- LED pads must be large and connected to other layers of metal to ensure proper heat sinking.

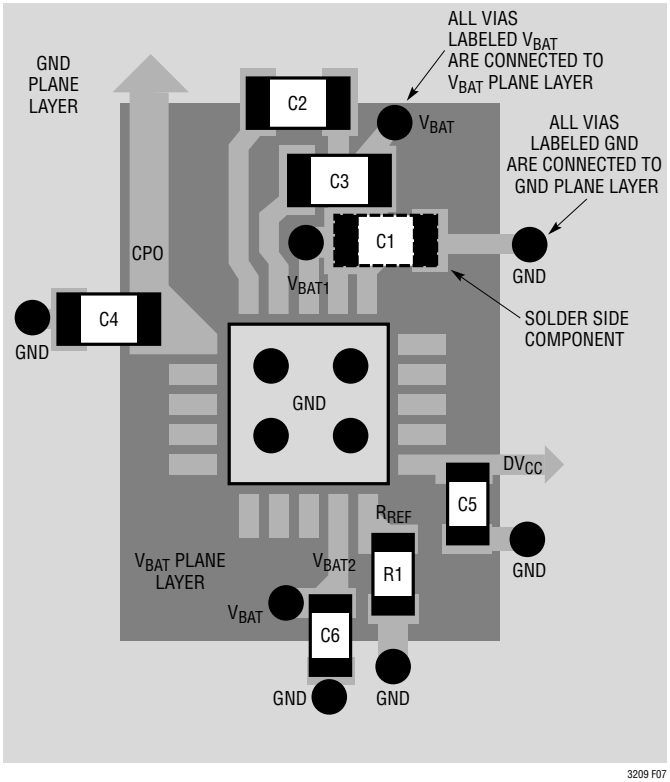


Figure 7. PC Board Layout Example (LTC3209-1)

APPLICATIONS INFORMATION

Power Efficiency

To calculate the power efficiency (η) of a white LED driver chip, the LED power should be compared to the input power. The difference between these two numbers represents lost power whether it is in the charge pump or the current sources. Stated mathematically, the power efficiency is given by:

$$\eta = \frac{P_{LED}}{P_{IN}}$$

The efficiency of the LTC3209-1/LTC3209-2 depends upon the mode in which it is operating. Recall that the LTC3209-1/LTC3209-2 operates as a pass switch, connecting V_{BAT} to CPO, until dropout is detected at the I_{LED} pin. This feature provides the optimum efficiency available for a given input voltage and LED forward voltage. When it is operating as a switch, the efficiency is approximated by:

$$\eta = \frac{P_{LED}}{P_{IN}} = \frac{(V_{LED} \bullet I_{LED})}{(V_{BAT} \bullet I_{BAT})} = \frac{V_{LED}}{V_{BAT}} \quad \text{(1x Mode)}$$

since the input current will be very close to the sum of the LED currents.

At moderate to high output power, the quiescent current of the LTC3209-1/LTC3209-2 is negligible and the expression above is valid.

Once dropout is detected at the LED pin, the LTC3209-1/LTC3209-2 enables the charge pump in 1.5x mode.

In 1.5x boost mode, the efficiency is similar to that of a linear regulator with an effective input voltage of 1.5 times the actual input voltage. This is because the input current for a 1.5x charge pump is approximately 1.5 times the load current. In an ideal 1.5x charge pump, the power efficiency would be given by:

$$\eta_{IDEAL} = \frac{P_{LED}}{P_{IN}} = \frac{(V_{LED} \bullet I_{LED})}{(V_{BAT} \bullet (1.5) \bullet I_{LED})} = \frac{V_{LED}}{(1.5 \bullet V_{BAT})}$$

(1.5x Mode)

Similarly, in 2x boost mode, the efficiency is similar to that of a linear regulator with an effective input voltage of 2 times the actual input voltage. In an ideal 2x charge pump, the power efficiency would be given by:

$$\eta_{IDEAL} = \frac{P_{LED}}{P_{IN}} = \frac{(V_{LED} \bullet I_{LED})}{(V_{BAT} \bullet (2) \bullet I_{LED})} = \frac{V_{LED}}{(2 \bullet V_{BAT})}$$

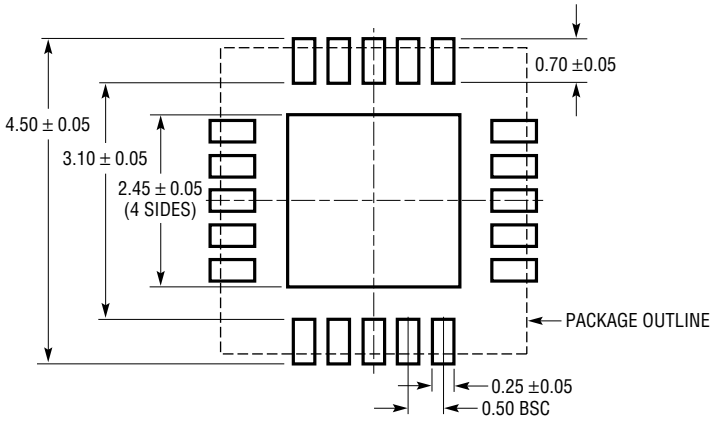
(2x Mode)

Thermal Management

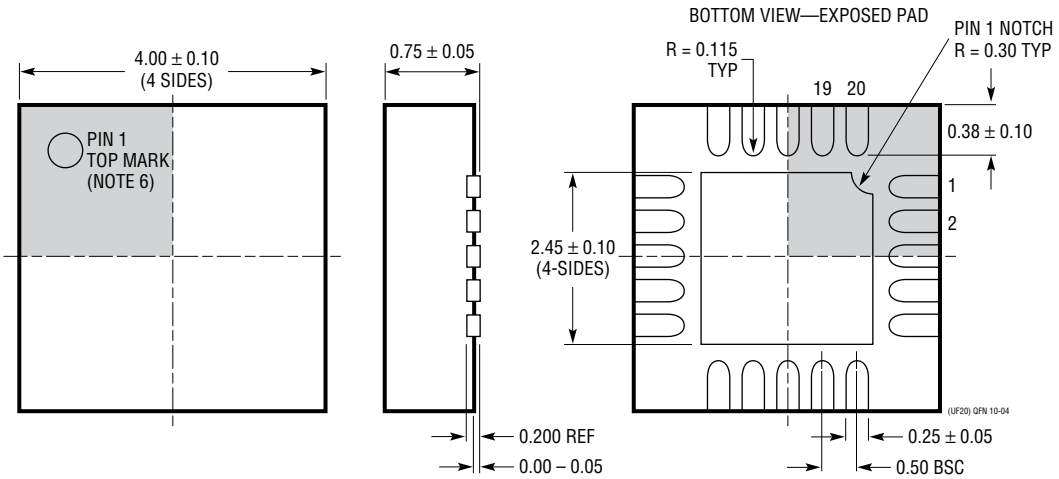
For higher input voltages and maximum output current, there can be substantial power dissipation in the LTC3209-1/LTC3209-2. If the junction temperature increases above approximately 150°C the thermal shutdown circuitry will automatically deactivate the output current sources and charge pump. To reduce maximum junction temperature, a good thermal connection to the PC board is recommended. Connecting the Exposed Pad to a ground plane and maintaining a solid ground plane under the device will reduce the thermal resistance of the package and PC board considerably.

PACKAGE DESCRIPTION

UF Package
20-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1710)



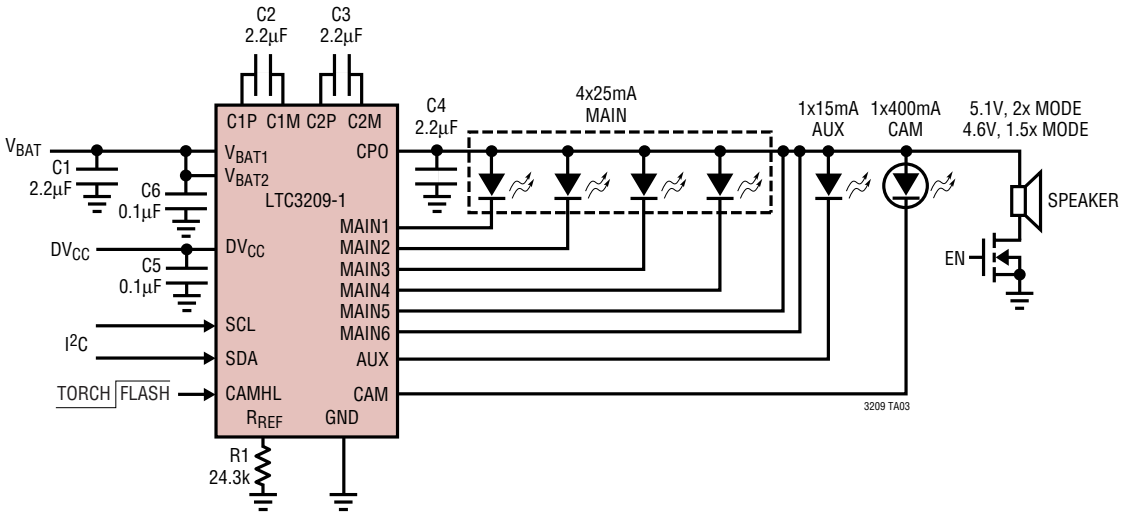
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING IS PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-1)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

4 LED MAIN, 1 LED SUB, 400mA CAM LED Controller Plus Regulated Output



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3200-5	Low Noise, 2MHz Regulated Charge Pump White LED Driver	Up to 6 White LEDs, V_{IN}: 2.7V to 4.5V, $V_{OUT(MAX)}$ = 5V, I_Q = 8mA, I_{SD} ≤1µA, ThinSOT Package
LTC3201	Low Noise, 1.7MHz Regulated Charge Pump White LED Driver	Up to 6 White LEDs, V_{IN}: 2.7V to 4.5V, $V_{OUT(MAX)}$ = 5V, I_Q = 6.5mA, I_{SD} ≤1µA, 10-Lead MS Package
LTC3202	Low Noise, 1.5MHz Regulated Charge Pump White LED Driver	Up to 8 White LEDs, V_{IN}: 2.7V to 4.5V, $V_{OUT(MAX)}$ = 5V, I_Q = 5mA, I_{SD} ≤1µA, 10-Lead MS Package
LTC3205	Multidisplay LED Controller	92% Efficiency, V_{IN}: 2.8V to 4.5V, I_Q = 50µA, I_{SD} ≤ 1µA, (4mm × 4mm) QFN Package
LTC3206	I^2C Multidisplay LED Controller	92% Efficiency, 400mA Continuous Output Current. Up to 11 White LEDs in (4mm × 4mm) QFN Package
LTC3208	High Current Software Configurable Multidisplay LED Controller	95% Efficiency, V_{IN}: 2.9V to 4.5V, $V_{OUT(MAX)}$: 5.5V, I_Q = 280µA, I_{SD} < 1µA, (5mm × 5mm) QFN-32 Package
LTC3214	500mA Camera LED Charge Pump	94% Efficiency, V_{IN}: 2.9V to 4.5V, I_Q = 300µA, I_{SD} < 2.5µA, 500mA Output Current, 10-Lead (3mm × 3mm) DFN Package
LTC3215	700mA Low Noise High Current LED Charge Pump	V_{IN}: 2.9V to 4.4V, $V_{OUT(MAX)}$ = 5.5V, I_Q = 300µA, I_{SD} < 2.5µA (3mm × 3mm) DFN Package
LTC3216	1A Low Noise High Current White LED Driver	93% Efficiency, 1A Output Current, 12-Lead (3mm × 4mm) DFN Package, Independent Low/High Current Programming
LTC3217	600mA Low Noise Multi-LED Camera Light	V_{IN}: 2.9V to 4.4V, I_Q = 400µA, Four Outputs, (3mm × 3mm) 16-Lead DFN Package
LTC3251	500mA (I_{OUT}), 1MHz to 1.6MHz Spread Spectrum Step-Down Charge Pump	85% Efficiency, V_{IN}: 3.1V to 5.5V, V_{OUT}: 0.9V to 1.6V, I_Q = 9µA, I_{SD} ≤1µA, 10-Lead MS Package
LTC3440	600mA (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 2.5V, I_Q = 25µA, I_{SD} ≤1µA, 10-Lead MS Package

ThinSOT is a trademark of Linear Technology Corporation.

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