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www.infineon.com

S6BP401A

Power Management IC for Automotive ADAS Platform

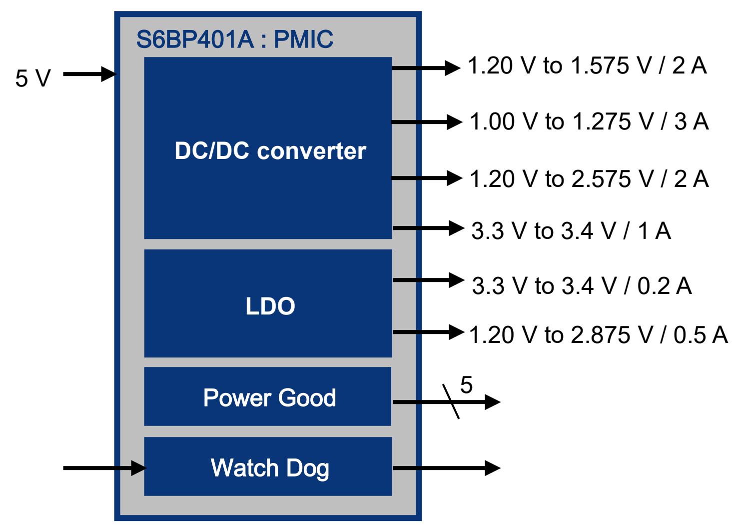
Quad Buck 2.1 MHz DC/DC Converter and Dual LDO with Watchdog Timer

S6BP401A is a power management IC, consists of quad buck 2.1 MHz DC/DC converter with built-in switching FETs, dual Low Drop-out regulator (LDOs) and a digital windowed watchdog timer. Having the switching FETs built-in, S6BP401A realizes high power conversion efficiency and high switching frequency up to 2.4 MHz. The internal FETs are capable to handle up to 3 A load. As S6BP401A employs the current mode architecture, it has fast load transient response. Built-in output voltage setting resistors and compensation circuits reduce BOM cost and component area.

Features

- Quad Buck DC/DC Converter (DD1 to DD4)
  - VIN Input Range: 4.5 V to 5.5 V
  - Switching Frequency
  - External clock mode: 1.8 MHz to 2.4 MHz
  - Internal clock mode: 2.0 MHz to 2.2 MHz
  - Built-in Switching FETs up to 3 A
  - Built-in Output Voltage Setting Resistors
  - Built-in Compensation Circuits
- Dual LDO (LD1, LD2)
  - VIN Input Voltage Range: 2.97 V to 5.5 V
  - Built-in Output Voltage Setting resistors
- Power Good Monitor Output for each DC/DC Converters, LDOs
- Built-in Windowed Watchdog Timer (WDT)
- Under Voltage Lockout (UVLO)
- Thermal Shutdown (TSD)
- Over Current Protection (OCP)
- Over Voltage Protection (OVP)
- Independent Enabling for each DC/DC Converters and LDOs
- Load-independent Soft-Start
- Built-in Discharge Resistors
- Small 6 mm × 6 mm QFN-40 Package
- AEC-Q100 compliant (Grade-1)

Block Diagram



Applications

- Automotive Applications
- Advanced Driver Assistance Systems (ADAS)
- Camera Systems such as Security Camera
- Industrial Applications

More Information

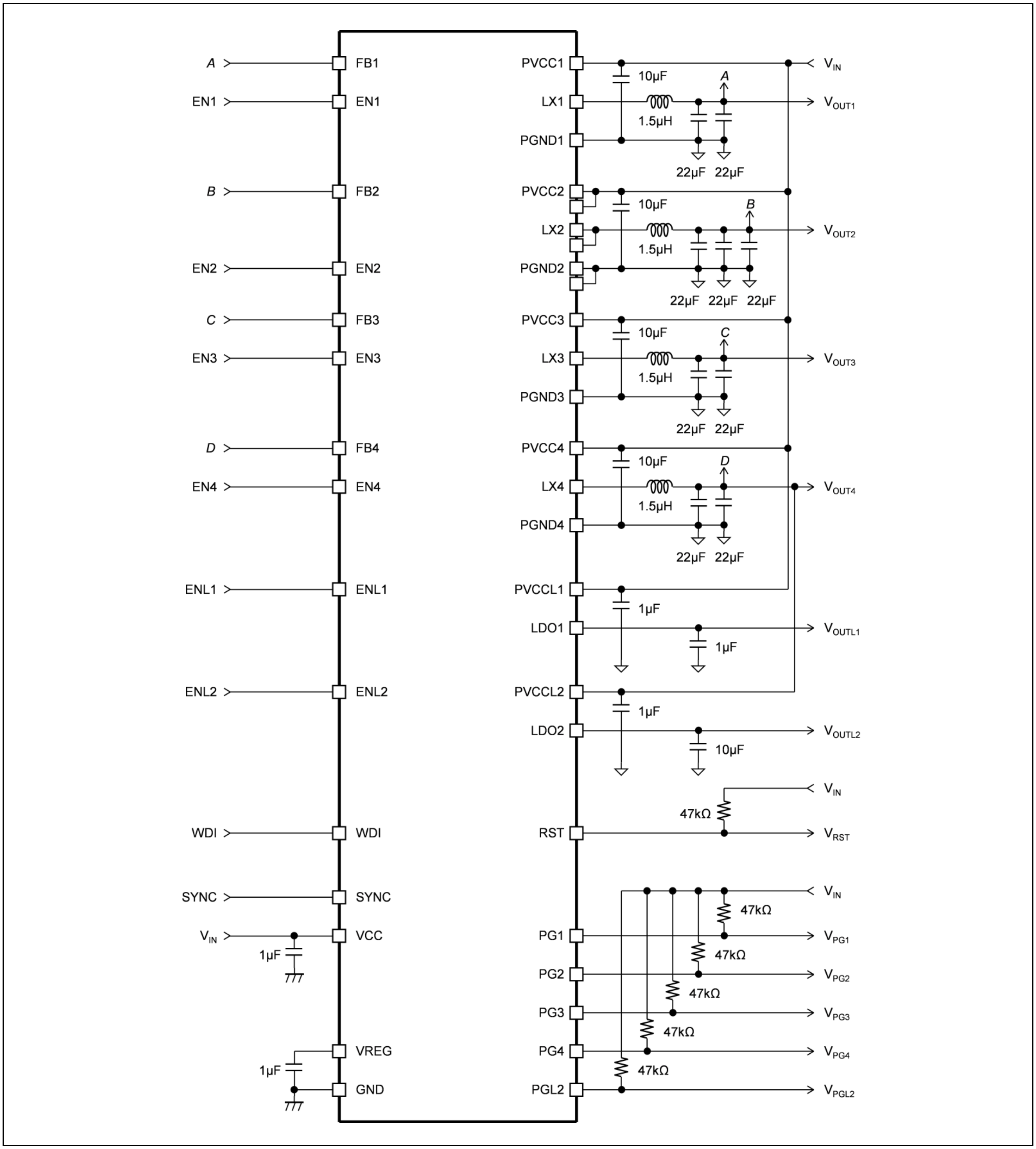
Cypress provides a wealth of data at www.cypress.com/pmic to help you to select the right PMIC device for your design, and to help you to quickly and effectively integrate the device into your design. Following is an abbreviated list for S6BP401A:

- Overview: Automotive PMIC Portfolio, Automotive PMIC Roadmap
- Product Selector:
  - S6BP401A: 6 ch Automotive PMIC for ADAS
- Application Notes: Cypress offers S6BP401A application notes. Recommended application notes for getting started with S6BP401A are:
  - AN98649: How to Design a Power Management System
  - AN201006: Thermal Considerations and Parameters
- Evaluation Kit Operation Manual:
  - S6SBP401AM2SA1001: Power block for automotive ADAS platform
- Related Products:
  - S6BP201A, S6BP202A, S6BP203A: 1 ch Buck-Boost Automotive PMIC
  - S6BP501A, S6BP502A: 3 ch Automotive PMIC for Instrument Cluster

Contents

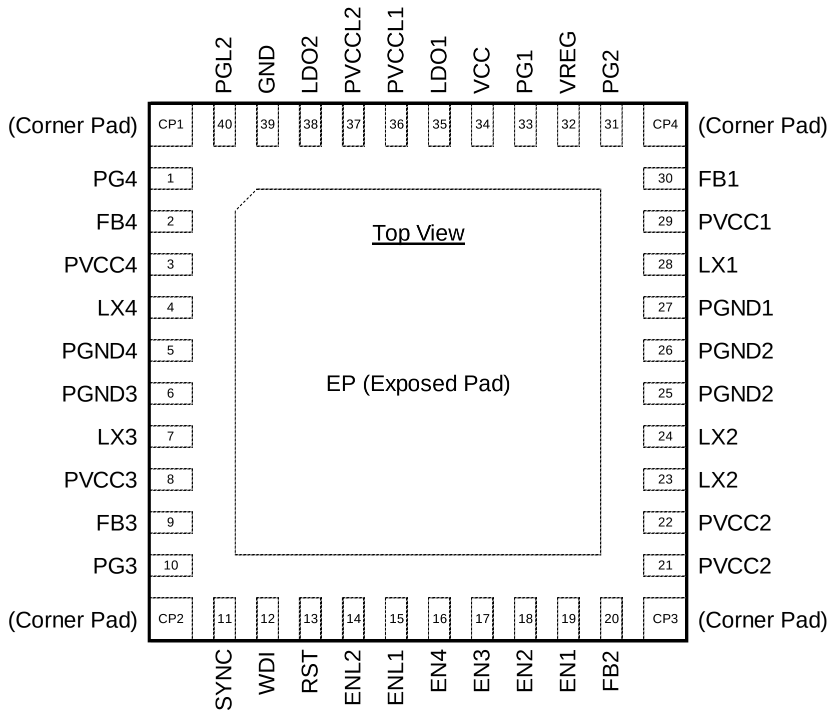
1. Typical Application

Figure 1-1 Typical Application



2. Pin Configuration

Figure 2-1 Pin Configuration



3. Pin Functions

Table 3-1 Pin Functions

Functional Block	Pin Number	Pin Name	I/O	Description	Pin Setting When Not Being Used
DD1	19	EN1	I	Enable input terminal of DD1.	Ground
	30	FB1	I	Output voltage feedback terminal of DD1.	Ground
	33	PG1	O	Power good output terminal of DD1.	Ground
	29	PVCC1	-	Power supply terminal of DD1.	VCC
	28	LX1	O	Inductor connect terminal of DD1.	Leave pin open
	27	PGND1	-	Power ground terminal of DD1.	Ground
DD2	18	EN2	I	Enable input terminal of DD2.	Ground
	20	FB2	I	Output voltage feedback terminal of DD2.	Ground
	31	PG2	O	Power good output terminal of DD2.	Ground
	21, 22	PVCC2	-	Power supply terminal of DD2.	VCC
	23, 24	LX2	O	Inductor connect terminal of DD2.	Leave pin open
	25, 26	PGND2	-	Power ground terminal of DD2.	Ground
DD3	17	EN3	I	Enable input terminal of DD3.	Ground
	9	FB3	I	Output voltage feedback terminal of DD3.	Ground
	10	PG3	O	Power good output terminal of DD3.	Ground
	8	PVCC3	-	Power supply terminal of DD3.	VCC
	7	LX3	O	Inductor connect terminal of DD3.	Leave pin open
	6	PGND3	-	Power ground terminal of DD3.	Ground
DD4	16	EN4	I	Enable input terminal of DD4.	Ground
	2	FB4	I	Output voltage feedback terminal of DD4.	Ground
	1	PG4	O	Power good output terminal of DD4.	Ground
	3	PVCC4	-	Power supply terminal of DD4.	VCC
	4	LX4	O	Inductor connect terminal of DD4.	Leave pin open
	5	PGND4	-	Power ground terminal of DD4.	Ground
LD1	15	ENL1	I	Enable input terminal of LD1.	Ground
	36	PVCCL1	-	Power supply terminal of LD1.	VCC
	35	LDO1	O	Output terminal of LD1.	Leave pin open
LD2	14	ENL2	I	Enable input of LD2.	Ground
	40	PGL2	O	Power good output terminal of LD2.	Ground
	37	PVCCL2	-	Power supply terminal of LD2.	VCC
	38	LDO2	O	Output terminal of LD2.	Leave pin open
WDT	12	WDI	I	Trigger input terminal of WDT.	Ground
	13	RST	O	Reset input terminal of WDT.	Ground
SYNC	11	SYNC	I	External clock input terminal.	Ground
-	34	VCC	-	Power supply terminal for analog controller.	–
-	32	VREG	O	Internal 1.8 V supply voltage capacitor terminal. Do NOT supply or load this terminal externally.	–
-	39	GND	-	Ground terminal for analog controller.	–
-	EP	EP	-	Exposed pad. Connect to ground plane.	–
-	CP1, CP2, CP3, CP4	CP	-	Corner pad for reinforcing attachment to a board. Connect to ground plane.	–

4. Preset Output Voltage

Table 4-1 Preset Output Voltage (Buck DC/DC Converter)

Channel	Preset Output Voltage [V]	Soft-start Time [ms]	Maximum Output Current [mA]	Under Voltage Threshold [%]	Over Voltage Threshold [%]
DD1	1.200	1.200	2000	94.0	106.0
	1.225	1.225			
	1.250	1.250			
	1.275	1.275			
	1.300	1.300			
	1.325	1.325			
	1.500	1.500			
	1.525	1.525			
	1.550	1.550			
	1.575	1.575			
DD2	1.000	1.000	3000	94.0	106.0
	1.025	1.025			
	1.050	1.050			
	1.075	1.075			
	1.100	1.100			
	1.125	1.125			
	1.150	1.150			
	1.175	1.175			
	1.200	1.200			
	1.225	1.225			
	1.250	1.250			
	1.275	1.275			
DD3	1.200	1.200	2000	95.2	106.0
	1.225	1.225			
	1.250	1.250			
	1.275	1.275			
	1.500	1.500			
	1.525	1.525			
	1.550	1.550			
	1.575	1.575			
	1.800	1.800			
	1.825	1.825			
	1.850	1.850			
	1.875	1.875			
	2.500	2.500			
	2.525	2.525			
	2.550	2.550			
	2.575	2.575			
DD4	3.300	3.300	1000	95.5	106.0
	3.325	3.325			
	3.350	3.350			
	3.375	3.375			
	3.400	3.400			

Notes:

− *Soft-start time values are at f_{OSC} = 2.1 MHz*

− *See 8. Electrical Characteristics for the minimum or maximum values of output voltage, under voltage threshold and over voltage threshold.*

Table 4-2 Preset Output Voltage (LDO)

Channel	Preset Output Voltage [V]	Soft-start Time [ms]	Maximum Output Current [mA]	Under Voltage Threshold [%]	Over Voltage Threshold [%]
LD1	3.300	3.300	200	94.0	106.0
	3.325	3.325			
	3.350	3.350			
	3.375	3.375			
	3.400	3.400			
LD2	1.200	1.200	500	94.0	106.0
	1.225	1.225			
	1.250	1.250			
	1.275	1.275			
	1.800	1.800			
	1.825	1.825			
	1.850	1.850			
	1.875	1.875			
	2.800	2.800			
	2.825	2.825			
	2.850	2.850			
	2.875	2.875			

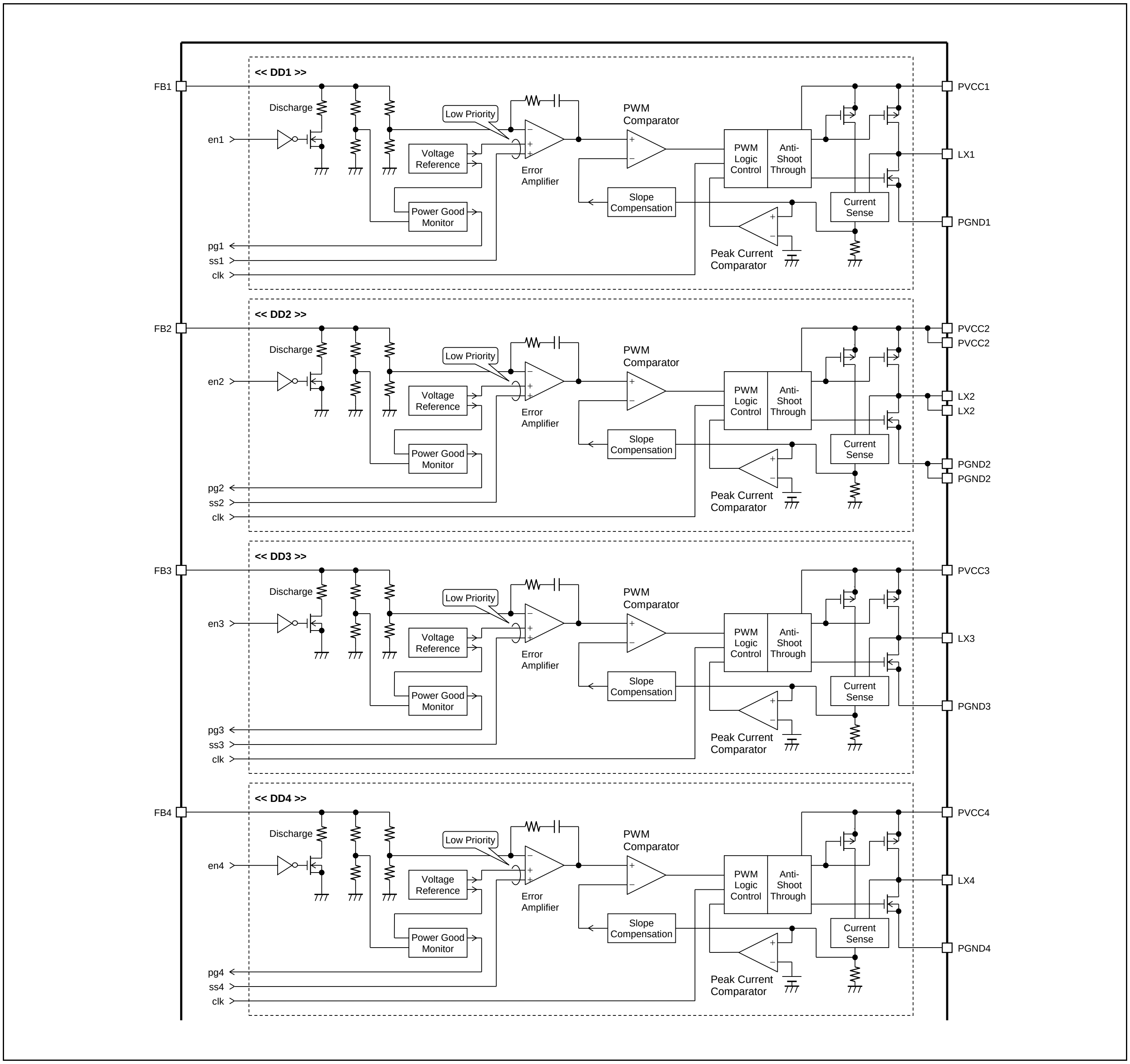
Notes:

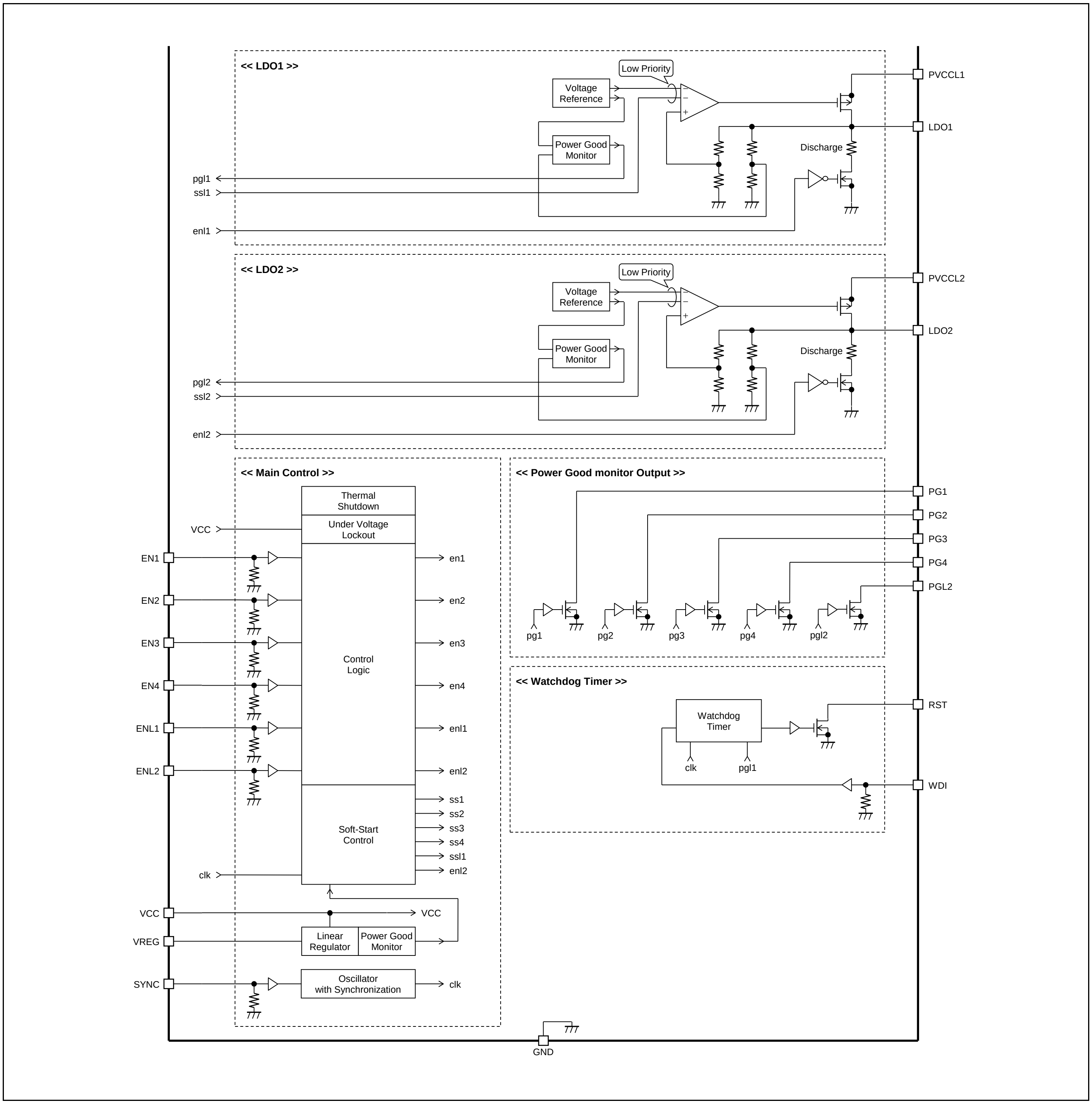
− *Soft-start time values are at f_{OSC} = 2.1 MHz*

− *See 8. Electrical Characteristics for the minimum or maximum values of output voltage, under voltage threshold and over voltage threshold.*

5. Architecture Block Diagram

Figure 5-1 Architechture Block Diagram





<< LDO1 >>
Low Priority
Voltage Reference
Power Good Monitor
Discharge
pgl1
ssl1
enl1
PVCCL1
LDO1
<< LDO2 >>
Low Priority
Voltage Reference
Power Good Monitor
Discharge
pgl2
ssl2
enl2
PVCCL2
LDO2
<< Main Control >>
Thermal Shutdown
Under Voltage Lockout
Control Logic
Soft-Start Control
VCC
EN1
EN2
EN3
EN4
ENL1
ENL2
en1
en2
en3
en4
enl1
enl2
ss1
ss2
ss3
ss4
ssl1
enl2
clk
VCC
VREG
SYNC
Linear Regulator
Power Good Monitor
Oscillator with Synchronization
clk
<< Power Good monitor Output >>
PG1
PG2
PG3
PG4
PGL2
pg1
pg2
pg3
pg4
pgl2
<< Watchdog Timer >>
Watchdog Timer
clk
pgl1
RST
WDI
GND

6. Absolute Maximum Ratings

Table 6-1 Absolute Maximum Ratings

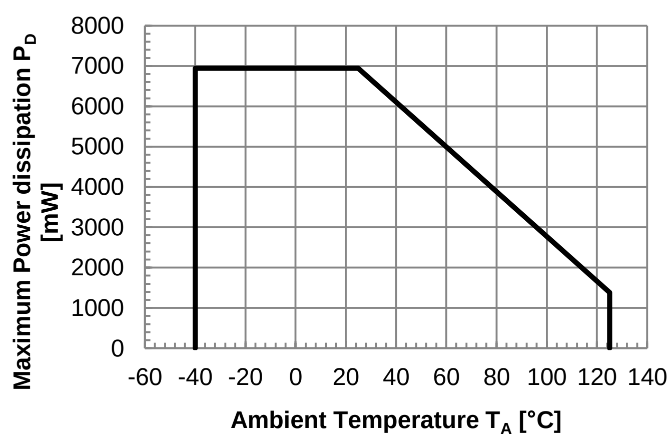
Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{VCC}	VCC	-0.3	+6.9	V
	V_{PVCC}	PVCC1, PVCC2, PVCC3, PVCC4	-0.3	+6.9	V
	V_{PVCCL}	PVCCL1, PVCCL2	-0.3	+6.9	V
Input voltage	V_{EN}	EN1, EN2, EN3, EN4, ENL1, ENL2	-0.3	+6.9	V
	V_{WDI}	WDI	-0.3	+6.9	V
	V_{SYNC}	SYNC	-0.3	+6.9	V
	V_{FB}	FB1, FB2, FB3, FB4	-0.3	+6.9	V
	V_{PG}	PG1, PG2, PG3, PG4, PGL2	-0.3	+6.9	V
	V_{RST}	RST	-0.3	+6.9	V
LX voltage	V_{LX}	LX1, LX2, LX3, LX4	-0.3	+6.9	V
Voltage difference	$V_{PVCC-VCC}$	PVCC1 -VCC, PVCC2-VCC, PVCC3-VCC, PVCC4-VCC	-0.3	+0.3	V
	$V_{PGND-GND}$	PGND1-GND, PGND2-GND, PGND3-GND, PGND4-GND	-0.3	+0.3	V
	$V_{PVCC-LX}$	PVCC1-LX1, PVCC2-LX2, PVCC3-LX3, PVCC4-LX4	-0.3	+6.9	V
	$V_{VCC-INPUT}$	VCC-EN1, VCC-EN2, VCC-EN3, VCC-EN4, VCC-EN1L, VCC-EN2L, VCC-WDI, VCC-SYNC, VCC-FB1, VCC-FB2, VCC-FB3, VCC-FB4	-0.3	+6.9	V
Power dissipation	P_D	$T_A \leq + 25$ °C, Thermal resistance (θ_{JA}): 18 °C /W (*1)	-	6940	mW
Junction temperature	T_J	-	-40	+150	°C
Storage temperature	T_{STG}	-	-55	+150	°C

*1: When the IC is mounted on 76.2 mm × 114.3 mm four-layer epoxy board. IC is mounted on a four-layer epoxy board, which terminal bias, and the IC's thermal pad is connected to the epoxy board.

WARNING

1. *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.*

Figure 6-1 Maximum Power Dissipation - Operating Ambient Temperature Characteristics



7. Recommended Operating Conditions

Table 7-1 Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{VCC}	VCC	+4.5	+5.0	+5.5	V
	V_{PVCC}	PVCC1, PVCC2, PVCC3, PVCC4	-	V_{VCC}	-	V
	V_{PVCCL}	PVCCL1, PVCCL2	+2.97	+5.0	V_{VCC}	V
Input voltage	V_{EN}	EN1, EN2, EN3, EN4, ENL1, ENL2	0	-	V_{VCC}	V
	V_{WDI}	WDI	0	-	V_{VCC}	V
	V_{SYNC}	SYNC	0	-	V_{VCC}	V
	V_{FB}	FB1, FB2, FB3, FB4	0	-	V_{VCC}	V
	V_{PG}	PG1, PG2, PG3, PG4, PGL2	0	-	+5.5	V
	V_{RST}	RST	0	-	+5.5	V
Operating ambient temperature	T_A	-	-40	+25	+125	°C

WARNING:

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*
2. *Any use of semiconductor devices will be under their recommended operating condition.*
3. *Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.*
4. *No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.*

8. Electrical Characteristics

V_{VCC} = V_{PVCC} = 5.0 V, V_{PVCCL} = 5.0 V, T_A = T_J = -40 to +125 °C, unless otherwise noted. Typical values are at T_A = +25 °C.

Table 8-1 Electrical Characteristics

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Supply Current						
Shutdown current	I_{VCCS}	VCC pin, V_{EN1} = V_{EN2} = V_{EN3} = V_{EN4} = V_{ENL1} = V_{ENL2} = 0 V	-	1	10	µA
UVLO: Under Voltage Lockout (VCC)						
Threshold voltage	V_{UVLOF}	V_{VCC} falling, UVLO stop voltage	3.80	3.95	4.10	V
Hysteresis	V_{UVHYS}	-	0.27	0.30	0.33	V
TSD: Thermal Shutdown						
Shutdown temperature	T_{TSD}	Temperature rising	-	165 (*1)	-	°C
Hysteresis	T_{TSDHYS}	-	-	10 (*1)	-	°C
Enable Inputs (EN1, EN2, EN3, EN4, ENL1, ENL2)						
Input high voltage	V_{IHEN}	-	2.0	-	V_{VCC}	V
Input low voltage	V_{ILEN}	-	0	-	0.4	V
Input current	I_{IHEN}	V_{EN} = 5.0 V	33	50	100	µA
Pull down resistance	R_{PDEN}	-	50	100	150	kΩ
Internal Linear Regulator Output (VREG)						
Output voltage	V_{VREG}	V_{VCC} = 5.0 V	1.74	1.80	1.86	V
Maximum output current	I_{VREG}	V_{VCC} = 5.0 V	5	-	-	mA
Over voltage lockout threshold	$V_{VREGOVR}$	V_{VREG} rising, Power fail	1.86	1.92	1.98	V
	$V_{VREGOVF}$	V_{VREG} falling, Power good	1.81	1.87	1.93	V
Under voltage lockout threshold	$V_{VREGUVR}$	V_{VREG} rising, Power good	1.67	1.73	1.79	V
	$V_{VREGUVF}$	V_{VREG} falling, Power fail	1.62	1.68	1.74	V
Oscillator						
Switching frequency	f_{OSC}	-	2.0	2.1	2.2	MHz
Synchronization Input (SYNC)						
Input high voltage	V_{IHSYNC}	-	2.0	-	V_{VCC}	V
Input Low voltage	V_{ILSYNC}	-	0	-	0.4	V
Input current	I_{IHSYNC}	V_{EN} = 5.0 V	33	50	100	µA
Pull down resistance	R_{PDSYNC}	-	50	100	150	kΩ
Input frequency	f_{SYNC}	-	1.8	2.1	2.4	MHz
Switching frequency	f_{OSC}	-	-	f_{SYNC}	-	MHz

Parameter	Symbol	Condition	Value Min	Value Typ	Value Max	Unit
Power Good Monitor (PG1, PG2, PGL2)						
Over voltage threshold	V_{PGOV}	Ratio of power fail threshold to V_{OUT1}, V_{OUT2}, V_{OUTL2} rising	104.5	106.0	107.5	%
Over voltage hysteresis	$V_{PGOVHYS}$	-	0.5	1.0	1.5	%
Under voltage threshold	V_{PGUV}	Ratio of power fail threshold to V_{OUT1}, V_{OUT2}, V_{OUT3} falling	92.5	94.0	95.5	%
Under voltage hysteresis	$V_{PGUVHYS}$	-	0.5	1.0	1.5	%
Leakage current	I_{LEAKPG}	V_{PG} = 5.0 V	-	-	1	µA
Output low voltage	V_{OLPG}	I_{PG} = 3 mA	-	0.15	0.30	V
Propagation time	T_{PPG}	5 % outside of the threshold, Power fail	-	4 (*1)	8 (*1)	µs
Power-on reset time	T_{RPG}	Power good	8	10	12	ms
Power Good Monitor (PG3)						
Over voltage threshold	V_{PGOV}	Ratio of power fail threshold to V_{OUT3} rising	104.5	106.0	107.5	%
Over voltage hysteresis	$V_{PGOVHYS}$	-	0.5	1.0	1.5	%
Under voltage threshold	V_{PGUV}	Ratio of power fail threshold to V_{OUT3} falling	93.7	95.2	96.7	%
Under voltage hysteresis	$V_{PGUVHYS}$	-	0.5	1.0	1.5	%
Leakage current	I_{LEAKPG}	V_{PG} = 5.0 V	-	-	1	µA
Output low voltage	V_{OLPG}	I_{PG} = 3 mA	-	0.15	0.30	V
Propagation time	T_{PPG}	5 % outside of the threshold, Power fail	-	4 (*1)	8 (*1)	µs
Power-on reset time	T_{RPG}	Power good	8	10	12	ms
Power Good Monitor (PG4)						
Over voltage threshold	V_{PGOV}	Ratio of power fail threshold to V_{OUT4} rising	104.5	106.0	107.5	%
Over voltage hysteresis	$V_{PGOVHYS}$	-	0.5	1.0	1.5	%
Under voltage threshold	V_{PGUV}	Ratio of power fail threshold to V_{OUT4} falling	94.0	95.5	97.0	%
Under voltage hysteresis	$V_{PGUVHYS}$	-	0.5	1.0	1.5	%
Leakage current	I_{LEAKPG}	V_{PG} = 5.0 V	-	-	1	µA
Output low voltage	V_{OLPG}	I_{PG} = 3 mA	-	0.15	0.30	V
Propagation time	T_{PPG}	5 % outside of the threshold, Power fail	-	4 (*1)	8 (*1)	µs
Power-on reset time	T_{RPG}	Power good	8	10	12	ms
Reset (RST)						
Over voltage threshold	V_{RSOV}	Ratio of power fail threshold to V_{OUTL1} rising	104.5	106.0	107.5	%
Over voltage hysteresis	$V_{RSOVHYS}$	-	0.5	1.0	1.5	%
Under voltage threshold	V_{RSUV}	Ratio of power fail threshold to V_{OUTL1} falling	92.5	94.0	95.5	%
Under voltage hysteresis	$V_{RSUVHYS}$	-	0.5	1.0	1.5	%
Leakage current	$I_{LEAKRST}$	V_{RST} = 5.0 V	-	-	1	µA
Output low voltage	V_{OLRST}	I_{PG} = 3 mA	-	0.15	0.30	V
Propagation time	T_{PRST}	5 % outside of the threshold, Power fail	-	4 (*1)	8 (*1)	µs
Power-on reset time	T_{RD}	Power good	25.6	32.0	38.4	ms

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Watchdog Timer (WDI)						
Watchdog sampling time	T_{SAM}	-	0.40	0.50	0.60	ms
Ignore window time	T_{IW}	-	25.6	32.0	38.4	ms
Open window time	T_{OW}	-	25.6	32.0	38.4	ms
Long open window time	T_{LOW}	-	102.4	128.0	153.6	ms
Closed window time	T_{CW}	-	25.6	32.0	38.4	ms
Window watchdog trigger time	T_{WD}	-	38.4	48	51.2	ms
Input high voltage	V_{IHWDI}	-	2.0	-	V_{VCC}	V
Input low voltage	V_{ILWDI}	-	0	-	0.4	V
Input current	I_{IHWDI}	V_{WDI} = 5.0 V	33	50	100	µA
Pull down resistance	R_{PDWDI}	-	50	100	150	kΩ
DD1: Buck DC/DC Converter						
Output voltage accuracy	V_{OUT1}	V_{VCC} = 5.0 V, I_{OUT1} = 10 mA	-1.8	0	+1.8	%
DC regulation	V_{REG1}	V_{VCC} = V_{PVCC1} = 4.5 to 5.5 V, I_{OUT1} = 0 to 2.0 A	-15 (*1)	0	+5 (*1)	mV
FB1 input resistance	R_{FB1}	V_{FB1} = 2.0 V	95	190	285	kΩ
Switching FET ON resistance	R_{ONHS1}	I_{LX1} = 20 mA (PVCC1 to LX1)	-	100	190	mΩ
	R_{ONLS1}	I_{LX1} = -20 mA (LX1 to PGND1)	-	65	125	mΩ
Switching FET leakage current	I_{LEAK1}	I_{PVCC1} = 5.0 V	-	1	10	µA
Maximum output current	I_{OUT1}	L = 1.5 µH	2 (*1)	-	-	A
LX1 peak current limit	I_{LIMIT1}	L = 1.5 µH	2.5 (*1)	-	-	A
Over voltage protection threshold	V_{OVP1}	V_{OUT1} rising, Switching termination threshold	125.0	130.0	135.0	%
Over voltage protection hysteresis	$V_{OVPHYS1}$	-	2.0	5.0	8.0	%
FB1 discharge resistance	R_{DIS1}	-	160	400	640	Ω
Soft-start time coefficient	T_{COESS1}	T_{SS1} = V_{OUT1} x T_{COESS1}	0.9	1.0	1.1	ms/V
DD2: Buck DC/DC Converter						
Output voltage accuracy	V_{OUT2}	V_{VCC} = 5.0 V, I_{OUT2} = 10 mA	-1.8	0	+1.8	%
DC regulation	V_{REG2}	V_{VCC} = V_{PVCC2} = 4.5 to 5.5 V I_{OUT2} = 0 to 3.0 A	-15 (*1)	0	+5 (*1)	mV
FB2 input resistance	R_{FB2}	V_{FB2} = 2.0 V	95	190	285	kΩ
Switching FET ON resistance	R_{ONHS2}	I_{LX2} = 20 mA (PVCC2 to LX2)	-	85	165	mΩ
	R_{ONLS2}	I_{LX2} = -20 mA (LX2 to PGND2)	-	55	105	mΩ
Switching FET leakage current	I_{LEAK2}	I_{PVCC2} = 5.0 V	-	1	10	µA
Maximum output current	I_{OUT2}	L = 1.5 µH	3 (*1)	-	-	A
LX2 peak current limit	I_{LIMIT2}	L = 1.5 µH	3.5 (*1)	-	-	A
Over voltage protection threshold	V_{OVP2}	V_{OUT2} rising, Switching termination threshold	125.0	130.0	135.0	%
Over voltage protection hysteresis	$V_{OVPHYS2}$	-	2.0	5.0	8.0	%
FB2 discharge resistance	R_{DIS2}	-	160	400	640	Ω
Soft-start time coefficient	T_{COESS2}	T_{SS2} = V_{OUT2} x T_{COESS2}	0.9	1.0	1.1	ms/V

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
DD3: Buck DC/DC Converter						
Output voltage accuracy	V_{OUT3}	V_{VCC} = 5.0 V, I_{OUT3} = 10 mA	-1.8	0	+1.8	%
DC regulation	V_{REG3}	V_{VCC} = V_{PVCC3} = 4.5 to 5.5 V, I_{OUT3} = 0 to 2.0 A	-15 (*1)	0	+5 (*1)	mV
FB3 input resistance	R_{FB3}	V_{FB3} = 2.0 V	95	190	285	kΩ
Switching FET ON resistance	R_{ONHS3}	I_{LX3} = 20 mA (PVCC3 to LX3)	-	100	190	mΩ
	R_{ONLS3}	I_{LX3} = -20 mA (LX3 to PGND3)	-	65	125	mΩ
Switching FET leakage current	I_{LEAK3}	I_{PVCC3} = 5.0 V	-	1	10	µA
Maximum output current	I_{OUT3}	L = 1.5 µH	2 (*1)	-	-	A
LX3 peak current limit	I_{LIMIT3}	L = 1.5 µH	2.5 (*1)	-	-	A
Over voltage protection threshold	V_{OVP3}	V_{OUT3} rising, Switching termination threshold	125.0	130.0	135.0	%
Over voltage protection hysteresis	$V_{OVPHYS3}$	-	2.0	5.0	8.0	%
FB3 discharge resistance	R_{DIS3}	-	160	400	640	Ω
Soft-start time coefficient	T_{COESS3}	T_{SS3} = V_{OUT3} × T_{COESS3}	0.9	1.0	1.1	ms/V
DD4: Buck DC/DC Converter						
Output voltage accuracy	V_{OUT4}	V_{VCC} = 5.0 V, I_{OUT4} = 10 mA	-1.8	0	+1.8	%
DC regulation	V_{REG4}	V_{VCC} = V_{PVCC4} = 4.5 to 5.5 V, I_{OUT4} = 0 to 1.0 A	-15 (*1)	0	+5 (*1)	mV
FB4 input resistance	R_{FB4}	V_{FB4} = 2.0 V	95	190	285	kΩ
Switching FET ON resistance	R_{ONHS4}	I_{LX4} = 20 mA (PVCC4 to LX4)	-	100	190	mΩ
	R_{ONLS4}	I_{LX4} = -20 mA (LX4 to PGND4)	-	65	125	mΩ
Switching FET leakage current	I_{LEAK4}	I_{PVCC4} = 5.0 V	-	1	10	µA
Maximum output current	I_{OUT4}	L = 1.5 µH	1 (*1)	-	-	A
LX4 peak current limit	I_{LIMIT4}	L = 1.5 µH	1.5 (*1)	-	-	A
Over voltage protection threshold	V_{OVP4}	V_{OUT4} rising, Switching termination threshold	125.0	130.0	135.0	%
Over voltage protection hysteresis	$V_{OVPHYS4}$	-	2.0	5.0	8.0	%
FB4 discharge resistance	R_{DIS4}	-	160	400	640	Ω
Soft-start time coefficient	T_{COESS4}	T_{SS4} = V_{OUT4} × T_{COESS4}	0.9	1.0	1.1	ms/V

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
LD1: LDO Regulator						
Output voltage accuracy	V_{OUTL1}	V_{VCC} = 5.0 V, I_{OUTL1} = 10 mA	-1.8	0	+1.8	%
DC regulation	V_{REGL1}	V_{VCC} = 4.5 to 5.5 V, V_{PVCCL1} = 2.97 to V_{VCC} I_{OUTL1} = 0 to I_{OUTL1}	-15 (*1)	0	+5 (*1)	mV
Output FET leakage current	I_{LEAKL1}	I_{PVCCL1} = 5.0 V	-	1	10	µA
Maximum output current	I_{OUTL1}	V_{PVCCL1} - V_{OUTL1} ≥ 1.6 V	200 (*1)	-	-	mA
		0.17 V ≤ V_{PVCCL1} - V_{OUTL1} < 1.6 V	100 (*1)	-	-	mA
Output current limit	$I_{LIMITL1}$	V_{PVCCL1} - V_{OUTL1} ≥ 1.6 V	210 (*1)	-	-	mA
		0.17 V ≤ V_{PVCCL1} - V_{OUTL1} < 1.6 V	105 (*1)	-	-	mA
LDO1 discharge resistance	R_{DISL1}	-	160	400	640	Ω
Soft-start time coefficient	$T_{COESSL1}$	$T_{SSL1} = V_{OUTL1} \times T_{COESSL1}$	0.9	1.0	1.1	ms/V
LD2: LDO Regulator						
Output voltage accuracy	V_{OUTL2}	V_{VCC} = 5.0 V, I_{OUTL2} = 10 mA	-1.8	0	+1.8	%
DC regulation	V_{REGL2}	V_{VCC} = 4.5 to 5.5 V, V_{PVCCL2} = 2.97 to V_{VCC} I_{OUTL2} = 0 to I_{OUTL2}	-15 (*1)	0	+5 (*1)	mV
Output FET leakage current	I_{LEAKL2}	I_{PVCCL2} = 5.0 V	-	1	10	µA
Maximum output current	I_{OUTL2}	V_{PVCCL2} - V_{OUTL2} ≥ 1.6 V	500 (*1)	-	-	mA
		0.17 V ≤ V_{PVCCL2} - V_{OUTL2} < 1.6 V	400 (*1)	-	-	mA
Output current limit	$I_{LIMITL2}$	V_{PVCCL2} - V_{OUTL2} ≥ 1.6 V	525 (*1)	-	-	mA
		0.17 V ≤ V_{PVCCL2} - V_{OUTL2} < 1.6 V	420 (*1)	-	-	mA
LDO2 discharge resistance	R_{DISL2}	-	160	400	640	Ω
Soft-start time coefficient	$T_{COESSL2}$	$T_{SSL2} = V_{OUTL2} \times T_{COESSL2}$	0.9	1.0	1.1	ms/V

*1: The electrical characteristic is ensured by statistical characterization and indirect tests.

9. Operating Mode List

Table 9-1 shows the operation list of S6BP401A.

Table 9-1 Operation Mode List

Condition					Operating Block				
T_J	SYNC	ENL1	EN1/ EN2/ EN3/ EN4/ ENL2	Chip Control	VREG LDO	Watch-dog Trigger Monitor	Freq. Sync.	LD1	DD1/ DD2/ DD3/ DD4/ LD2
< T_{TSD}	L or H	L	L	OFF	OFF	OFF	OFF	OFF	OFF
< T_{TSD}	L or H	L	H	ON	ON	OFF	OFF	OFF	ON
< T_{TSD}	L or H	H	L	ON	ON	ON	OFF	ON	OFF
< T_{TSD}	L or H	H	H	ON	ON	ON	OFF	ON	ON
< T_{TSD}	clock	L	L	OFF	OFF	OFF	OFF	OFF	OFF
< T_{TSD}	clock	L	H	ON	ON	OFF	ON	OFF	ON
< T_{TSD}	clock	H	L	ON	ON	ON	ON	ON	OFF
< T_{TSD}	clock	H	H	ON	ON	ON	ON	ON	ON
≥ T_{TSD}	L or H	L	L	OFF	OFF	OFF	OFF	OFF	OFF
≥ T_{TSD}	L or H	L	H	ON	ON	OFF	OFF	OFF	OFF
≥ T_{TSD}	L or H	H	L	ON	ON	OFF	OFF	OFF	OFF
≥ T_{TSD}	L or H	H	H	ON	ON	OFF	OFF	OFF	OFF
≥ T_{TSD}	clock	L	L	OFF	OFF	OFF	OFF	OFF	OFF
≥ T_{TSD}	clock	L	H	ON	ON	OFF	OFF	OFF	OFF
≥ T_{TSD}	clock	H	L	ON	ON	OFF	OFF	OFF	OFF
≥ T_{TSD}	clock	H	H	ON	ON	OFF	OFF	OFF	OFF

10. Function

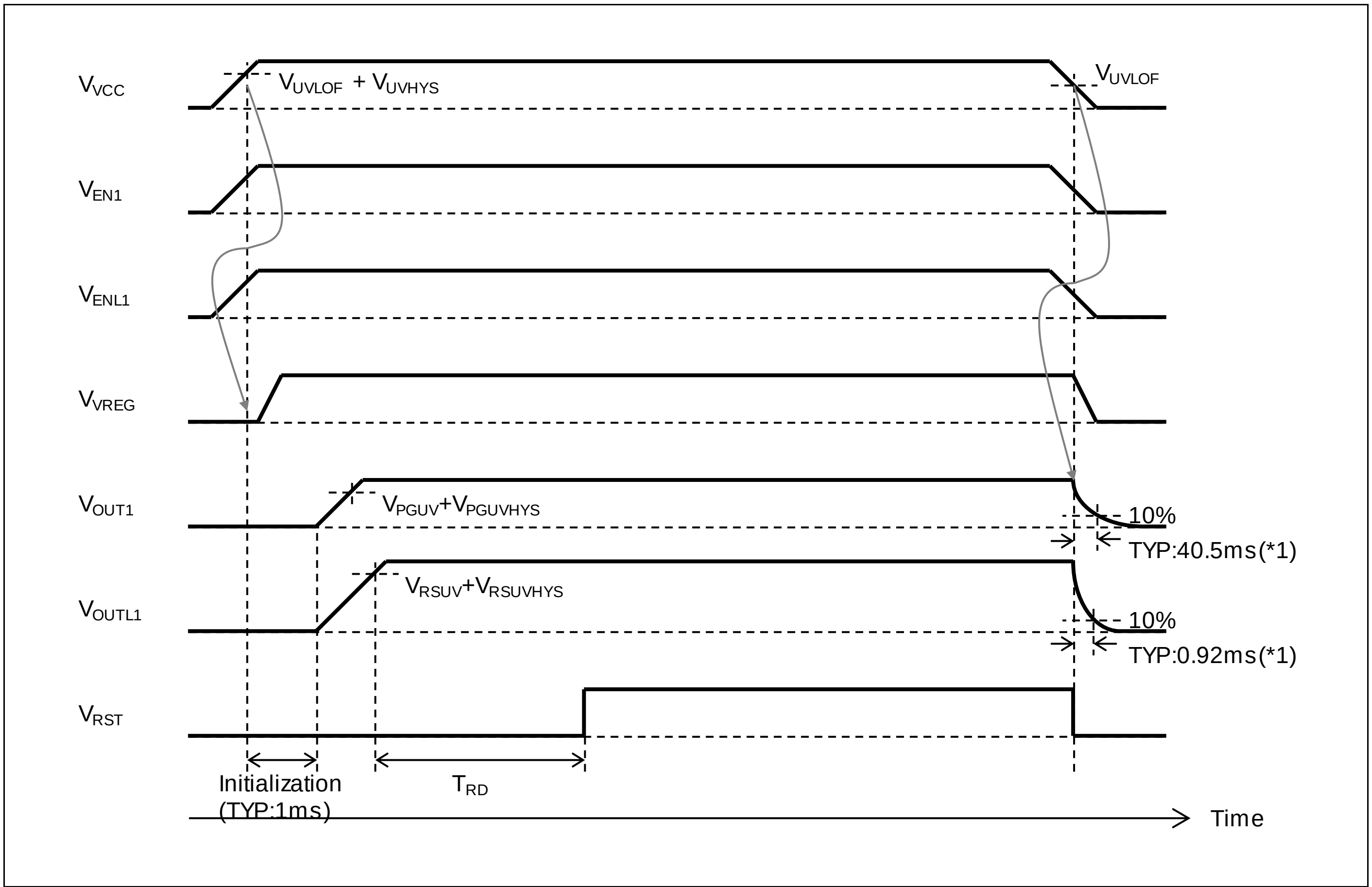
10.1 Turning ON and OFF Sequence

When all of the enable input terminals (EN1, EN2, EN3, EN4, ENL1 and ENL2) are "Low", the device is in shutdown state. When any one or more than one of them go "High," the device is initialized, then the internal linear regulator (VREG) starts generating 1.8 V internal supply voltage. After that, each DC/DC converters and LDOs state is transitioned to the state which can be started.

In order for the device to start, the VCC terminal voltage must be higher than the under-voltage lockout threshold (V_{UVLOF} + V_{UVHYS}).

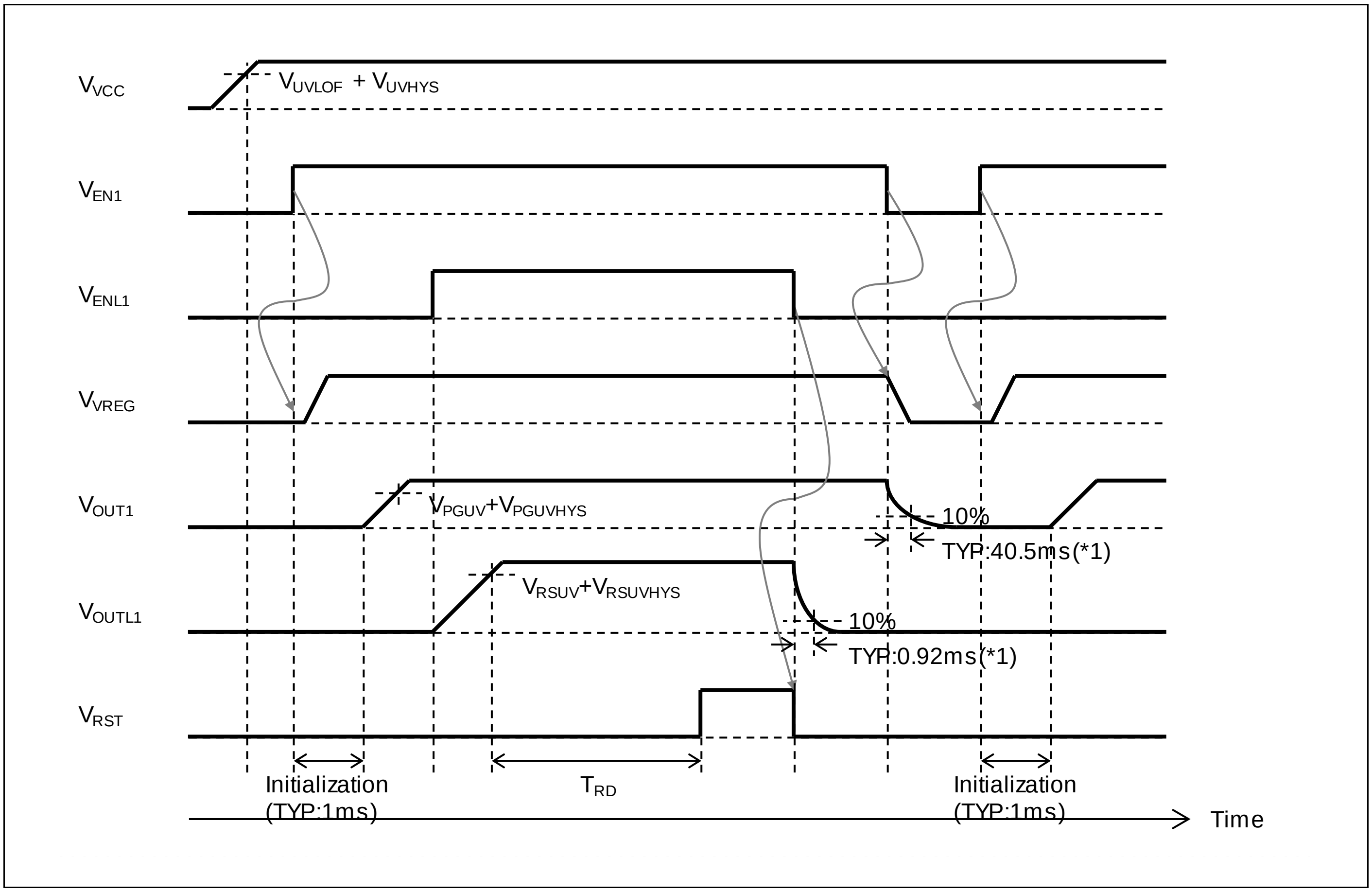
Figure 10-1 depicts the turning-on and off sequence where the enable signals are connected to VCC. Figure 10-2 depicts that where the enable signals are respectively controlled after the IC is powered.

Figure 10-1 Turning ON and OFF Sequence (where EN1 and ENL1 are Connected to VCC)



*1: Given that the system employs the same external parts with those specified in "11. Application Circuit Example".

Figure 10-2 Turning ON and OFF Sequence (where EN1 and ENL1 are Respectively Controlled)



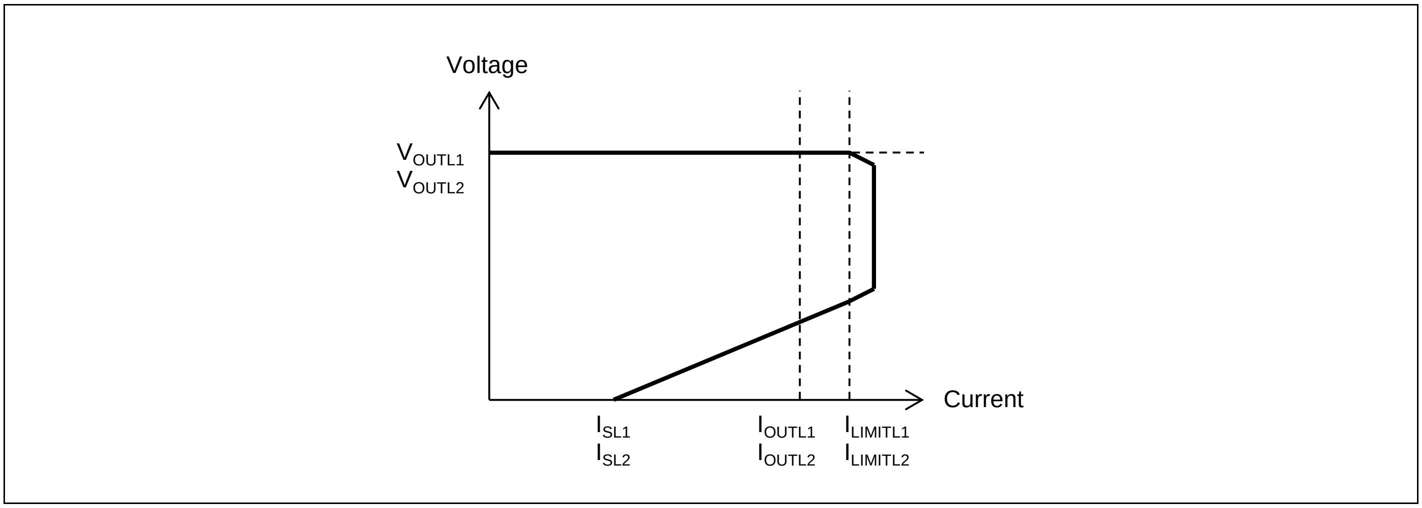
*1: Given that the system employs the same external parts with those specified in "11. Application Circuit Example".

10.2 Over Current Protection

The over current protection of the DC/DC converters detects the inductor peak current with on-resistance of Internal high side switching FET. If the DC/DC converter is over current state, the corresponding output voltage is decreased. If the device returns from over current state, the output voltage is target voltage.

Each LDOs equips foldback current limiter in order to prevent the IC itself from being damaged or destroyed. The curve of output current and output voltage in over current state is shown in the Figure 10-3.

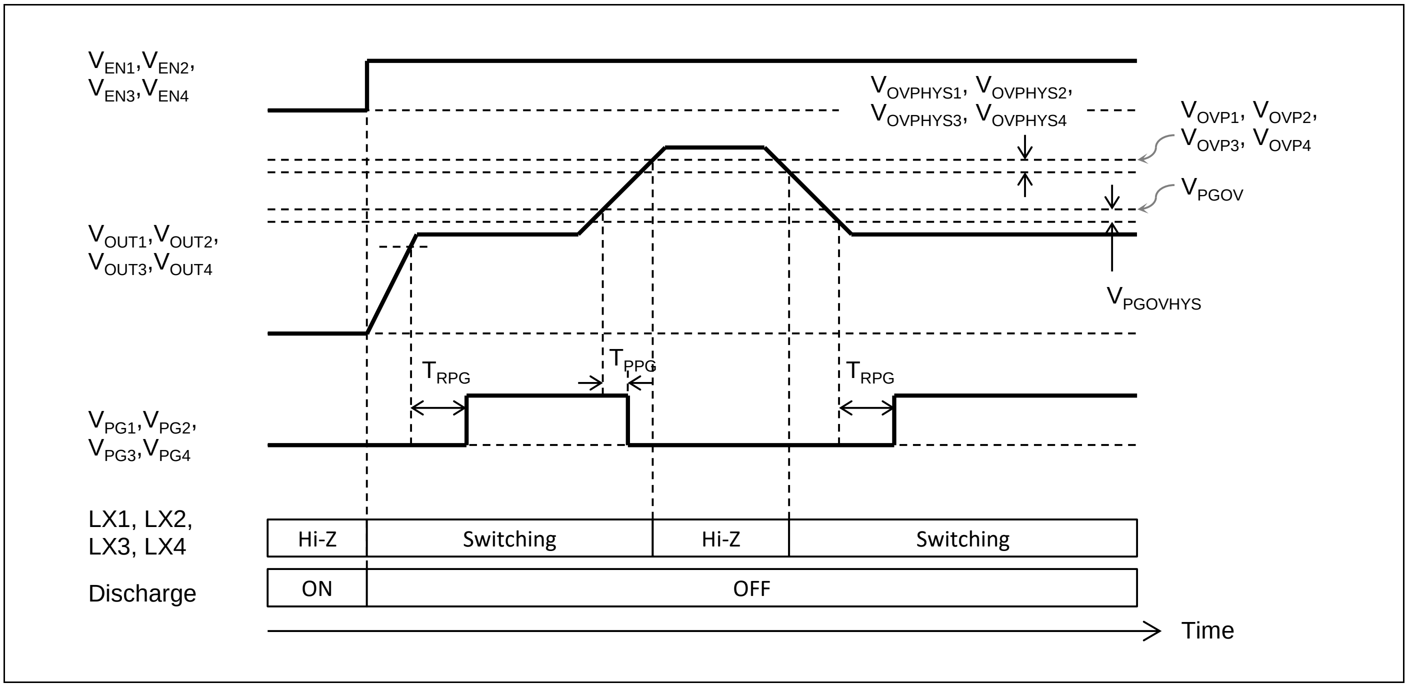
Figure 10-3 LDO Foldback Over Current Protection Characteristic



10.3 Over Voltage Protection

The over voltage protection of the DC/DC converters detects the output voltage. If the DC/DC converter is over voltage state, the corresponding channel stops switching and inductor connecting terminal (LX1, LX2, LX3, LX4) is held at high impedance. If the device returns from over voltage state, the channel returns switching automatically.

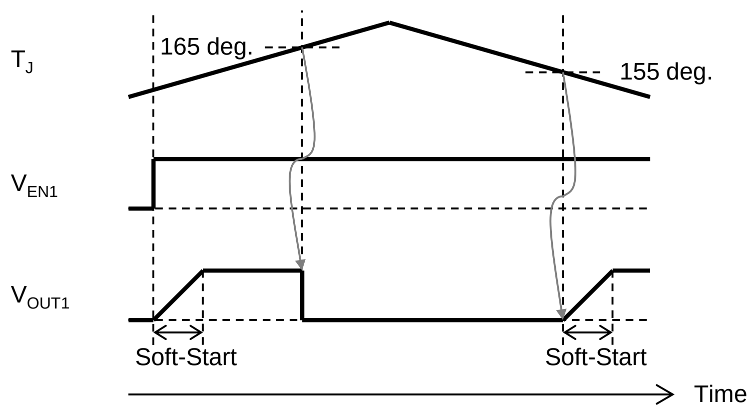
Figure 10-4 Over Voltage Protection Timing Chart



10.4 Thermal Shutdown (TSD)

If the junction temperature reaches +165 °C, all DC/DC converters and LDOs stop outputting voltage. Then the discharge operation is carried out to discharge the output capacitor (The discharge operation continues until the state of the thermal shutdown released.) When the junction temperature drops below +155 °C, the soft-starters activate regulators and start generating voltage gradually if the enable is "High."

Figure 10-5 Thermal Shutdown Timing Chart



10.5 Under Voltage Lockout (UVLO)

If the VCC terminal voltage (V_{VCC}) drops below the lower UVLO threshold (V_{UVLOF}), all DC/DC converters (DD1, DD2, DD3, DD4), LDOs (LD1, LD2), windowed watchdog timer (WDT) and the internal linear regulator (VREG) stop working. When the VCC terminal voltage (V_{VCC}) is raised higher than the higher UVLO threshold (V_{UVLOF} + V_{UVHYS}), the device returns automatically.

10.6 Soft-Start Operation

S6BP401A equips load-independent soft-start function in order to prevent the DC/DC converters and LDOs from having rush current at the start-up. The soft-start timing is shown in the Figure 10-6, and is given by the following equation;

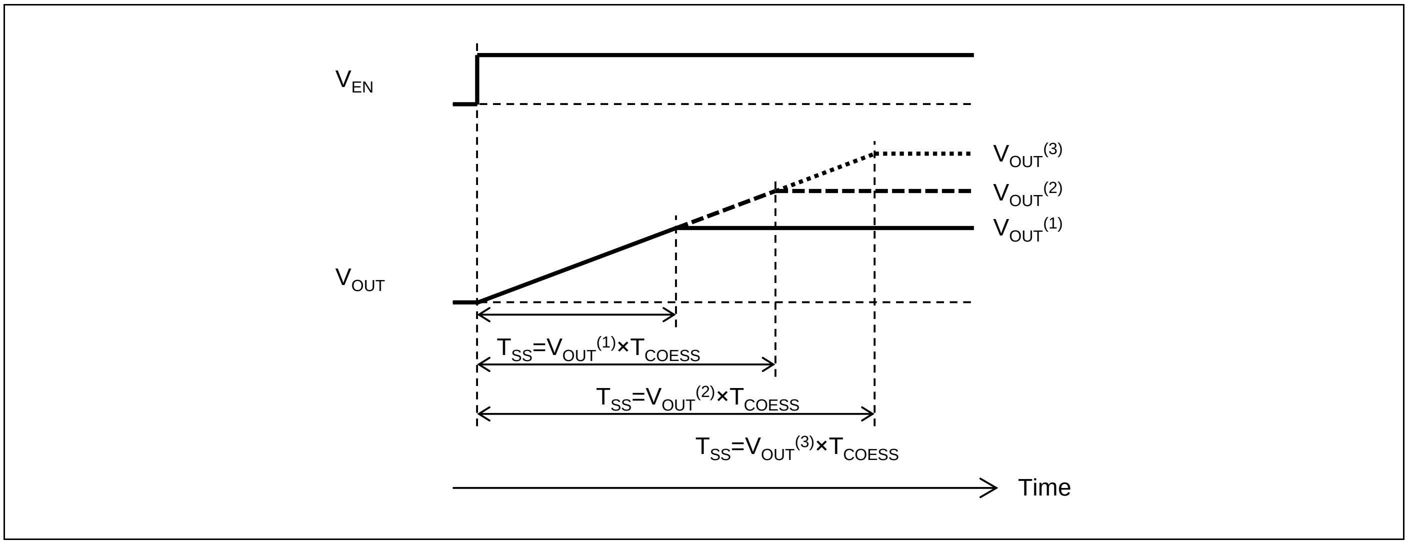
$$T_{SS} = V_{OUT} \times T_{COESS}, \text{ where}$$

T_{SS} [ms] : Soft-start time

V_{OUT} [V] : Output voltage (V_{OUT1}, V_{OUT2}, V_{OUT3}, V_{OUT4}, V_{OUTL1}, V_{OUTL2})

T_{COESS} [ms/V] : Soft-start time coefficient (T_{COESS1}, T_{COESS2}, T_{COESS3}, T_{COESS4}, $T_{COESSL1}$, $T_{COESSL2}$)

Figure 10-6 Soft-Start Operation Timing Chart



10.7 Discharge Operation

When an enable signal goes "Low", the corresponding output capacitor is discharged by the internal discharge resistor and the output voltage is decreased gradually. Note that the discharge time is not consistent: it depends on the output load current.

As for a DC/DC converter, the output capacitor is discharged from FB1, FB2, FB3 and FB4 terminal to PGND1, PGND2, PGND3 and PGND4 terminal respectively. As for a LDO, the output capacitor is dis-charged from LDO1, LDO2 terminal to GND terminal.

The discharge time required to decrease the output voltage by 90 % without any explicit load given by the following equation;

$$T_{DIS} = 2.3 \times R_{DIS} \times C_{OUT}, \text{ where}$$

T_{DIS} [ms] : Discharge time

R_{DIS} [kΩ] : Discharge resistance (R_{DIS1}, R_{DIS2}, R_{DIS3}, R_{DIS4}, R_{DISL1}, R_{DISL2})

C_{OUT} [µF] : Output capacitor

Figure 10-7 Discharge Diagram (DC/DC Converter)

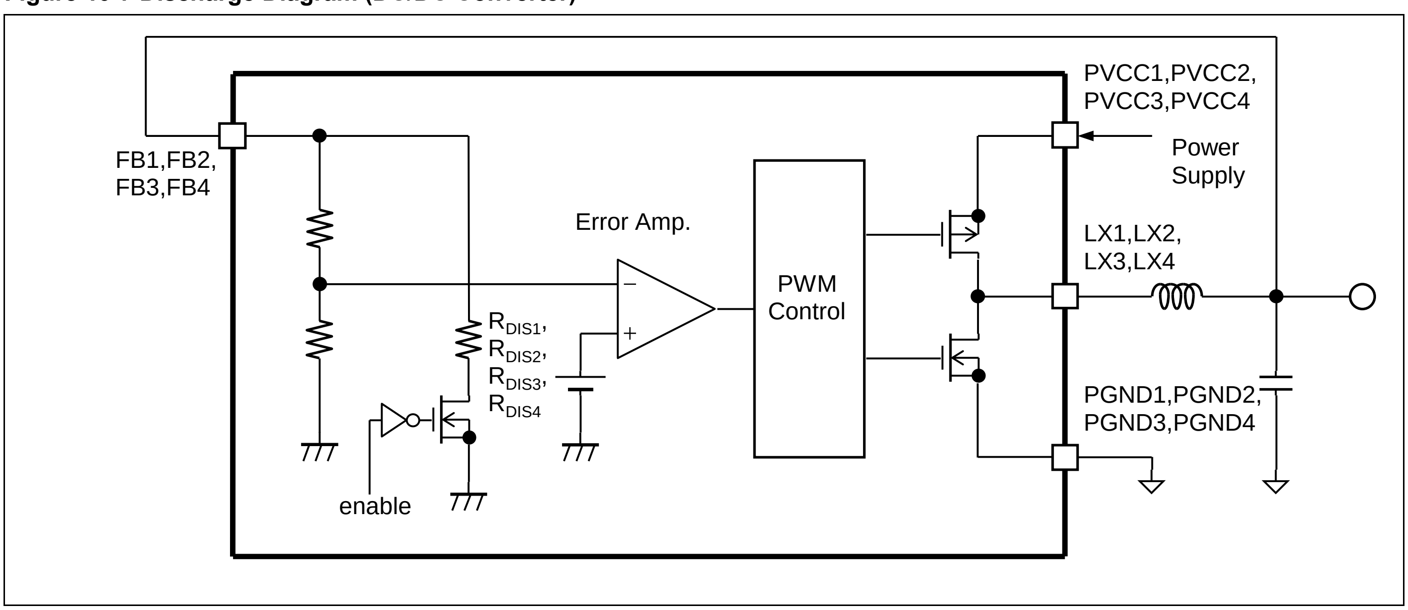
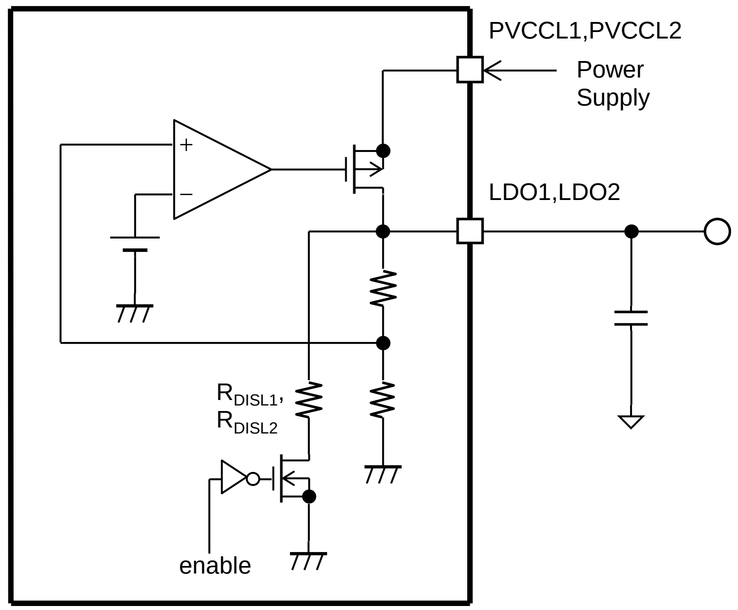


Figure 10-8 Discharge Diagram (LDO)



10.8 Power Good Monitor and Reset Function

Each DC/DC converters and LDOs has power good function to indicate whether the output voltage is in the expected range. The Table 10-1 describes the power good pin names and their functions of each DC/DC converters and LDOs. The Figure 10-9 and Figure 10-10 depict power-good timing chart.

Table 10-1 Power Good Monitor and Reset Function Pin List

Channel	Pin Name	Description
DD1	PG1	Enabling DD1 is followed by rising of the DD1 output voltage (V_{OUT1}). Once V_{OUT1} reaches within the power good range ($V_{PGUV} + V_{PGUVHYS} < V_{OUT1} < V_{PGOV} – V_{PGOVHYS}$), the power good monitor output (PG1 terminal) changes its state from “Low” to “Open” after a power-on-reset time (T_{RPG}). When V_{OUT1} is out of the power good range ($V_{OUT1} \leq V_{PGUV}$ or $V_{OUT1} \geq V_{PGOV}$), PG1 terminal changes its state from “Open” to “Low” after the propagation delay (T_{PPG}). The glitch within T_{PPG} does not affect the power good monitor output.
DD2	PG2	Enabling DD2 is followed by rising of the DD2 output voltage (V_{OUT2}). Once V_{OUT2} reaches within the power good range ($V_{PGUV} + V_{PGUVHYS} < V_{OUT2} < V_{PGOV} – V_{PGOVHYS}$), the power good monitor output (PG2 terminal) changes its state from “Low” to “Open” after a power-on-reset time (T_{RPG}). When V_{OUT2} is out of the power good range ($V_{OUT2} \leq V_{PGUV}$ or $V_{OUT2} \geq V_{PGOV}$), PG2 terminal changes its state from “Open” to “Low” after the propagation delay (T_{PPG}). The glitch within T_{PPG} does not affect the power good monitor output.
DD3	PG3	Enabling DD3 is followed by rising of the DD3 output voltage (V_{OUT3}). Once V_{OUT3} reaches within the power good range ($V_{PGUV} + V_{PGUVHYS} < V_{OUT3} < V_{PGOV} – V_{PGOVHYS}$), the power good monitor output (PG3 terminal) changes its state from “Low” to “Open” after a power-on-reset time (T_{RPG}). When V_{OUT3} is out of the power good range ($V_{OUT3} \leq V_{PGUV}$ or $V_{OUT3} \geq V_{PGOV}$), PG3 terminal changes its state from “Open” to “Low” after the propagation delay (T_{PPG}). The glitch within T_{PPG} does not affect the power good monitor output.
DD4	PG4	Enabling DD4 is followed by rising of the DD4 output voltage (V_{OUT4}). Once V_{OUT4} reaches within the power good range ($V_{PGUV} + V_{PGUVHYS} < V_{OUT4} < V_{PGOV} – V_{PGOVHYS}$), the power good monitor output (PG4 terminal) changes its state from “Low” to “Open” after a power-on-reset time (T_{RPG}). When V_{OUT4} is out of the power good range ($V_{OUT4} \leq V_{PGUV}$ or $V_{OUT4} \geq V_{PGOV}$), PG4 terminal changes its state from “Open” to “Low” after the propagation delay (T_{PPG}). The glitch within T_{PPG} does not affect the power good monitor output.

Channel	Pin Name	Description
LD1	RST	Enabling LD1 is followed by rising of the LD1 output voltage (V_{OUTL1}). Once V_{OUTL1} reaches within the power good range ($V_{RSUV} + V_{RSUVHYS} < V_{OUTL1} < V_{RSOV} - V_{RSOVHYS}$), the RST terminal changes its state from “Low” to “Open” after a power-on-reset time (T_{RD}). When V_{OUTL1} is out of the power good range ($V_{OUTL1} \leq V_{RSUV}$ or $V_{OUTL1} \geq V_{RSOV}$), RST terminal changes “Open” to “Low” after the propagation delay (T_{PRST}). The glitch within T_{PRST} does not affect the power good monitor output.
LD2	PGL2	Enabling LD2 is followed by rising of the LD2 output voltage (V_{OUTL2}). Once V_{OUTL2} reaches within the power good range ($V_{PGUV} + V_{PGUVHYS} < V_{OUTL2} < V_{PGOV} – V_{PGOVHYS}$), the power good monitor output (PGL2 terminal) changes its state from “Low” to “Open” through the power-on-reset time (T_{RPG}). When V_{OUTL2} is out of the power good range ($V_{OUTL2} \leq V_{PGUV}$ or $V_{OUTL2} \geq V_{PGOV}$), PGL2 terminal changes “Open” to “Low” after the propagation delay (T_{PPG}). The glitch within T_{PPG} does not affect the power good monitor output.

Figure 10-9 Power-Good Monitor Output Timing Chart (PG1, PG2, PG3, PG4, PGL2)

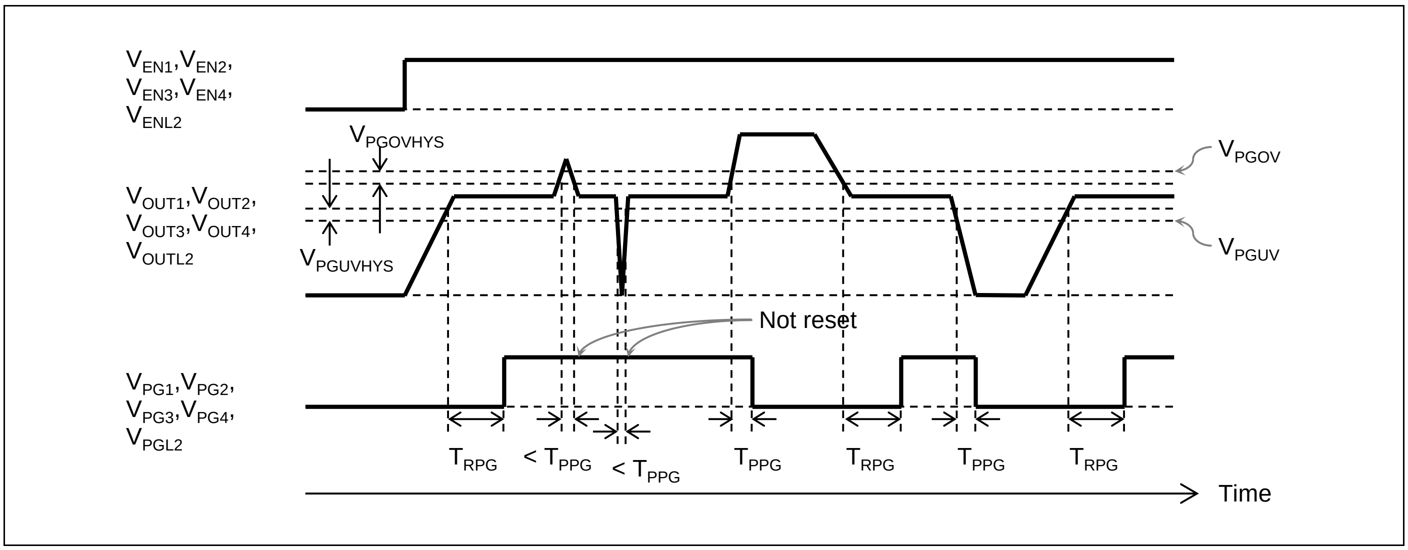
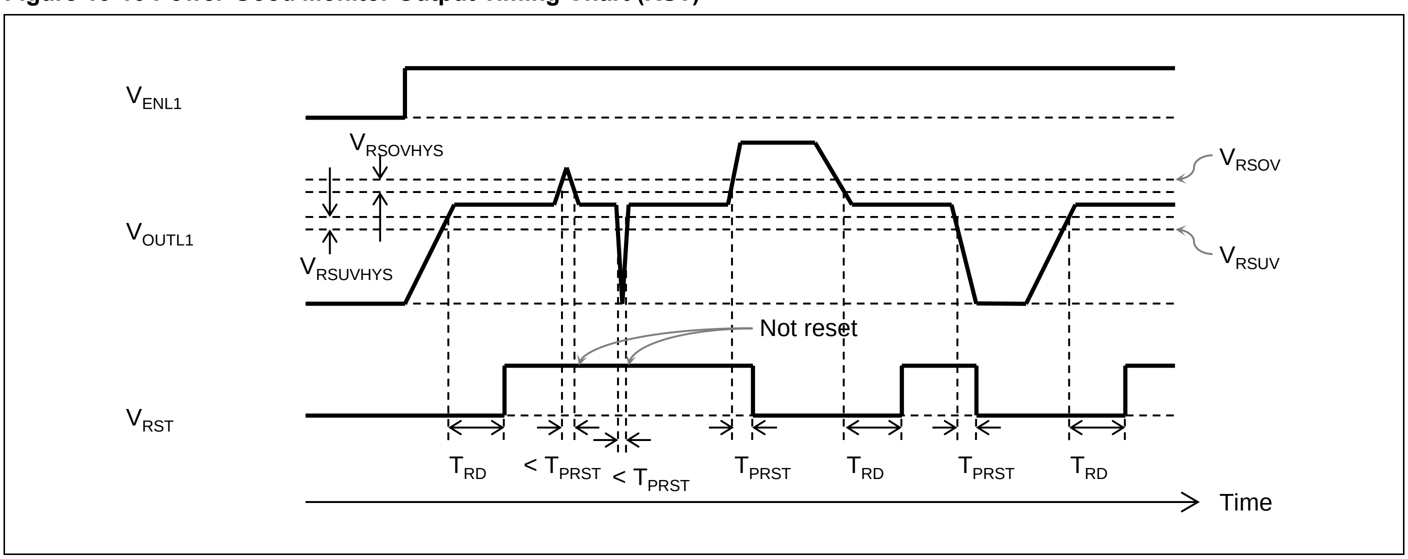


Figure 10-10 Power-Good Monitor Output Timing Chart (RST)



10.9 Watchdog Timer

S6BP401A employs a digital windowed watchdog timer. The digital windowed watchdog timer starts monitoring trigger signal, when the LD1 output voltage (V_{OUTL1}) reaches the power good level after enabling LD1.

Figure 10-11 shows the state diagram of the digital watchdog timer. There are six states in the diagram. In the normal operation, the state is expected to move back and forth between "CW" and "OW",

At first, as described in the section 10.8, enabling LD1 brings "RESET" state, and the "RESET" state is kept for the "Reset Time (T_{RD})" outputting "Low" from RST terminal.

In the second, after T_{RD} in the "RESET" state, the state will transition to "Ignore Window (IW)", and let RST terminal be "Open". The "IW" state will be elapsed in the "Ignore Window Time (T_{IW}.)"

In the third, after elapsing, the state will transition to "Long Open Window (LOW)" state, and let RST terminal be "Open." In this state, a trigger signal is expected to be input: if an input trigger arrives, the state will immediately transition to the "Closed Window (CW)" state. Without an input trigger in the "Long Open Window Time (T_{LOW},)" the state will be elapsed and will transition to "RESET" state.

In the "CW" state, a trigger signal is expected NOT to be input: if an input trigger arrives, the state will immediately transition to the "RESET" state. Without an input trigger in the "Closed Window Time (T_{CW},)" the state will be elapsed and will transition to "Open Window (OW)" state.

In the "OW" state, a trigger signal is expected to be input: if an input trigger arrives, the state will immediately transition to the "Closed Window (CW)" state. Without an input trigger in the "Open Window Time (T_{OW},)" the state will be elapsed and will transition to "RESET" state.

Figure 10-14 shows that to avoid wrong triggering due to glitch noise two "High" samples followed by two "Low" samples to input WDI pin are decoded as a trigger.

In any states above, a power failure of LD1 will cause a transition to "OFF" state, and output "Low" from RST terminal until LD1 goes well.

Figure 10-11 Watchdog Timer State Diagram

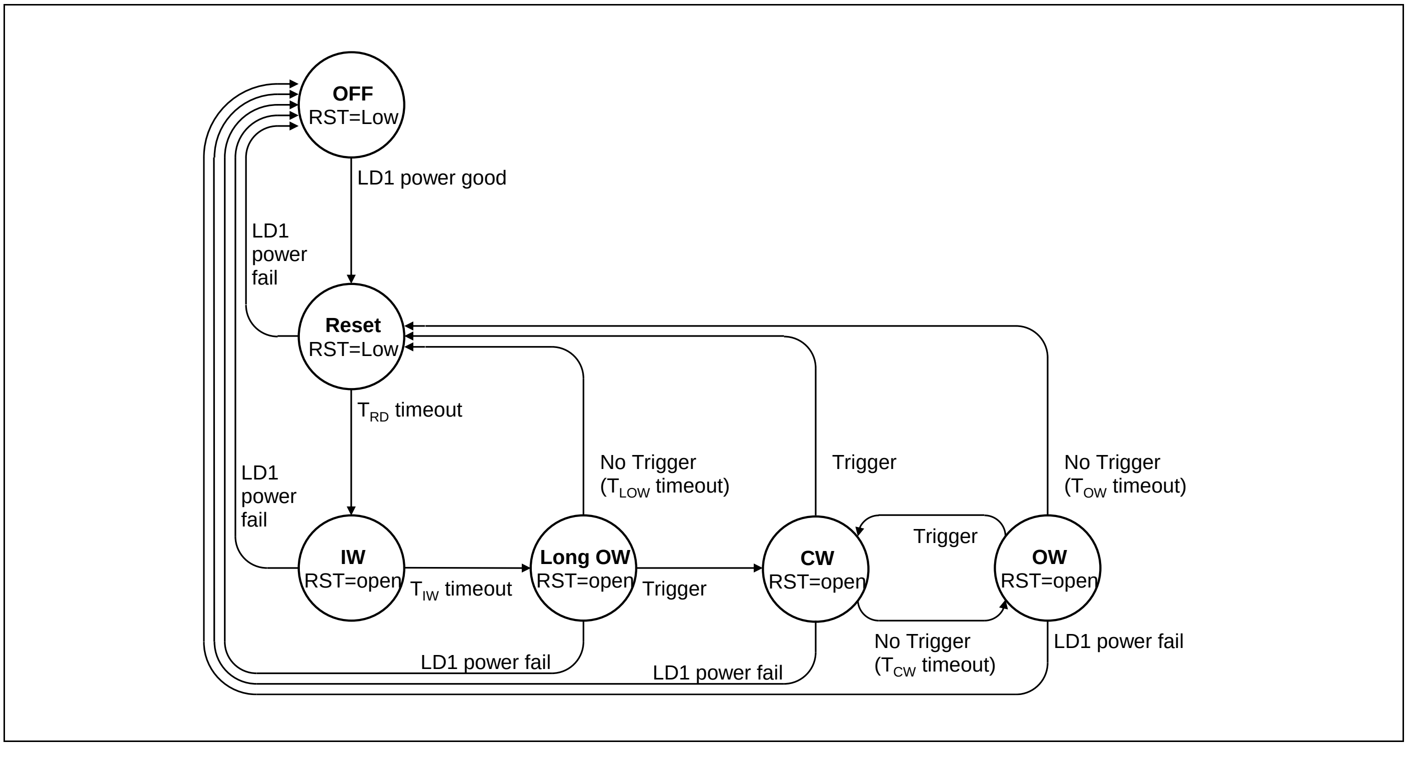


Figure 10-12 Window Watchdog Timing Chart (WDI)

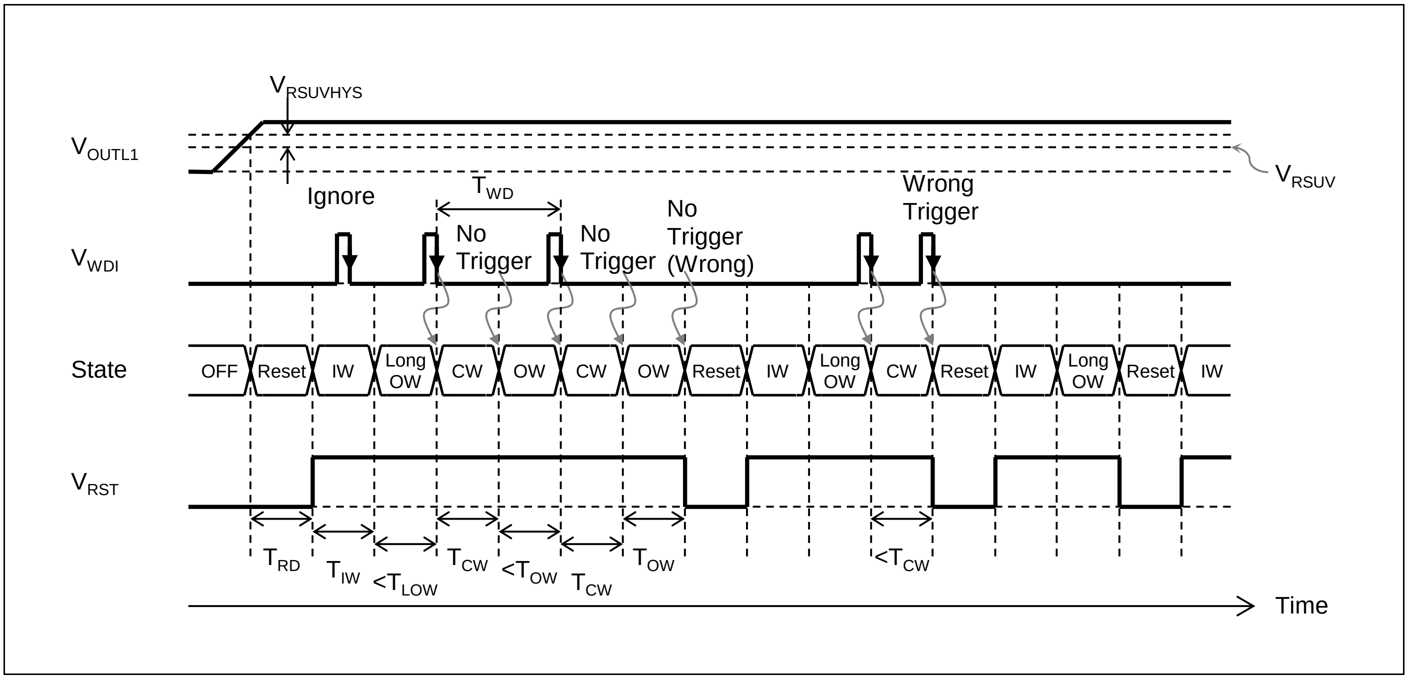


Figure 10-13 Window Watchdog Timing Chart (LD1)

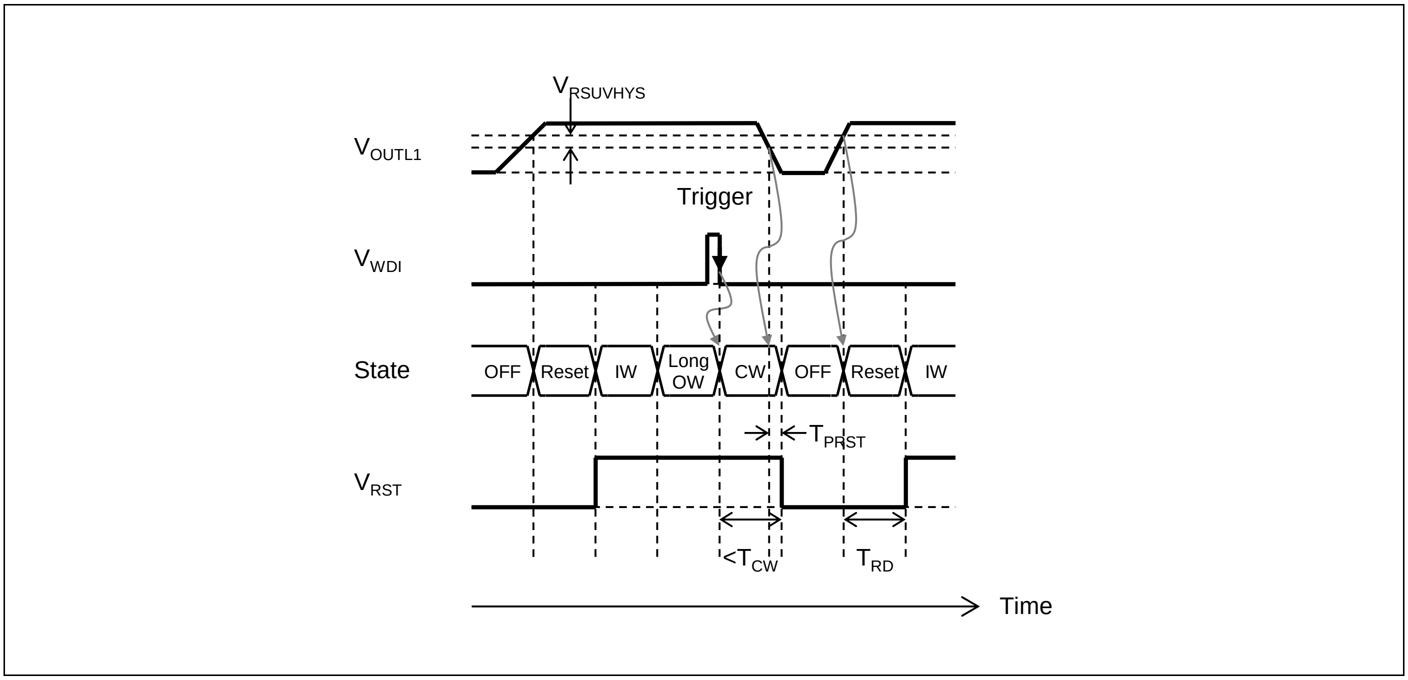
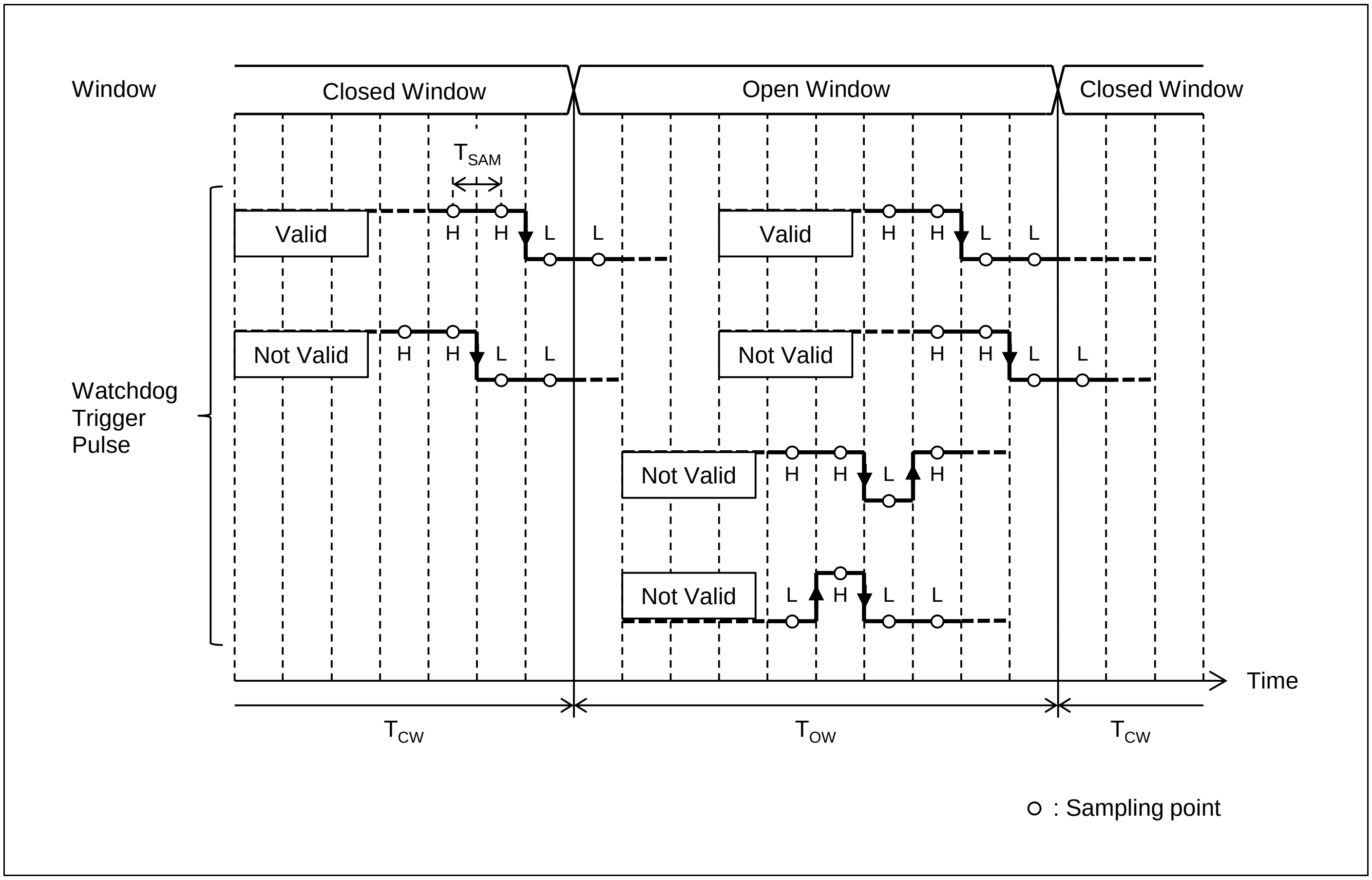


Figure 10-14 De-glitch of Window Watchdog Trigger Pulse

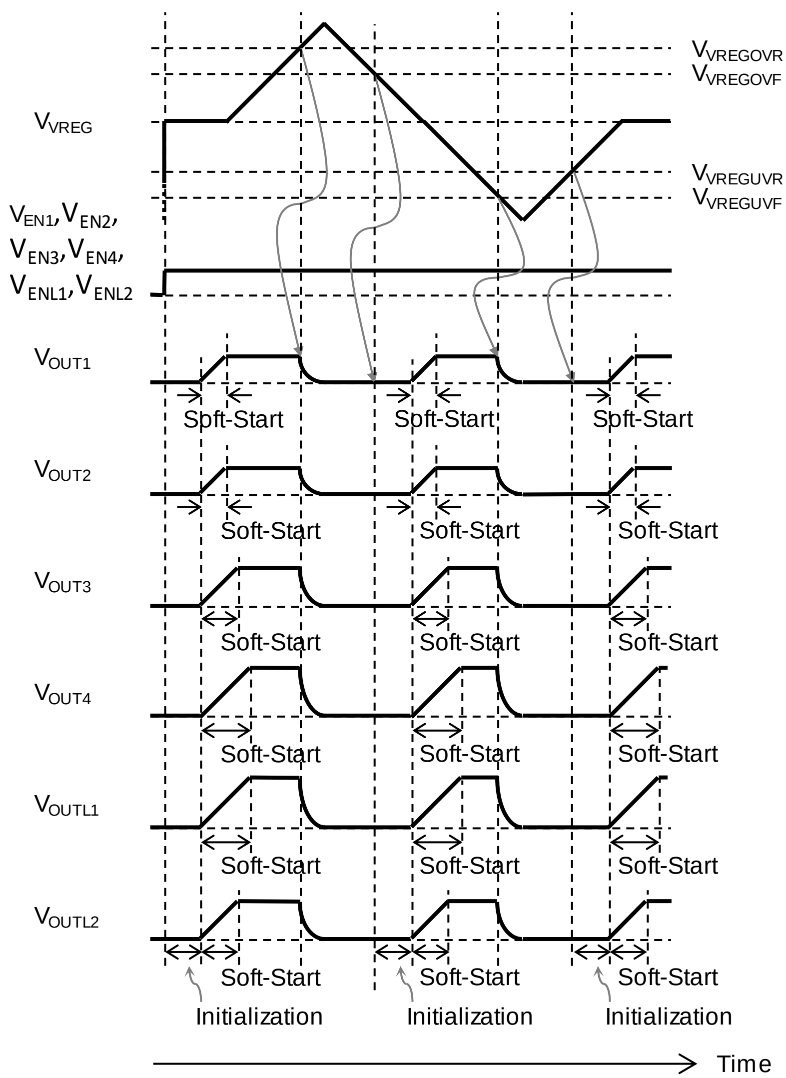


10.10 Internal Linear Regulator Output (VREG)

S6BP401A equips a 1.8 V linear regulator as the power source for its internal circuit. A low ESR 1.0 μF ceramic capacitor should be connected from VREG pin to GND. VREG is not designed to supply to external load.

Unless the VREG terminal voltage is in the range between the over voltage lockout level $V_{VREGOVR}$ and the under voltage lockout level $V_{VREGUVF}$, S6BP401A considers it abnormal and halts all DC/DC converters, LDOs and windowed watchdog timer. When the VREG terminal voltage returns to the power good voltage range ($V_{VREGUVR} \leq V_{VREG} \leq V_{VREGOVF}$), S6BP401A returns the DC/DC converters, LDOs and window watchdog timer to the normal mode. Soft-start circuits of each regulator gradually generates supply voltage as described in the section 10.6.

Figure 10-15 VREG OVLO/UVLO Timing Chart



11. Application Circuit Example

Figure 11-1 Application Circuit Example

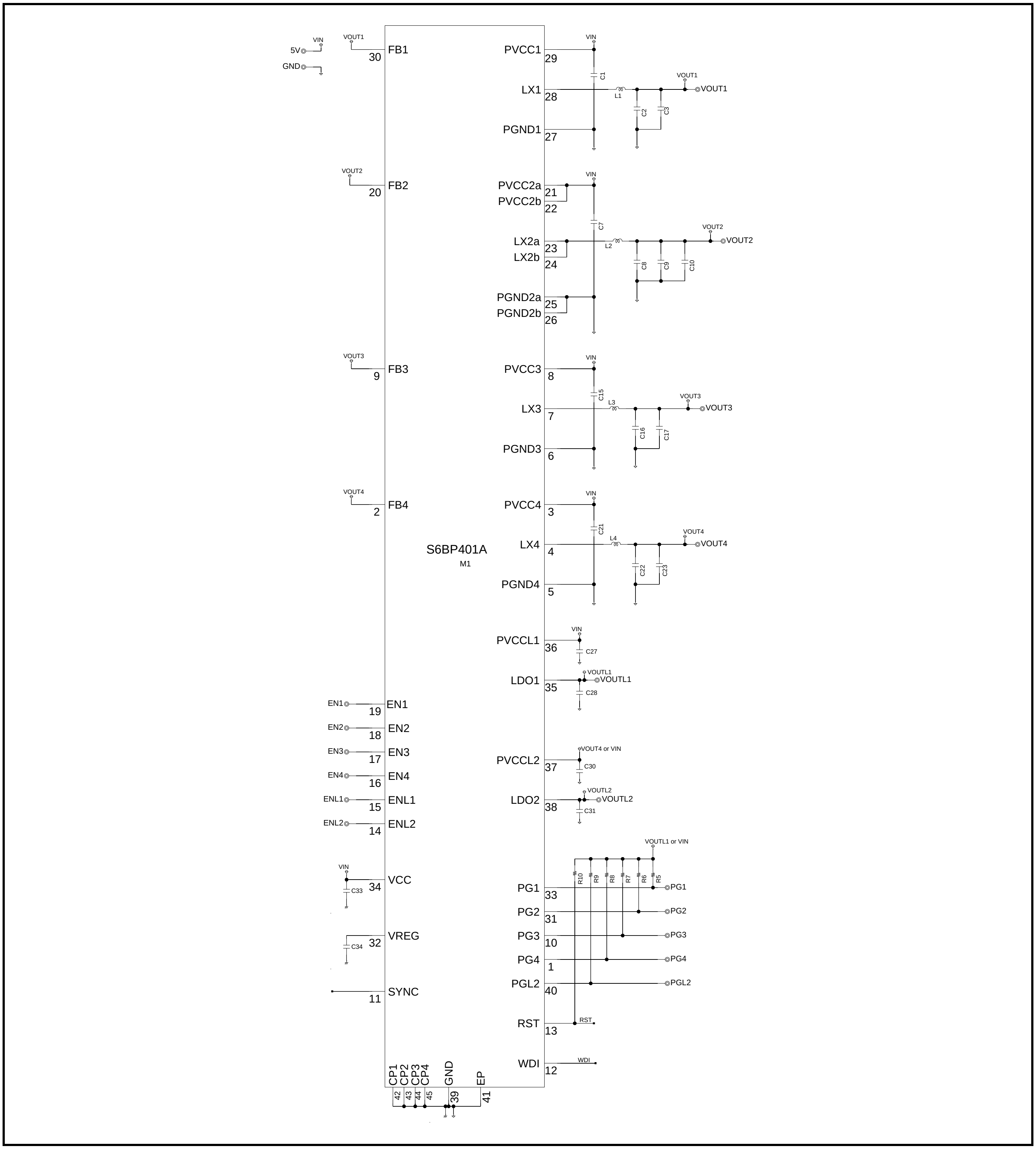


Table 11-1 Parts List

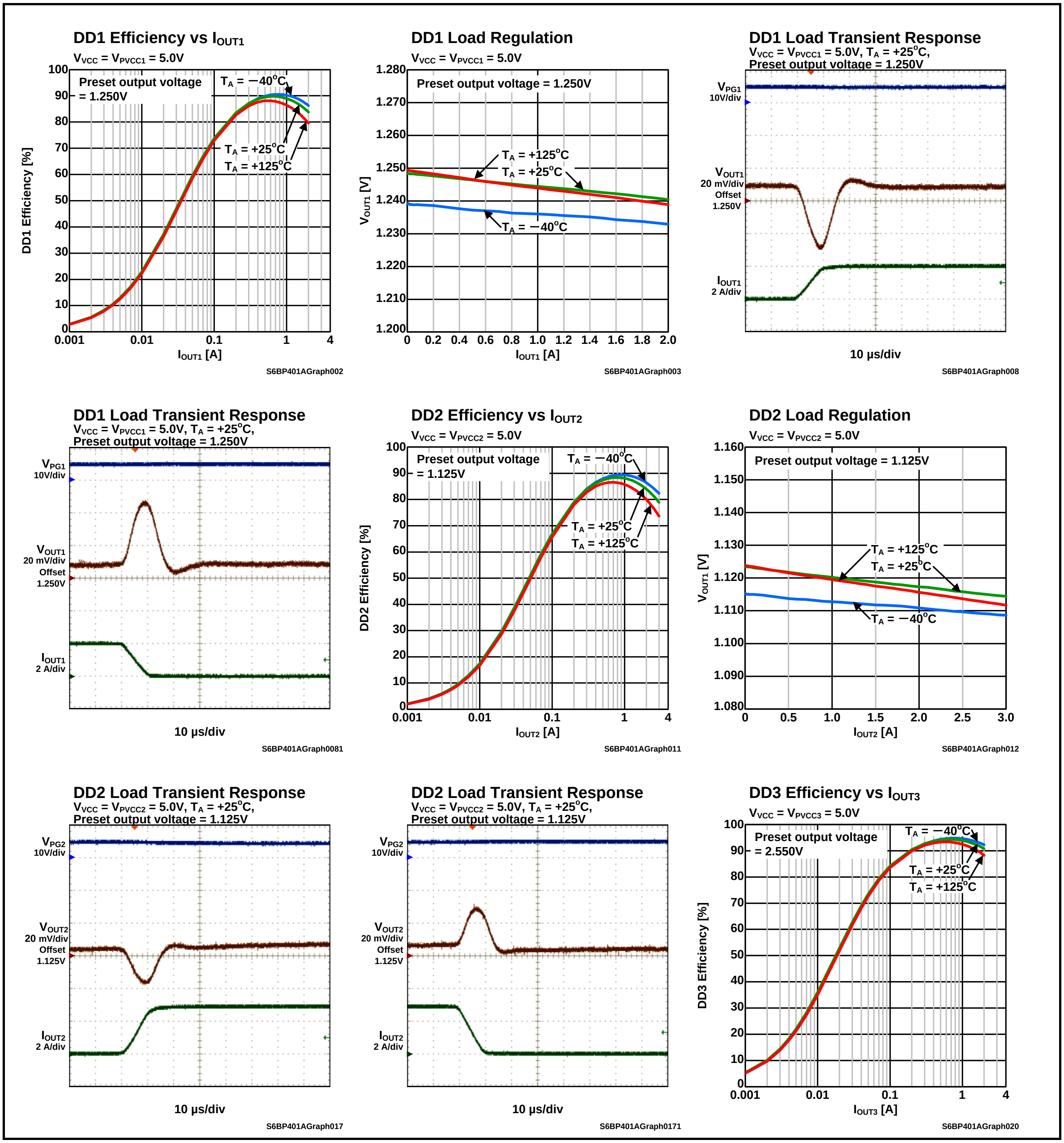
Symbol	Parts	Part Number	Specifications	Vendor
C1	Ceramic Capacitor	CGA5L1X7R1C106K160AC	10 μF	TDK
C2	Ceramic Capacitor	CGA6P1X7R1C226M250AC	22 μF	TDK
C3	Ceramic Capacitor	CGA6P1X7R1C226M250AC	22 μF	TDK
C7	Ceramic Capacitor	CGA5L1X7R1C106K160AC	10 μF	TDK
C8	Ceramic Capacitor	CGA6P1X7R1C226M250AC	22 μF	TDK
C9	Ceramic Capacitor	CGA6P1X7R1C226M250AC	22 μF	TDK
C10	Ceramic Capacitor	CGA6P1X7R1C226M250AC	22 μF	TDK
C15	Ceramic Capacitor	CGA5L1X7R1C106K160AC	10 μF	TDK
C16	Ceramic Capacitor	CGA6P1X7R1C226M250AC	22 μF	TDK
C17	Ceramic Capacitor	CGA6P1X7R1C226M250AC	22 μF	TDK
C21	Ceramic Capacitor	CGA5L1X7R1C106K160AC	10 μF	TDK
C22	Ceramic Capacitor	CGA6P1X7R1C226M250AC	22 μF	TDK
C23	Ceramic Capacitor	CGA6P1X7R1C226M250AC	22 μF	TDK
C27	Ceramic Capacitor	CGA3E1X7R1C105M080AC	1 μF	TDK
C28	Ceramic Capacitor	CGA3E1X7R1C105M080AC	1 μF	TDK
C30	Ceramic Capacitor	CGA3E1X7R1C105M080AC	1 μF	TDK
C31	Ceramic Capacitor	CGA5L1X7R1C106K160AC	10 μF	TDK
C33	Ceramic Capacitor	CGA3E1X7R1C105M080AC	1 μF	TDK
C34	Ceramic Capacitor	CGA3E1X7R1C105M080AC	1 μF	TDK
L1	Inductor	CLF6045T-1R5N-D	1.5 μH	TDK
L2	Inductor	CLF6045T-1R5N-D	1.5 μH	TDK
L3	Inductor	CLF6045T-1R5N-D	1.5 μH	TDK
L4	Inductor	CLF6045T-1R5N-D	1.5 μH	TDK
R5	Resistor	RG1608P-473-B	47 kΩ	SSM
R6	Resistor	RG1608P-473-B	47 kΩ	SSM
R7	Resistor	RG1608P-473-B	47 kΩ	SSM
R8	Resistor	RG1608P-473-B	47 kΩ	SSM
R9	Resistor	RG1608P-473-B	47 kΩ	SSM
R10	Resistor	RG1608P-473-B	47 kΩ	SSM

TDK : TDK Corporation
SSM : SUSUMU CO., LTD.

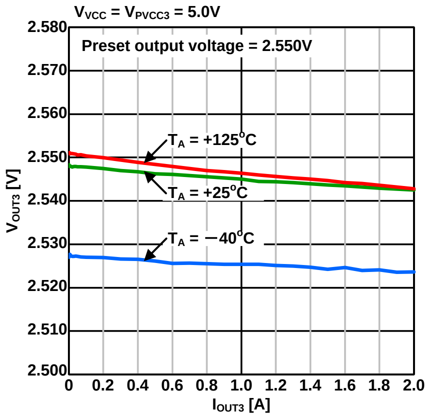
12. Reference Data

The followings are the reference data measured under the conditions shown in "11. Application Circuit Example".

Figure 12-1 DC/DC Converter

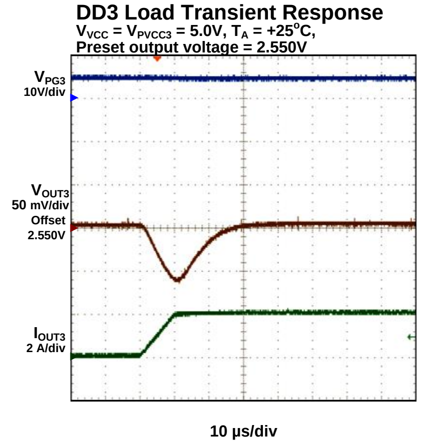


DD3 Load Regulation



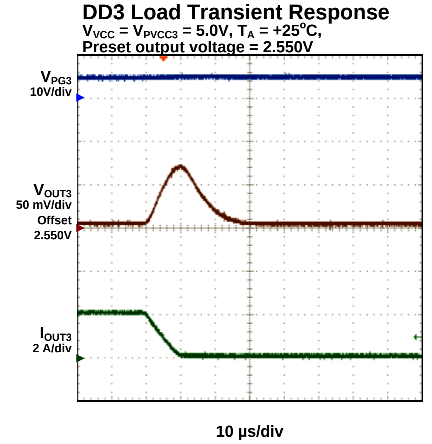
S6BP401AGraph021

DD3 Load Transient Response



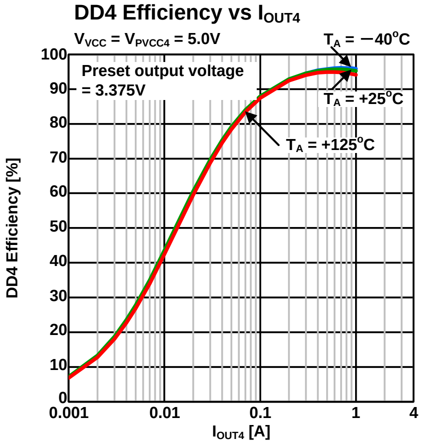
S6BP401AGraph026

DD3 Load Transient Response



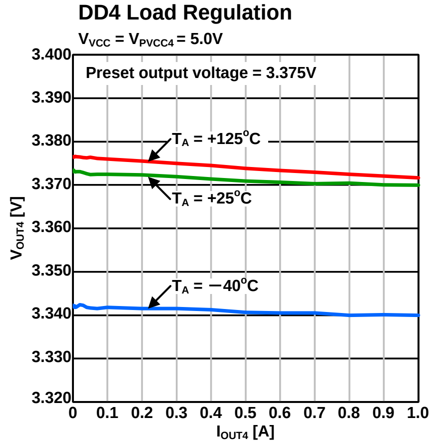
S6BP401AGraph0261

DD4 Efficiency vs IOUT4



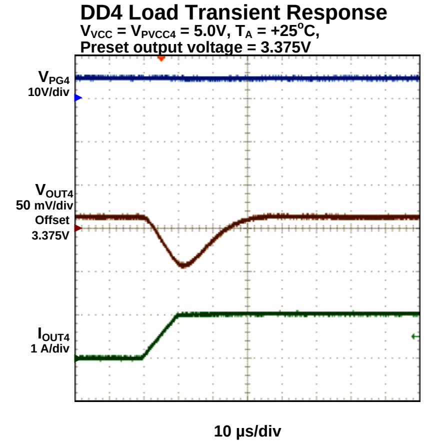
S6BP401AGraph029

DD4 Load Regulation



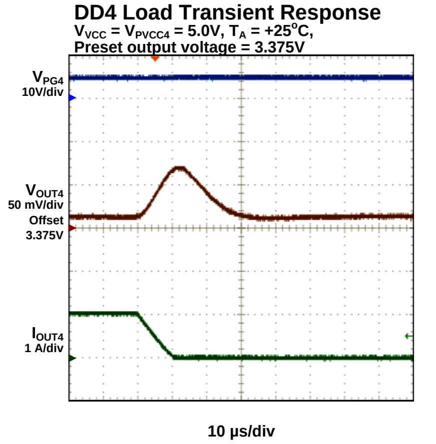
S6BP401AGraph030

DD4 Load Transient Response



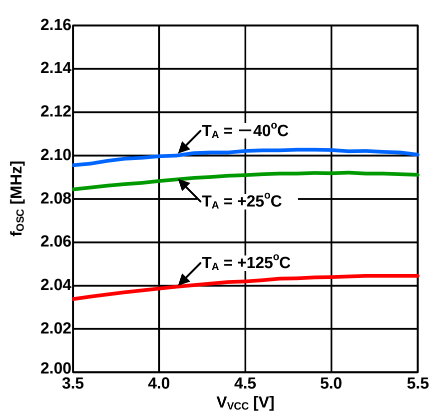
S6BP401AGraph035

DD4 Load Transient Response



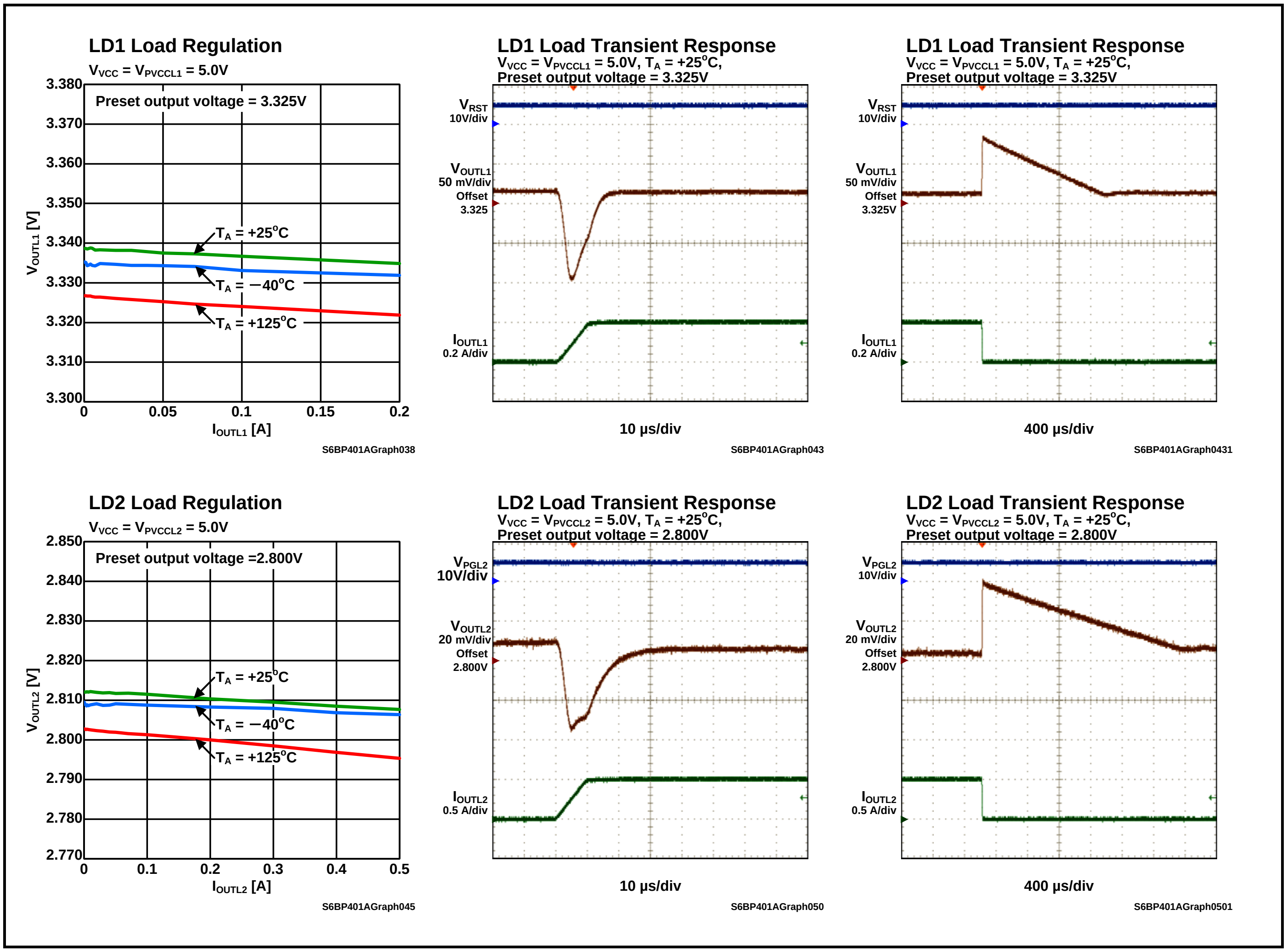
S6BP401AGraph0351

fOSC vs VVCC



S6BP401AGraph0531

Figure 12-2 LDO Regulator



13. Ordering Information

Table 13-1 Ordering Information

Part Number (MPN) (*1)	Output Voltage [V]						Package
	DD1	DD2	DD3	DD4	LD1	LD2	
S6BP401AB1SN1B000, S6BP401AB1SN1B200	1.250	1.250	1.250	3.375	3.325	1.850	Plastic, QFN (0.50 mm pitch), 40-pin (VND040)
S6BP401AJ0SN1B000, S6BP401AJ0SN1B200	1.250	1.250	1.850	3.375	3.300	2.800	
S6BP401AJ2SN1B000, S6BP401AJ2SN1B200	1.200	1.100	1.800	3.300	3.300	2.800	
S6BP401AL2SN1B000, S6BP401AL2SN1B200	1.250	1.125	2.550	3.375	3.325	1.850	
S6BP401AL3SN1B000, S6BP401AL3SN1B200	1.250	1.125	2.550	3.350	3.325	1.850	
S6BP401AM2SN1B000, S6BP401AM2SN1B200	1.250	1.125	2.550	3.375	3.325	2.800	

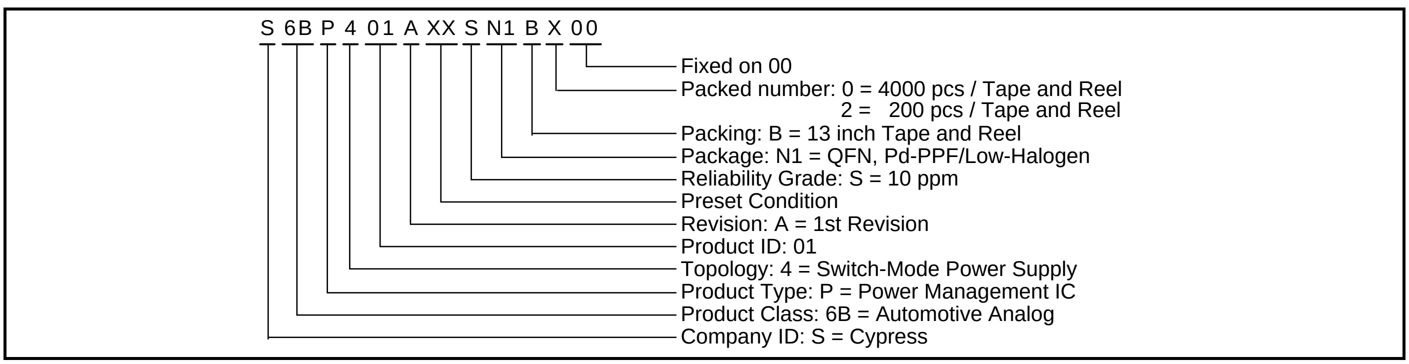
MPN: Marketing Part Number

*1: Please contact our sales division for the output voltage combination not mentioned in this table.

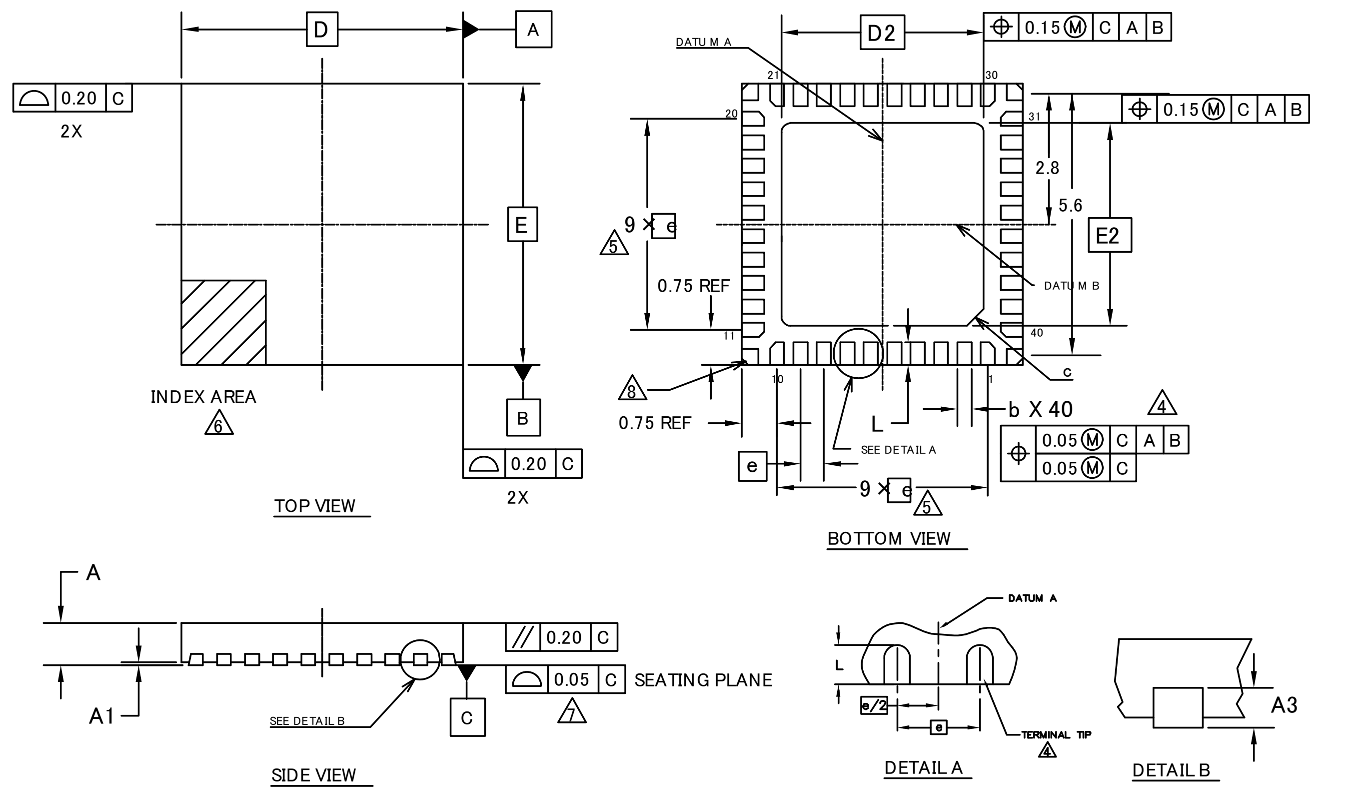
Part Numbering Conventions

These ICs follow the part numbering convention described in the following table. Each single-character is alphanumeric (0, 1, 2, …, 9, A, B, …, Z) unless stated otherwise. The part numbers are defined as follows.

Figure 13-1 Part Numbering Conventions



14. Package Dimensions



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	0.90
A1	0.00	—	0.05
A3	0.20 REF		
D	6.00 BSC		
E	6.00 BSC		
b	0.20	0.25	0.30
D2	4.20 BSC		
E2	4.20 BSC		
e	0.50 BSC		
c	0.50		
L	0.30	0.40	0.50
N	40		
ND	10		
NE	10		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5-1994.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E RESPECTIVELY.
6. PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
7. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
8. REINFORCEMENT LAND SIZE 0.35mm SQ.
9. JEDEC SPECIFICATION NO. REF. : N/A.

002-10861 **

PACKAGE OUTLINE, 40 LEAD QFN
6.0X6.0X0.9 MM VND040 4.2X4.2 MM EPAD Rev**

15. Major Changes

Spansion Publication Number: S6BP401A_DS405-00024

Page	Section	Change Results
Revision 0.1 (February 19, 2015)		
-	-	Initial release

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: S6BP401A Power Management IC for Automotive ADAS Platform
Document Number: 002-03341

Revision	ECN	Submission Date	Description of Change
**	4922113	09/16/2015	New Spec. Updated Ordering Information
*A	5085035	01/14/2016	Updated “3. Pin Functions” Updated “6. Absolute Maximum Ratings” Updated “7. Recommended Operating Conditions” Added “Development Support” Added “12. Reference Data” Updated “13. Ordering Information”
*B	5160391	03/04/2016	Added “AEC-Q100 compliant (Grade-1)” in “Features” Added the following values in “8. Electrical Characteristics” Supply Current I_{VCCS}: Max value UVLO: Under Voltage Lockout (VCC) V_{UVHYS}: Min and Max values Enable Inputs (EN1, EN2, EN3, EN4, ENL1, ENL2) I_{IHEN}: Min and Max values Synchronization Input (SYNC) I_{IHSYNC}: Min and Max values Power Good Monitor (PG1, PG2, PG3, PG4, PGL2, RST) $V_{PGOVHYS}$: Min and Max values $V_{PGUVHYS}$: Min and Max values Watchdog Timer (WDI) T_{WD}: Min and Max values I_{IHWDI}: Min and Max values DD1: Buck DC/DC Converter R_{FB1}: Min and Max values R_{ONHS1}: Max values R_{ONLS1}: Max values I_{LEAK1}: Max value $V_{OVPHYS1}$: Min and Max values R_{DIS1}: Min and Max values T_{COESS1}: Min and Max values DD2: Buck DC/DC Converter R_{FB2}: Min and Max values R_{ONHS2}: Max values R_{ONLS2}: Max values

Revision	ECN	Submission Date	Description of Change
*B	5160391	03/04/2016	I_{LEAK2}: Max value $V_{OVPHYS2}$: Min and Max values R_{DIS2}: Min and Max values T_{COESS2}: Min and Max values DD3: Buck DC/DC Converter R_{FB3}: Min and Max values R_{ONHS3}: Max values R_{ONLS3}: Max values I_{LEAK3}: Max value $V_{OVPHYS3}$: Min and Max values R_{DIS3}: Min and Max values T_{COESS3}: Min and Max values DD4: Buck DC/DC Converter R_{FB4}: Min and Max values R_{ONHS4}: Max values R_{ONLS4}: Max values I_{LEAK4}: Max value $V_{OVPHYS4}$: Min and Max values R_{DIS4}: Min and Max values T_{COESS4}: Min and Max values LD1: LDO Regulator I_{LEAKL1}: Max value R_{DISL1}: Min and Max values $T_{COESSL1}$: Min and Max values LD2: LDO Regulator I_{LEAKL2}: Max value R_{DISL2}: Min and Max values $T_{COESSL2}$: Min and Max values Updated the following values in “8. Electrical Characteristics” DD1: Buck DC/DC Converter R_{ONHS1}: Typ value R_{ONLS1}: Typ value DD2: Buck DC/DC Converter R_{ONHS2}: Typ value R_{ONLS2}: Typ value DD3: Buck DC/DC Converter R_{ONHS3}: Typ value R_{ONLS3}: Typ value DD4: Buck DC/DC Converter R_{ONHS4}: Typ value R_{ONLS4}: Typ value Delete the following values in “8. Electrical Characteristics” Updated “Figure 10-1” and “Figure 10-2” Updated “10.5 Under Voltage Lockout (UVLO)” Added a part number, S6BP401AL2SN1B000, in “Table 13-1”. Corrected an error in “Table 13-1”. from S6BP401AW1SN1B000 to S6BP401AW0SN1B000
*C	5396389	08/09/2016	Deleted “Development Support” and added “More Information” Added “S6BP401AY2SN1B000” to “Table 13-1 Ordering information”
*D	5824031	07/19/2017	Adapted Cypress new logo.

Revision	ECN	Submission Date	Description of Change
*E	5929778	11/22/2017	Updated 14. Package Dimensions to the Cypress format Changed the suffix of the Part Number from “000” to “00A” in Table 13-1 Ordering information and Figure 13-1 Part numbering conventions
*F	6007678	01/18/2018	Added “S6BP401AL3SN1B00A” to “Table 13-1 Ordering Information” Fixed VVREG waveform in figure 10-15. VREG is in shutdown state when all of the enable input terminals are “Low”.
*G	6174086	05/14/2018	Added the description for Figure 10-14 in “10.9 Watchdog Timer”.
*H	6283903	08/17/2018	No update due to sunset review
*I	6771563	01/16/2020	Updated MPN in Table 13-1 Ordering information and Figure 13-1 Part numbering conventions.

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