

Evaluating TxVGAs for Use with RF DACs and Transceivers

FEATURES

Full featured evaluation board for the [ADL6317](#)
 SPI control via [SDP-S](#) board
 5.0 V single-supply operation

EVALUATION KIT CONTENTS

ADL6317-EVALZ evaluation board

ADDITIONAL HARDWARE REQUIRED

Analog signal generator
 Analog signal analyzer
 Power supplies (6 V, 5 A)
 PC with Windows® XP, Windows 7, or Windows 10 operating system
 USB 2.0 port, recommended (USB 1.1-compatible)
[EVAL-SDP-CS1Z \(SDP-S\)](#) controller board
ADDITIONAL SOFTWARE REQUIRED
[Analysis | Control | Evaluation \(ACE\)](#) software

GENERAL DESCRIPTION

The [ADL6317](#) is a transmit variable gain amplifier (VGA) that provides an interface from radio frequency (RF) digital-to-analog converters (DACs), transceivers, and systems on a chip (SoC) to power amplifiers (PAs). Integrated balun and hybrid couplers allow high performance RF capability in the 1.5 GHz to 3.0 GHz frequency range

To optimize performance vs. power level, the [ADL6317](#) includes a voltage variable attenuator (VVA), high linearity amplifiers, and a digital step attenuator (DSA). The devices integrated into the [ADL6317](#) are programmable via a 4-wire serial port interface (SPI).

This user guide describes the evaluation board and software for the [ADL6317](#). See the [ADL6317](#) data sheet for full details, which must be consulted in conjunction with this user guide when using the evaluation board. The [ADL6317](#) evaluation board was fabricated using FR-370HR, Rogers 4350B in four layers.

EVALUATION BOARD PHOTOGRAPH

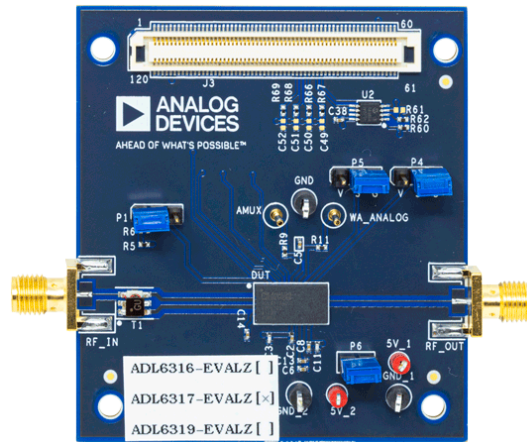


Figure 1. ADL6317 Evaluation Board

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REVISION HISTORY

10/2019—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The ADL6317-EVALZ evaluation board provides the support circuitry required to operate the ADL6317 in various modes and configurations. Figure 2 shows the typical bench setup to evaluate the performance of the ADL6317.

POWER SUPPLY

The ADL6317-EVALZ evaluation board requires a single, 5.0 V power supply.

RF INPUT

The on-board balun enables single-ended driving. The ADL6317 operates over a frequency range of 1.5 GHz to 3.0 GHz.

RF OUTPUTS

The RF outputs are available on the evaluation board at the RF_OUT SMA connectors, which can drive a load of 50 Ω.

SIGNAL PATH MODES SELECTION

The ADL6317 has two signal path modes. This feature allows two predefined modes of operation to be controlled by the logic level on TXEN, a real-time external pin (Pin 37) with no SPI latency. Table 1 shows the hardware configuration to select the desired mode.

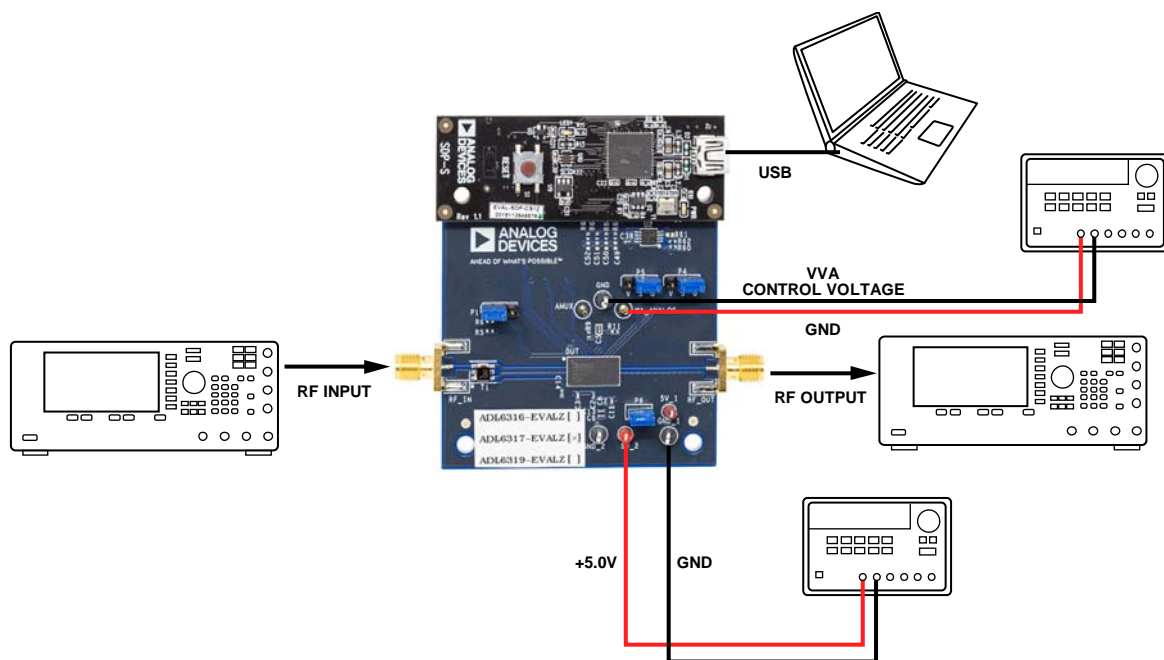


Figure 2. ADL6317 Typical Measurement Setup

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Table 1. Mode Selection and Setup Registers

TXEN(Pin 37)	Register	Functional Blocks	Description
0	0x0102	DSA attenuation	0 dB to ~15.5 dB range, 0.5dB step
	0x0107	AMP1	Amplifier 1 optimization
	0x0108	AMP1	Amplifier 1 enable
	0x0109	AMP2	Amplifier 2 optimization
	0x010A	AMP2	Amplifier 2 enable
1	0x0112	DSA attenuation	0 dB to ~15.5 dB range, 0.5dB step
	0x0117	AMP1	Amplifier 1 optimization
	0x0118	AMP1	Amplifier 1 enable
	0x0119	AMP2	Amplifier 2 optimization
	0x011A	AMP2	Amplifier 2 enable

EVALUATION BOARD SOFTWARE

The **ADL6317** on the ADL6317-EVALZ evaluation board and the **SDP-S** controller board are configured with a USB friendly interface to allow programmability of the **ADL6317** registers.

SOFTWARE REQUIREMENTS AND INSTALLATION

The **Analysis | Control | Evaluation (ACE)** software is required to program and control the **ADL6317** and the ADL6317-EVALZ evaluation board.

The **ACE** software suite allows bit control of the **ADL6317** register map via the SPI, and communicates to the **SDP-S** controller board via the USB connection. The **SDP-S** controller board configures the SPI lines (CS, SDI, SDO, and SCLK) accordingly to communicate to the **ADL6317**.

Installing the ACE Software Suite

To install the **ACE** software suite, take the following steps:

1. Download the software from the **ACE** product page.
2. Open the downloaded file to begin the installation process. The default installation path is **C:\Program Files (x86)\Analog Devices\ACE**.
3. If desired, the user can create a desktop icon for the **ACE** software. Otherwise, the **ACE** executable can be found by clicking **Start > Analog Devices > ACE**.

INSTALLING ADL6317 ACE PLUGINS

When the **ACE** software installations are complete, the user must install the evaluation board plugins to the hard drive of the PC.

1. Download **ADL6317 ACE** plugins (**Board.ADL631x.1.2019.34200.acezip**) from the ADL6317-EVALZ product page.
2. Double-click the **Board.ADL631x.1.2019.34200.acezip** file to install the evaluation board plugins.
3. Ensure that the **Board.ADL631x.1.2019.34200** and **Chip.ADL631x.1.2019.34200** folders are located inside the **C:\ProgramData\Analog Devices\ACE\Plugins** folder.

ACE SOFTWARE SUITE

Power up the ADL6317-EVALZ evaluation board and connect the USB cable to the PC and to the **SDP-S** board mounted on the ADL6317-EVALZ evaluation board.

1. Double-click the **ACE** shortcut on the PC desktop of the computer (if created). The software automatically detects the ADL6317-EVALZ evaluation board. The software opens the **ACE** plugin view, as shown in Figure 3.

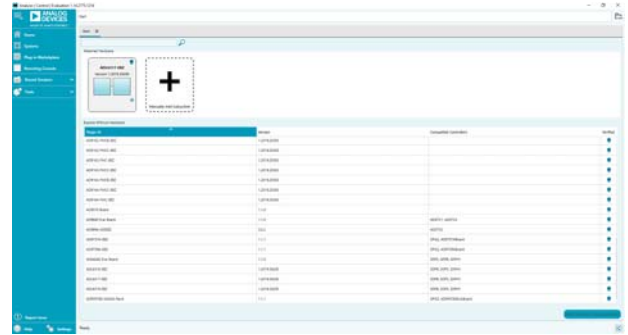


Figure 3. ACE Plugin View

2. Double-click the **ADL6317-EBZ** board icon, as shown in Figure 4.

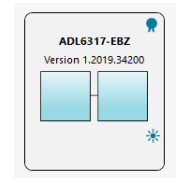


Figure 4. ADL6317-EBZ Board Icon

3. The software opens the **ACE** chip view as shown in Figure 5.

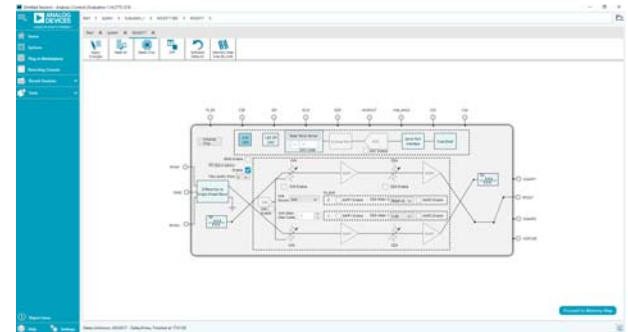


Figure 5. ACE Chip View

CONFIGURATION AND PROGRAMMING SEQUENCE

To configure and program the evaluation board, take the following steps:

1. Run the **ACE** software as explained in the ACE Software Suite.
2. Click **Initialize Chip** (Label A, see Figure 6).
3. Click and adjust the blocks in **Label B to Label H**, as shown in Figure 6, if necessary.

4. After changing the block as directed in Step 3, in the **ACE** software, click **Apply Changes** (Label K, see Figure 7) to update to **ADL6317**.
5. To adjust an individual register and bit, click **Proceed to Memory Map**. This button opens the **ADL6317** memory map for bit control (see Figure 8). The **ADL6317** can be configured by either putting data into **Data(Hex)** column or by clicking a specific bit in the **Data(Binary)** column of the register map (see Figure 8). Click **Apply Changes** to save changes and program the **ADL6317**.

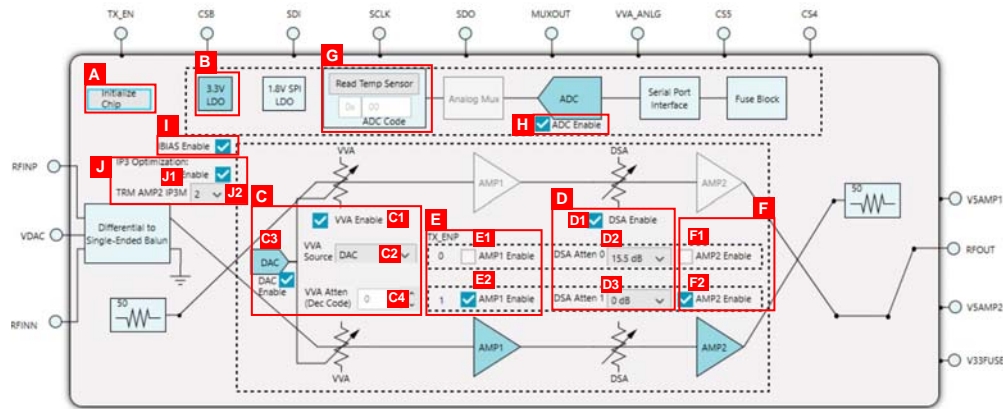


Figure 6. ADL6317 Chip Block Diagram

Table 2. Main Screen Functionality (see Figure 6)

Label	Function
A	Initialize chip button.
B	3.3 V low dropout regulator (LDO) enable.
C	VVA control block.
C1	VVA Enable checkbox.
C2	Selects VVA voltage source: DAC: VVA attenuation set by internal 12-bit DAC, set DAC code (0 to ~4095 range) in VVA Atten (Dec Code) field. VVA_ANALOG: VVA attenuation set by analog voltage applied on ANALG pin.
C3	DAC Enable checkbox for VVA attenuation when the VVA Source field is set to DAC .
C4	VVA Atten (Dec Code) menu. Selects VVA DAC code in decimal (0 to ~4095 range). Higher numbers equal less attenuation.
D	DSA control block, DSA Atten 0 and DSA Atten 1 are selected by the logic level on TXEN (see Table 1).
D1	DSA Enable checkbox.
D2	Set DSA Atten 0 attenuation.
D3	Set DSA Atten 1 attenuation.
E	AMP1 Enable checkbox. AMP1 can be set individually by the logic level on TXEN (see Table 1).
F	AMP2 Enable checkbox. AMP2 can be set individually by the logic level on TXEN (see Table 1).
G	Read Temp Sensor button and ADC Code text fields. These functions are for proportional to absolute temperature (PTAT) ADC code readback.
H	ADC Enable checkbox.
I	IBIAS Enable checkbox. This function enables the bias generator.
J	IP3 Optimization control block.
J1	Enable checkbox for IP3 optimization.
J2	TRM AMP2 IP3M dropdown menu. Set the TRM_AMP2_IP3 bits value for IP3 optimization.

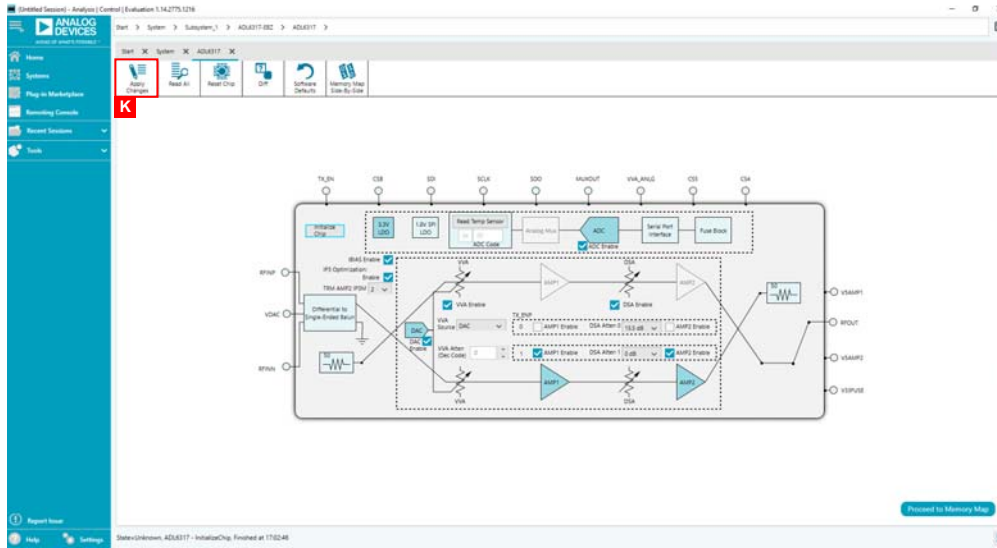


Figure 7. ADL6317-EVALZ ACE Chip View After Chip Initialization

Address (Hex)	Name	Data (Hex)	Data (Binary)
00000000	1_SPL_SEL1	00	0 0 0 0 0 0 0 0
00000000	1_VIAAMP_PFEED	00	0 0 0 0 0 0 0 0
00000001	1_BIASL_SF	00	0 0 0 0 0 0 0 0
00000010	1_SMAIR_SEL2	00	0 0 0 0 0 0 0 0
00000013	1_SMAIR_SEL10	00	0 0 0 0 0 0 0 0
00000100	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
00000101	SIG_BNDR_0	00	0 0 0 0 0 0 0 0
00000102	SIG_BNDR_0	00	0 0 0 0 0 0 0 0
00000103	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
00000110	VIA_ATTEN11_B	00	0 0 0 0 0 0 0 0
00000105	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
00000106	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
00000107	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
00000108	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
00000109	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
0000010A	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
0000010B	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
0000010C	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
0000010D	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
0000010E	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
0000010F	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
00000110	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
00000111	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
00000112	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
00000113	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
00000114	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
00000115	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
00000116	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
00000117	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
00000118	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
00000119	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
0000011A	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
0000011B	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
0000011C	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
0000011D	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
0000011E	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
0000011F	SIG_BNDR0_0	00	0 0 0 0 0 0 0 0
00000120	BIASL_SF	00	0 0 0 0 0 0 0 0
00000121	BIASL_SF_CTRL_0111	00	0 0 0 0 0 0 0 0

Figure 8. ADL6317-EVALZ ACE Memory Map View

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EVALUATION BOARD SCHEMATIC

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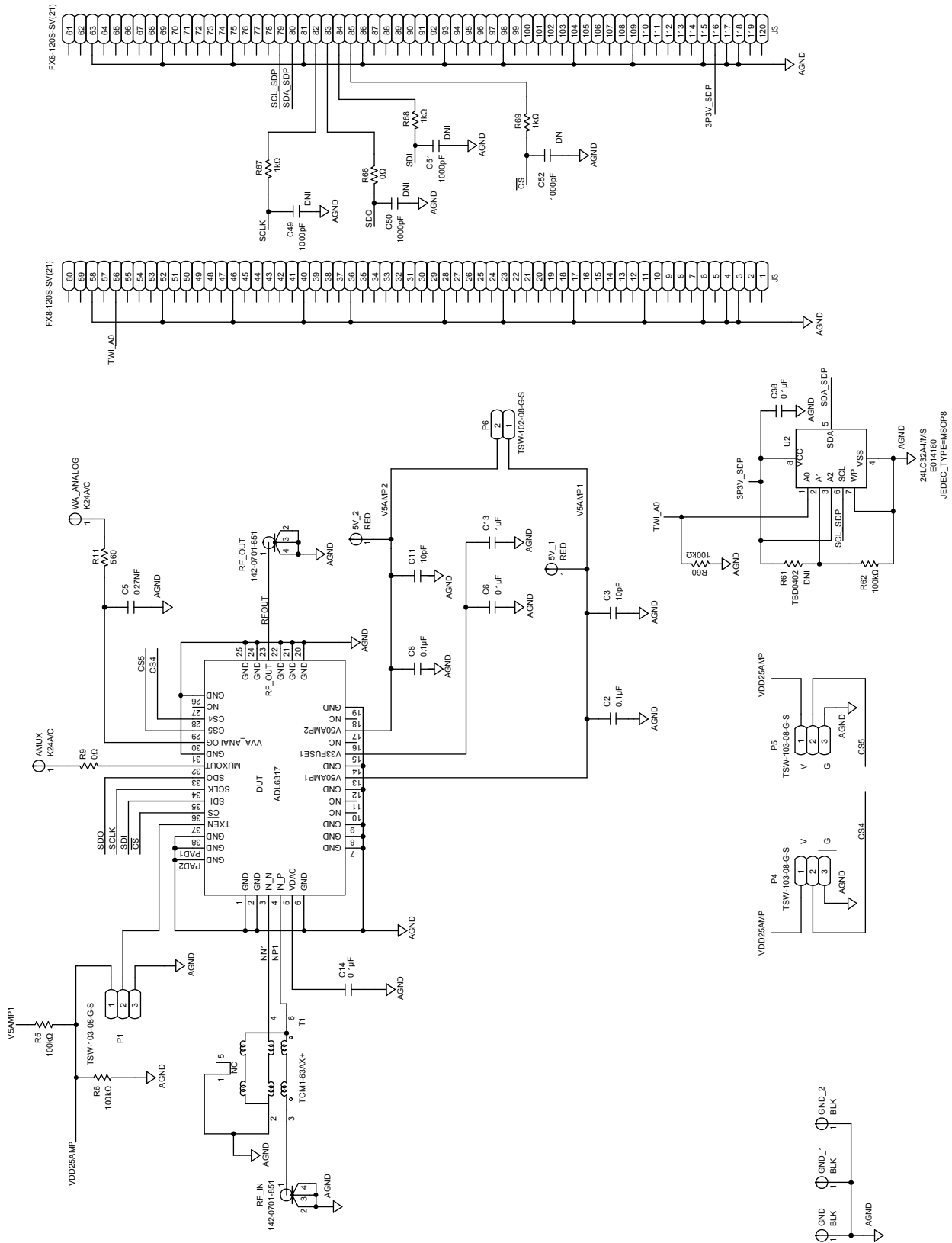


Figure 9. ADL6317-EVALZ Evaluation Board Schematic

NOTES

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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