RF tuner IC
For DVB-H,DVB-T and DMB-TH

ADMTV102

FEATURES

- **Single chip synthesized tuner for dual-band mobile-TV applications**
- **Zero-IF single-conversion architecture which eliminates all SAW filters**
- **Covers whole VHF (174 ~ 245 MHz) and UHF (470 MHz ~ 862 MHz)**
- **Typical AGC dynamic range: -102 ~ 0 dBm**
- **Ultra low power consumption**
  - **VHF: 180 mW**
  - **UHF: 200 mW**
- **On-chip fast switching fractional-N PLL**
- **On-chip low phase noise and wide frequency range VCO**
- **On-chip bandwidth-adjustable low pass filter**
- **Integrated baseband variable gain amplifier for direct connection to digital demodulators**
- **Noise/Linearity optimization through internal RFAGC loop**
- **Adjustable take-over point**
- **I²C serial bus interface**
- **Small 32-QFN package (5 × 5 mm²)**
- **Minimal external components**

FUNCTIONAL BLOCK DIAGRAM

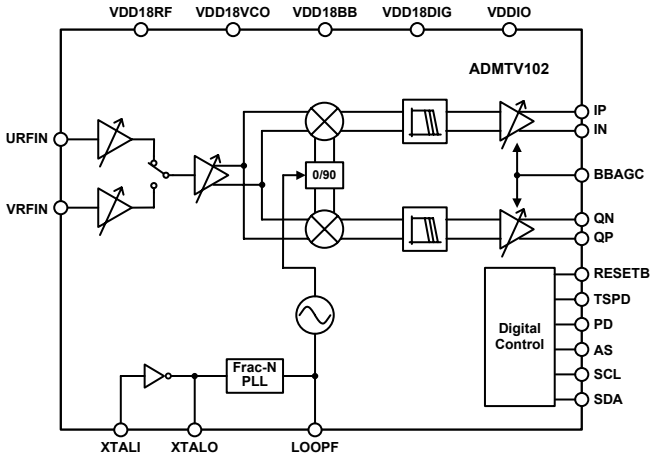

Figure 1. Block Diagram

APPLICATIONS

- **DVB-H/DVB-T/DMB-TH mobile and portable TV receivers**
- **VHF and UHF mobile and portable TV receivers**

GENERAL DESCRIPTION

The ADMTV102 is a highly integrated CMOS single chip zero-IF conversion tuner IC for mobile-TV standards, such as DVB-H, DVB-T and DMB-TH. It includes dual RF input bands, which are VHF and UHF. The building blocks of ADMTV102 are LNAs, RFPGAs, I/Q down-conversion mixers, bandwidth adjustable low pass filters, baseband variable gain amplifiers, VCOs and a fractional-N PLL, etc. On-chip low phase noise VCO along with high resolution fractional-N frequency synthesizer make in-band phase noise low enough for mobile-TV applications.

The ADMTV102 supports dual-band mobile TV standards with ultra low power consumption such as 200 mW for DVB-H. Using small leadless 5 mm × 5 mm 32-LD QFN package, the ADMTV102 is the best solution for highly integrated dual-band mobile and portable applications where low power consumption is critical. It has an industry standard I²C serial bus interface. Applications of the ADMTV102 are DVB-H, DVB-T and DMB-TH.

Rev. 0
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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
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REVISION HISTORY

08/31—Revision 0: Initial Version

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SPECIFICATIONS

Table 1. DC Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
OPERATING CONDITIONS					
1.8 V Supply Voltage (VDD18RF, VDD18VCO, VDD18BB, VDD18DIG)	V_{DD18}	1.7	1.8	1.9	V
IO Supply Voltage	V_{DDIO}	1.7	3.3	3.6	V
BBAGC Input Voltage	V_{BBAGC}	0		1.8	V
BBAGC Input Current	I_{BBAGC}	-10		10	µA
DIGITAL IN/OUTPUT PINS (RESETB, TSPD, PD, AS, SCL,SDA, HOLDAGC)					
Maximum Low Input Voltage	V_{IL}			$0.3\times V_{DDIO}$	V
Minimum High Input Voltage	V_{IH}	$0.7\times V_{DDIO}$			V
Maximum Low Output Voltage	V_{OL}			$0.3\times V_{DDIO}$	V
Minimum High Output Voltage	V_{OH}	$0.7\times V_{DDIO}$			V
High Level Input Current (VIN=V_{DDIO})	I_{IH}	-10		10	µA
Low Level Input Current (VIN=GND)	I_{IL}	-10		10	µA
VHF POWER CONSUMPTION					
1.8 V Analog Current Consumption	$I_{DD18AVHF}$		98		mA
1.8 V Digital Current Consumption	$I_{DD18DVHF}$		1		mA
IO Digital Current Consumption	$I_{DDIOVHF}$		1		mA
Power Down Current Consumption	I_{PDVHF}		1	200	µA
Total Power Consumption	P_{VHF}		180		mW
UHF POWER CONSUMPTION					
1.8 V Analog Current Consumption	$I_{DD18AUHF}$		110		mA
1.8 V Digital Current Consumption	$I_{DD18DUHF}$		1		mA
IO Digital Current Consumption	$I_{DDIOUHF}$		1		mA
Power Down Current Consumption	I_{PDUHF}		1	200	µA
Total Power Consumption	P_{UHF}		200		mW

Table 2. AC Electrical Characteristics

T_A = 25°C, V_{DD18} = 1.8 V, V_{DDIO} = 3.3 V, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit
Reference Crystal or Clock Input Frequency	f_{CLK}	13		40	MHz
VHF CHARACTERISTICS[1]					
RF Frequency Range	f_{VHF}	174		245	MHz
RF Input Impedance	Z_{IN}		50		Ω
Input VSWR	VSWR			2:1	
Typical AGC Dynamic Range	P_{IN}	-102		0	dBm
Noise Figure @ Max Gain	NF		3	TBD	dB
In-Band Two Tone IMD_3[2] (U/D)	IMD_3		-45	TBD	dBc
Out-band IIP_3[3]	IIP_3	TBD	-4		dBm
3 dB Cut-off Frequency[4]	f_{3dB}	2.5		4	MHz
Stop Band Attenuation[5]	SBA		55		dBc
LO Phase Noise (SSB @ 10 kHz Offset)	PN		-90	TBD	dBc/Hz
Baseband Output Amplitude Vpp, Single	V_{OUTAC}	300	500	700	mV
Maximum Load @ BB Output Pins, Differential	Z_{MAX}		2		kΩ
				20	pF
Output DC Voltage @ BB Output Pins	V_{OUTDC}		0.9		V

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Parameter	Symbol	Min	Typ	Max	Unit
UHF CHARACTERISTICS					
RF Frequency Range	f_{UHF}	470		862	MHz
RF Input Impedance	Z_{IN}		50		Ω
Input VSWR	VSWR			2:1	
Typical AGC Dynamic Range	P_{IN}	-102		0	dBm
Noise figure @ Max Gain	NF		4.5	TBD	dB
In-band Two Tone IMD_3[2](U/D)	IMD_3		-48	TBD	dBc
Out-band IIP_3[3]	IIP_3	TBD	-5		dBm
3 dB Cut-off Frequency[4]	f_{3dB}	2.5		4	MHz
Stop Band Attenuation[5]	SBA		55		dBc
LO Phase Noise (SSB @ 10 kHz Offset)	PN		-90	TBD	dBc/Hz
Baseband Output Amplitude Vpp, Single	V_{OUTAC}	300	500	700	mV
Maximum Load @ BB Output Pins, Differential	Z_{MAX}		2		kΩ
				20	pF
Output DC Voltage @ BB Output Pins	V_{OUTDC}		0.9		V

NOTES
[1]VHF band is supported by ADMTV102BCPZRL. See Ordering Guide.
[2]For RF input power P_{IN} < -30 dBm, f1, f2 = 200 kHz Frequency offset.
[3]For RF input power P_{IN} = -80 dBm, two-tone interferer power is -35 dBm, Frequency offset f1 = 13.25 MHz, f2 = 29.25 MHz. RFAGC: closed loop gain control, BBAGC: external gain control.
[4]Programmable.
[5] For 6 MHz offset @ LPF cut-off 4 MHz

Table 3. Digital Timing Diagram

Characteristic	Symbol	Min	Unit
PD Set-up Margin	a	Don't Care	µs
Power up Set-up Margin for V_{DD18}	b	Don't Care	µs
Power up Set-up Margin for V_{DDIO}	c	Don't Care	µs
RESETB Set-up Time for RESETB	d	100	µs
Set-up Time for I^2C Interface	e	100	µs

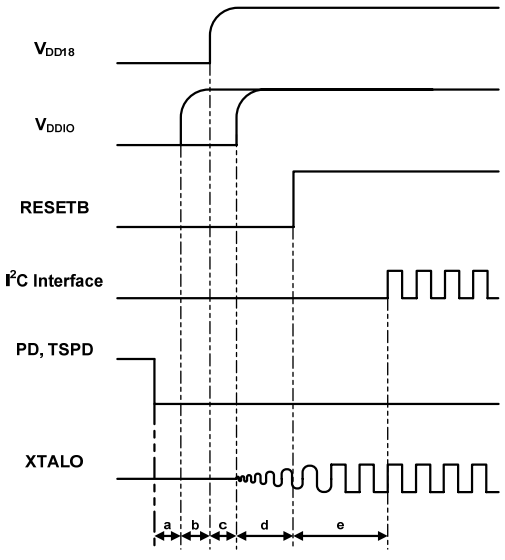

Figure 2. Digital Timing Diagram

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ABSOLUTE MAXIMUM RATINGS

Table 4. (T_A = 25°C, unless otherwise noted.)

Parameter	Rating
1.8 V Supply Voltage (VDD18RF, VDD18VCO, VDD18BB, VDD18DIG)	–0.3 V to +3.5 V
IO Supply Voltage (VDDIO)	-0.3 V to +5.5 V
Analog Input Voltage	–0.3 V to V_{DD18} +0.3 V
Digital Input Voltage	–0.3 V to V_{DDIO} +0.3 V
Analog Output Voltage	–0.3 V to V_{DD18} +0.3 V
Digital Output Voltage	–0.3 V to V_{DDIO} +0.3 V
Operating Temperature	–45°C to +85°C
Storage Temperature Range	–65°C to +150°C

NOTES
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

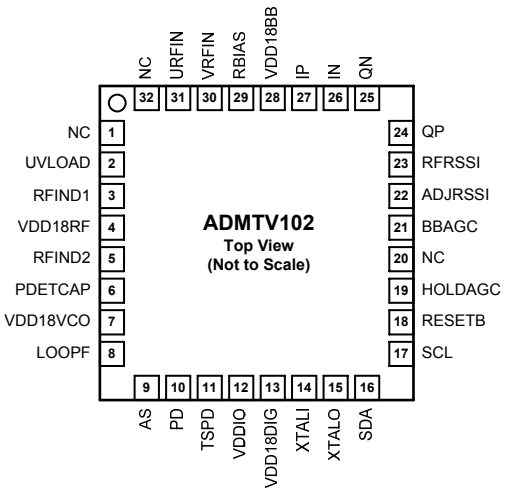

Figure 3. 32-Lead QFN Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	I/O Type	Description
1	NC		No connection.
2	UVLOAD	AO	VHF/UHF LNA load inductor. Connect a 39 nH from this pin to VDD18RF as close as possible.
3	RFIND1	AI	RFPGA inductor for bias. Connect a 100 nH from this pin to GND as close as possible.
4	VDD18RF	Power	RF power 1.8 V. Power decoupling capacitor is required. See application schematic.
5	RFIND2	AI	RFPGA inductor for bias. Connect a 100 nH from this pin to GND as close as possible.
6	PDETCAP	AO	External capacitor for RF power detector. Connect a 100 pF to GND.
7	VDD18VCO	Power	VCO power 1.8 V. Power decoupling capacitor is required. See application schematic..
8	LOOPF	AI	External loop filter components. Connect from this pin as close as possible.
9	AS	DI	Address select input. I^2C address can be determined by AS pin. If AS is GND, read mode: 0×c3, write mode: 0×c2. If AS is VDDIO, read mode: 0×c5, write mode: 0×c4.
10	PD	DI	Hardware power down. 0 V for operation and VDDIO for power down. To recover from the hardware PD state, PD control signal level from the controller should be low first. So the clock oscillator is powered up and the tuner can operate.
11	TSPD	DI	Time-slicing hardware power down. 0 V for operation and VDDIO for power down.
12	VDDIO	Power	IO power. 1.8 V ~ 3.3 V wide range IO. Power decoupling capacitor is required. See application schematic.
13	VDD18DIG	Power	Digital power 1.8 V. Power decoupling capacitor is required. See application schematic.
14	XTALI	DI	Crystal oscillator input. Inverter buffer input. PD should be 'low' state to oscillate.
15	XTALO	DO	Crystal oscillator output. Inverter buffer output. PD should be 'low' state to oscillate.
16	SDA	DB	I^2C data. Bi-directional pin. Open drain output. Requires a pull-up resistor to VDDIO.
17	SCL	DI	I^2C clock. Requires a pull-up resistor to VDDIO.
18	RESETB	DI	Reset input. 0 V for reset, VDDIO for normal operation.
19	HOLDAGC	DI	Test pin for holding AGC operation. Connect to GND for operation.
20	NC		No connection.
21	BBAGC	AI	External BBAGC input. 0 V ~ 1.8 V analog input.
22	ADJRSSI	AO	RSSI output voltage for adjacent channels. Connect a 33 nF to GND.
23	RFRSSI	AO	RSSI output voltage for wanted channel. Connect a 33 nF to GND.
24	QP	AO	Quadrature-phase positive output.

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Pin No.	Mnemonic	I/O Type	Description
25	QN	AO	Quadrature-phase negative output.
26	IN	AO	In-phase negative output.
27	IP	AO	In-phase positive output.
28	VDD18BB	Power	Baseband block power 1.8 V. Power decoupling capacitor is required. See application schematic.
29	RBIAS	AI	Bias reference input. Connect a 8.2 kΩ (1% tolerance) from this pin to GND as close as possible
30	VRFIN	AI	VHF RF input.
31	URFIN	AI	UHF RF input.
32	NC		No connection.

NOTES
AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, DB = Digital Bi-directional

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TERMINOLOGY

Table 6. Terminology

Parameter	Description
AGC	Automatic gain control.
IMD	Intermodulation distortion.
RSSI	Received signal strength indicator.
LNA	Low noise amplifier.
LPF	Low pass filter.
PGA	Programmable gain amplifier.
PLL	Phase locked loop.
QFN	Quad flat no-lead package.
SCL	Serial clock.
SDA	Serial data.
SNR	Signal to noise ratio.
T_A	Ambient temperature.
VCO	Voltage controlled oscillator.
VGA	Variable gain amplifier.
VSWR	Voltage standing wave ratio.

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TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD18} = 1.8 V, V_{DDIO} = 3.3 V, unless otherwise noted.

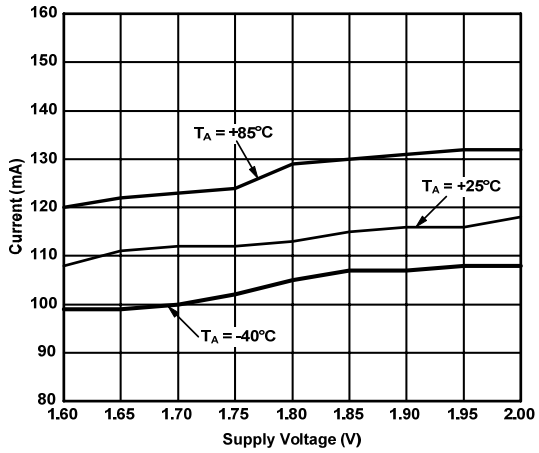

Figure 4 .UHF Receiver Mode Current vs. Supply Voltage

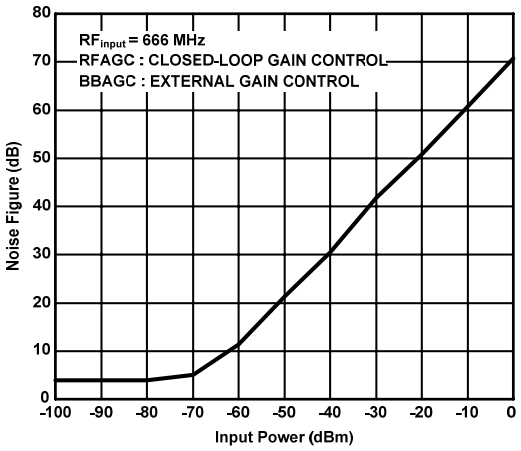

Figure 7 . UHF Noise Figure vs. Input Power

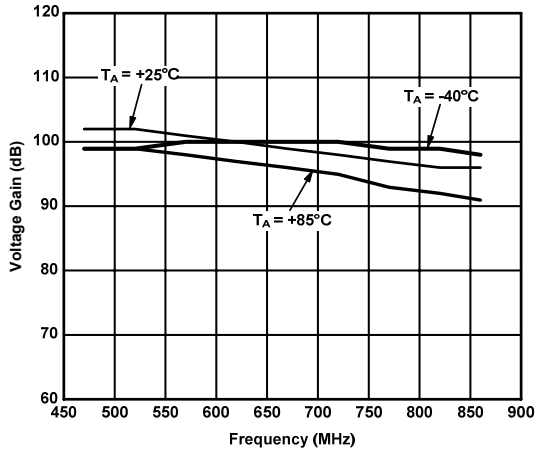

Figure 5. UHF Voltage Gain vs. Frequency

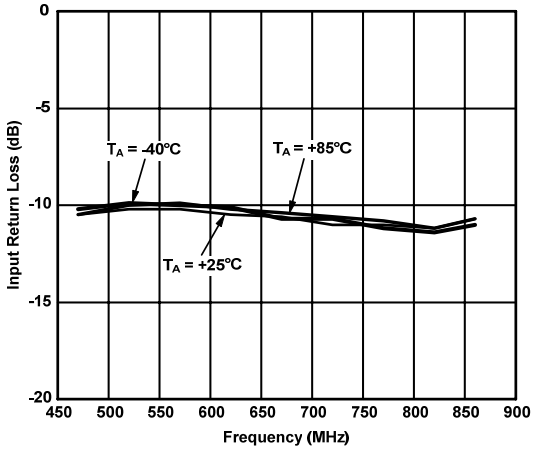

Figure 8 . UHF Input Return Loss vs. Frequency [LNA Gain Mode: High]

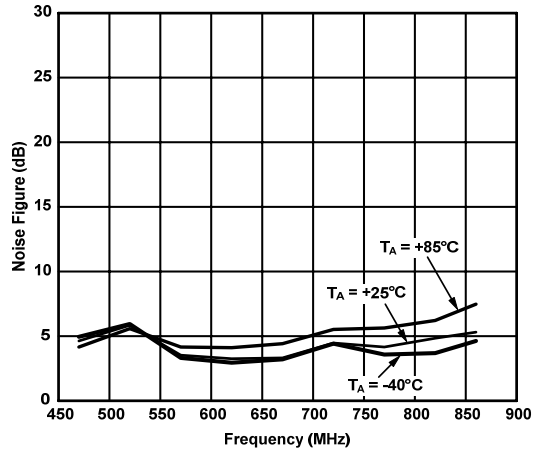

Figure 6 . UHF Noise Figure vs. Frequency

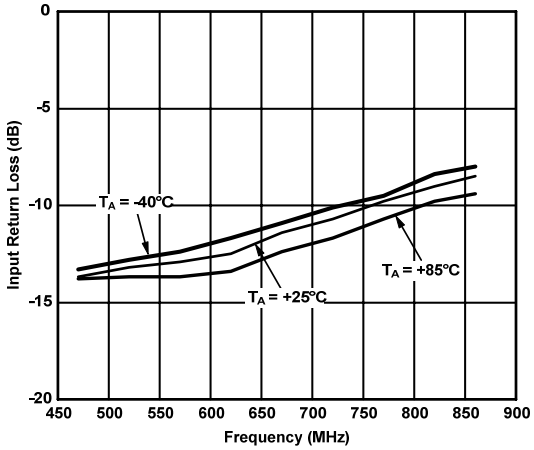

Figure 9 . UHF Input Return Loss vs. Frequency [LNA Gain Mode: Low]

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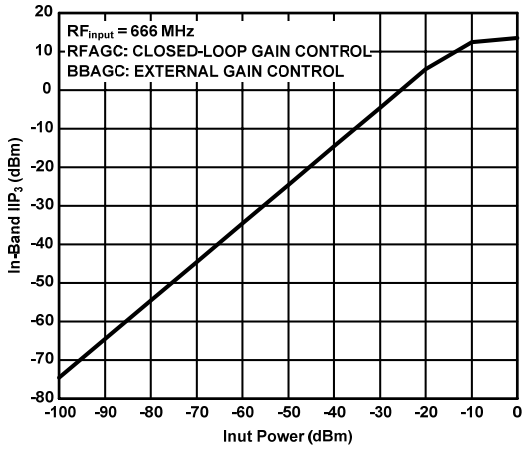

Figure 10. UHF In-Band IIP$_3$ vs. Input Power

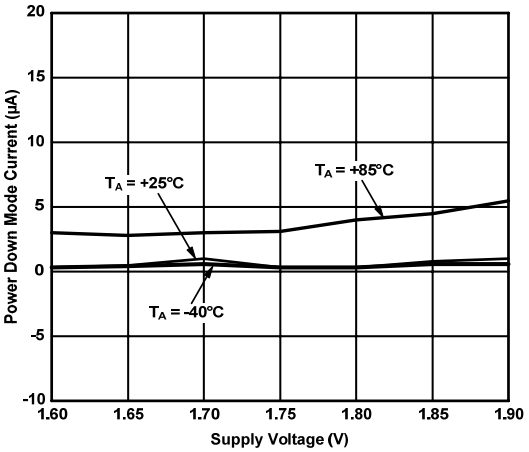

Figure 13.UHF Power Down Mode Current vs. Supply Voltage

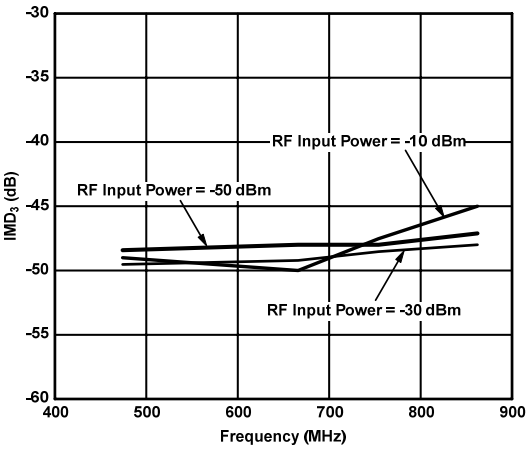

Figure 11. UHF In-Band IMD$_3$ vs. Frequency

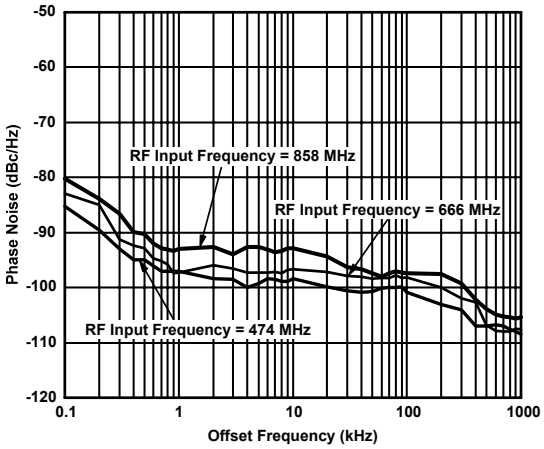

Figure 14. UHF Phase Noise vs. Offset Frequency

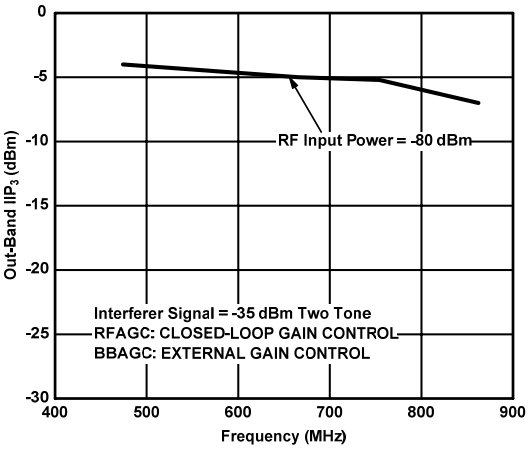

Figure 12. UHF Out-Band IIP$_3$ vs. Frequency

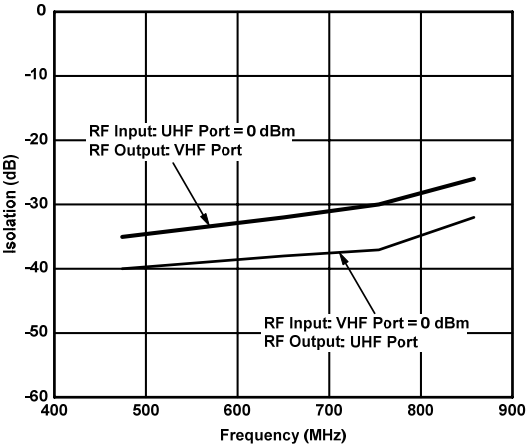

Figure 15. Port-to-Port Isolation

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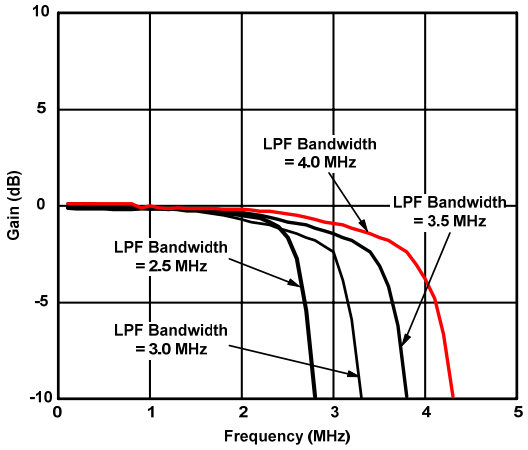

Figure 16. UHF Tunable Low Pass Filter Response

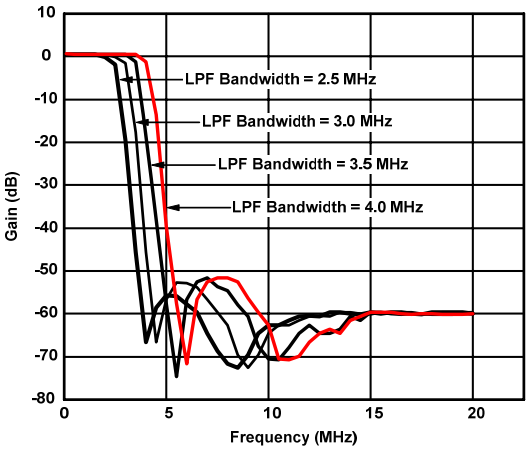

Figure 17. UHF Tunable Low Pass Filter Attenuation

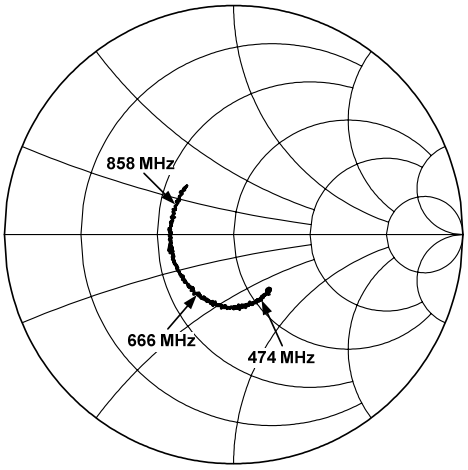

Figure 18. S_{11} of UHF RFIN vs. Frequency [High Gain Mode]

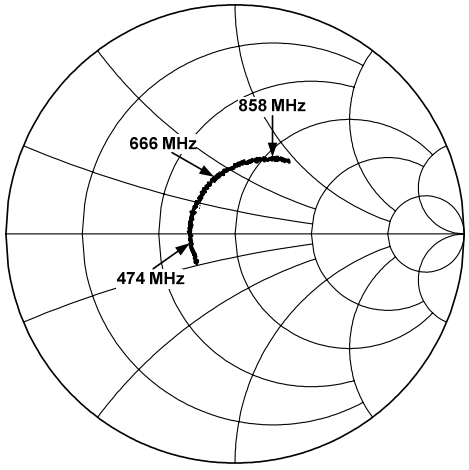

Figure 19. S_{11} of UHF RFIN vs. Frequency [Low Gain Mode]

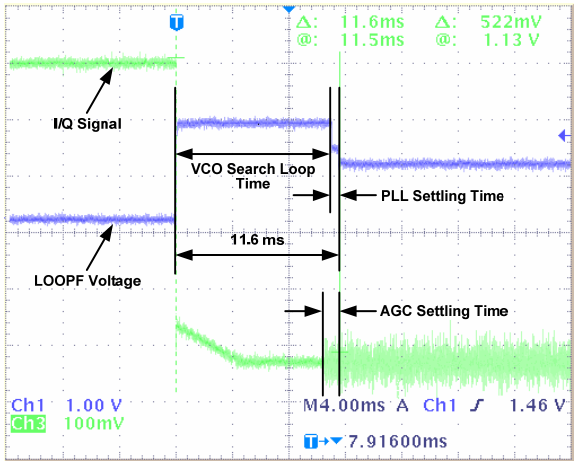

Figure 20. Software Power ON Timing

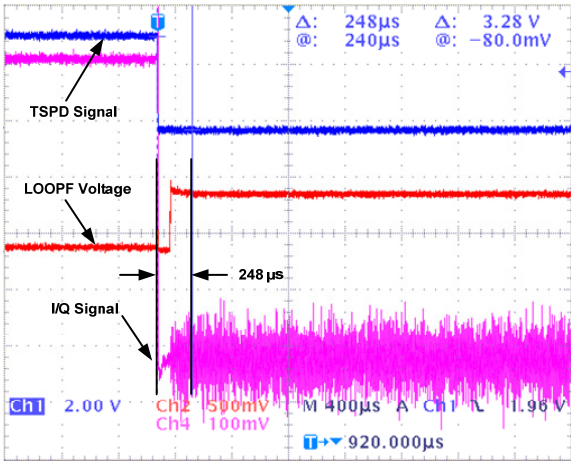

Figure 21. Time-slicing Power ON Timing

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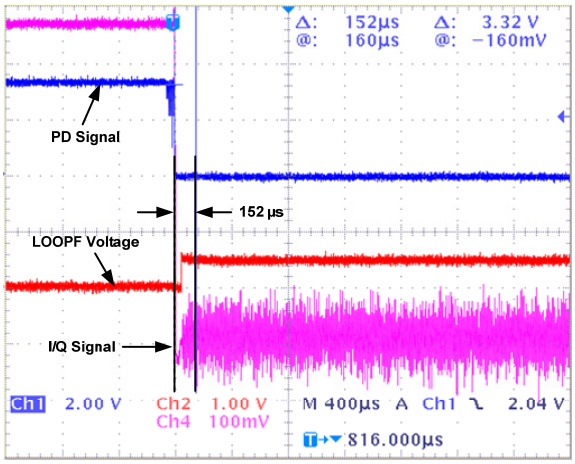

Figure 22. Hardware Power ON Timing

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FUNCTIONAL DESCRIPTIONS

I²C OPERATION

The ADMTV102 is controlled by an I²C data bus and is compatible with industry standard supporting fast mode format. Data and clock are fed on the SDA and SCL lines, respectively, as defined by the I²C bus format. The device can either accept data in the write-mode, or send data in the read-mode. The LSB of the address byte sets the device into write mode if it is low and read mode if it is high.

I²C READ/WRITE ADDRESS

Table 7. I²C Read/Write Address

Address Select Pin	Address								
READ MODE									
AS	MSB							LSB	Hex
Low	1	1	0	0	0	0	1	1	C3
High	1	1	0	0	0	1	0	1	C5
WRITE MODE									
AS	MSB							LSB	Hex
Low	1	1	0	0	0	0	1	0	C2
High	1	1	0	0	0	1	0	0	C4

I²C BUS FORMAT

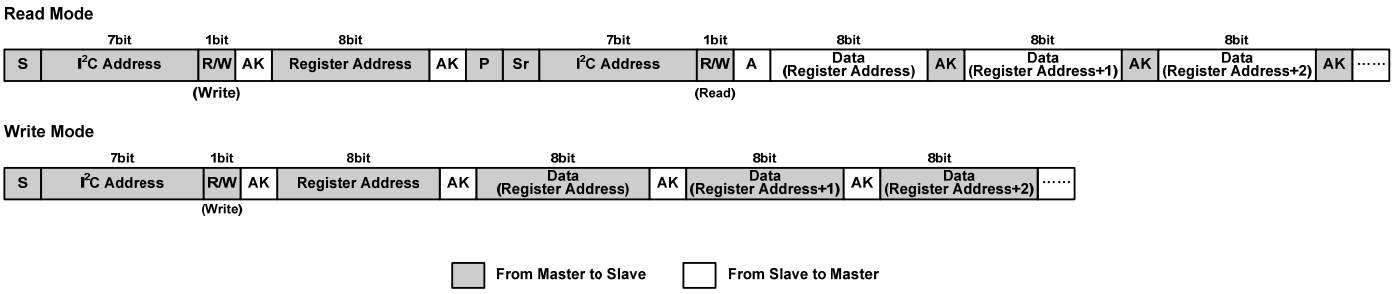

Figure 23. I²C Bus Format

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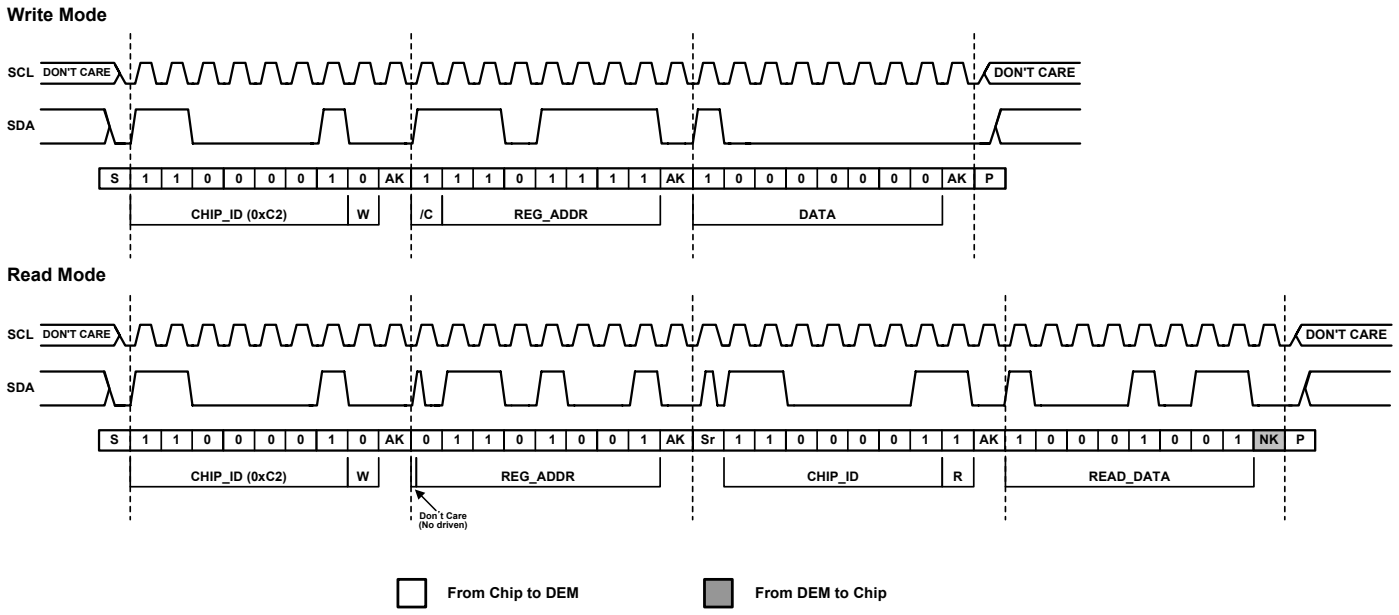
TIMING CHARACTERISTICS

(T_A = 25°C, V_{DDIO} = 3.3 V, GND = 0 V, unless otherwise noted.)

According to standard I²C specification, the CLK frequency reaches maximum 400 kHz in fast-mode and 100 kHz in standard-mode. To communicate with RF tuner, you need to comply as the following timing diagrams.



NOTES
S = Start Condition, P = Stop Condition, Sr = Repeated Start (Stop + Start, fast transition) condition, AK = Acknowledge : Active low, NK = Not Acknowledge : Active high, W = Write mode, R = Read mode, C = Automatic Address Increase mode, /C = Single Input Address mode
ADMTV102 meets the demanding performance specification of I²C combined mode. Therefore, upper access condition is able to be modified on standard I²C.

Figure 24. Serial Control Port Write/ Read Mode

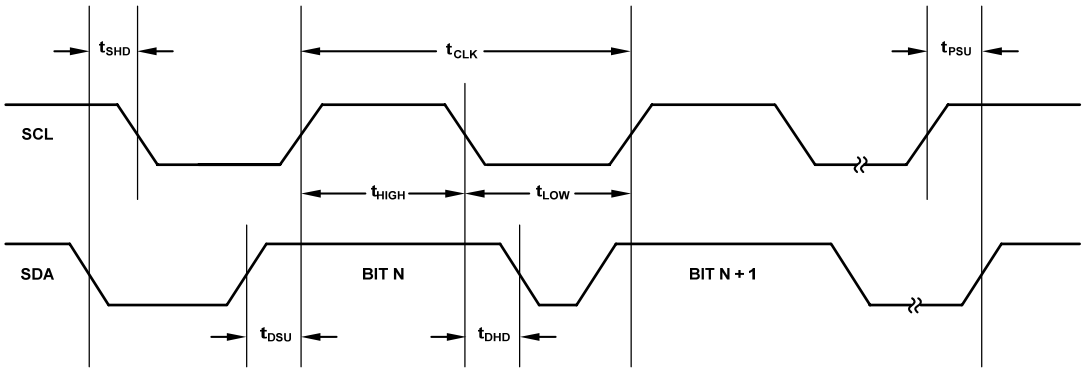


Figure 25. Serial Control Port Timing

Table 8. Serial Control Port Timing

Parameter	Symbol	Standard-mode		Fast-mode		Unit
		Min	Max	Min	Max	
Hold Time (Repeat) Start Condition[1]	t_{SHD}	4.0		0.6		µs
SCL Clock Period	t_{CLK}	0	100	0	400	kHz
HIGH Period of the SCL Clock	t_{HIGH}	4.0		0.6		µs
LOW Period of the SCL Clock	t_{LOW}	4.7		1.3		µs

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Parameter	Symbol	Standard-mode		Fast-mode		Unit
		Min	Max	Min	Max	
Set-up Time for STOP Condition	t_{PSU}	4.0		0.6		µs
Data Set-up Time	t_{DSU}	250		100[2]		µs
Data Hold Time for I²C Bus Devices.	t_{DHD}	5.0				µs
		0[3]	3.45[4]	0[3]	0.9[4]	µs

NOTES
[1]Afer this period, the first clock pulse is generated.
[2]A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{DSU} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal.
[3]A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.
[4]The maximum t_{DHD} has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

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I²C REGISTER MAP

Table 9. I²C Register Map.

Addr (Hex)	Type	Parameter	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Reset Value (Hex)	Initialization Value (Hex)
00	R	SPLITID	SPLITID<7:0>								0e	
01	R	CHIPID 0	CHIPID<15:8>								02	
02	R	CHIPID 1	CHIPID<7:0>								00	
03	R	Reserved										
04	R	BBAGC 0 and Loop Filter	GVBB<3:0>				ADCOUT<3:0>					
05	R	RFAGC 0	RFAGC<7:0>									
06	R	RFAGC 1	Reserved						LOCK<0>	RFAGC<8>		
07 to 09	R	Reserved										
0a	R	I/Q OFFSET 0	IOFFSET<11:8>				QOFFSET<11:8>					
0b	R	IOFFSET 1	IOFFSET<7:0>									
0c	R	QOFFSET 1	QOFFSET<7:0>									
0d	R	LNA 0 and VCO 0	Blank	LNAGAIN<1:0>		VCORG<4:0>						
0e	R	Low Pass Filter 0	Blank			CTUNEI2C<4:0>						
0f	R	Low Pass Filter 1	Blank			CTUNE<4:0>						
10	R/W	RF Band Select	BAND<1:0>		Reserved						49	4c
11 to 14	R/W	Reserved										
15	R/W	Low Pass Filter 2	Blank		Reserved			LPFBW<2:0>			25	3d
16	R/W	Reserved										
17	R/W	RSSI	Reserved	ADJ<2:0>			TOP<3:0>				c8	9a
18	R/W	Reserved										
19	R/W	PLL 0	Reserved				PLLR<3:0>				01	
1a	R/W	PLL 1	ICP<5:0>						PLLN<9:8>		28	
1b	R/W	PLL 2	PLLN<7:0>								20	
1c	R/W	VCO 1 And PLL 3	VCOSEL<0>	DIVSEL<2:0>			PLLF<19:16>				30	
1d	R/W	PLL 4	PLLF<15:8>								00	
1e	R/W	PLL 5	PLLF<7:0>								80	
1f to 23	R/W	Reserved										
24	R/W	Low Pass Filter 3	Reserved	CLKSELI2C<2:0>			Reserved				ad	1a
25	R/W	Low Pass Filter 4	CTUNEOFS<4:0>					EXTUNE<0>	TUNEEN<0>	Reserved	02	6e
26 to 2e	R/W	Reserved										
2f	R/W	PLL 6	RST_PLL<0>	PC4<0>	PC8_16<0>	VCORG_I2C<4:0>					10	
30	R/W	Reserved										
31	R/W	BBAGC 1	Reserved					DIVAGOCK<2:0>			44	04

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Addr (Hex)	Type	Parameter	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Reset Value (Hex)	Initialization Value (Hex)
32 to 38	R/W	Reserved										
39	R/W	VCO 2	Reserved	EXTVCORG <0>	Reserved						80	
3a to 42	R/W	Reserved										
43	R/W	TSPD 0	Blank	TSPD ALL<0>	TSPD PLL<0>	TSPD VCO<0>	TSPD RSSIRTUNE <0>	TSPD RFRSSI<0>	TSPD ADJRSSI<0>	TSPD PWDET<0>	7f	
44	R/W	TSPD 1	TSPD OSC<0>	TSPD LPF<0>	TSPD MIX<0>	TSPD RFPGA<0>	TSPD LNA<0>	TSPD BGR<0>	TSPD TPSNS<0>	TSPD BBPGA<0>	ff	f8
45	R/W	SWPD 0	Blank	SWPD ALL<0>	SWPD PLL<0>	SWPD VCO<0>	SWPD RSSIRTUNE <0>	SWPD RFRSSI<0>	SWPD ADJRSSI<0>	SWPD PWDET<0>	00	
46	R/W	SWPD 1	Blank	SWPD LPF<0>	SWPD MIX<0>	SWPD RFPGA<0>	SWPD LNA<0>	SWPD BGR<0>	SWPD TPSNS<0>	SWPD BBPGA<0>	00	
47	R/W	RF Gain And BBAGC 2	LNAGAINI2C <1:0>	Reserved						EXTGVBB <0>	c2	
48	R/W	BBAGC 3	GVBBI2C<3:0>				Reserved				82	21
49 to 50	R/W	Reserved										
51	R/W	RFAGC 2	Blank					RFAGCMAX <8>	RFAGCMIN <8>	RFAGCI2C <8>	05	
52	R/W	RFAGC3	RFAGCMAX<7:0>								7f	
53	R/W	RFAGC 4	RFAGCMIN<7:0>								01	
54	R/W	RFAGC 5	RFAGCI2C<7:0>								7f	
55	R/W	TSPD Polarity	Reserved							TSPDPOL <0>	f0	

NOTES
This table has reserved bits in order to guarantee performance. Contact Analog Devices to get the latest initialization file.
Reset value is factory value.
R: Read Only.
R/W: Read and Write.

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DETAILED REGISTER DESCRIPTION

Table 10. Read-only Register

Reg. Addr (Hex)	Bit(s)	Name	Description
00	<7:0>	SPLITID<7:0>	Chip split ID.
01	<7:0>	CHIPID<15:8>	Chip ID.
02	<7:0>	CHIPID<7:0>	Chip ID.
04	<3:0>	ADCOUT<3:0>	VLFO(PLL loop filter output voltage) = 0.2 + ADCOUT × 0.1 ~ 0.3 + ADCOUT × 0.1 If ADCOUT is 0×C2. <3:0> = 0×2: VLFO = 0.2 + 2 × 0.1= 0.4 V <3:0> = 0×C: VLFO = 0.2 + 12 × 0.1= 1.3 V
04	<7:4>	GVBB<3:0>	Baseband PGA gain control. Step: 3 dB. <3:0> = 0×00: Minimum gain. <3:0> = 0×0e: Maximum gain.
05	<7:0>	RFAGC<7:0>	Gain code value of RFPGA. <8:0> = 0×000: RFAGC minimum gain. <8:0> = 0×17f: RFAGC maximum gain.
06	<0>	RFAGC<8>	
06	<1>	LOCK<0>	PLL lock indicator. <0> = 0×1: PLL is locked. <0> = 0×0: PLL is unlocked.
0a	<3:0>	QOFFSET<11:8>	I/Q path DC offset digital code value. <11:0> = 0×000: Minimum value. <11:0> = 0×800: Norminal center value when there is no DC offset. <11:0> = 0×fff: Maximum value.
0a	<7:4>	IOFFSET<11:8>	
0b	<7:0>	IOFFSET<7:0>	
0c	<7:0>	QOFFSET<7:0>	
0d	<4:0>	VCORG<4:0>	VCO varactor diode operation range (varactor switch). <4:0> = 0×00: Lowest frequency of VCO oscillation. <4:0> = 0×1f: Highest frequency of VCO oscillation.
0d	<6:5>	LNAGAIN<1:0>	LNAGAIN status. <1:0> = 0×0: Low gain. <1:0> = 0×3: High gain.
0e	<4:0>	CTUNEI2C<4:0>	Cap bank value after auto tuning without offset value.
0f	<4:0>	CTUNE<4:0>	CTUNE is a low pass filter's cap bank value plus offset. CTUNE value is calculated as below condition. CTUNE value. 1) If EXTUNE = 0, CTUNE<4:0> = CTUNEI2C<4:0> + CTUNEOFS<3:0> when CTUNEOFS<4> = 0, CTUNE<4:0> = CTUNEI2C<4:0> – CTUNEOFS<3:0> when CTUNEOFS<4> = 1, 2) If EXTUNE = 1, CTUNE<4:0> = CTUNEOFS<4:0>

NOTES
Initialization file overrides reset value. Contact Analog Devices to get the latest initialization file.

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Table 11. Signal Path Register Setting

Reg. Addr (Hex)	Bit(s)	Name	Description
10	<7:6>	BAND<1:0>	RF input band selection. <1:0> = 0×0: VHF <1:0> = 0×1: UHF <1:0> = 0×2: UHF
15	<2:0>	LPFBW<2:0>	Low pass filter cut-off frequency selection. <2:0> = 0×5: 4 MHz (For 8 MHz channel bandwidth) <2:0> = 0×4: 3.5 MHz (For 7 MHz channel bandwidth) <2:0> = 0×3: 3 MHz (For 6 MHz channel bandwidth) <2:0> = 0×2: 2.5 MHz (For 5 MHz channel bandwidth)
24	<6:4>	CLKSELI2C<2:0>	Reference clock selection. <2:0> = 0×0: 13 MHz <2:0> = 0×1: 16.384 MHz <2:0> = 0×2: 19.2 MHz <2:0> = 0×3: 20.48 MHz <2:0> = 0×4: 24.576 MHz <2:0> = 0×5: 26 MHz <2:0> = 0×6: 36 MHz <2:0> = 0×7: 38.4 MHz
25	<1>	TUNEEN<0>	Cut-off frequency auto tuning enable of low pass filter. <0> = 0×0: Disable. <0> = 0×1: Enable.
25	<2>	EXTUNE<0>	External setting enable of low pass filter cap bank. See CTUNE<4:0> description (0×0f address). <0> = 0×0: Disable. <0> = 0×1: Enable.
25	<7:3>	CTUNEOFS<4:0>	Cap bank offset value. It needs to change the CTUNE value after cut-off frequency auto tuning. See CTUNE<4:0> description (0×0f address).

NOTES
Initialization file overrides reset value. Contact Analog Devices to get the latest initialization file.

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Table 12. VCO/PLL Register Setting

Reg. Addr (Hex)	Bit(s)	Name	Description
19	<3:0>	PLLR<3:0>	PLL reference divider: Fref (Reference frequency) = Fck (Reference clock) ÷ PLLR (Reference divider). <3:0> = 0×1: Default value.
1a	<7:2>	ICP<5:0>	Charge pump current control. Current = {ICP (decimal) + 1} × 10 µA
1a	<1:0>	PLLN<9:8>	PLLN is integral part of feedback divider. PLLF is fractional part of feedback divider. LO frequency = {Clock frequency × (PLLN + PLLF ÷ 2^20)} ÷ PLLR
1b	<7:0>	PLLN<7:0>	
1c	<6:4>	DIVSEL<2:0>	Divider value selection register. <2:0> = 0×0: Generate divider 32 value of VCO frequency. (LO output frequency: 58.75 ~ 117.5 MHz) <2:0> = 0×1: Generate divider 16 value of VCO frequency. (LO output frequency: 117.5 ~ 235 MHz) <2:0> = 0×2: Generate divide 8 value of VCO frequency. (LO output frequency: 235 ~ 470 MHz) <2:0> = 0×3: Generate divide 4 value of VCO freuqency (LO output frequency: 470 ~ 940 MHz) <2:0> = 0×4: Generate divide 2 value of VCO frequency. (LO output frequency: 940 ~ 1880 MHz)
1c	<7>	VCOSEL<0>	VCO selection register. <0> = 0×0: Enable low band VCO. Low band VCO frequency range: 1880 ~ 2630 MHz. <0> = 0×1: Enable high band VCO. High band VCO frequency: 2630 ~ 3760 MHz.
1c	<3:0>	PLLF<19:16>	PLLF is fractional part of feedback divider. LO frequency = {Clock frequency × (PLLN + PLLF ÷ 2^20)} ÷ PLLR
1d	<7:0>	PLLF<15:8>	
1e	<7:0>	PLLF<7:0>	
2f	<4:0>	VCORG_I2C<4:0>	External registers setting for capacitor bank in VCO core. Write mode: When EXTVCORG<0> is enable. <4:0> = 0×00: Mimimum oscillation frequency. <4:0> = 0×1f: Maximum oscillation frequency.
2f	<5>	PC8_16<0>	Prescaler divider ratio setting value:
2f	<6>	PC4<0>	PC4<0> PC8_16<0> Prescaler divider 0 0 8/9 ratio 0 1 16/17 ratio 1 0 4/5 ratio 1 1 4/5 ratio
2f	<7>	RST_PLL<0>	PLL Reset. <0> = 0×1: Reset.
39	<6>	EXTVCORG<0>	Manual control of VCO search loop. <0> = 0×1: When EXTVCORG<0> is enabled, VCORG_I2C register operates.

NOTES
Initialization file overrides reset value. Contact Analog Devices to get the latest initialization file.

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Table 13. AGC Register Setting

Reg. Addr (Hex)	Bit(s)	Name	Description
17	<3:0>	TOP<3:0>	TOP is RF gain control register. When close to 0×0, linearity is improved, but tuner output SNR and NF are degraded. When close to 0×b, linearity is degraded, but tuner output SNR and NF are improved. Step is 3 dB. <3:0> = 0×0: 33 dB <3:0> = 0×1: 30 dB <3:0> = 0×2: 27 dB <3:0> = 0×3: 24 dB <3:0> = 0×4: 21 dB <3:0> = 0×5: 18 dB <3:0> = 0×6: 15 dB <3:0> = 0×7: 12 dB <3:0> = 0×8: 9 dB <3:0> = 0×9: 6 dB <3:0> = 0×a: 3 dB <3:0> = 0×b: 0 dB
17	<6:4>	ADJ<2:0>	ADJ is gain control register of adjacent channel power detector. Gain step is 3 dB. <2:0> = 0×0: 6 dB <2:0> = 0×1: 3 dB <2:0> = 0×2: 0 dB <2:0> = 0×3: -3 dB <2:0> = 0×4: -6 dB <2:0> = 0×5: -9 dB <2:0> = 0×6: -2 dB <2:0> = 0×7: -5 dB
31	<2:0>	DIVAGOCK<2:0>	DIVAGOCK is digital gain switching speed of BBPGA. Fck is a reference clock. Baseband digital gain switching speed = Fck/2^(DIVAGOCK+8)
47	<0>	EXTGVBB<0>	Enternal GVBB setting when EXTGVBB is 0x1. <0> = 0×0: Disable. <0> = 0×1: Enable.
47	<7:6>	LNAGAINI2C<1:0>	LNA Gain mode manual setting when TOP is 0×f. If UHF mode, <1:0> = 0×0: Low gain. <1:0> = 0×3: High gain. If VHF mode, <1:0> = 0×0: Low gain. <1:0> = 0×1, 0×2, 0×3: High gain.
48	<7:4>	GVBBI2C<3:0>	GVBBI2C is external baseabnd PGA gain control when EXTGVBB<0> = 0×1. <3:0> = 0×00: Minimum gain. <3:0> = 0×0e: Maximum gain.
51	<0>	RFAGCI2C<8>	RFAGC manual gain setting when TOP = 0×f.
54	<7:0>	RFAGCI2C<7:0>	
53	<7:0>	RFAGCMIN<7:0>	RFAGC minimum limit value.
51	<1>	RFAGCMIN<8>	
52	<7:0>	RFAGCMAX<7:0>	RFAGC maximum limit value.
51	<2>	RFAGCMAX<8>	

NOTES
Initialization file overrides reset value. Contact Analog Devices to get the latest initialization file.

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Table 14. Miscellaneous Register Setting

Reg. Addr (Hex)	Bit(s)	Name	Description
43	<0>	TSPDPWDET<0>	Time slicing power down control register for RF power detector. 1: PD. 0: Enable.
43	<1>	TSPDADJRSSI<0>	Time slicing power down control register for ADJRSSI. 1: PD. 0: Enable.
43	<2>	TSPDRFRSSI<0>	Time slicing power down control register for RFRSSI. 1: PD. 0: Enable.
43	<3>	TSPDRSSIRTUNE<0>	Time slicing power down control register for resistor tuning block of RSSI. 1: PD. 0: Enable.
43	<4>	TSPDVCO<0>	Time slicing power down control register for VCO. 1: PD. 0: Enable. Power saving current: 25.28 mA
43	<5>	TSPDPLL<0>	Time slicing power down control register for PLL. 1: PD. 0: Enable. Power saving current: 3.83 mA
43	<6>	TSPDALL<0>	Time slicing power down control register for all block. 1: PD. 0: Enable. Power saving current: 110 mA
44	<0>	TSPDBBPGA<0>	Time slicing power down control register for BBPGA. 1: PD. 0: Enable. Power saving current: 4.25 mA
44	<1>	TSPDTPSNS<0>	Time slicing power down control register for temperature sensor. 1: PD. 0: Enable.
44	<2>	TSPDBGR<0>	Time slicing power down control register for band gap reference. 1: PD. 0: Enable. Power saving current: 0.61 mA
44	<3>	TSPDLNA<0>	Time slicing power down control register for LNA. 1: PD. 0: Enable.
44	<4>	TSPDRFPGA<0>	Time slicing power down control registe for RFPGA. 1: PD. 0: Enable.
44	<5>	TSPDMIX<0>	Time slicing power down control register for Mixer. 1: PD. 0: Enable.
44	<6>	TSPDLPF<0>	Time slicing power down control register for LPF. 1: PD. 0: Enable.
44	<7>	TSPDOSC<0>	Time slicing power down control register for crystal oscillator. 1: PD. 0: Enable.
45	<0>	SWPDPWDET<0>	Software power down control register for RF power detector. 1: PD. 0: Enable.
45	<1>	SWPDADJRSSI<0>	Software power down control register for ADJRSSI. 1: PD. 0: Enable.
45	<2>	SWPDRFRSSI<0>	Software power down control register for RFRSSI. 1: PD. 0: Enable.
45	<3>	SWPDRSSIRTUNE<0>	Software power down control register for resistor tuning block of RSSI. 1 : PD. 0: Enable.
45	<4>	SWPDVCO<0>	Software power down control register for VCO. 1: PD. 0: Enable.
45	<5>	SWPDPLL<0>	Software power down control register for PLL. 1: PD. 0: Enable.
45	<6>	SWPDALL<0>	Software power down control register for all block. 1: PD. 0: Enable.
46	<0>	SWPDBBPGA<0>	Software power down control register for BBPGA. 1: PD. 0: Enable.
46	<1>	SWPDTPSNS<0>	Software power down control register for temperature sensor. 1: PD. 0: Enable.
46	<2>	SWPDBGR<0>	Software power down control register for band gap reference. 1: PD. 0: Enable.
46	<3>	SWPDLNA<0>	Software power down control register for LNA. 1: PD. 0: Enable.
46	<4>	SWPDRFPGA<0>	Software power down control register for RFPGA. 1: PD. 0: Enable.
46	<5>	SWPDMIX<0>	Software power down control register for Mixer. 1: PD. 0: Enable.
46	<6>	SWPDLPF<0>	Software power down control register for LPF. 1: PD. 0: Enable.
55	<0>	TSPDPOL<0>	Time slicing power down polarity control register.1: Inverting. 0: Normal. To use this feature, use the recommended programming guide for operation.

NOTES
Initialization file overrides reset value. Contact Analog Devices to get the latest initialization file.

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RFAGC SETTING

ADMTV102 has RF/BB dual AGC loops. RFAGC loop is controlled internally and BBAGC is controlled by BBAGC voltage from demodulator. RF gain is digitally controlled by internal power detectors, which are RF power detector, ADJRSSI and RFRSSI. For test purpose, RF gain and baseband gain can also be set manually.

AUTOMATIC RF GAIN SETTING USING INTERNAL RFAGC (DEFAULT)

For TOP (address = 0×17) value from 0×0 to 0×b, internal RFAGC operates. When increasing TOP (address = 0×17) value, TOP (take-over point) increases by 3 dB step.

TOP value is optimized considering various tuner performances. If TOP value is decreased, tuner linearity is improved but tuner output SNR and NF are degraded. When TOP value is increased, tuner linearity is degraded but the tuner output SNR and NF are improved.

MANUAL RF GAIN SETTING

For RFAGC manual gain setting, TOP (address = 0×17) should be set 0×f. With this setting, RFAGC (address = 0×06 & 0×05) value is loaded from RFAGCI2C (address = 0×51 & 0×54). RFAGC value should be between 0×000 and 0×17f.

LNA gain is also set manually. LNAGAINI2C (address = 0×47) value = 0×0 is low gain state and 0×3 is high gain state.

In order to set RF gain manually, set as following:

1. TOP (address = 0×17) = 0×0f
2. RFAGCI2C<8:0> (address = 0×51 & 54) = Desired value (0×0 ~ 0×17f)
3. LNAGAINI2C<1:0> (address = 0×47) = Desired value (0×0 or 0×3)

BBAGC SETTING

ADMTV102 supports two BBAGC modes, which are external (from demodulator) BBAGC mode, and manual gain setting mode for test purpose.

EXTERNAL BBAGC MODE (DEFAULT AND AUTOMAIC GAIN CONTROL FROM DEMODULATOR)

At default, BBAGC of the ADMTV102 is controlled by BBAGC voltage from demodulator. In order to use AGC signal from demodulator, set as following:

1. EXTGVBB (address = 0×47) = 0
2. Connect BBAGC voltage line from demodulator (0 ~ 1.8 V) to BBAGC (pin 21) via proper low pass filter.

MANUAL BBAGC SETTING

By changing GVBBI2C<3:0> (address = 0×48), baseband gain can be changed.

For baseband manual gain setting, EXTGVBB (address=0×47) should be set as 0×1. At this setting, GVBB (address: 0×4) value is loaded from GVBBI2C (address: 0×48).

In order to set baseband gain manually, set as following:

1. EXTGVBB (address = 0×47) = 1
2. GVBBI2C (address = 0×48) = Desired value (0×00 ~ 0×0e)
3. Connect BBAGC voltage (0 ~ 1.8 V) to BBAGC (pin 21) via proper low pass filter.

Baseband gain is controlled by digital and analog part. External analog voltage changes baseband gain by 12 dB (0 ~ 1.8 V). For GVBB value from 0×0 to 0×e, digital gain is controlled by 3 dB step.

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THEORY OF OPERATION

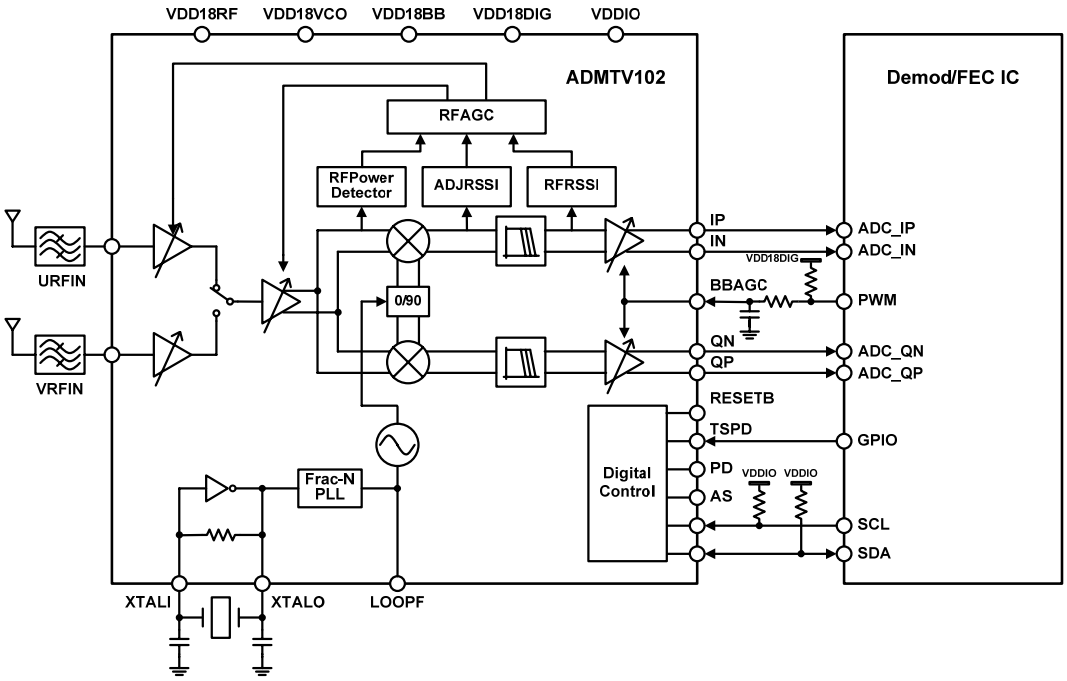

Figure 26. ADMTV102 Interface

RF LNA, PGA AND I/Q DOWN-CONVERTER

RF LNA, PGA and I/Q down-converter amplify coming RF signals and down-convert to baseband. LNA gain switches between high and low gain with 20 dB step. LNA gain state can be read from LNA gain register (0: low gain, 3: high gain). RFPGA has around 50 dB gain dynamic range. RFPGA gain is controlled by digital gain code, which can be read from RFAGC<8:0> register. RFPGA gain is from 0×000 (minimum gain) to 0×17f (maximum gain). Gain step is around 0.5 dB.

I/Q down conversion mixer converts the signal from RFPGA's output to baseband.

LOCAL OSCILLATOR

The ADMTV102 includes an on-chip VCO, which eliminates the external LC tank. There is no need for external LC tank tuning. The VCO in ADMTV102 uses only 1.8 V. The internal VCO covers whole VHF (174 ~ 245 MHz) and UHF (470 ~ 862 MHz). Along with fractional-N PLL, this low phase noise VCO guarantees sufficient performance for mobile reception of worldwide mobile-TV signals.

PLL

ADMTV102 local oscillator consists of a sigma-delta fractional-N frequency synthesizer and a VCO. The integrated VCO covers whole VHF and UHF frequency range.

The synthesizer uses fractional-N type architecture with high performance 20-bit sigma-delta modulator to get a high resolution and the fast switching time as well as a good phase noise. The charge pump is programmed by 6-bit digital control and its current range is from 10 µA to 640 µA. Charge pump current can be adjusted by loop filter voltage and VCO range.

Unlike the integer-N type synthesizer, sigma-delta modulated frequency synthesizer provides: 1. Fast switching time, 2. Ultra high frequency resolution, 3. Good phase noise due to its wide bandwidth. The switching time is less than 30 µsec for the worst case of power up sequence. Using 16.384 MHz oscillator, 20-bit sigma-delta modulated fractional-N phase locked loop exhibits very fine frequency resolution of 16 Hz. It can compensate the frequency offset induced by the reference crystal frequency error, the temperature drift of crystal, etc. The LO frequency, f_{LO}, is calculated as following equation,

$$\text{LO frequency} = \{\text{Clock frequency} \times (\text{PLLN} + \text{PLLF} \div 2^{20})\} \div \text{PLLS}$$

where PLLN is N-counter divide value, PLLF is the fractional value, and PLLS is reference divide ratio.

BASEBAND LPF AND VGA

The baseband block contains LPF and VGA. The RF signal goes down to baseband through I/Q down-converter. The baseband LPF selects the wanted signal at the output of down-converter. The cut-off frequency of LPF is programmable according to

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application. To compensate the variation of cut-off frequency in the LPF, the automatic cut-off tuning circuit is included and this circuit guarantees the cut-off frequency accuracy.

The baseband VGA controls the input level of ADC in demodulators. It consists of PGA cell and VGA cell which is controlled by 15-step digital gain mode and analog AGC voltage respectively. Baseband PGA and VGA are also controlled by BBAGC voltage. The PGA gain setting is read from GVBB register. The GVBB ranges from 0×00 to 0×0e. Digital gain step is 3 dB. Baseband PGA gain setting can be programmed manually by GVBBI2C register for ADMTV102 test mode.

AUTOMATIC GAIN CONTROL

In ADMTV102, LNA has 2-step gain control, and gain range is 20 dB. RFPGA has around 50 dB gain dynamic range, and controlled by RFAGC<8:0> register. The register value is from 0×000 (minimum gain) to 0×17f (maximum gain). RFAGC consists of these 2 blocks. RFAGC dynamic range is around 70 dB.

Also, ADMTV102 BBVGA has programmable gain amplifier which gain step is 3 dB. ADMTV102 step gain is controlled by detection of external BBAGC. Baseband gain is determined by digital gain setting and analog voltage (0 ~ 1.8 V). Baseband gain varies by 12 dB according to analog voltage control from 0 V (minimum gain) to 1.8 V (maximum gain). Digital gain setting can be read via GVBB<3:0> register. The register value is from 0×00 (minimum gain) to 0×0e (maximum gain). BBVGA dynamic range is around 50 dB. With these two dynamic ranges (RFAGC 70 dB, BBAGC 50 dB), ADMTV102 dynamic range is larger than 100 dB.

Recommended output amplitude of ADMTV102 is from 300 mV to 700 mV (peak-to-peak voltage at each I/Q output pins). At 500 mV amplitude, ADMTV102 shows the best performance.

RFRSSI

The operation range of RFAGC block and BBAGC block is divided by TOP point. BBVGA is controlled by BBAGC voltage from demodulator. The demodulator generates the BBAGC voltage by measuring the tuner output I or Q level. When RF input level is weaker than TOP point, BBAGC block operates. BBAGC block consists of BBPGA and BBVGA. BBVGA operation range is from 0.0 V to 1.1 V and at these points the trip to BBPGA high or low operation occurs. When RF input level is stronger than the TOP point, RFPGA block operates. As the RF input level increases or decreases, RFPGA value decreases or increases. In the middle of the RFPGA operation range, the LNA ON/OFF operation occurs and this operation expands the dynamic range of the RFAGC block. The reason for the LNA ON/OFF hysteresis region is to avoid the LNA toggling action in case that LNA ON/OFF level is the same.

Following is the RFRSSI formula covering from -100 dBm to 0 dBm.

RF input power = −(RFAGC[8:0] × 0.12 dB) − (LNAGAIN[1:0] × 8.3 dB) + 8 − 3(GVBB[3:0] − 5) dB − 10(BBAGC_Control_Input − 0.5) dB

(±3 dB tolerance)

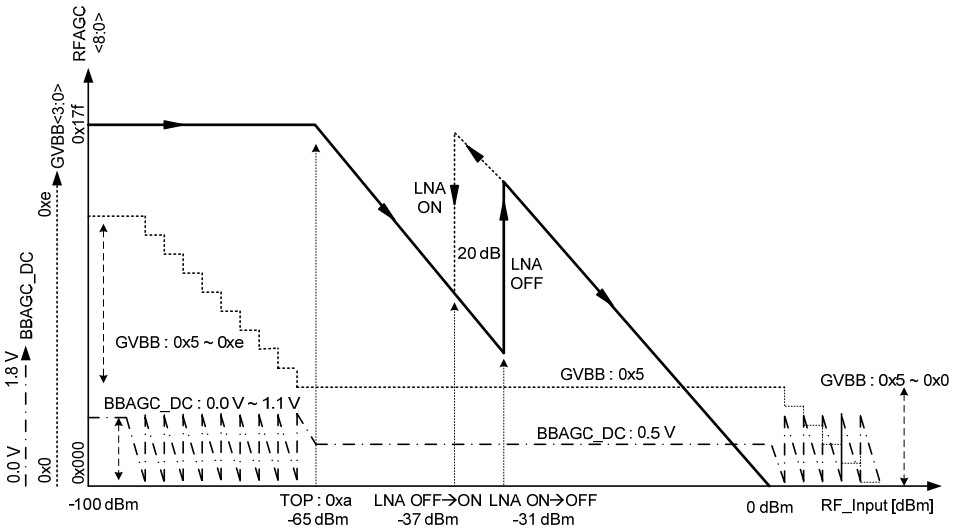

Figure 27. RFRSSI Graph

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I²C INTERFACE AND CLOCK CONTROL

ADMTV102 uses I²C bus interface (refer to the I²C-bus specification available from Philips Semiconductor). Serial data (SDA) and serial clock (SCL) carry information between the devices connected to the bus. Each device is recognized by a unique address and can operate as either a transmitter or receiver, depending on the function of the device.

HARDWARE/SOFTWARE/TIME-SLICING POWER DOWN

There is a hardware power-down pin (#10). If PD is high, ADMTV102 goes to hardware power down mode. To restart, PD should be low.

ADMTV102 also has software power down mode controlled by I²C SWPD register. At software power down mode, digital part keeps alive.

Along with two power down modes described above, ADMTV102 also supports time-slicing power down mode. User can select which blocks should be powered down in time-slicing power down mode.

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APPLICATIONS

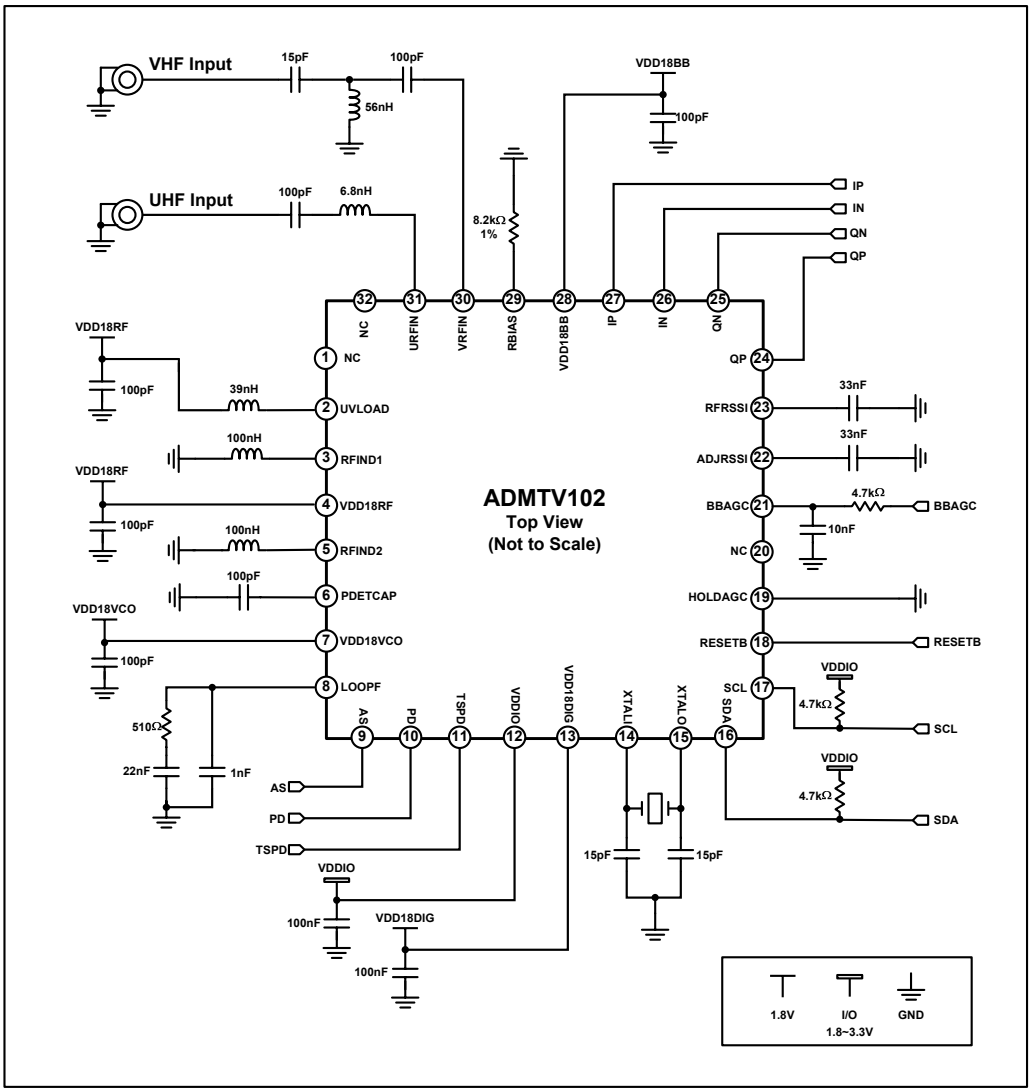

Figure 28. Application Schematic

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RF INPUT STAGE

RF matching components should be located as close as possible to chip. RF matching value should be changed to optimize.

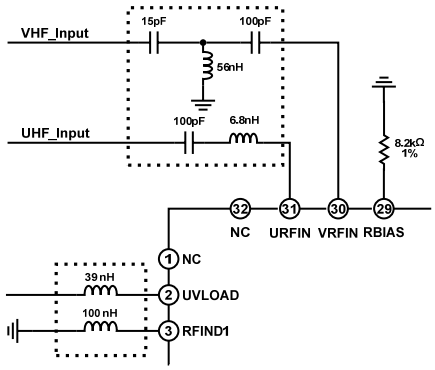

Figure 29. RF Input Stage

ESD PROTECTION

To improve ESD/EOS reliability, it is highly recommended to use TVS diode for ESD protection. When the TVS diode is applied, RF matching should be changed to optimize RF performance. RF matching should be similar to smith chart of Figure 18 and 19 in order to satisfy RF performance.

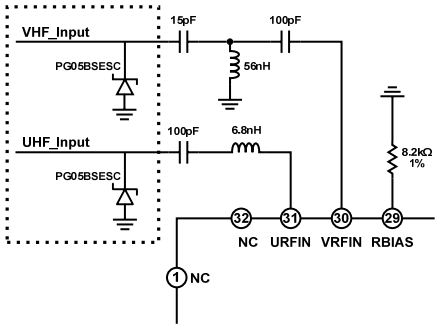

Figure 30. ESD Protection Application

VCO BIAS/BYPASS CAPACITORS

ADMTV102 has integrated VCO/PLLs for LO generation. The bypass capacitor of VDD18VCO rejects high frequency noise in power supply. Also, isolation of VDD18VCO power line from noisy power source is very important. These components should be located as close as possible to chip.

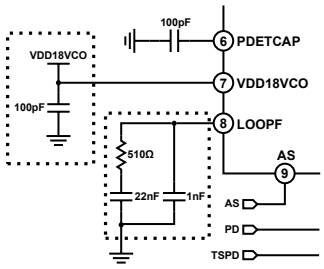

Figure 31. VCO Bias/Bypass Capacitors

DIGITAL INTERFACE - I²C/RESET

ADMTV102 is controlled by the I²C communication protocol. Maximum operating frequency of ADMTV102 I²C SCL is 400 kHz (2.5 µs). I²C address can be determined by AS pin. If AS is GND, read mode: 0×c3, write mode: 0×c2. If AS is VDDIO, read mode: 0×c5, write mode: 0×c4. SCL/SDA switching noise can degrade VCO phase noise and RC noise filter can help to reject this type of noise. ADMTV102 has a reset for I²C initialization and internal logic initialization. The reset pin is RESETB which is active low. If RESETB is low, ADMTV102 is in the reset state. If RESETB is high, ADMTV102 is in normal operation. Voltage of level high is VDDIO.

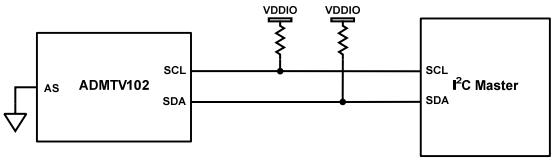

Figure 32. I²C Interface between ADMTV102 and I²C Controller

ISOLATION FROM DIGITAL PART

ADMTV102 is sensitive to digital switching noise. The digital part should be isolated from RF input of ADMTV102.

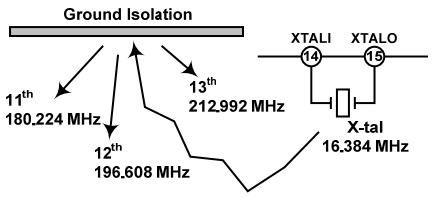

Figure 33. Isolation from Digital Part

BBVGA INTERCONNECTIONS

ADMTV102 supports only external BBAGC mode.

In order to use AGC signal from demodulator,

1. EXTGVBB (address = 0×47) = 0
2. Connect BBVGA control voltage (0 ~ 1.8 V) to pin 21 via proper LPF

If demodulator has open collector, ADMTV102 needs pull-up resistor.

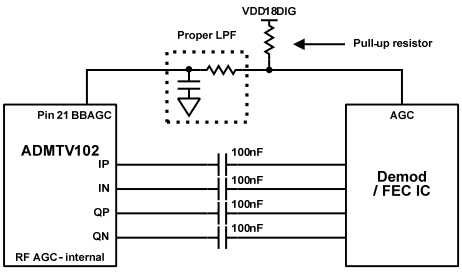

Figure 34. AGC Connection

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REFERENCE CLOCK SELECTION

ADMTV102 supports eight crystal/TCXO frequencies. Crystal load capacitor depends on crystal itself. Proper load capacitor should be used according to various crystals.

Table 15 shows reference clock related registers. When other reference clock is required, use the register settings in Table 15.

For each crystal frequency,

1. CLKSELI2C<2:0> = 0×24<6:4>
2. RFDIV<3:0> = 0×38<7:4>
3. DIVVCOCK<2:0> = 0×31<6:4>
4. DIVAGOCK<2:0> = 0×31<2:0>
5. DIVDCOFS<1:0> = 0×38<1:0>

Table 15. Reference Clock Selection Table

Crystal Frequncy (MHz)	CLKSELI2C <2:0>	RFDIV <3:0>	DIVVCOCK <2:0>	DIVAGOCK <2:0>	DIVDCOFS <1:0>
13	0	4	0	4	0
16.384	1	4	0	4	0
19.2	2	4	0	4	0
20.48	3	4	0	4	0
24.576	4	5	1	5	1
26	5	5	1	5	1
36	6	5	1	5	1
38.4	7	5	1	5	1

NOTES
Contact Analog Devices when another clock reference is desired.

PLL SETTING

ADMTV102 supports a set of eight crystal frequencies. If you want to use other clock frequency, you have to calculate the PLLN <9:0>, PLLF<19:0> register value manually. Below is the example.

Table 16. PLLS Register Value Selection

DIVSEL (PLLS)	VCOSEL 0		VCOSEL 1		Unit
	N2 > LO Freq. ≤ N3		N3 > LO Freq. ≤ N1		
0 (16)	N2/16	N3/16	N3/16	N1/16	MHz
1 (8)	N2/8	N3/8	N3/8	N1/8	MHz
2 (4)	N2/4	N3/4	N3/4	N1/4	MHz
3 (2)	N2/2	N3/2	N3/2	N1/2	MHz
4 (1)	N2/1 (PLLS)	N3/1	N3/1	N1/1	MHz

53	81	81	117
117	162	162	235
235	324	324	470
470	648	648	940
940	1296	1296	1880

DIVSEL: Register read value

VCOSEL: Register read value

VCO High Boundary N1 = 1880 MHz

Low Boundary N2 = 940 MHz

Mid Boundary N3 = 1296 MHz

PLLR = 0×1 (Default Value)

EXAMPLE)

1. LO Frequency = 666 MHz, Clock Frequency = 16.384 MHz

   PLLS = 2

2. Formula:

   LO Frequency = {(Clock frequency ÷ PLLR) × [PLLN + (PLLF ÷ 2^{20})]} ÷ PLLS

3. PLLN, PLLF value

   40.64941406 = PLLN + (PLLF ÷ 2^{20})

   (Integer) PLLN = 81 → (Hex) PLLN = 51

   (Floating) PLLF = 313344 → (Hex) PLLF = 4c800

TCXO INTERCONNECTION

In case of using a TCXO, interface pin of ADMTV102 is XTALI with DC block capacitor of 10 nF.

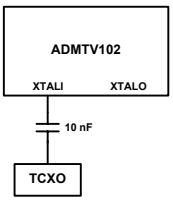

Figure 35. TCXO Application

TSPD CONTROL SIGNAL INVERTING

ADMTV102 TSPD control signal polarity can be inverted on the demand of user. To do this, you should change the following register values. Refer to the recommended programming guide for operation.

1. Normal TSPD: Low level is active, high level is inactive.

   → TSPDOSC<0> (address = 0×44) = 0×1

   → TSPDPOL<0> (address = 0×55) = 0×0

2. Inverting TSPD: Low level is inactive, high level is active

   → TSPDOSC<0> (address = 0×44) = 0×0

   → TSPDPOL<0> (address = 0×55) = 0×1

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THREE POWER DOWN MODES

ADMTV102 has three power down modes, which are hardware power down (PD pin), time-slicing power down (TSPD pin), and software power down (register setting).

Recovery time from power down depends on the PLL lock time and the demodulator's AGC response.

1. If PD pin is high, then all blocks including crystal oscillator are powered down.
2. If TSPD pin is high and TSPDxxx block register is high, then xxxBlock is powered down.
3. If SWPDxxx block register is high, then xxxBlock is powered down.
4. Power down and on timing.
   In case of hardware PD and TSPD, all blocks including the crystal oscillator block are powered down. So, all digital parameters are stored as just before powered down. After powered on by PD or TSPD pin, the tuner does not need to operate the VCO searching loop and the automatic gain control. So the power-on delay time is about 250 µs. However, after the SWPD ON the tuner needs to operate the VCO searching loop and automatic gain control because the digital block is alive during the SWPD. So the software power on delay time of around 12 ms is relatively longer than PD or TSPD. See figure 20 ~ 22.

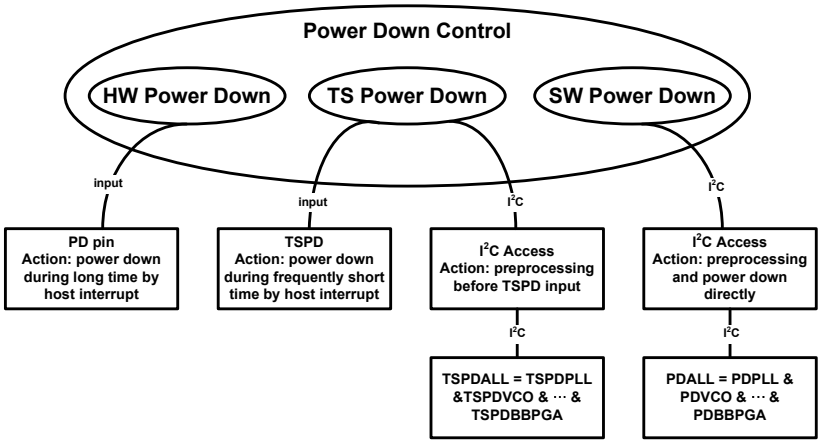

Figure 36. Three Power Down Modes

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EVALUATION BOARD

EVALUATION BOARD BILL OF MATERIALS (BOM)

Table 17. BOM List

Qty	Reference Designator	Name	Description	Manufacturer	Part Number
12	C3, C7, C10, C11, C17, C18, 22, C29, C33, C35, C44, C45	Capacitors	Capacitor, MLCC, 100 pF, 50 V, 1005, SMD	Murata	GRM1551X1H100J
6	C2, C6, C8, C15, C16, C28	Capacitors	Capacitor, MLCC, 10 nF, 50 V, 1005, SMD	Murata	GRM1551X1H103J
3	C25, C26, C4	Capacitors	Capacitor, MLCC, 15 pF, 50 V, 1005, SMD	Murata	GRM1551X1H150J
2	C1, C48	Capacitors	Capacitor, MLCC, 1 nF, 50 V, 1005, SMD	Murata	GRM1551X1H102J
1	C5	Capacitor	Capacitor, MLCC, 22 nF, 50 V, 1005, SMD	Murata	GRM1551X1H223J
2	C30, C31	Capacitors	Capacitor, MLCC, 33 nF, 50 V, 1005, SMD	Murata	GRM1551X1H333J
1	C19	Capacitor	Capacitor, MLCC, 470 nF, 50 V, 1005, SMD	Murata	GRM1551X1H474J
2	L5, L6	Inductors	Inductor, 100 nH, 1005, SMD	Toko	LL1005-FH101NJ
1	L2	Inductor	Inductor, 6.8 nH, 1005, SMD	Toko	LL1005-FH6R8NJ
1	L1	Inductor	Inductor, 23 nH, 1005, SMD	Toko	LL1005-FH230NJ
1	L4	Inductor	Inductor, 39 nH, 1005, SMD	Toko	LL1005-FH390NJ
1	L7	Inductor	Inductor, 56 nH, 1005, SMD	Toko	LL1005-FH560NJ
6	L8, L9, L10, L11, L12, L15	Inductors	NC		
1	VHF_Filter1	BPF	BPF	Murata	LFB32205MSK1-948
1	U1	Tuner	5 × 5 mm, QFN-32 pin	Analog Devices	ADMTV102ACPZRL
2	R12, R13	Resistors	Resistor, 0 Ω, 5%, 1005, SMD	ROHM	MCR01MZPJ0R0
1	R18	Resistor	Resistor, 510 Ω, 5%, 1005, SMD	ROHM	MCR01MZPJ511
1	R6	Resistor	Resistor, 4.7 kΩ, 5%, 1005, SMD	ROHM	MCR01MZPJ472
1	R15	Resistor	Resistor, 8.2 k Ω, 1%, 1005, SMD	ROHM	MCR01MZPF8201
1	U4	BPF	GSM Rejection BPF	Murata	SAEEB897MBA0B00
2	S3, S4	SMAs	RF 50 Ω	Telcon	
1	Y1	Crystal	16.384 MHz, load cap 15 pF Tolerance 30 ppm	QMAX Electronics	QX10M351B16.384

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EVALUATION BOARD SCHEMATICS

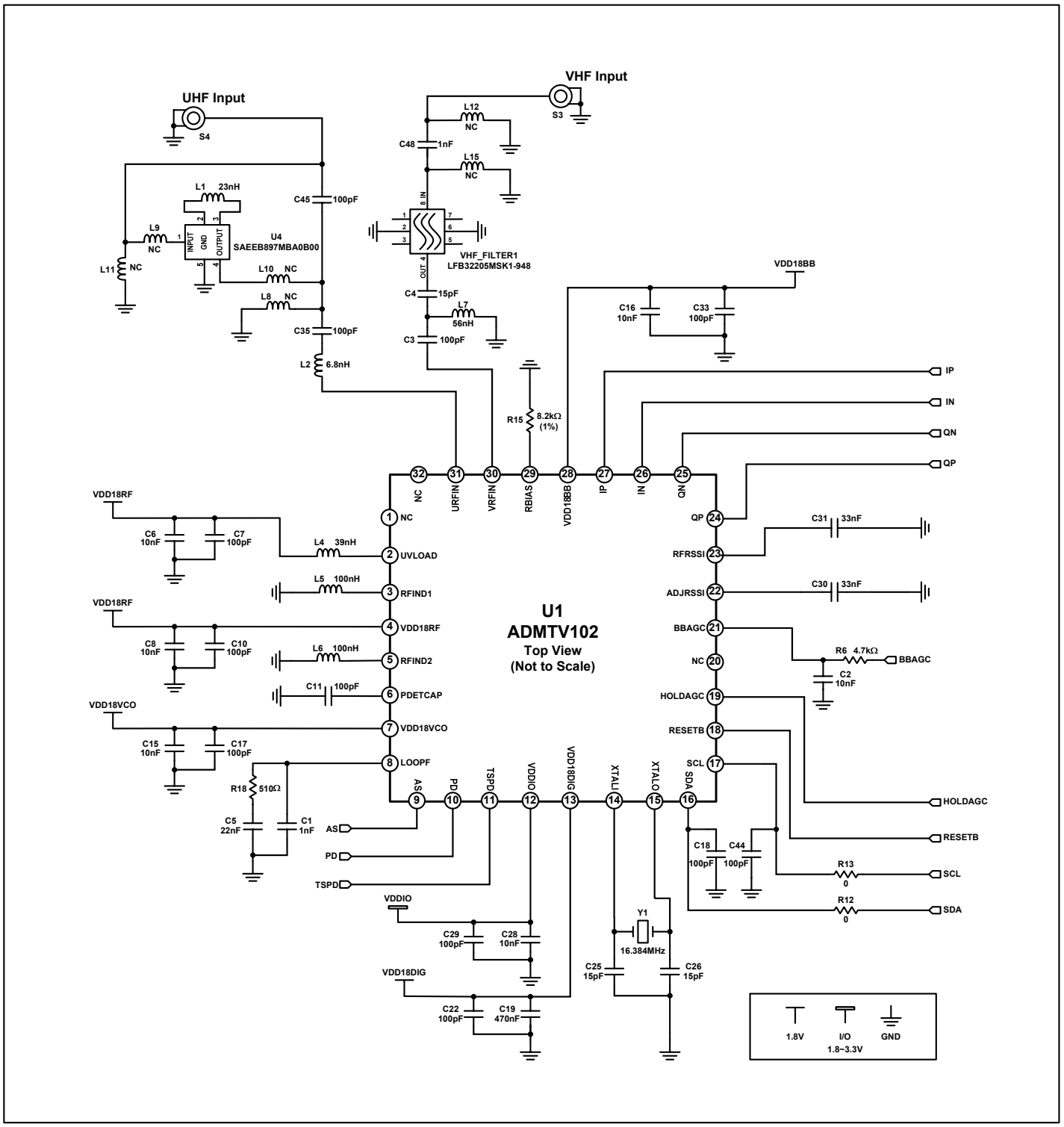

Figure 37. Evaluation Board Schematic

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PCB LAYERS

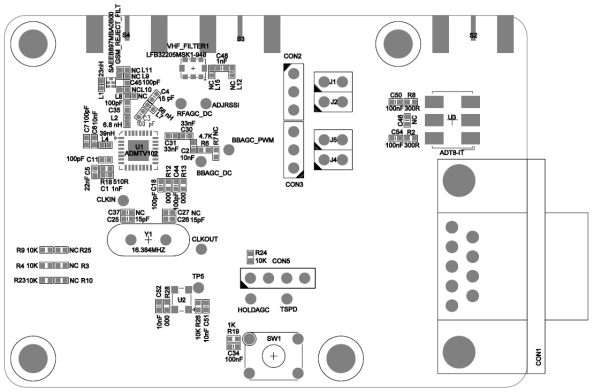

Figure 38. Evaluation Board Silkscreen Top View

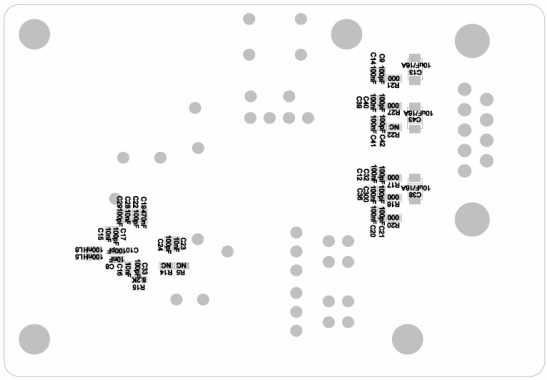

Figure 39. Evaluation Board Silkscreen Bottom View

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THERMAL CONSIDERATIONS

The ADMTV102 QFN has an integrated heat slug which improves the thermal and electrical properties of the package when locally attached to a ground planes at the PCB. A thermal (filled) via array to a ground beneath the part provides a path for heat to escape the package, lowering junction temperature. Improved electrical performance also results from the reduction in parasitic element of the package due to proximity of the ground plane. Recommended array is 0.3 mm via with 1.0 mm pitch. θ_{JA} = 27.46°C/W with this recommended configuration. Soldering the slug to the PCB is a requirement for this package.

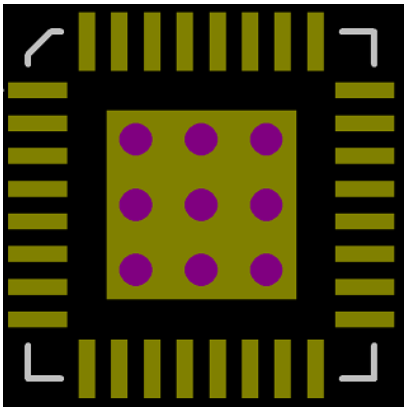

Figure 40. ADMTV102 QFN Recommended PCB Landing Pattern.

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OUTLINE DIMENSIONS

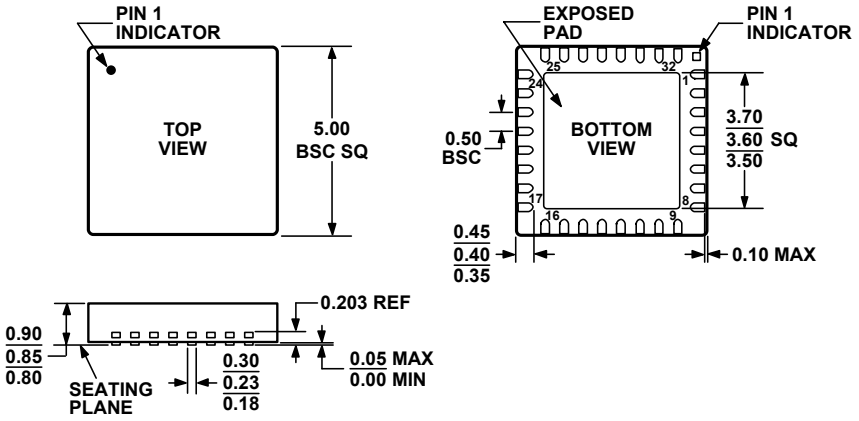

Figure 41. 32-Lead QFN Package

5 mm × 5 mm Body

(CP-32)

Dimensions shown in millimeters

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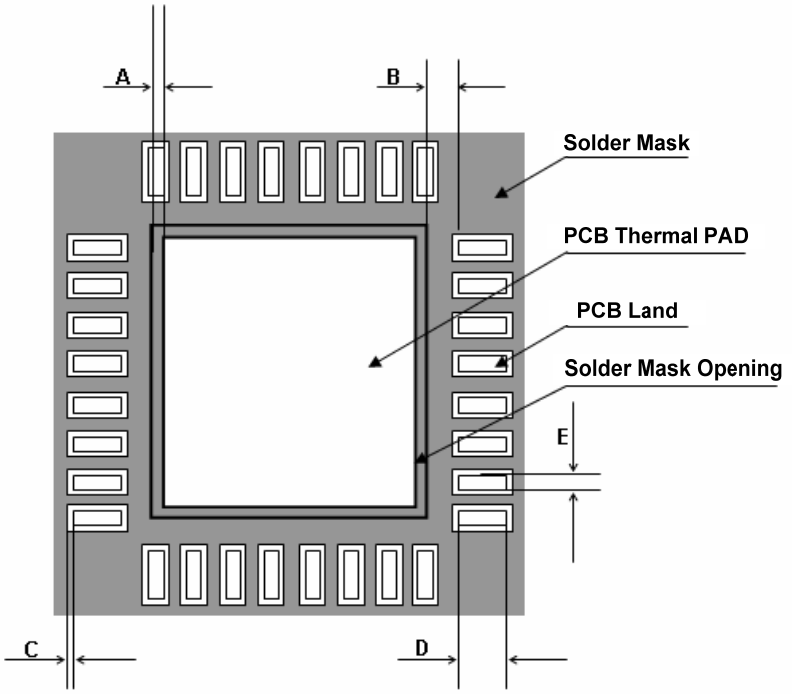
RECOMMENDED PCB LAND PATTERN

Table 18. Recommended PCB Land Pattern

Reference	Min	Typ	Max
A	0.0635		
B	0.2		
C	As tight as possible		
D	Solder pad length (L) + 0.1		
E	Solder pad width (b) + 0.1		
N	32		

Unit: mm



NOTES
A= Clearance from PCB thermal pad to solder mask opening.
B= Clearance from solder mask opening to PCB land edge
C= Clearance from PCB land edge to solder mask opening.
D= PCB land length
E= PCB land width
N= Total number of solder pads.
The exposed pad must be connected to the ground through the via holes and the via holes must be as many as possible

Figure 42. Recommended PCB LAND Pattern

ORDERING GUIDE

Model	Band	Temperature Range	Package Description	Package Option
ADMTV102ACPZRL	UHF	−40°C to + 85°C	32-Lead QFN	CP-32
ADMTV102BCPZRL	UHF/VHF	−40°C to + 85°C	32-Lead QFN	CP-32
ADMTV102-EB			Evaluation Board	

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NOTES

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