0.1 GHz to 20 GHz, GaAs, Nonreflective, SP4T Switch

Enhanced Product

HMC641ATCPZ-EP

FEATURES

- Broadband frequency range: 0.1 GHz to 20 GHz
- Nonreflective 50 Ω design
- Low insertion loss: 3.0 dB up 20 GHz
- High isolation: 40 dB up 20 GHz
- High input linearity at 250 MHz to 20 GHz
  - P1dB: 24 dBm typical, V_{SS} = −5 V
  - IP3: 41 dBm typical
- High power handling, V_{SS} = −5 V
  - 26.5 dBm through path
  - 23 dBm terminated path
- Integrated 2 to 4 line decoder
- 24-lead, 4 mm × 4 mm LFCSP
- ESD sensitivity, HBM: 250 V (Class 1A)

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range: −55°C to +125°C
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- Test instrumentation
- Microwave radios and very small aperture terminals (VSATs)
- Military radios, radars, and electronic counter measures (ECMs)
- Broadband telecommunications systems

FUNCTIONAL BLOCK DIAGRAM

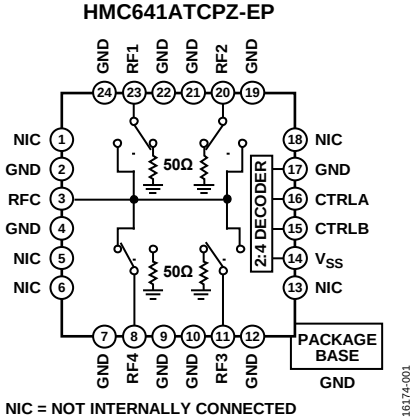

Figure 1.

GENERAL DESCRIPTION

The HMC641ATCPZ-EP is a general-purpose, nonreflective, single-pole, four-throw (SP4T) switch manufactured using a gallium arsenide (GaAs) process. This switch offers high isolation, low insertion loss, and on-chip termination of the isolated ports.

The switch operates with a negative supply voltage range of −5 V to −3 V and requires two negative logic control voltages.

The HMC641ATCPZ includes an on-chip, binary 2 to 4 line decoder that provides logic control from two logic input lines.

The HMC641ATCPZ comes in a 24-lead, 4 mm × 4 mm LFCSP and operates from 0.1 GHz to 20 GHz.

Additional application and technical information can be found in the HMC641ALP4E data sheet.

Rev. A

Document Feedback

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REVISION HISTORY

11/2017—Rev. 0 to Rev. A

Changes to Reflow (MSL3 Rating) Parameter, Table 2 4
Changes to Ordering Guide 8

8/2017—Revision 0: Initial Version

SPECIFICATIONS

V_{SS} = −3 V or −5 V, control voltage (V_{CTRL}) = 0 V or V_{SS}, case temperature (T_{CASE}) = 25°C, and 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.1		20	GHz
INSERTION LOSS						
Between RFC and RF1 to RF4 (On)		0.1 GHz to 12 GHz		2.0		dB
		12 GHz to 20 GHz		3.0		dB
ISOLATION						
Between RFC and RF1 to RF4 (Off)		0.1 GHz to 12 GHz	30	42		dB
		12 GHz to 20 GHz	30	40		dB
RETURN LOSS						
RFC and RF1 to RF4 (On)		0.1 GHz to 12 GHz		18		dB
		12 GHz to 20 GHz		17		dB
RF1 to RF4 (Off)		0.1 GHz to 20 GHz		13		dB
SWITCHING						
Rise Time and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of radio frequency (RF) output		30		ns
On Time and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF output		100		ns
INPUT LINEARITY[1]		250 MHz to 20 GHz				
1 dB Power Compression	P1dB	V_{SS} = −5 V	20	24		dBm
		V_{SS} = −3 V		22		dBm
Third-Order Intercept	IP3	10 dBm per tone, 1 MHz spacing				
		V_{SS} = −5 V		41		dBm
		V_{SS} = −3 V		41		dBm
SUPPLY		V_{SS} pin				
Voltage	V_{SS}		−5		−3	V
Current	I_{SS}			1.7	5	mA
DIGITAL CONTROL INPUTS		CTRLA and CTRLB pins				
Voltage	V_{CTRL}					
Low	V_{INL}	V_{SS} = −5 V	−3		0	V
		V_{SS} = −3 V	−1		0	V
High	V_{INH}	V_{SS} = −5 V	−5		−4.2	V
		V_{SS} = −3 V	−3		−2.2	V
Current	I_{CTRL}					
Low	I_{INL}			30		µA
High	I_{INH}			0.5		µA

[1] Input linearity performance degrades at frequencies less than 250 MHz.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 2.

Parameter	Rating
Negative Supply Voltage (V_{SS})	−7 V
Digital Control Input Voltage	V_{SS} − 0.5 V to + 1 V
RF Input Power[1] (f = 250 MHz to 20 GHz, T_{CASE} = 85°C)	
V_{SS} = −5 V	
Through Path	26.5 dBm
Terminated Path	23 dBm
Hot Switching	20 dBm
V_{SS} = −3 V	
Through Path	21 dBm
Terminated Path	20 dBm
Hot Switching	17 dBm
Temperature	
Junction, T_J	150°C
Case, T_{CASE}	−55°C to +125°C
Storage	−65°C to +150°C
Reflow (MSL3 Rating)[2]	260°C
Junction to Case Thermal Resistance, θ_{JC}	
Through Path	201°C/W
Terminated Path	321°C/W
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	250 V (Class 1A)

[1] For power derating at frequencies less than 250 MHz, see Figure 2, and for the maximum input power vs. the case temperature, see Figure 3.
[2] See the Ordering Guide section.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

POWER DERATING CURVES

Figure 2 shows power derating vs. frequency at <250 MHz, and Figure 3 shows the maximum power dissipation vs. the case temperature.

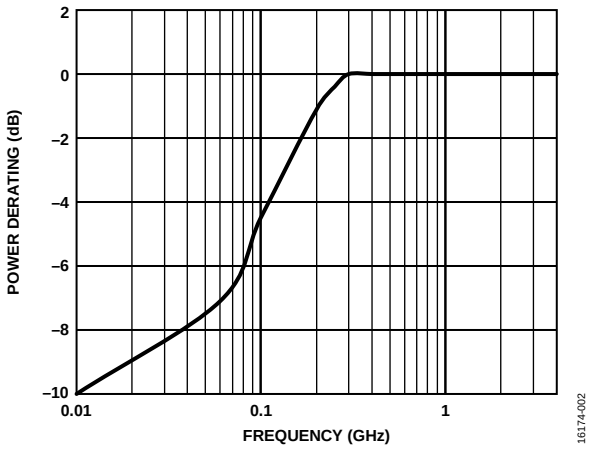


Figure 2. Power Derating at Frequencies Less than 250 MHz

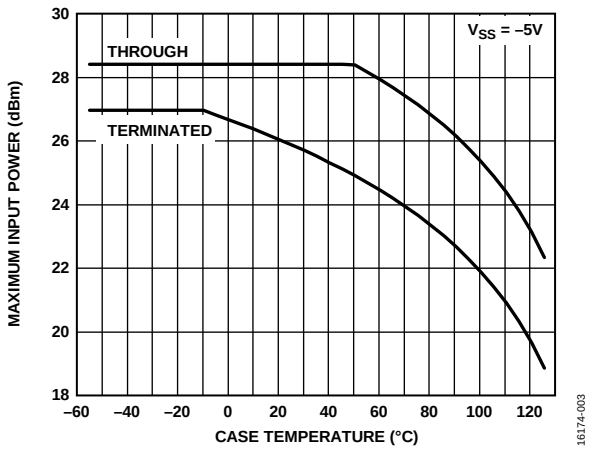
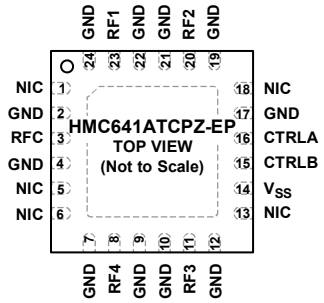


Figure 3. Maximum Input Power vs. Case Temperature (T_{CASE})

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NOT INTERNALLY CONNECTED. THE PINS ARE NOT CONNECTED INTERNALLY; HOWEVER, ALL DATA SHOWN IN THIS DATA SHEET IS MEASURED WITH THESE PINS CONNECTED TO RF/DC GROUND EXTERNALLY.
2. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO THE RF/DC GROUND OF THE PCB.

Figure 4. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 5, 6, 13, 18	NIC	Not Internally Connected. The pins are not connected internally; however, all data shown in this data sheet is measured with these pins connected to RF/dc ground externally.
2, 4, 7, 9, 10, 12, 17, 19, 21, 22, 24	GND	Ground. These pins must be connected to the RF/dc ground of the printed circuit board (PCB).
3	RFC	RF Common Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc. See Figure 5 for the interface schematic.
8	RF4	RF4 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc. See Figure 5 for the interface schematic.
11	RF3	RF3 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc. See Figure 5 for the interface schematic.
14	V_{SS}	Negative Supply Voltage Pin. See Figure 6 for the interface schematic.
15	CTRLB	Control Input 2 Pin. See Table 4 for the control voltage truth table. See Figure 6 for the interface schematic.
16	CTRLA	Control Input 1 Pin. See Table 4 for the control voltage truth table. See Figure 6 for the interface schematic.
20	RF2	RF2 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc. See Figure 5 for the interface schematic.
23	RF1	RF1 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc. See Figure 5 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/dc ground of the PCB.

INTERFACE SCHEMATICS

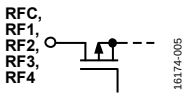


Figure 5. RFC to RF4 Interface Schematic

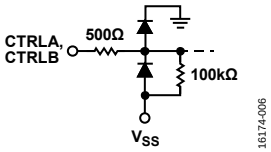


Figure 6. CTRLA, CTRLB, and V_{SS} Interface Schematic

TRUTH TABLE

Table 4. Control Voltage Truth Table

Digital Control Input		RF Paths			
CTRLA	**CTRLB**	**RFC to RF1**	**RFC to RF2**	**RFC to RF3**	**RFC to RF4**
High	High	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
Low	High	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
High	Low	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
Low	Low	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)

TYPICAL PERFORMANCE CHARCTERISTICS

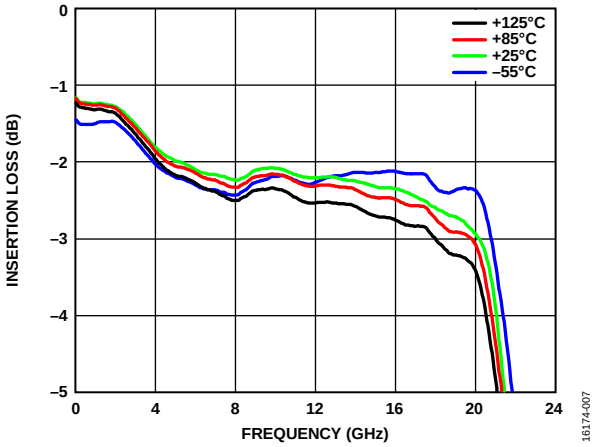
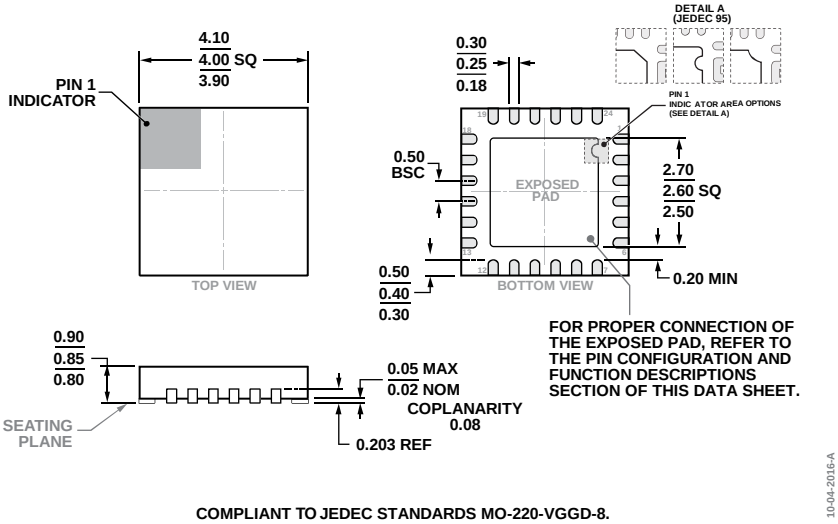


Figure 7. Insertion Loss Between RFC and RF1 vs. Frequency for Various Temperatures

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-8.

Figure 8. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.85 mm Package Height
(CP-24-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option
HMC641ATCPZ-EP-PT	−55°C to +125°C	MSL3	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-22
HMC641ATCPZ-EP-RL7	−55°C to +125°C	MSL3	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-22

[1] Z = RoHS Compliant Part.
[2] See the Absolute Maximum Ratings section.