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AD9837 FMC-SDP Interposer & Evaluation Board / Xilinx KC705 Reference Design

Supported Devices

- AD9837

Evaluation Boards

- EVAL-AD9837SDZ

Overview

This document presents the steps to setup an environment for using the **EVAL-AD9837SDZ** evaluation board together with the Xilinx KC705 FPGA board and the Xilinx Embedded Development Kit (EDK). Below is presented a picture of the EVAL-AD9837SDZ Evaluation Board with the Xilinx KC705 board.

For component evaluation and performance purposes, as opposed to quick prototyping, the user is directed to use the part evaluation setup. This consists of:

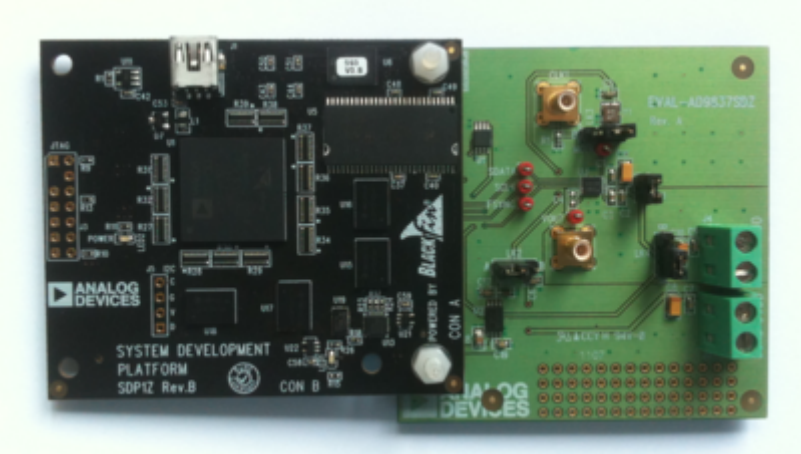
- 1. A controller board like the SDP-B (EVAL-SDP-CS1Z)
- 2. The component SDP compatible product evaluation board
- 3. Corresponding PC software (shipped with the product evaluation board)

The SDP-B controller board is part of Analog Devices System Demonstration Platform (SDP). It provides a high speed USB 2.0 connection from the PC to the component evaluation board. The PC runs the evaluation software. Each evaluation board, which is an SDP compatible daughter board, includes the necessary installation file required for performance testing.

Note: it is expected that the analog performance on the two platforms may differ.

28 Sep 2012 09:32 · Adrian Costina

Below is presented a picture of **SDP-B** Controller Board with the **EVAL-AD9837SDZ** Evaluation Board.



The **EVAL-AD9837SDZ** evaluation board is designed to help customers quickly prototype new AD9837 circuits and reduce design time. A high performance, on-board 16 MHz trimmed general oscillator is available to use as the master clock for the AD9837 system. Various links and SMB connectors are also available on the EVAL-AD9837SDZ board to maximize usability.

The AD9837 is a 16 MHz low power DDS device capable of producing high performance sine and triangular outputs. It also has an on-board comparator that allows a square wave to be produced for clock generation. Consuming only 20 mW of power at 3 V makes the AD9837 an ideal candidate for power-sensitive applications.

More information

- AD9837 Product Info - pricing, samples, datasheet
- EVAL-AD9837SDZ evaluation board user guide
- Xilinx KC705 FPGA board

Getting Started

The first objective is to ensure that you have all of the items needed and to install the software tools so that you are ready to create and run the evaluation project.

Required Hardware

- Xilinx KC705 FPGA board
- FMC-SDP adapter board
- **EVAL-AD9837** evaluation board

Required Software

- Xilinx ISE 14.6.
- UART Terminal (Termite/Tera Term/Hyperterminal), baud rate 115200.
- The EVAL-AD9837 reference project for Xilinx KC705 FPGA.

Downloads

- **AD9837 Driver:** https://github.com/analogdevicesinc/no-OS/tree/master/device_drivers/AD9833
- **AD9837 Commands:** https://github.com/analogdevicesinc/no-OS/tree/master/device_commands/AD9833
- **Xilinx Boards Common Drivers:** https://github.com/analogdevicesinc/no-OS/tree/master/platform_drivers/Xilinx/SDP_Common
- **EDK KC705 Reference project:** https://github.com/analogdevicesinc/fpgahdl_xilinx/tree/master/cf_sdp_kc705

Run the Demonstration Project

Hardware setup

Before connecting the ADI evaluation board to the Xilinx KC705 make sure that the VADJ_FPGA voltage of the KC705 is set to 3.3V. For more details on how to change the setting for VADJ_FPGA visit the Xilinx KC705 product page.

- Use the FMC-SDP interposer to connect the ADI evaluation board to the Xilinx KC705 board on the FMC LPC connector.
- Connect the JTAG and UART cables to the KC705 and power up the FPGA board.

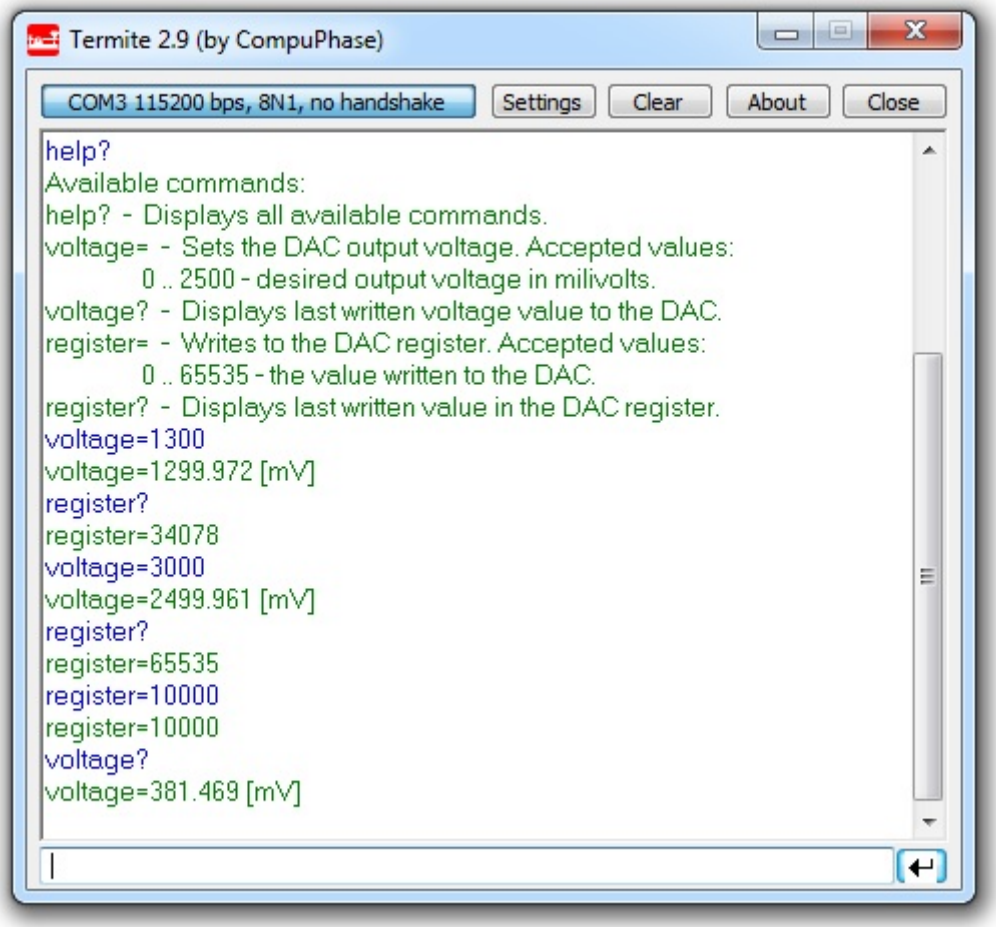
Reference Project Overview

The following commands were implemented in this version of EVAL-AD9837 reference project for Xilinx KC705 FPGA board.

Command	Description
help?	Displays all available commands.
output=	Selects the type of output. Accepted values: 0 - Sinusoid.(default) 1 - Triangle. 2 - DAC Data MSB/2. 3 - DAC Data MSB.
output?	Displays the type of output.
loadFreqReg=	Loads a frequency value in one selected register. Accepted values: Register number: 0 - Frequency Register 0. 1 - Frequency Register 1. Value: 0 .. 8 000 000 - the frequency value in Hz.
freqRegVal?	Displays the value from one selected frequency register. Accepted values: Register number: 0 - Frequency Register 0. 1 - Frequency Register 1.
loadPhaseReg=	Loads a phase value in one selected register. Accepted values: Register number: 0 - Phase Register 0. 1 - Phase Register 1. Value: 0 .. 2PI - the phase value in radians.
phaseRegVal?	Displays the value from one selected phase register. Accepted values: Register number: 0 - Phase Register 0. 1 - Phase Register 1.
freqRegNo=	Select the frequency register to be used. Accepted values: Register number: 0 - Frequency Register 0. 1 - Frequency Register 1.
freqRegNo?	Displays the selected frequency register.
phaseRegNo=	Select the phase register to be used. Accepted values: Register number: 0 - Phase Register 0. 1 - Phase Register 1.
phaseRegNo?	Displays the selected phase register.
sleepMode=	Select one sleep mode. Accepted values: Sleep mode: 0 - No power-down.(default) 1 - DAC powered down. 2 - Internal clock disabled. 3 - DAC powered down and Internal clock disabled.
sleepMode?	Displays the selected sleep mode.

Commands can be executed using a serial terminal connected to the UART peripheral of Xilinx KC705 FPGA.

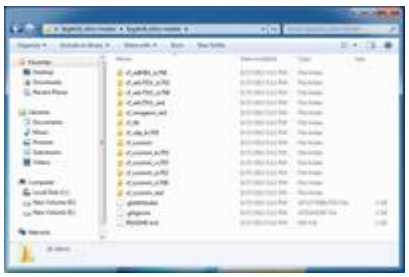
The following image shows a generic list of commands in a serial terminal connected to Xilinx KC705 FPGA's UART peripheral.



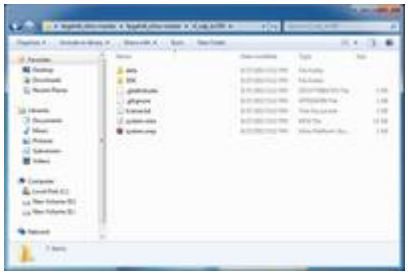
Software Project Setup

The hardware platform for each reference projects with FMC-SDP interposer and KC705 evaluation board is common. The next steps should be followed to recreate the software project of the reference design:

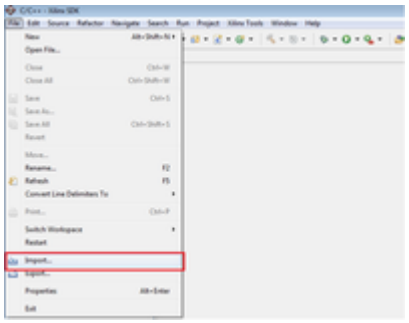
- First download the **KC705 Reference project** from Github on your computer. You can do this by clonning this repository: https://github.com/analogdevicesinc/fpgahdl_xilinx.



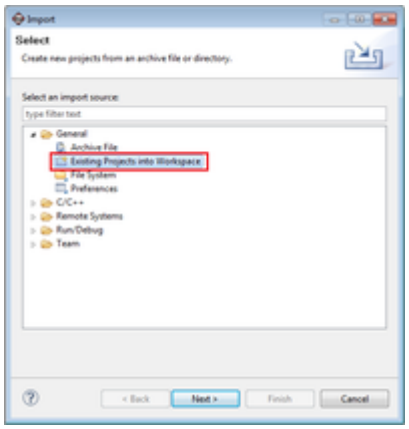
- From this entire repository you will use **cf_sdp_kc705** folder. This is common for all KC705 projects.



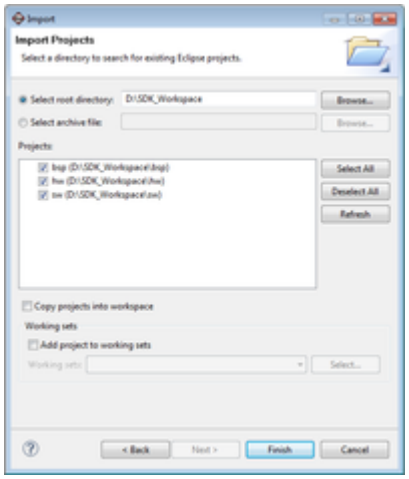
- Open the Xilinx SDK. When the SDK starts, it asks you to provide a folder where to store the workspace. Any folder can be provided. Make sure that the path where it is located does not contain any spaces.
- In the SDK select the ***File→Import*** menu option to import the software projects into the workspace.



- In the *Import* window select the ***General→Existing Projects into Workspace*** option.

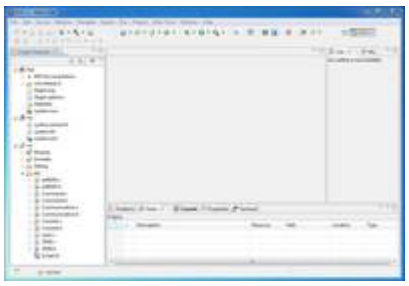


- In the *Import Projects* window select the **cf_sdp_kc705** folder as root directory and check the **Copy projects into workspace** option. After the root directory is chosen the projects that reside in that directory will appear in the *Projects* list. Press *Finish* to finalize the import process.

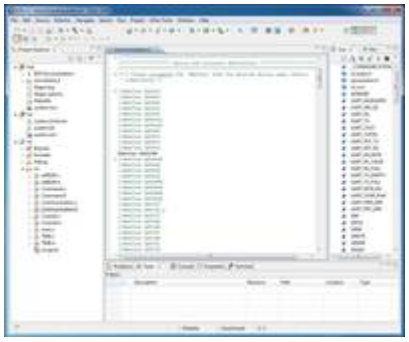


- The *Project Explorer* window now shows the projects that exist in the workspace without software files.

- Now the software must be added in your project. For downloading the software, you must use 3 links from Github given in **Downloads** section. From there you'll download the specific driver, the specific commands and the Xilinx Boards Common Drivers(which are commons for all Xilinx boards). All the software files downloaded must be copied in **src** folder from sw folder.



- Before compilation in the file called **Communication.h** you have to uncomment the name of the device that you currently use. In the picture below there is an example of this, which works only with AD5629R project. For another device, uncomment only the respective name. You can have one driver working on multiple devices, so the drivers's name and the uncommented name may not be the same for every project.



- The SDK should automatically build the project and the *Console* window will display the result of the build. If the build is not done automatically, select the ***Project→Build Automatically*** menu option.
- If the project was built without any errors, you can program the FPGA and run the software application.

13 Aug 2013 08:22 · Lucian Sin

More information

- AD9837 IIO Direct Digital Synthesis Linux Driver

- ask questions about the FPGA reference design
- Example questions:
  - FMCDAQ2+KCU105 DHCP issues by ic70
  - What's the width and deepth of the FIFO in Fmcomms2 adc_dmac? by l312361206
  - Have you any JESD204B reference design that has not microblaze and MIG7 Axi_ddr_cntrl? by saban
  - FMCOMMS3 and ethernet data extraction by Cman
  - FMCOMMS1 AD9548 clock derivation explanation by cherif.chibane@ll.mit.edu

28 May 2012 14:18