

Am29F800B

Known Good Die

Data Sheet



July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number **21631** Revision **C** Amendment **+3** Issue Date **July 27, 2007**



Am29F800B Known Good Die

8 Megabit (1 M x 8-Bit/512 K x 16-Bit)

CMOS 5.0 Volt-only, Boot Sector Flash Memory—Die Revision 2

DISTINCTIVE CHARACTERISTICS

- **Single power supply operation**
 - 5.0 Volt-only operation for read, erase, and program operations
 - Minimizes system level requirements
- **Manufactured on 0.32 μm process technology**
 - Compatible with 0.5 μm Am29F800 device
- **High performance**
 - 90 or 120 ns access time
- **Low power consumption (typical values at 5 MHz)**
 - 1 μA standby mode current
 - 20 mA read current (byte mode)
 - 28 mA read current (word mode)
 - 30 mA program/erase current
- **Flexible sector architecture**
 - One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and fifteen 64 Kbyte sectors (byte mode)
 - One 8 Kword, two 4 Kword, one 16 Kword, and fifteen 32 Kword sectors (word mode)
 - Supports full chip erase
 - Sector Protection features:
 - A hardware method of locking a sector to prevent any program or erase operations within that sector
 - Sectors can be locked via programming equipment
 - Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
 - Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
 - Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Minimum 1,000,000 write cycles per sector guaranteed**
- **Compatibility with JEDEC standards**
 - Pinout and software compatible with single-power-supply Flash
 - Superior inadvertent write protection
- **Data# Polling and toggle bits**
 - Provides a software method of detecting program or erase operation completion
- **Ready/Busy# pin (RY/BY#)**
 - Provides a hardware method of detecting program or erase cycle completion
- **Erase Suspend/Erase Resume**
 - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset pin (RESET#)**
 - Hardware method to reset the device to reading array data
- **20-year data retention at 125°C**
- **Tested to datasheet specifications at temperature**
- **Quality and reliability levels equivalent to standard packaged components**

GENERAL DESCRIPTION

The Am29F800B in Known Good Die (KGD) form is a 8 Mbit, 5.0 volt-only Flash memory. AMD defines KGD as standard product in die form, tested for functionality and speed. AMD KGD products have the same reliability and quality as AMD products in packaged form.

Am29F800B Features

The Am29F800B is an 8 Mbit, 5.0 volt-only Flash memory organized as 1,048,576 bytes or 524,288 words. The word-wide data (x16) appears on DQ15–DQ0; the byte-wide (x8) data appears on DQ7–DQ0. This device is designed to be programmed in-system with the standard system 5.0 volt V_{CC} supply. A 12.0 V V_{PP} is not required for write or erase operations. The device can also be programmed in standard EPROM programmers.

This device is manufactured using AMD's 0.32 μm process technology, and offers all the features and benefits of the Am29F800, which was manufactured using 0.5 μm process technology.

To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 5.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically pre-

programs the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The system can place the device into the **standby mode**. Power consumption is greatly reduced in this mode.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

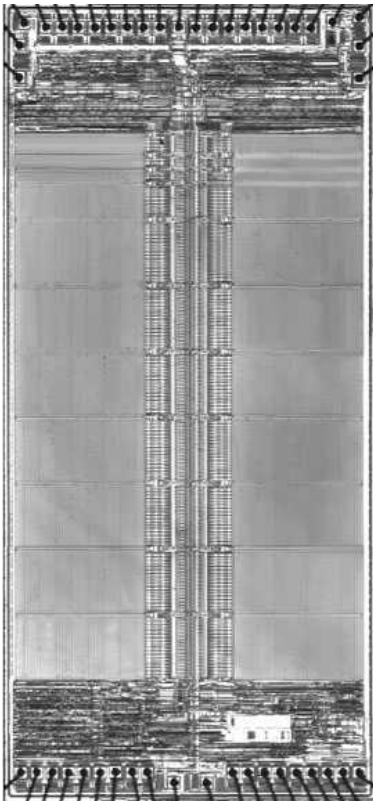
Electrical Specifications

Refer to the Am29F800B data sheet, PID 21504, for full electrical specifications on the Am29F800B in KGD form.

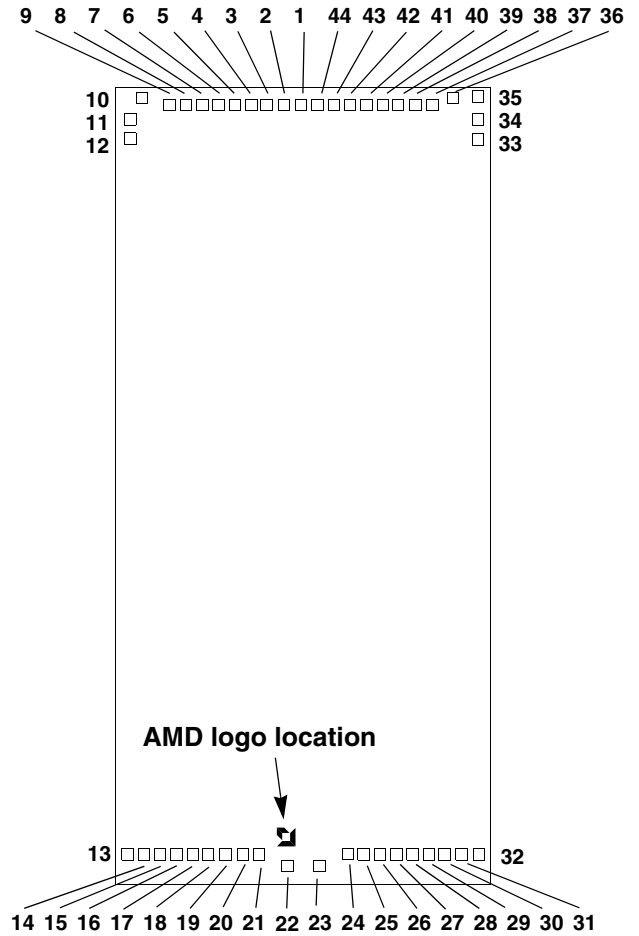
PRODUCT SELECTOR GUIDE

Family Part Number	Am29F800B KGD	
Speed Option ($V_{CC} = 5.0 V \pm 10\%$)	-90	-120
Max access time, ns (t_{ACC})	90	120
Max CE# access time, ns (t_{CE})	90	120
Max OE# access time, ns (t_{OE})	35	50

DIE PHOTOGRAPH



DIE PAD LOCATIONS



PAD DESCRIPTION

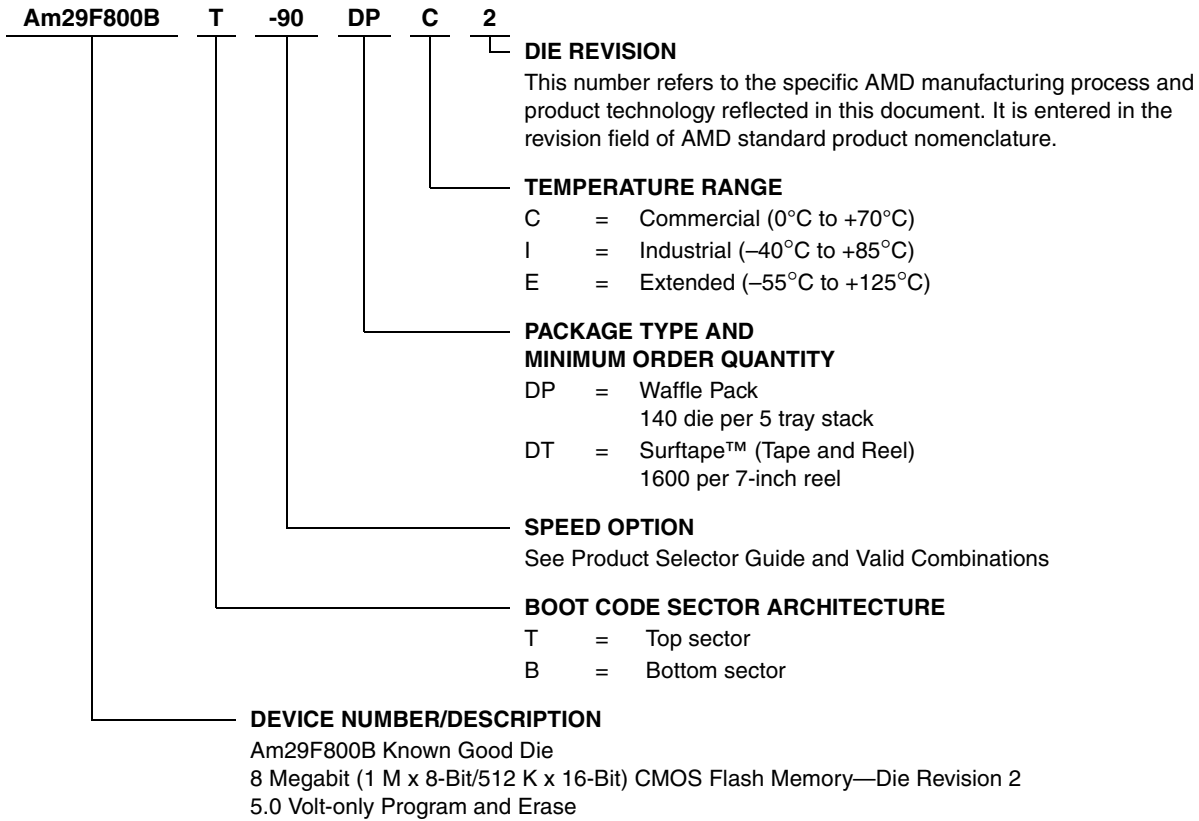
Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
1	V _{CC}	0.00	0.00	0.0000	0.0000
2	DQ4	-6.86	0.00	-0.1743	0.0000
3	DQ12	-12.78	0.00	-0.3246	0.0000
4	DQ5	-18.61	0.00	-0.4728	0.0000
5	DQ13	-24.53	0.00	-0.6231	0.0000
6	DQ6	-30.37	0.00	-0.7713	0.0000
7	DQ14	-36.28	0.00	-0.9216	0.0000
8	DQ7	-42.12	0.00	-1.0698	0.0000
9	DQ15/A-1	-48.03	0.00	-1.2201	0.0000
10	V _{SS}	-55.68	1.35	-1.4143	0.0343
11	BYTE#	-57.48	-6.50	-1.4599	-0.1651
12	A16	-57.48	-18.04	-1.4599	-0.4582
13	A15	-57.13	-265.89	-1.4510	-6.7536
14	A14	-51.29	-265.89	-1.3028	-6.7536
15	A13	-45.87	-265.89	-1.1651	-6.7536
16	A12	-40.03	-265.89	-1.0169	-6.7536
17	A11	-34.61	-265.89	-0.8791	-6.7536
18	A10	-28.78	-265.89	-0.7309	-6.7536
19	A9	-23.35	-265.64	-0.5932	-6.7473
20	A8	-17.43	-265.89	-0.4426	-6.7536
21	WE#	-12.00	-265.89	-0.3049	-6.7536
22	RESET#	-2.42	-269.66	-0.0614	-6.8493
23	RY/BY#	9.49	-269.66	0.2411	-6.8493
24	A18	19.06	-265.89	0.4841	-6.7536
25	A17	24.48	-265.89	0.6219	-6.7536
26	A7	30.32	-265.89	0.7701	-6.7536
27	A6	35.74	-265.89	0.9078	-6.7536
28	A5	41.58	-265.89	1.0560	-6.7536
29	A4	47.00	-265.89	1.1938	-6.7536
30	A3	52.83	-265.89	1.3420	-6.7536
31	A2	58.26	-265.89	1.4797	-6.7536
32	A1	64.09	-265.89	1.6279	-6.7536
33	A0	64.44	-18.04	1.6368	-0.4582
34	CE#	64.44	-6.50	1.6368	-0.1651
35	V _{SS}	64.44	3.80	1.6368	0.0964
36	OE#	54.95	2.27	1.3956	0.0578
37	DQ0	47.37	0.00	1.2031	0.0000
38	DQ8	41.45	0.00	1.0528	0.0000
39	DQ1	35.61	0.00	0.9046	0.0000
40	DQ9	29.70	0.00	0.7543	0.0000
41	DQ2	23.86	0.00	0.6061	0.0000
42	DQ10	17.95	0.00	0.4558	0.0000
43	DQ3	12.11	0.00	0.3076	0.0000
44	DQ11	6.19	0.00	0.1573	0.0000

Note: The coordinates above are relative to the center of pad 1 and can be used to operate wire bonding equipment.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



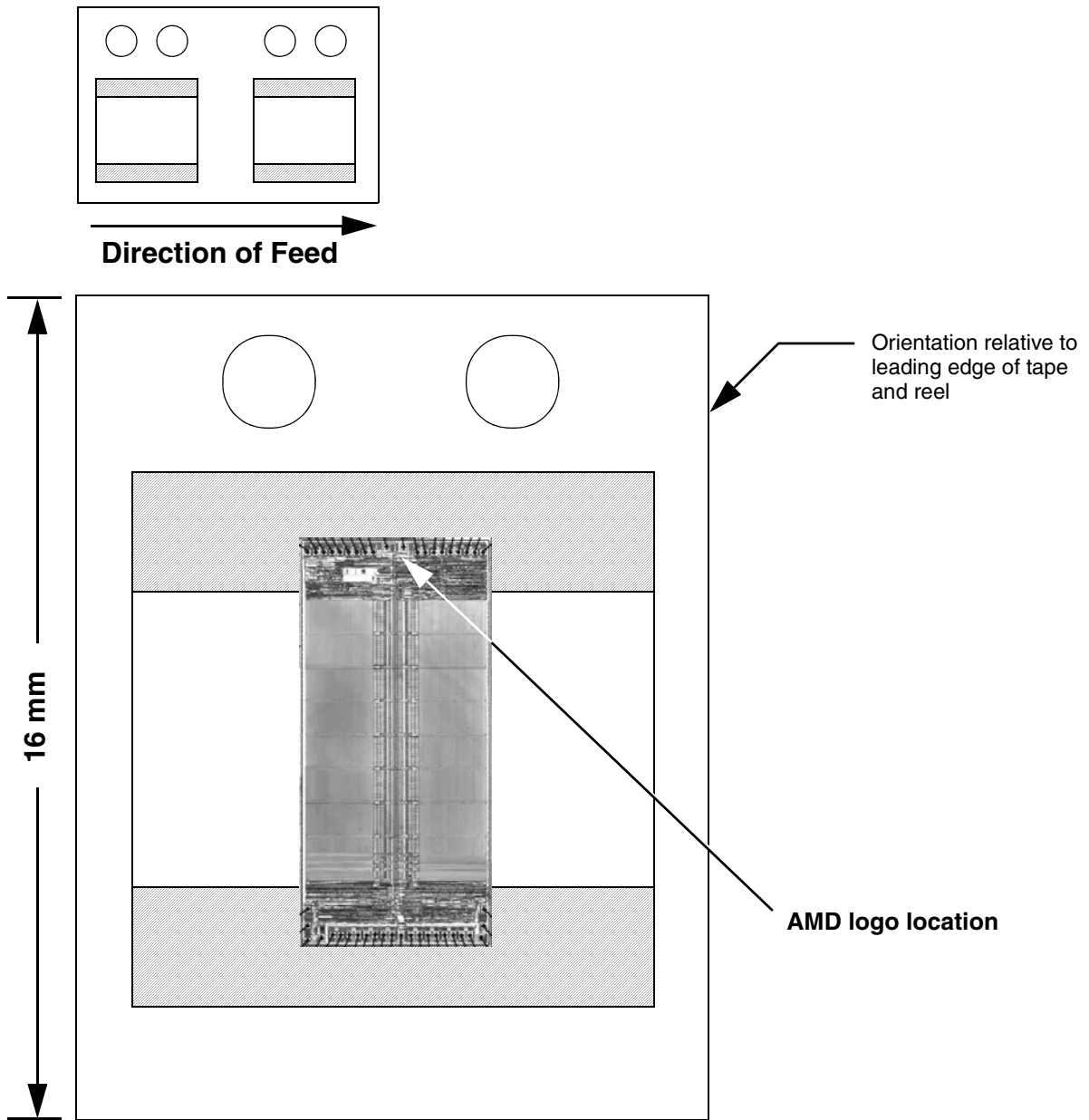
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

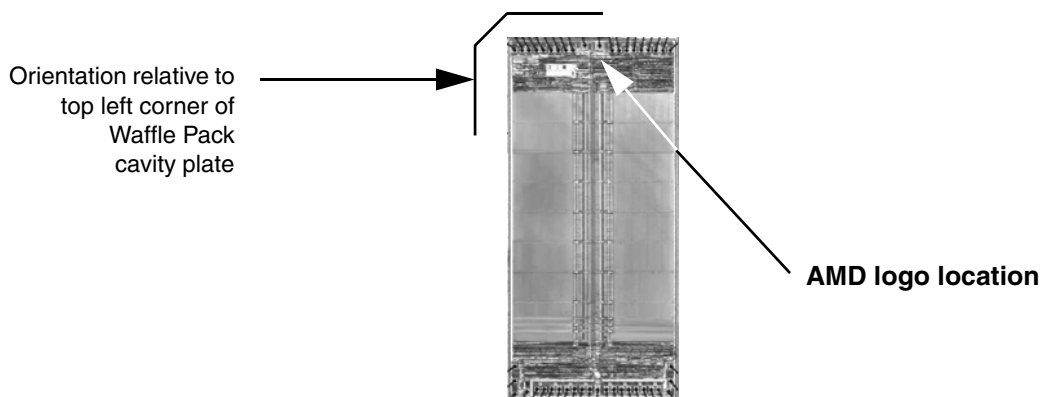
Valid Combinations	
AM29F800BT-90, AM29F800BB-90,	DPC 2, DPI 2, DPE 2, DTC 2, DTI 2, DTE 2,
AM29F800BT-120 AM29F800BB-120	

PACKAGING INFORMATION

Surftape Packaging



Waffle Pack Packaging



PRODUCT TEST FLOW

Figure 1 provides an overview of AMD's Known Good Die test flow. For more detailed information, refer to the Am29F800B product qualification database supplement for KGD. AMD implements quality assurance procedures throughout the product test flow. In addition,

an off-line quality monitoring program (QMP) further guarantees AMD quality standards are met on Known Good Die products. These QA procedures also allow AMD to produce KGD products without requiring or implementing burn-in.

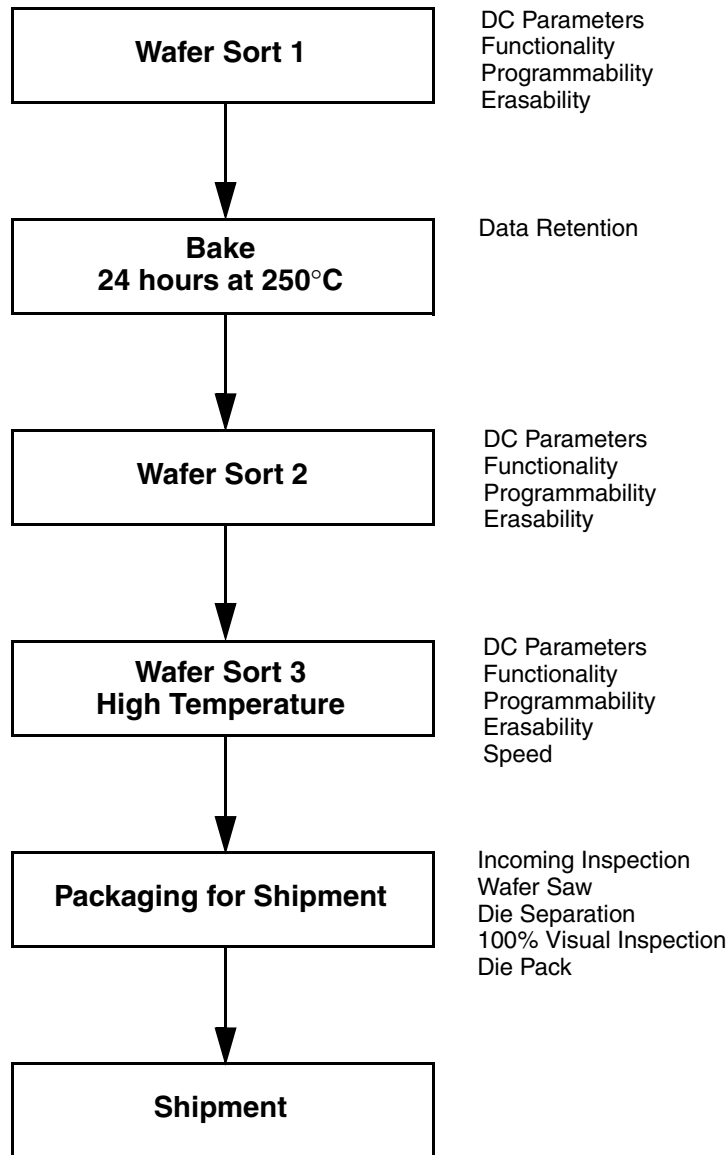


Figure 1. AMD KGD Product Test Flow

PHYSICAL SPECIFICATIONS

Die Dimensions	135 mils x 292 mils
	3.43 mm x 7.42 mm
Die Thickness	~19.7 mils
	~500 μm^2
Bond Pad Size	4.69 mils x 4.69 mils
	115.9 μm x 115.9 μm
Pad Area Free of Passivation	13.99 mils ²
	9025 μm^2
Pads Per Die	44
Bond Pad Metalization	Al/Cu
Die Backside	No metal, may be grounded (optional)
Passivation	Nitride/SOG/Nitride

DC OPERATING CONDITIONS

V_{CC} (Supply Voltage)	4.5 V to 5.5 V
Junction Temperature Under Bias .. T_J (max)	= 130°C
Operating Temperature	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Extended	-55°C to +125°C

MANUFACTURING INFORMATION

Manufacturing	FASL
Wafer Sort Test	Sunnyvale, CA, USA and Penang, Malaysia
Manufacturing ID (Top Boot)	98H05AK
(Bottom Boot)	98H05ABK
Preparation for Shipment	Penang, Malaysia
Fabrication Process	CS39S
Die Revision	2

SPECIAL HANDLING INSTRUCTIONS**Processing**

Do not expose KGD products to ultraviolet light or process them at temperatures greater than 250°C. Failure to adhere to these handling instructions will result in irreparable damage to the devices. For best yield, AMD recommends assembly in a Class 10K clean room with 30% to 60% relative humidity.

Storage

Store at a maximum temperature of 30°C in a nitrogen-purged cabinet or vacuum-sealed bag. Observe all standard ESD handling procedures.

TERMS AND CONDITIONS OF SALE FOR AMD NON-VOLATILE MEMORY DIE

All transactions relating to unpackaged die under this agreement shall be subject to AMD's standard terms and conditions of sale, or any revisions thereof, which revisions AMD reserves the right to make at any time and from time to time. In the event of conflict between the provisions of AMD's standard terms and conditions of sale and this agreement, the terms of this agreement shall be controlling.

AMD warrants unpackaged die of its manufacture ("Known Good Die" or "Die") against defective materials or workmanship for a period of one (1) year from date of shipment. This warranty does not extend beyond the first purchaser of said Die. Buyer assumes full responsibility to ensure compliance with the appropriate handling, assembly and processing of Known Good Die (including but not limited to proper Die preparation, Die attach, wire bonding and related assembly and test activities), and compliance with all guidelines set forth in AMD's specifications for Known Good Die, and AMD assumes no responsibility for environmental effects on Known Good Die or for any activity of Buyer or a third party that damages the Die due to improper use, abuse, negligence, improper installation, accident, loss, damage in transit, or unauthorized repair or alteration by a person or entity other than AMD ("Warranty Exclusions").

The liability of AMD under this warranty is limited, at AMD's option, solely to repair the Die, to send replacement Die, or to make an appropriate credit adjustment or refund in an amount not to exceed the original purchase price actually paid for the Die returned to AMD, provided that: (a) AMD is promptly notified by Buyer in writing during the applicable warranty period of any defect or nonconformity in the Known Good Die; (b) Buyer obtains authorization from AMD to return the defective Die; (c) the defective Die is returned to AMD by Buyer in accordance with AMD's shipping instructions set forth below; and (d) Buyer shows to AMD's satisfaction that such alleged defect or nonconformity actually exists and was not caused by any of the above-referenced Warranty Exclusions. Buyer shall ship such defective Die to AMD via AMD's carrier, collect. Risk of loss will transfer to AMD when the defective Die is provided to AMD's carrier. If Buyer fails to adhere to these warranty returns guidelines, Buyer shall assume all risk of loss and shall pay for all freight to AMD's specified location. The aforementioned provisions do not extend the original warranty period of any Known Good Die that has either been repaired or replaced by AMD.

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Buyer agrees that it will make no warranty representations to its customers which exceed those given by AMD to Buyer unless and until Buyer shall agree to indemnify AMD in writing for any claims which exceed AMD's warranty.

Known Good Die are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of the Die can reasonably be expected to result in a personal injury. Buyer's use of Known Good Die for use in life support applications is at Buyer's own risk and Buyer agrees to fully indemnify AMD for any damages resulting in such use or sale.

REVISION SUMMARY

Revision A (January 1998)

Initial release.

Revision A+1, A+2 (February & April 1998)

Distinctive Characteristics

Changed typical program/erase time to 30 mA to match the CMOS DC Characteristics table in the Am29F400B full data sheet.

The minimum guarantee per sector is now 1 million cycles.

Pad Description

Corrected the following dimensions:

X (mils): pads 15, 18, 36

Y (mils): pads 10–12, 35, 36

X (mm): pads 2–22, 37, 38

Y (mm): pads 10–12, 23–32, 35, 36

Physical Specifications

Changed die thickness specification to ~20 mils.

Revision A+3 (May 1998)

Die Pad Locations

Corrected the location of the AMD logo from above pad 13 to above pad 23.

Revision B (November 1998)

Distinctive Characteristics, General Description, Pad Description, Ordering Information, Physical Specifications, Manufacturing Information

Updated for CS39S process technology.

Colophon

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Terms and Conditions

Replaced warranty with new version.

Revision C (December 1998)

Ordering Information

Changed Gel-Pak quantity to 396. Changed Valid Combinations to reflect die revision 2.

Packaging Information

Added section. Moved orientation information from die photograph section into this section.

Revision C+1 (June 14, 1999)

Physical Specifications

Corrected the bond pad dimensions. Deleted Si from the bond pad metalization specification.

Revision C+2 (June 27, 2001)

Manufacturing Information

Added Penang, Malaysia as a test facility (ACN2016).

Revision C+3 (July 27, 2007)

Ordering Information

Removed package type options DG and DW

Packaging Information

Removed all references to Gel-Pak