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CY14V116N

16-Mbit (1024K × 16) nvSRAM

Features

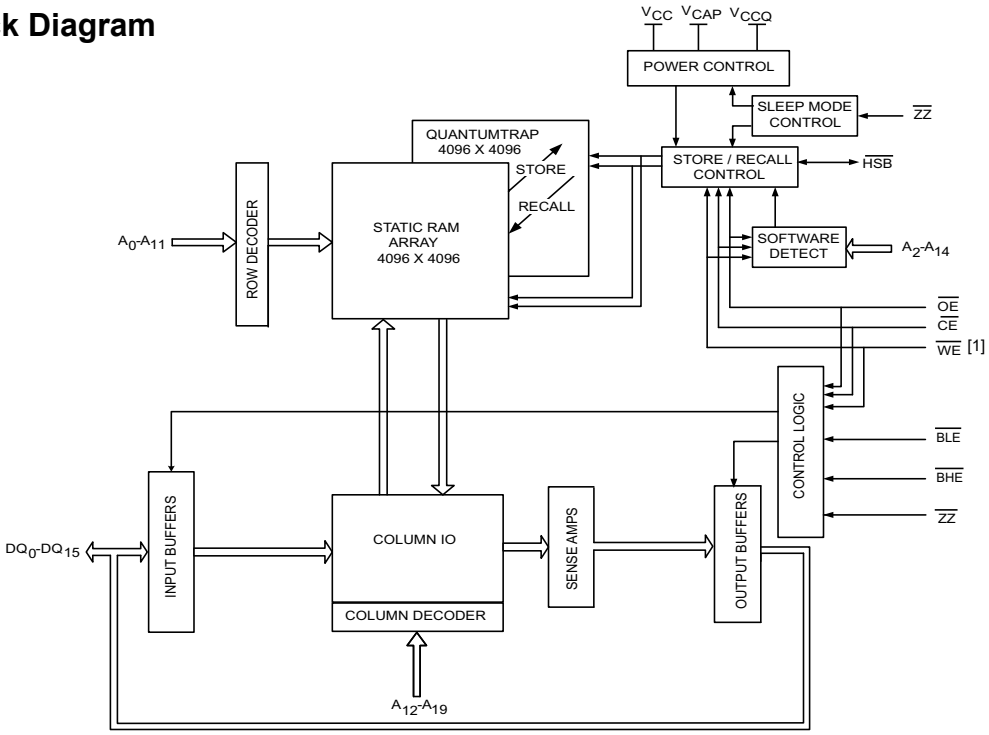
- 16-Mbit nonvolatile static random access memory (nvSRAM)
  - 30-ns and 45-ns access times
  - Logically organized as 1024K × 16
  - Hands-off automatic STORE on power-down with only a small capacitor
  - STORE to QuantumTrap nonvolatile elements is initiated by software, device pin, or AutoStore on power-down
  - RECALL to SRAM initiated by software or power-up
- High reliability
  - Infinite read, write, and RECALL cycles
  - 1 million STORE cycles to QuantumTrap
  - Data retention: 20 years
- Sleep mode operation
- Low power consumption
  - Active current of 75 mA at 45 ns
  - Standby mode current of 650 µA
  - Sleep mode current of 10 µA
- Operating voltage
  - Core V_{CC} = 2.7 V to 3.6 V; I/O V_{CCQ} = 1.65 V to 1.95 V
- Industrial temperature: –40 °C to +85 °C
- 165-ball fine-pitch ball grid array (FBGA) package
- Restriction of hazardous substances (RoHS) compliant

Functional Description

The Cypress CY14V116N is a fast SRAM, with a nonvolatile element in each memory cell. The memory is organized as 1024K words of 16 bits each. The embedded nonvolatile elements incorporate QuantumTrap technology, producing the world's most reliable nonvolatile memory. The SRAM can be read and written an infinite number of times. The nonvolatile data residing in the nonvolatile elements do not change when data is written to the SRAM. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power-down. On power-up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control.

For a complete list of related documentation, click here.

Logic Block Diagram



Note

1. In this datasheet, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2, such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.

Contents

Pinout

Figure 1. Pin Diagram: 165-Ball FBGA (×16)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A_6	A_8	$\overline{WE}$	$\overline{BLE}$	$\overline{CE_1}$	NC	$\overline{OE}$	A_5	A_3	NC
B	NC	DQ_0	DQ_1	A_4	$\overline{BHE}$	CE_2	NC	A_2	NC	NC	NC
C	$\overline{ZZ}$	NC	NC	V_{SS}	A_0	A_7	A_1	V_{SS}	NC	DQ_{15}	DQ_{14}
D	NC	DQ_2	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	V_{CAP}	NC	V_{CCQ}	V_{SS}	V_{SS}	V_{SS}	V_{CCQ}	NC	DQ_{13}	NC
F	NC	DQ_3	NC	V_{CCQ}	V_{CC}	V_{SS}	V_{CC}	V_{CCQ}	NC	NC	DQ_{12}
G	$\overline{HSB}$	NC	NC	V_{CCQ}	V_{CC}	V_{SS}	V_{CC}	V_{CCQ}	NC	NC	NC
H	NC	NC	V_{CCQ}	V_{CCQ}	V_{CC}	V_{SS}	V_{CC}	V_{CCQ}	V_{CCQ}	NC	NC
J	NC	NC	NC	V_{CCQ}	V_{CC}	V_{SS}	V_{CC}	V_{CCQ}	NC	DQ_8	NC
K	NC	NC	DQ_4	V_{CCQ}	V_{CC}	V_{SS}	V_{CC}	V_{CCQ}	NC	NC	NC
L	NC	DQ_5	NC	V_{CCQ}	V_{SS}	V_{SS}	V_{SS}	V_{CCQ}	NC	NC	DQ_9
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ_{10}	NC
N	NC	DQ_6	DQ_7	V_{SS}	A_{11}	A_{10}	A_9	V_{SS}	NC	NC	NC
P	NC	NC	NC	A_{13}	A_{19}	NC	A_{18}	A_{12}	NC	DQ_{11}	NC
R	NC	NC	A_{15}	NC	A_{17}	NC	A_{16}	NC[2]	A_{14}	NC	NC

Note
2. Address expansion for 32-Mbit. NC pin not connected to die.

Pin Definitions

Pin Name	I/O Type	Description
A_0–A_{19}	Input	**Address inputs.** Used to select one of the 1,048,576 words of the nvSRAM.
DQ_0–DQ_{15}	Input/Output	**Bidirectional data I/O lines**. Used as input or output lines depending on operation.
$\overline{WE}$	Input	**Write Enable input, Active LOW**. When selected LOW, data on the I/O pins is written to the specific address location.
$\overline{CE}_1$, CE_2	Input	**Chip Enable input.** The device is selected and a memory access begins on the falling edge of $\overline{CE}_1$ (while CE_2 is HIGH) or the rising edge of CE_2 (while $\overline{CE}_1$ is LOW).
$\overline{OE}$	Input	**Output Enable, Active LOW.** The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ HIGH causes the I/O pins to tristate.
$\overline{BLE}$	Input	**Byte Enable, Active LOW**. When selected LOW, enables DQ_7–DQ_0.
$\overline{BHE}$	Input	**Byte Enable, Active LOW**. When selected LOW, enables DQ_{15}–DQ_8.
$\overline{ZZ}$	Input	**Sleep Mode Enable.** When the $\overline{ZZ}$ pin is pulled LOW, the device enters a low-power Sleep mode and consumes the lowest power. Because this input is logically AND'ed with $\overline{CE}$, $\overline{ZZ}$ must be HIGH for normal operation.
V_{CC}	Power supply	**Power.** Power supply inputs to the core of the device.
V_{CCQ}	Power supply	**I/O Power.** Power supply inputs for the inputs and outputs of the device.
V_{SS}	Power Supply	**Ground for the device**. Must be connected to ground of the system.
$\overline{HSB}$	Input/Output	**Hardware STORE Busy ($\overline{HSB}$)**.When LOW, this output indicates that a Hardware STORE is in progress. When pulled LOW external to the chip, it initiates a nonvolatile STORE operation. After each Hardware and Software STORE operation, $\overline{HSB}$ is driven HIGH for a short time (t_{HHHD}) with standard output high current and then a weak internal pull-up resistor keeps this pin HIGH (external pull-up resistor connection optional).
V_{CAP}	Power Supply	**AutoStore capacitor**. Supplies power to the nvSRAM during power loss to store data from SRAM to nonvolatile elements.
NC	NC	**No Connect**. Die pads are not connected to the package pin.

Device Operation

The CY14V116N nvSRAM is made up of two functional components paired in the same physical cell. These are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation) automatically at power-down, or from the nonvolatile cell to the SRAM (the RECALL operation) on power-up. Both the STORE and RECALL operations are also available under software control. Using this unique architecture, all cells are stored and recalled in parallel. During the STORE and RECALL operations, SRAM read and write operations are inhibited. The CY14V116N supports infinite reads and writes to the SRAM. In addition, it provides infinite RECALL operations from the nonvolatile cells and up to 1 million STORE operations. See the Truth Table For SRAM Operations on page 23 for a complete description of read and write modes.

SRAM Read

The CY14V116N performs a read cycle whenever $\overline{CE}$ and $\overline{OE}$ are LOW, and $\overline{WE}$, ZZ, and $\overline{HSB}$ are HIGH. The address specified on pins A_0–A_{19} determines which of the 1,048,576 words of 16 bits each are accessed. Byte enables ($\overline{BHE}$, $\overline{BLE}$) determine which bytes are enabled to the output. When the read is initiated by an address transition, the outputs are valid after a delay of t_{AA} (read cycle 1). If the read is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at t_{ACE} or at t_{DOE}, whichever is later (read cycle 2). The data output repeatedly responds to address changes within the t_{AA} access time without the need for transitions on any control input pins. This remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ or $\overline{HSB}$ is brought LOW.

SRAM Write

A write cycle is performed when $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{HSB}$ is HIGH. The address inputs must be stable before entering the write cycle and must remain stable until $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common I/O pins DQ_0–DQ_{15} is written into the memory if it is valid t_{SD} before the end of a $\overline{WE}$-controlled write or before the end of a $\overline{CE}$-controlled write. The Byte Enable inputs ($\overline{BHE}$, $\overline{BLE}$) determine which bytes are written. Keep $\overline{OE}$ HIGH during the entire write cycle to avoid data bus contention on common I/O lines. If $\overline{OE}$ is left LOW, the internal circuitry turns off the output buffers t_{HZWE} after $\overline{WE}$ goes LOW.

AutoStore Operation (Power-Down)

The CY14V116N stores data to the nonvolatile QuantumTrap cells using one of the three storage operations. These three operations are: Hardware STORE, activated by the $\overline{HSB}$; Software STORE, activated by an address sequence; AutoStore, on device power-down. The AutoStore operation is a unique feature of nvSRAM and is enabled by default on the CY14V116N device.

During normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a STORE operation during power-down. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC} and a STORE operation is initiated with power provided by the V_{CAP} capacitor.

Note If the capacitor is not connected to the V_{CAP} pin, AutoStore must be disabled using the soft sequence specified in the section Preventing AutoStore on page 9. If AutoStore is enabled without a capacitor on the V_{CAP} pin, the device attempts an AutoStore operation without sufficient charge to complete the STORE. This corrupts the data stored in the nvSRAM.

Figure 2. AutoStore Mode

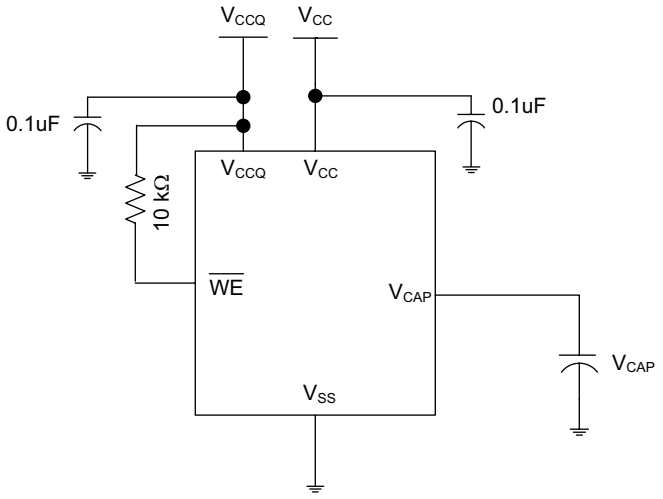


Figure 2 shows the proper connection of the storage capacitor (V_{CAP}) for automatic STORE operation. Refer to DC Electrical Characteristics on page 10 for the size of the V_{CAP}. The voltage on the V_{CAP} pin is driven to V_{VCAP} by a regulator on the chip. A pull-up resistor should be placed on $\overline{WE}$ to hold it inactive during power-up. This pull-up resistor is only effective if the $\overline{WE}$ signal is in tristate during power-up. When the nvSRAM comes out of power-up-RECALL, the host microcontroller must be active or the $\overline{WE}$ held inactive until the host microcontroller comes out of reset.

To reduce unnecessary nonvolatile STOREs, AutoStore and Hardware STORE operations are ignored unless at least one write operation has taken place (which sets a write latch) since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a write operation has taken place.

Hardware STORE ($\overline{HSB}$) Operation

The CY14V116N provides the $\overline{HSB}$ pin to control and acknowledge the STORE operations. The $\overline{HSB}$ pin is used to request a Hardware STORE cycle. When the $\overline{HSB}$ pin is driven LOW, the device conditionally initiates a STORE operation after t_{DELAY}. A STORE cycle begins only if a write to the SRAM has taken place since the last STORE or RECALL cycle. The $\overline{HSB}$ pin also acts as an open drain driver (an internal 100-kΩ weak pull-up resistor) that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

Note After each Hardware and Software STORE operation, $\overline{HSB}$ is driven HIGH for a short time (t_{HHHD}) with standard output high current and then remains HIGH by an internal 100-kΩ pull-up resistor.

SRAM write operations that are in progress when $\overline{HSB}$ is driven LOW by any means are given time (t_{DELAY}) to complete before the STORE operation is initiated. However, any SRAM write cycles requested after $\overline{HSB}$ goes LOW are inhibited until $\overline{HSB}$ returns HIGH. If the write latch is not set, $\overline{HSB}$ is not driven LOW by the device. However, any of the SRAM read and write cycles are inhibited until $\overline{HSB}$ is returned HIGH by the host microcontroller or another external source.

During any STORE operation, regardless of how it is initiated, the device continues to drive the $\overline{HSB}$ pin LOW, releasing it only when the STORE is complete. Upon completion of the STORE operation, the nvSRAM memory access is inhibited for t_{LZHSB} time after the $\overline{HSB}$ pin returns HIGH. Leave the $\overline{HSB}$ unconnected if it is not used.

Hardware RECALL (Power-Up)

During power-up or after any low-power condition ($V_{CC} < V_{SWITCH}$), an internal RECALL request is latched. When V_{CC} again exceeds the V_{SWITCH} on power-up, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete. During this time, the $\overline{HSB}$ pin is driven LOW by the HSB driver and all reads and writes to nvSRAM are inhibited.

Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. A Software STORE cycle is initiated by executing sequential $\overline{CE}$ or $\overline{OE}$ controlled read cycles from six specific address locations in exact order. During the STORE cycle, the previous nonvolatile data is first erased, followed by a store into the nonvolatile elements. After a STORE cycle is initiated, further reads and writes are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence. Otherwise, the sequence is aborted and no STORE or RECALL takes place.

To initiate the Software STORE cycle, the following read sequence must be performed:

1. Read address 0x4E38 Valid Read
2. Read address 0xB1C7 Valid Read
3. Read address 0x83E0 Valid Read
4. Read address 0x7C1F Valid Read
5. Read address 0x703F Valid Read
6. Read address 0x8FC0 Initiate STORE cycle

The software sequence may be clocked with $\overline{CE}$-controlled reads or $\overline{OE}$-controlled reads, with $\overline{WE}$ kept HIGH for all the six read sequences. After the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. $\overline{HSB}$ is driven LOW. After the t_{STORE} cycle time is fulfilled, the SRAM is activated again for the read and write operation.

Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of read operations in a manner similar to the Software STORE initiation.

To initiate the RECALL cycle, perform the following sequence of $\overline{CE}$ or $\overline{OE}$ controlled read operations:

1. Read address 0x4E38 Valid Read
2. Read address 0xB1C7 Valid Read
3. Read address 0x83E0 Valid Read
4. Read address 0x7C1F Valid Read
5. Read address 0x703F Valid Read
6. Read address 0x4C63 Initiate RECALL cycle

Internally, RECALL is a two-step procedure. First, the SRAM data is cleared; then, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is again ready for read and write operations. The RECALL operation does not alter the data in the nonvolatile elements.

Table 1. Mode Selection

$\overline{CE}$[3]	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$, $\overline{BLE}$	A_{15}–A_0[4]	Mode	I/O	Power
H	X	X	X	X	Not selected	Output High Z	Standby
L	H	L	L	X	Read SRAM	Output Data	Active
L	L	X	L	X	Write SRAM	Input Data	Active
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Disable	Output Data Output Data Output Data Output Data Output Data Output Data	Active[5]
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Enable	Output Data Output Data Output Data Output Data Output Data Output Data	Active[5]
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output Data Output Data Output Data Output Data Output Data Output High Z	Active I_{CC2}[5]
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output Data Output Data Output Data Output Data Output Data Output High Z	Active[5]

Notes

3. In this datasheet, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. Intermediate voltage levels are not permitted on any of the chip enable pins.
4. While there are 20 address lines on the CY14V116N, only 13 address lines (A_{14}–A_2) are used to control software modes. The remaining address lines are don't care.
5. The six consecutive address locations must be in the order listed. $\overline{WE}$ must be HIGH during all six cycles to enable a nonvolatile operation.

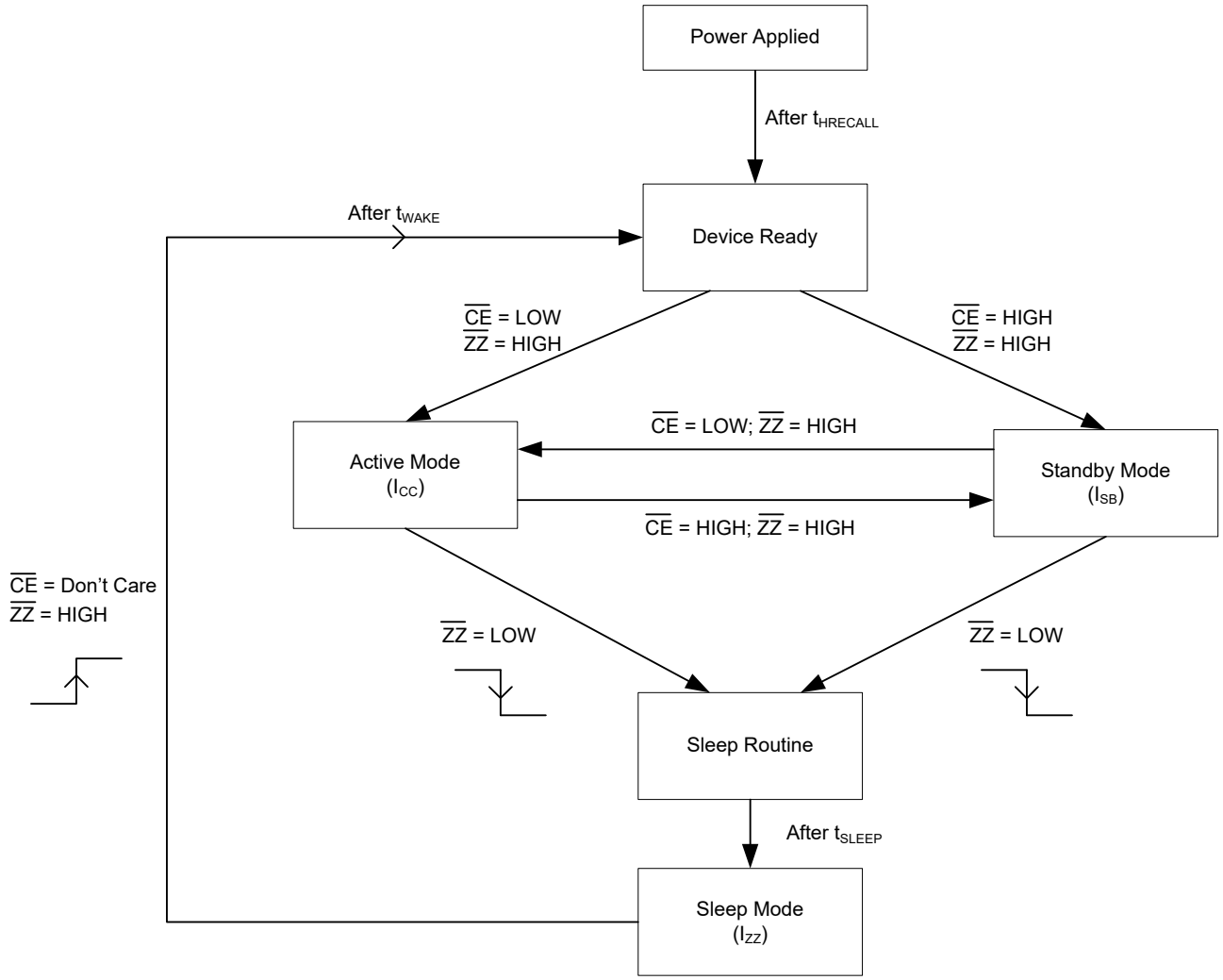
Sleep Mode

In Sleep mode, the device consumes the lowest power supply current (I_{ZZ}). The device enters a low-power Sleep mode after asserting the $\overline{ZZ}$ pin LOW. After the Sleep mode is registered, the nvSRAM does a STORE operation to secure the data to the nonvolatile memory and then enters the low-power mode. The device starts consuming I_{ZZ} current after t_{SLEEP} time from the instance when the Sleep mode is initiated. When the $\overline{ZZ}$ pin is LOW, all input pins are ignored except the $\overline{ZZ}$ pin. The nvSRAM is not accessible for normal operations while it is in Sleep mode.

When the $\overline{ZZ}$ pin is de-asserted (HIGH), there is a delay t_{WAKE} before you can access the device. If Sleep mode is not used, the $\overline{ZZ}$ pin should be tied to V_{CCQ}.

Note When nvSRAM enters the Sleep mode, it initiates a nonvolatile STORE cycle, which results in losing one endurance cycle for every Sleep mode entry unless the data was not written to the nvSRAM since the last nonvolatile STORE/RECALL operation.

Figure 3. Sleep Mode ($\overline{ZZ}$) Flow Diagram



Preventing AutoStore

The AutoStore function is disabled by initiating an AutoStore disable sequence. A sequence of read operations is performed in a manner similar to the Software STORE initiation.

To initiate the AutoStore disable sequence, the following sequence of $\overline{CE}$ or $\overline{OE}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid Read
2. Read address 0xB1C7 Valid Read
3. Read address 0x83E0 Valid Read
4. Read address 0x7C1F Valid Read
5. Read address 0x703F Valid Read
6. Read address 0x8B45 AutoStore Disable

AutoStore is re-enabled by initiating an AutoStore enable sequence. A sequence of read operations is performed in a manner similar to the software RECALL initiation.

To initiate the AutoStore enable sequence, the following sequence of $\overline{CE}$ or $\overline{OE}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid Read
2. Read address 0xB1C7 Valid Read
3. Read address 0x83E0 Valid Read
4. Read address 0x7C1F Valid Read
5. Read address 0x703F Valid Read
6. Read address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or re-enabled, a manual software STORE operation must be performed to save the AutoStore state through subsequent power-down cycles. The part comes from the factory with AutoStore enabled and 0x00 written in all cells.

Data Protection

The CY14V116N protects data from corruption during low-voltage conditions by inhibiting all externally initiated STORE and write operations. The low-voltage condition is detected when V_{CC} is less than V_{SWITCH}. If the CY14V116N is in a Write mode at power-up (both $\overline{CE}$ and $\overline{WE}$ are LOW), after a RECALL or STORE, the write is inhibited until the SRAM is enabled after t_{LZHSB} ($\overline{HSB}$ to output active). When $V_{CC} < V_{IODIS}$, I/Os are disabled (no STORE takes place). This protects against inadvertent writes during power-up or brown out conditions.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Maximum accumulated storage time
At 150 °C ambient temperature ..... 1000 h
At 85 °C ambient temperature ..... 20 Years
Maximum junction temperature ..... 150 °C

Supply voltage on V_{CC} relative to V_{SS} .....–0.5 V to +4.1 V

Supply voltage on V_{CCQ} relative to V_{SS} .....–0.5 V to +2.45 V

Voltage applied to outputs
in high-Z state .....–0.5 V to V_{CCQ} + 0.5 V

Input voltage .....–0.5 V to V_{CCQ} + 0.5 V

Transient voltage (<20 ns)
on any pin to ground potential .....–2.0 V to V_{CCQ} + 2.0 V

Package power dissipation capability
(T_A = 25 °C) ..... 1.0 W

Surface mount lead soldering temperature
(3 Seconds) ..... +260 °C

DC output current (1 output at a time, 1s duration) .... 20 mA

Static discharge voltage
(per MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 140 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC}	V_{CCQ}
Industrial	–40 °C to +85 °C	2.7 V to 3.6 V	1.65 V to 1.95 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ[6]	Max	Unit
V_{CC}	Core power supply	–		2.7	3.0	3.6	V
V_{CCQ}	I/O power supply			1.65	1.80	1.95	V
I_{CC1}	Average V_{CC} current	Values obtained without output loads (I_{OUT} = 0 mA)	t_{RC} = 30 ns	–	–	95	mA
			t_{RC} = 45 ns	–	–	75	mA
I_{CCQ1}	Average V_{CCQ} current	Values obtained without output loads (I_{OUT} = 0 mA)	t_{RC} = 30 ns	–	–	30	mA
			t_{RC} = 45 ns	–	–	25	mA
I_{CC2}	Average V_{CC} current during STORE	All inputs don't care, V_{CC} = V_{CC} (max). Average current for duration t_{STORE}		–	–	10	mA
I_{CC3}	Average V_{CC} current at t_{RC} = 200 ns, V_{CC} (typ), 25 °C	All inputs cycling at CMOS levels. Values obtained without output loads (I_{OUT} = 0 mA).		–	50	–	mA
I_{CCQ3}	Average V_{CC} current at t_{RC} = 200 ns, V_{CCQ} (typ), 25 °C	All inputs cycling at CMOS levels. Values obtained without output loads (I_{OUT} = 0 mA).		–	15	–	mA
I_{CC4}[7]	Average V_{CAP} current during AutoStore cycle	All inputs don't care. Average current for duration t_{STORE}		–	–	6	mA

Notes

6. Typical values are at 25 °C, V_{CC} = V_{CC} (typ) and V_{CCQ} = V_{CCQ} (typ). Not 100% tested.
7. This parameter is only guaranteed by design and is not tested.
8. The $\overline{HSB}$ pin has I_{OUT} = -4 µA for V_{OH} of 1.07 V when both active HIGH and LOW drivers are disabled. When they are enabled standard V_{OH} and V_{OL} are valid. This parameter is characterized but not tested.
9. Min V_{CAP} value guarantees that there is a sufficient charge available to complete a successful AutoStore operation. Max V_{CAP} value guarantees that the capacitor on V_{CAP} is charged to a minimum voltage during a Power-Up RECALL cycle so that an immediate power-down cycle can complete a successful AutoStore. Therefore, it is always recommended to use a capacitor within the specified min and max limits.
10. Maximum voltage on V_{CAP} pin (V_{VCAP}) is provided for guidance when choosing the V_{CAP} capacitor. The voltage rating of the V_{CAP} capacitor across the operating temperature range should be higher than the V_{VCAP} voltage.
11. These parameters are only guaranteed by design and are not tested.

DC Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ[6]	Max	Unit
I_{SB}	V_{CC} standby current	$\overline{CE} \geq (V_{CCQ} - 0.2\ V)$. $V_{IN} \leq 0.2\ V$ or $\geq (V_{CCQ} - 0.2\ V)$. Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.	t_{RC} = 30 ns	–	–	650	µA
			t_{RC} = 45 ns	–	–	500	µA
I_{ZZ}	Sleep mode current	All inputs are static at CMOS level		–	–	10	µA
I_{IX}[8]	Input leakage current (except $\overline{HSB}$)	$V_{CC} = V_{CC}$ (max), $V_{SS} \leq V_{IN} \leq V_{CC}$		–1	–	+1	µA
	Input leakage current (for $\overline{HSB}$)	$V_{CC} = V_{CC}$ (max), $V_{SS} \leq V_{IN} \leq V_{CC}$		–100	–	+1	µA
I_{OZ}	Off state output leakage current	$V_{CC} = V_{CC}$ (max), $V_{SS} \leq V_{OUT} \leq V_{CC}$, $\overline{CE}$ or $\overline{OE} \geq V_{IH}$ or $\overline{BLE}/\overline{BHE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$		–1	–	+1	µA
V_{IH}	Input HIGH voltage	–		0.7 × V_{CCQ}	–	V_{CCQ} + 0.3	V
V_{IL}	Input LOW voltage	–		V_{ss} – 0.3	–	0.3 × V_{CCQ}	V
V_{OH}	Output HIGH voltage	I_{OUT} = –1 mA		V_{CCQ} – 0.45	–	–	V
V_{OL}	Output LOW voltage	I_{OUT} = 2 mA		–	–	0.45	V
V_{CAP}[9]	Storage capacitor	Between V_{CAP} pin and V_{SS}		19.8	22.0	82.0	µF
V_{VCAP}[10, 11]	Maximum voltage driven on V_{CAP} pin by the device	$V_{CC} = V_{CC}$ (max)		–	–	5.0	V

Notes

6. Typical values are at 25 °C, $V_{CC} = V_{CC}$ (typ) and $V_{CCQ} = V_{CCQ}$ (typ). Not 100% tested.
7. This parameter is only guaranteed by design and is not tested.
8. The $\overline{HSB}$ pin has I_{OUT} = -4 µA for V_{OH} of 1.07 V when both active HIGH and LOW drivers are disabled. When they are enabled standard V_{OH} and V_{OL} are valid. This parameter is characterized but not tested.
9. Min V_{CAP} value guarantees that there is a sufficient charge available to complete a successful AutoStore operation. Max V_{CAP} value guarantees that the capacitor on V_{CAP} is charged to a minimum voltage during a Power-Up RECALL cycle so that an immediate power-down cycle can complete a successful AutoStore. Therefore, it is always recommended to use a capacitor within the specified min and max limits.
10. Maximum voltage on V_{CAP} pin (V_{VCAP}) is provided for guidance when choosing the V_{CAP} capacitor. The voltage rating of the V_{CAP} capacitor across the operating temperature range should be higher than the V_{VCAP} voltage.
11. These parameters are only guaranteed by design and are not tested.

Data Retention and Endurance

Over the Operating Range

Parameter	Description	Min	Unit
$DATA_R$	Data retention	20	Years
NV_C	Nonvolatile STORE operations	1,000,000	Cycles

Capacitance

In the following table, the capacitance parameters are listed.

Parameter [12]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = V_{CC} (typ), V_{CCQ} = V_{CCQ} (typ)	10	pF
C_{IO}	Input/Output capacitance		10	pF
C_{OUT}	Output capacitance		10	pF

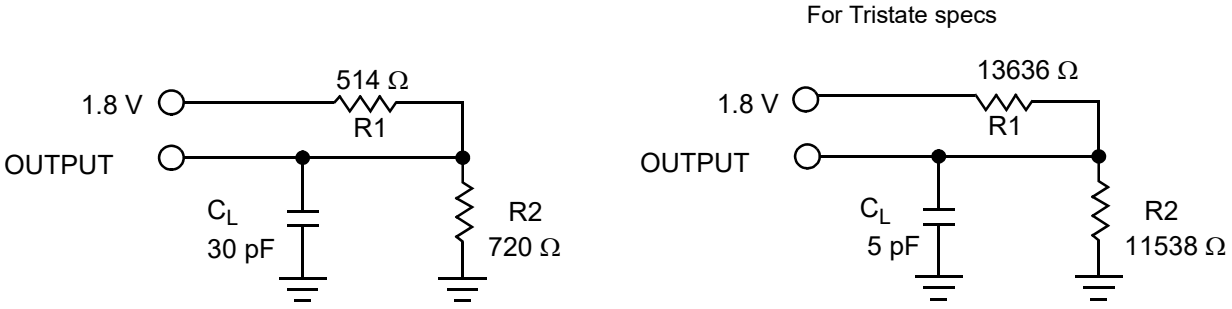
Thermal Resistance

In the following table, the thermal resistance parameters are listed.

Parameter [12]	Description	Test Conditions	165-ball FBGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	15.6	°C/W
Θ_{JC}	Thermal resistance (junction to case)		2.9	°C/W

AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms



AC Test Conditions

Input pulse levels .....0 V to 1.8 V
Input rise and fall times (10%–90%) ..... ≤ 3 ns
Input and output timing reference levels ..... 0.9 V

Note
12. These parameters are only guaranteed by design and are not tested.

AC Switching Characteristics

Over the Operating Range

Parameters [13]		Description	30 ns		45 ns		Unit
Cypress Parameter	Alt Parameter		Min	Max	Min	Max	
SRAM Read Cycle							
t_{ACE}	t_{ACS}	Chip enable access time	–	30	–	45	ns
t_{RC} [14]	t_{RC}	Read cycle time	30	–	45	–	ns
t_{AA} [15]	t_{AA}	Address access time	–	30	–	45	ns
t_{DOE}	t_{OE}	Output enable to data valid	–	14	–	20	ns
t_{OHA} [15]	t_{OH}	Output hold after address change	3	–	3	–	ns
t_{LZCE} [16]	t_{LZ}	Chip enable to output active	3	–	3	–	ns
t_{HZCE} [16, 17]	t_{HZ}	Chip disable to output inactive	–	12	–	15	ns
t_{LZOE} [16]	t_{OLZ}	Output enable to output active	0	–	0	–	ns
t_{HZOE} [16, 17]	t_{OHZ}	Output disable to output inactive	–	12	–	15	ns
t_{PU} [16]	t_{PA}	Chip enable to power active	0	–	0	–	ns
t_{PD} [16]	t_{PS}	Chip disable to power standby	–	30	–	45	ns
t_{DBE}	-	Byte enable to data valid	–	14	–	20	ns
t_{LZBE} [16]	-	Byte enable to output active	0	–	0	–	ns
t_{HZBE} [16, 17]	-	Byte disable to output inactive	–	12	–	15	ns
SRAM Write Cycle							
t_{WC}	t_{WC}	Write cycle time	30	–	45	–	ns
t_{PWE}	t_{WP}	Write pulse width	24	–	30	–	ns
t_{SCE}	t_{CW}	Chip enable to end of write	24	–	30	–	ns
t_{SD}	t_{DW}	Data setup to end of write	14	–	15	–	ns
t_{HD}	t_{DH}	Data hold after end of write	0	–	0	–	ns
t_{AW}	t_{AW}	Address setup to end of write	24	–	30	–	ns
t_{SA}	t_{AS}	Address setup to start of write	0	–	0	–	ns
t_{HA}	t_{WR}	Address hold after end of write	0	–	0	–	ns
t_{HZWE} [16, 17, 18]	t_{WZ}	Write enable to output disable	–	12	–	15	ns
t_{LZWE} [16]	t_{OW}	Output active after end of write	3	–	3	–	ns
t_{BW}	-	Byte enable to end of write	24	–	30	–	ns

Notes

13. Test conditions assume a signal transition time of 3 ns or less, timing reference levels of $V_{CCQ}/2$, input pulse levels of 0 to V_{CCQ} (typ), and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as shown in Figure 4 on page 12.
14. $\overline{WE}$ must be HIGH during SRAM read cycles.
15. Device is continuously selected with $\overline{CE}$, $\overline{OE}$ and $\overline{BLE}$, $\overline{BHE}$ LOW.
16. These parameters are only guaranteed by design and are not tested.
17. t_{HZCE}, t_{HZOE}, t_{HZBE}, and t_{HZWE} are specified with a load capacitance of 5 pF. Transition is measured ±200 mV from the steady state output voltage.
18. If $\overline{WE}$ is LOW when $\overline{CE}$ goes LOW, the outputs remain in the high impedance state.

Figure 5. SRAM Read Cycle 1: Address Controlled[19, 20, 21]

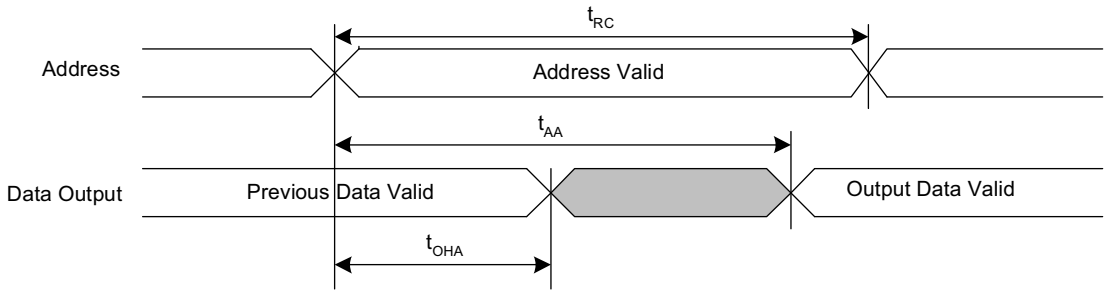
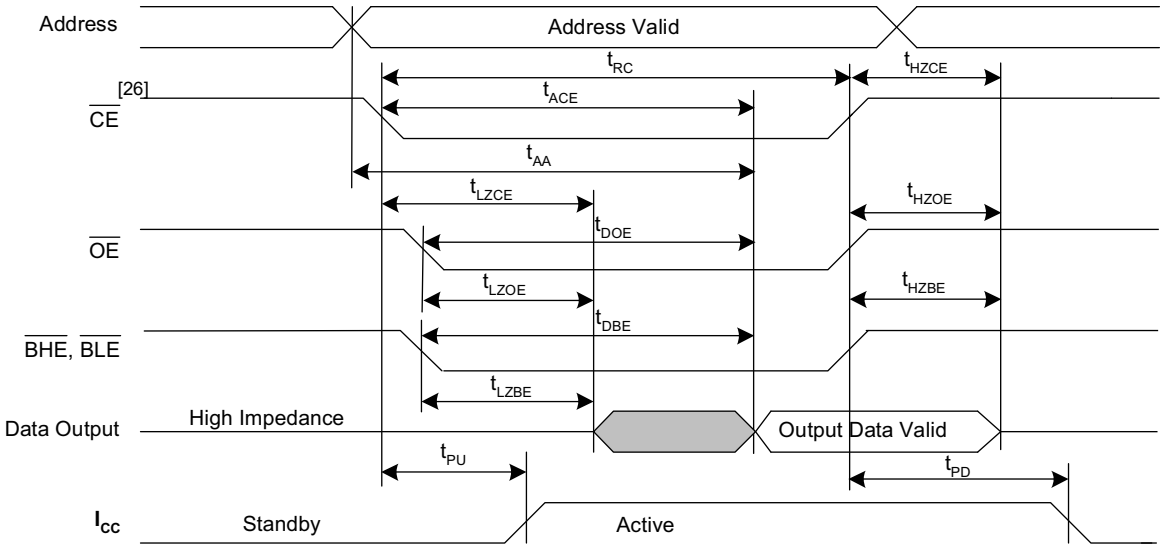
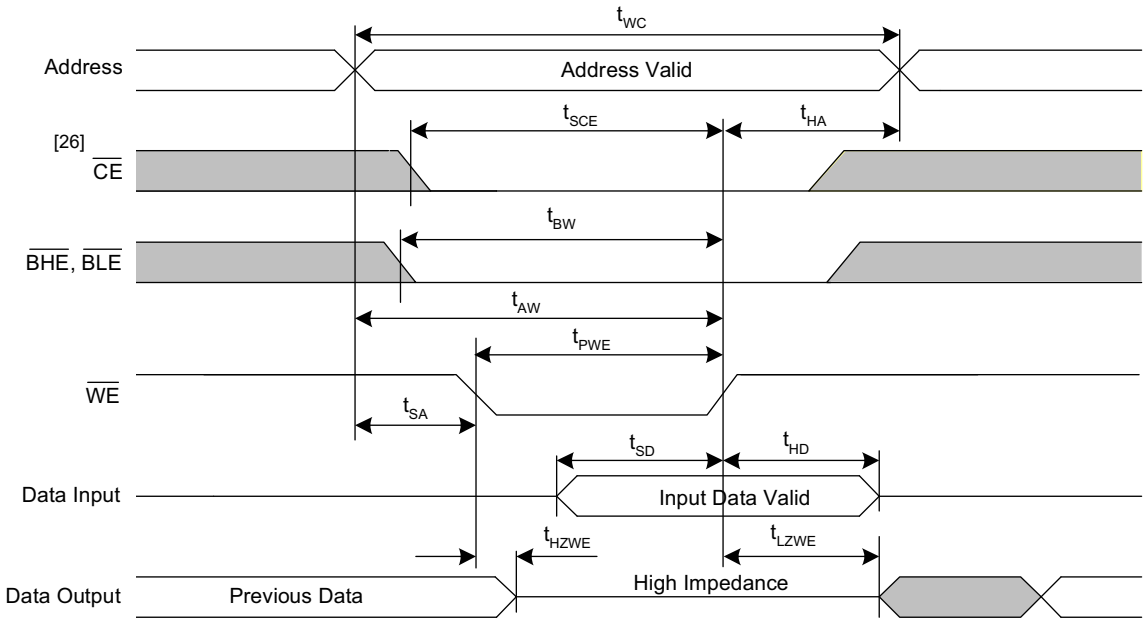


Figure 6. SRAM Read Cycle 2: $\overline{CE}$ and $\overline{OE}$ Controlled[22, 23]



Notes
19. $\overline{WE}$ must be HIGH during SRAM read cycles.
20. Device is continuously selected with $\overline{CE}$, $\overline{OE}$ and $\overline{BLE}$, $\overline{BHE}$ LOW.
21. $\overline{HSB}$ must remain HIGH during Read and Write cycles.
22. $\overline{WE}$ must be HIGH during SRAM read cycles.
23. $\overline{HSB}$ must remain HIGH during Read and Write cycles.

Figure 7. SRAM Write Cycle 1: $\overline{WE}$ Controlled[27, 25, 28]



Notes

24. $\overline{WE}$ must be HIGH during SRAM read cycles.
25. $\overline{HSB}$ must remain HIGH during Read and Write cycles.
26. In this datasheet $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. Intermediate voltage levels are not permitted on any of the chip enable pins.
27. If $\overline{WE}$ is LOW when $\overline{CE}$ goes LOW, the outputs remain in the high impedance state.
28. $\overline{CE}$ or $\overline{WE}$ must be $\geq V_{IH}$ during address transitions.

Figure 8. SRAM Write Cycle 2: $\overline{CE}$ Controlled[29, 30, 31]

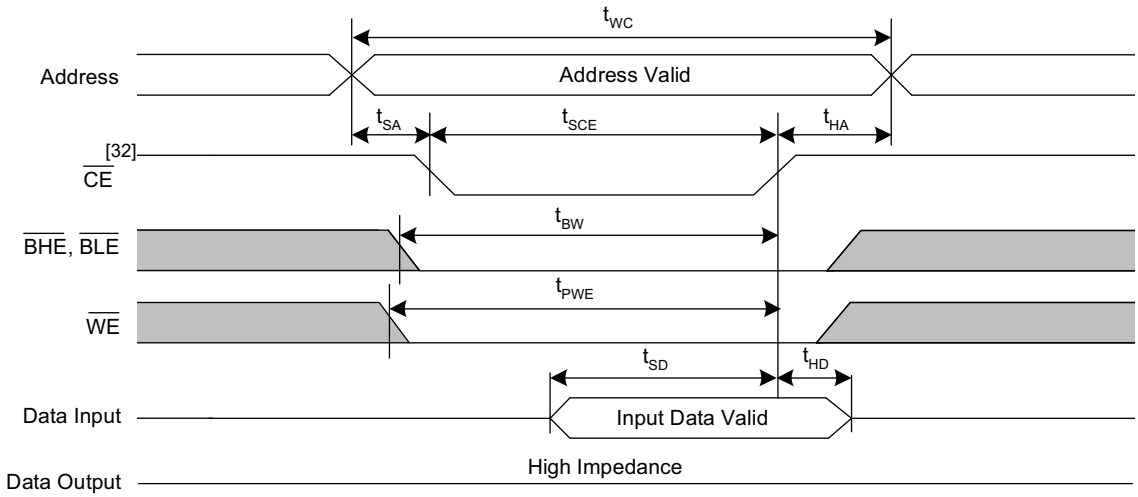
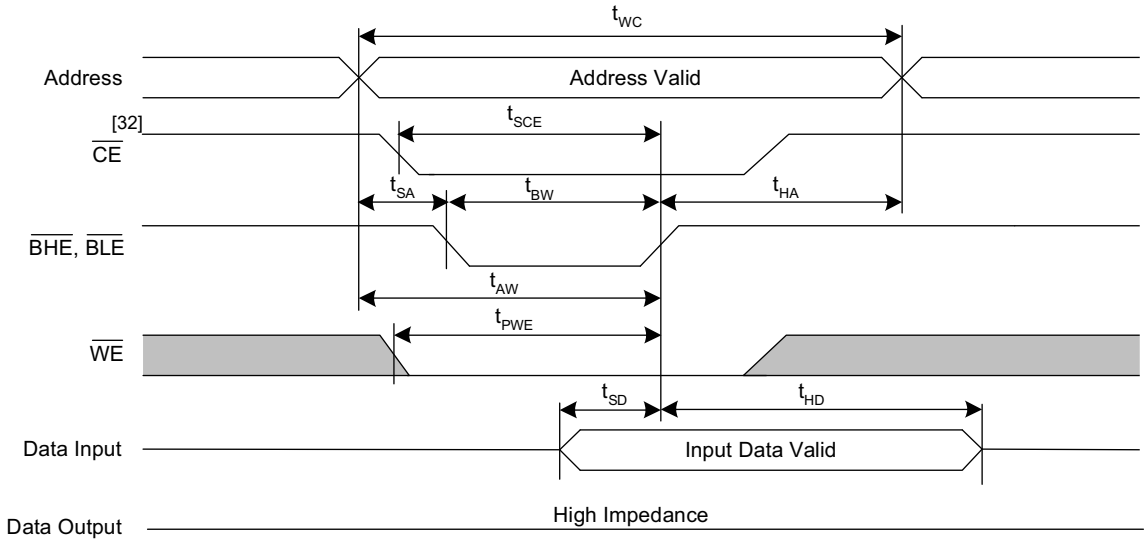


Figure 9. SRAM Write Cycle 3: $\overline{BHE}$, $\overline{BLE}$ Controlled[29, 30, 31]



Notes

29. If $\overline{WE}$ is LOW when $\overline{CE}$ goes LOW, the outputs remain in the high-impedance state.
30. $\overline{HSB}$ must remain HIGH during Read and Write cycles.
31. $\overline{CE}$ or $\overline{WE}$ must be $\geq V_{IH}$ during address transitions.
32. In this datasheet, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. Intermediate voltage levels are not permitted on any of the chip enable pins.

AutoStore/Power-Up RECALL Characteristics

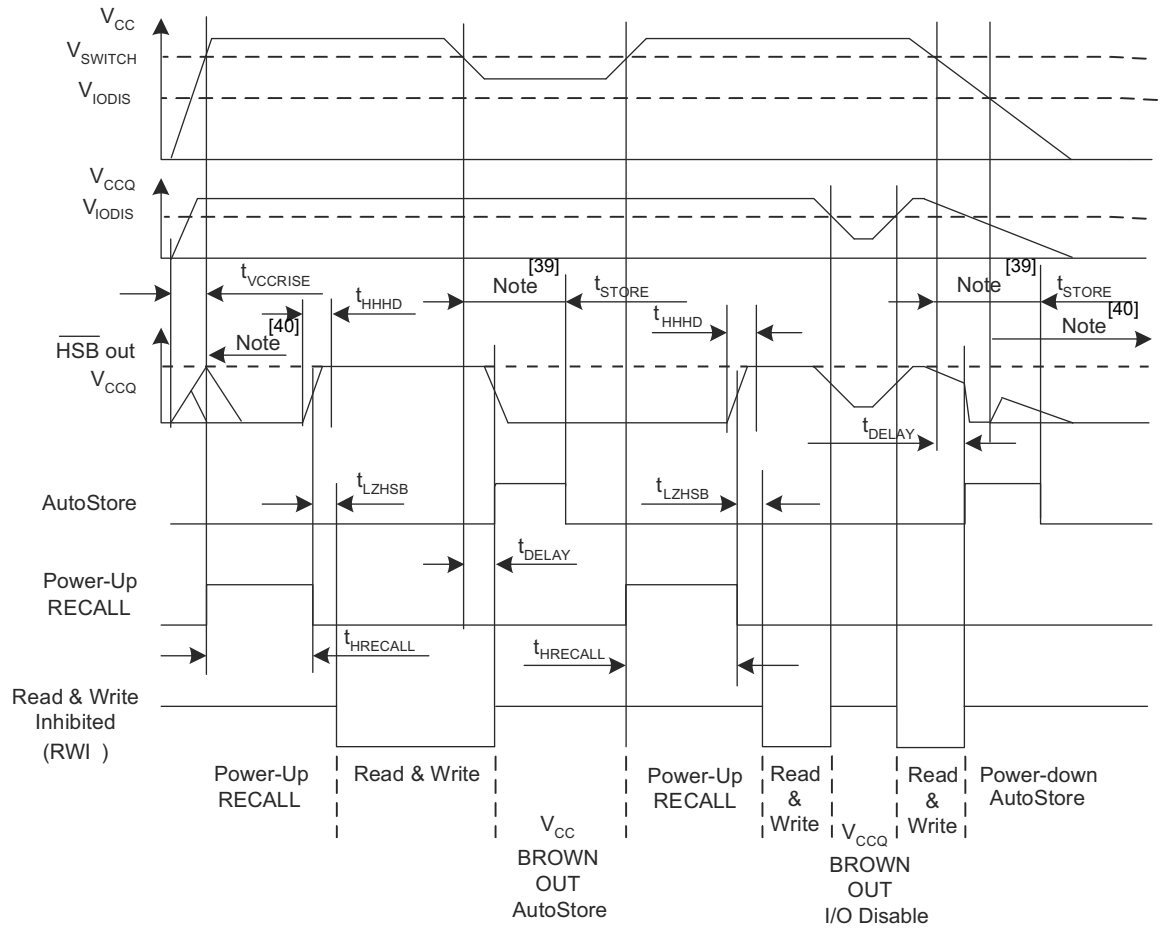
Over the Operating Range

Parameter	Description	Min	Max	Unit
$t_{HRECALL}$ [33]	Power-Up RECALL duration	–	30	ms
t_{STORE} [34]	STORE cycle duration	–	8	ms
t_{DELAY} [35, 36]	Time allowed to complete SRAM write cycle	–	25	ns
V_{SWITCH}	Low voltage trigger level	–	2.65	V
$t_{VCCRISE}$[36]	V_{CC} rise time	150	–	µs
V_{IODIS}[37]	I/O disable voltage on V_{CCQ}	–	1.5	V
V_{HDIS}[36]	$\overline{HSB}$ output disable voltage	–	1.9	V
t_{LZHSB}[36]	$\overline{HSB}$ to output active time	–	5	µs
t_{HHHD}[36]	$\overline{HSB}$ HIGH active time	–	500	ns

Notes

33. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.
34. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
35. On a Hardware STORE and AutoStore initiation, SRAM write operation continues to be enabled for time t_{DELAY}.
36. These parameters are only guaranteed by design and are not tested.
37. $\overline{HSB}$ is not defined below V_{IODIS} voltage.

Figure 10. AutoStore or Power-Up RECALL[38]



Notes

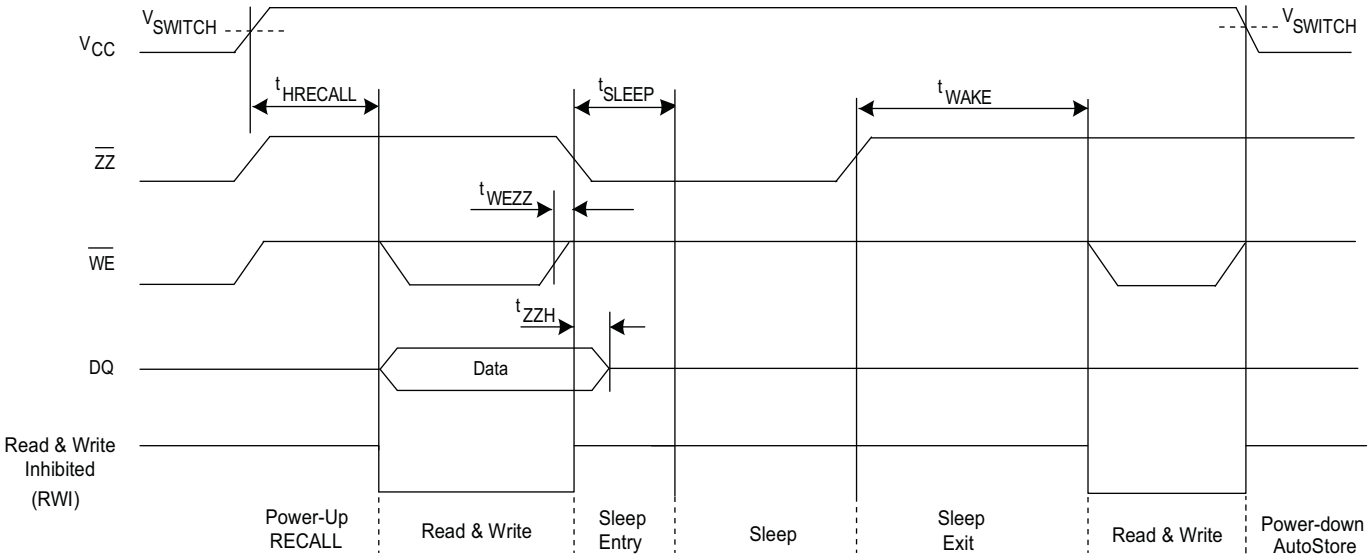
38. Read and Write cycles are ignored during STORE, RECALL, and while V_{CC} is below V_{SWITCH}.
39. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
40. During power-up and power-down, $\overline{HSB}$ glitches when $\overline{HSB}$ pin is pulled up through an external resistor.

Sleep Mode Characteristics

Over the Operating Range

Parameter	Description	Min	Max	Unit
t_{WAKE}	Sleep mode exit time ($\overline{ZZ}$ HIGH to first access after wakeup)	–	30	ms
t_{SLEEP}	Sleep mode enter time ($\overline{ZZ}$ LOW to $\overline{CE}$ don't care)	–	8	ms
t_{ZZL}	$\overline{ZZ}$ active LOW time	50	–	ns
t_{WEZZ}	Last write to Sleep mode entry time	0	–	µs
t_{ZZH}	$\overline{ZZ}$ active to DQ Hi-Z time	–	70	ns

Figure 11. Sleep Mode [41]



Note
41. Device initiates sleep routine and enters into Sleep mode after t_{SLEEP} duration.

Software Controlled STORE and RECALL Characteristics

Over the Operating Range

Parameter [42, 43]	Description	30 ns		45 ns		Unit
		Min	Max	Min	Max	
t_{RC}	STORE/RECALL initiation cycle time	30	–	45	–	ns
t_{SA}	Address setup time	0	–	0	–	ns
t_{CW}	Clock pulse width	24	–	30	–	ns
t_{HA}	Address hold time	0	–	0	–	ns
t_{RECALL}	RECALL duration	–	600	–	600	µs
t_{SS} [44, 45]	Soft sequence processing time	–	500	–	500	µs

Notes

42. The software sequence is clocked with $\overline{CE}$ controlled or $\overline{OE}$ controlled reads.
43. The six consecutive addresses must be read in the order listed in Table 1 on page 7. $\overline{WE}$ must be HIGH during all six consecutive cycles.
44. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain high to effectively register command.
45. Commands such as STORE and RECALL lock out I/O until the operation is complete which further increases this time. See the specific command.

Figure 12. $\overline{CE}$ and $\overline{OE}$ Controlled Software STORE and RECALL Cycle[46]

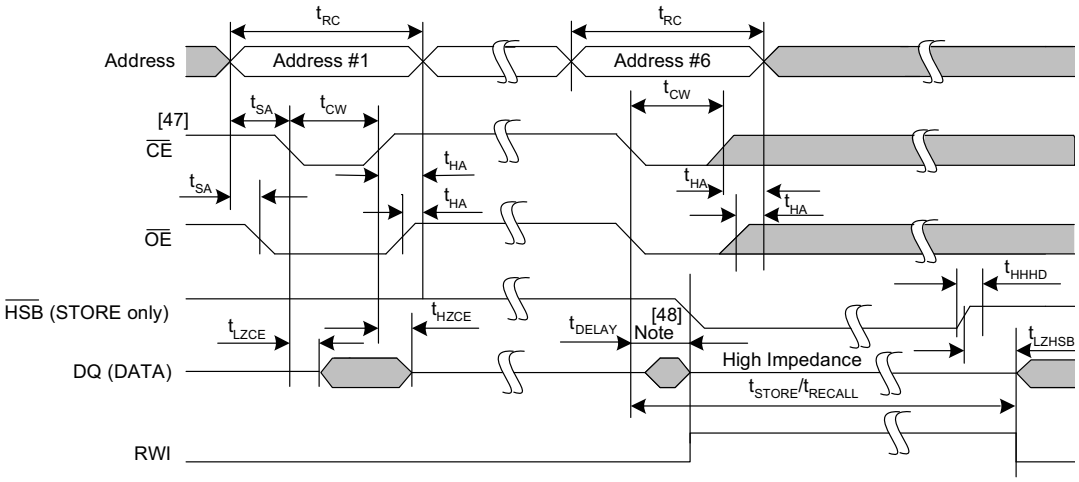
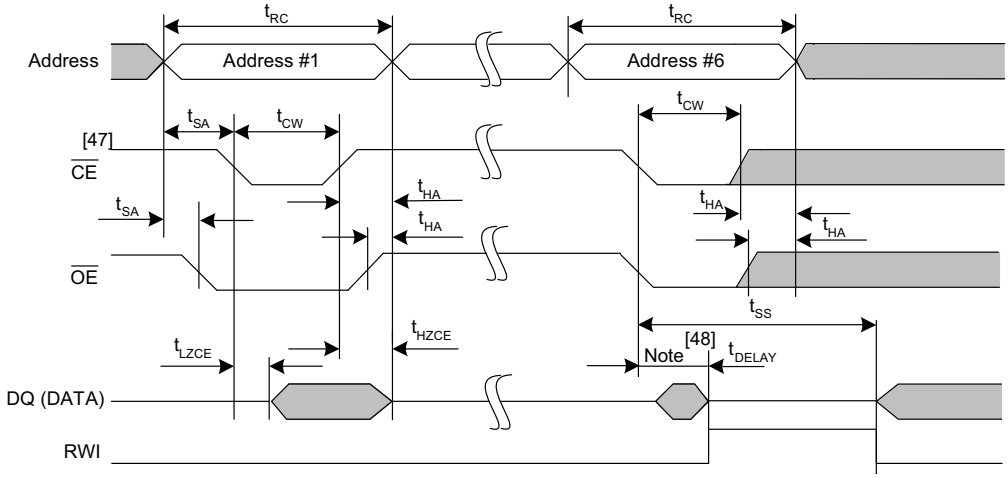


Figure 13. AutoStore Enable and Disable Cycle



Notes

46. The six consecutive addresses must be read in the order listed in Table 1 on page 7. $\overline{WE}$ must be HIGH during all six consecutive cycles.
47. In this datasheet, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. Intermediate voltage levels are not permitted on any of the chip enable pins.
48. DQ output data at the sixth read may be invalid because the output is disabled at t_{DELAY} time.

Hardware STORE Characteristics

Over the Operating Range

Parameter	Description	Min	Max	Unit
t_{DHSB}	$\overline{HSB}$ to output active time when write latch not set	–	25	ns
t_{PHSB}	Hardware STORE pulse width	15	–	ns

Figure 14. Hardware STORE Cycle[49]

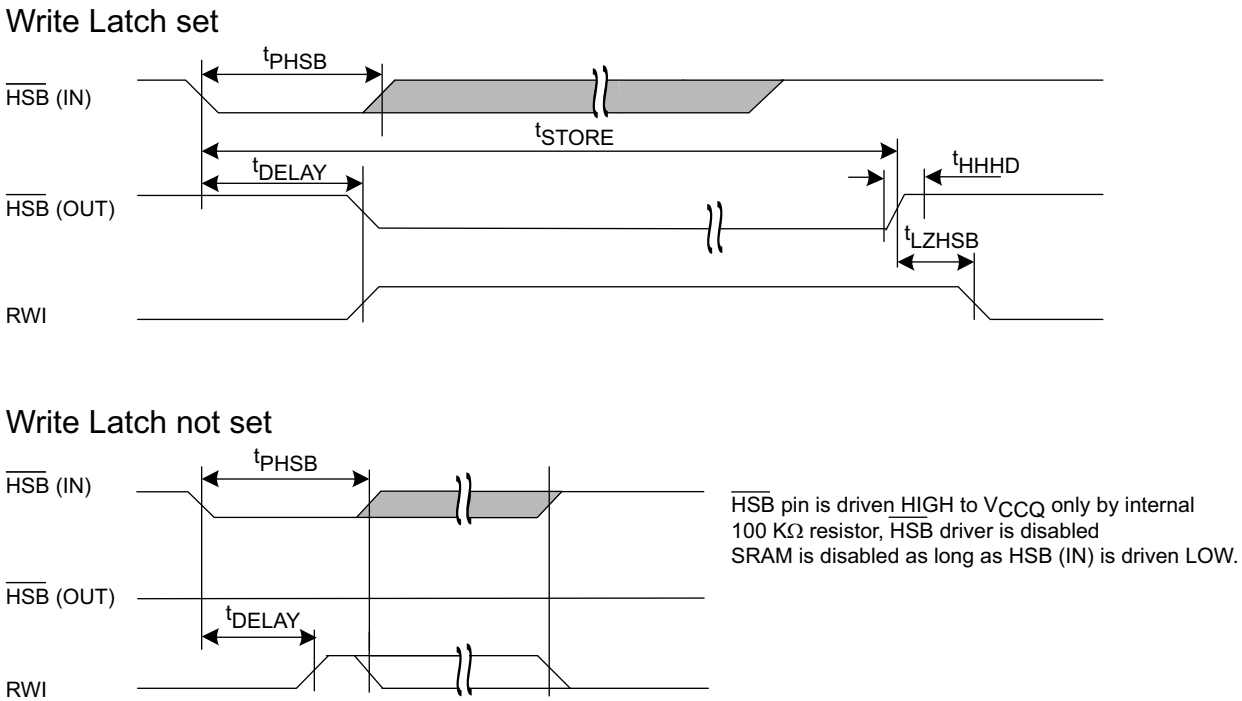
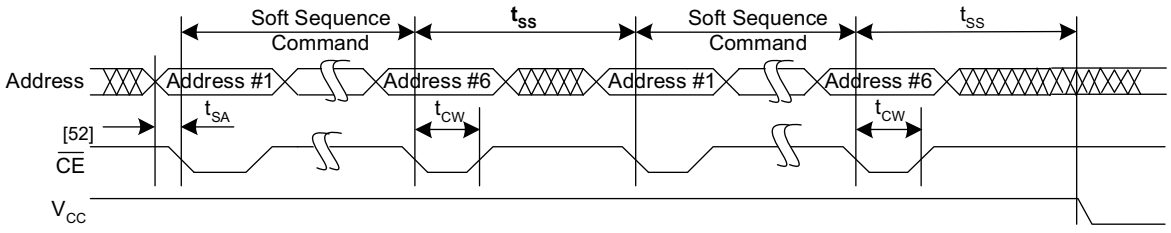


Figure 15. Soft Sequence Processing[50, 51]



Notes

49. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
50. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain high to effectively register command.
51. Commands, such as STORE and RECALL, lock out I/O until the operation is complete which further increases this time. See the specific command.
52. In this datasheet, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. Intermediate voltage levels are not permitted on any of the chip enable pins.

Truth Table For SRAM Operations

$\overline{HSB}$ should remain HIGH for SRAM Operations.

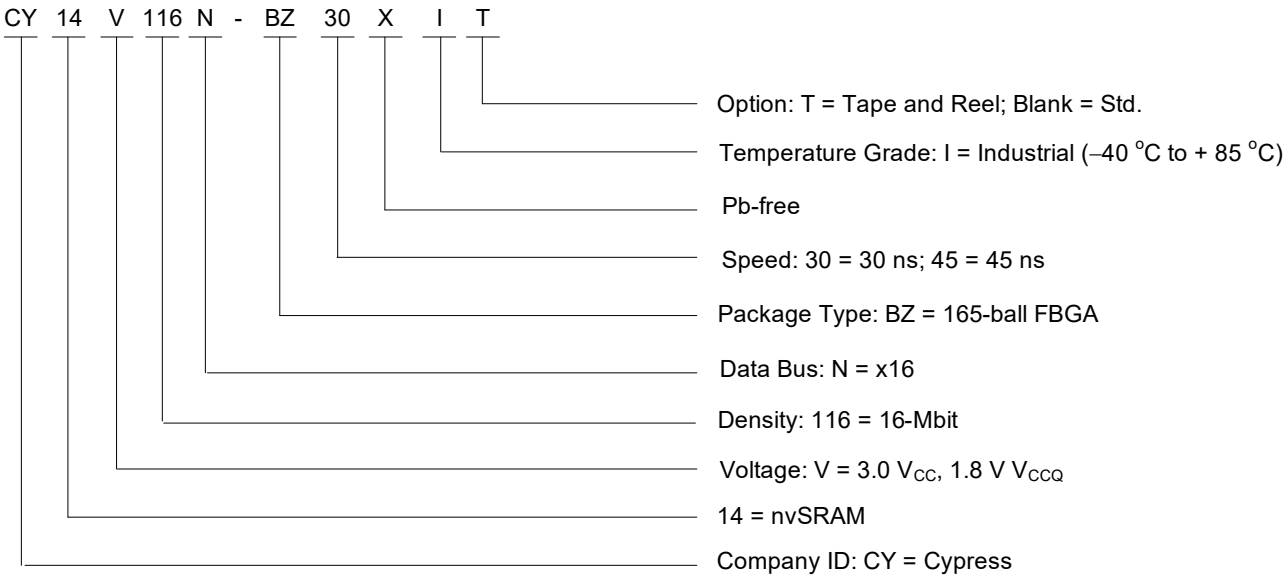
$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs and Outputs	Mode	Power
H	X	X	X	X	X	High-Z	Deselect/Power-down	Standby
X	L	X	X	X	X	High-Z	Deselect/Power-down	Standby
L	H	X	X	H	H	High-Z	Output disabled	Active
L	H	H	L	L	L	Data out (DQ_0–DQ_{15})	Read	Active
L	H	H	L	H	L	Data out (DQ_0–DQ_7); DQ_8–DQ_{15} in High-Z	Read	Active
L	H	H	L	L	H	Data out (DQ_8–DQ_{15}); DQ_0–DQ_7 in High-Z	Read	Active
L	H	H	H	X	X	High-Z	Output disabled	Active
L	H	L	X	L	L	Data in (DQ_0–DQ_{15})	Write	Active
L	H	L	X	H	L	Data in (DQ_0–DQ_7); DQ_8–DQ_{15} in High-Z	Write	Active
L	H	L	X	L	H	Data in (DQ_8–DQ_{15}); DQ_0–DQ_7 in High-Z	Write	Active

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
30	CY14V116N-BZ30XI	51-85195	165-ball FBGA	Industrial
	CY14V116N-BZ30XIT			

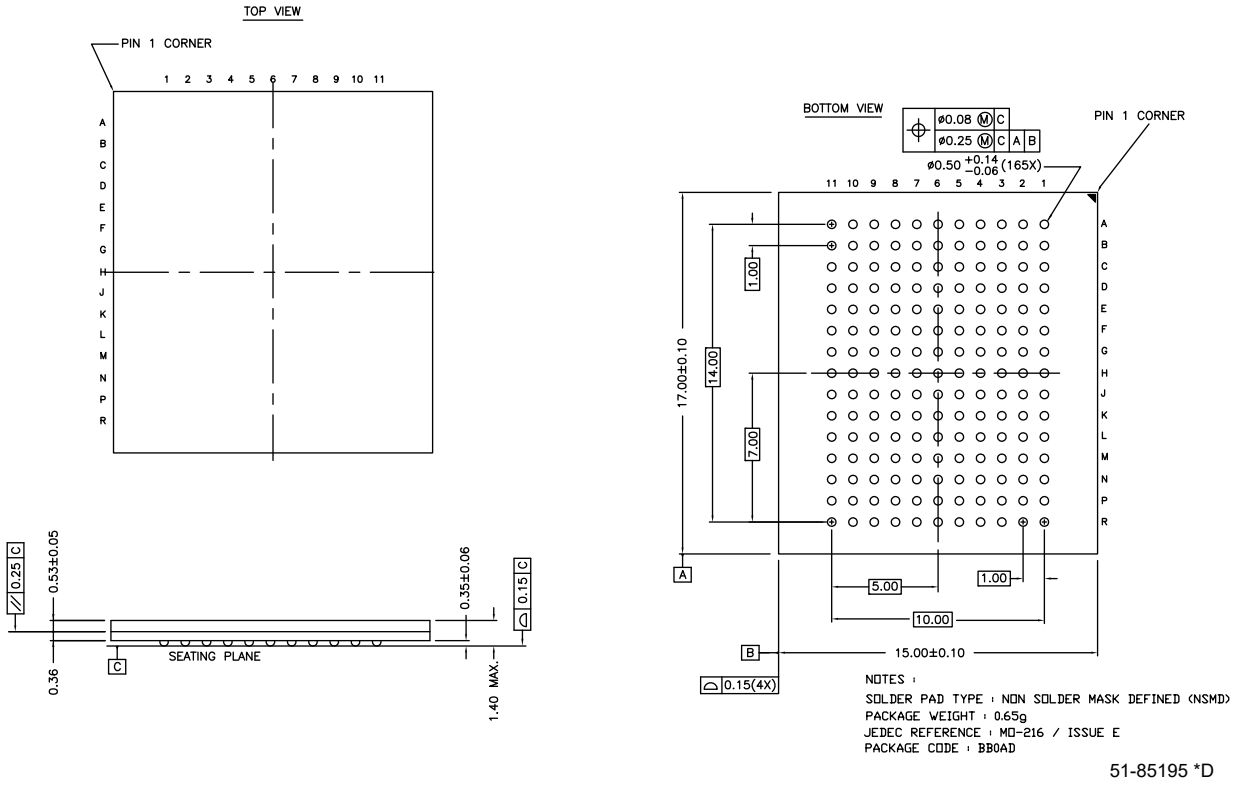
All parts are Pb-free. Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagram

Figure 16. 165-ball FBGA (15 mm × 17 mm × 1.40 mm) Package Outline, 51-85195



Acronyms

Table 2. Acronyms Used in this Document

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
EIA	Electronic Industries Alliance
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
JESD	JEDEC Standards
nvSRAM	nonvolatile Static Random Access Memory
RoHS	Restriction of Hazardous Substances
RWI	Read and Write Inhibited

Document Conventions

Units of Measure

Table 3. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
Kbit	kilobit
kHz	kilohertz
kΩ	kiloohm
µA	microampere
mA	milliampere
µF	microfarad
Mbit	megabit
MHz	megahertz
µs	microsecond
ms	millisecond
ns	nanosecond
pF	picofarad
V	volt
Ω	ohm
W	watt

Document History Page

Document Title: CY14V116N, 16-Mbit (1024K × 16) nvSRAM Document Number: 001-75791			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
**	3516347	02/03/2011	New data sheet.
*A	3733467	09/14/2012	Updated Device Operation: Updated Sleep Mode: Added Figure 3. Updated Maximum Ratings: Removed “Ambient temperature with power applied” and its details. Added “Maximum junction temperature” and its details. Updated DC Electrical Characteristics: Added V_{VCAP} parameter and its details. Added Note 9 and referred the same note in V_{VCAP} parameter. Updated Capacitance: Changed maximum value of C_{IN} and C_{OUT} parameters from 7 pF to 11.5 pF. Added Sleep Mode Characteristics.
*B	3944873	03/26/2013	Removed CY14W116N, CY14W116S, CY14V116S part related information in all instances across the document. Removed “V_{CC} = 2.375 V to 2.625 V” operating range related information in all instances across the document. Removed 25 ns speed bin related information in all instances across the document. Added 30 ns speed bin related information in all instances across the document. Removed × 32 Configuration related information in all instances across the document. Updated Features: Replaced “I/O V_{CCQ} = 1.65 V to V_{CC}” with “I/O V_{CCQ} = 1.65 V to 1.95 V”. Updated DC Electrical Characteristics: Updated details corresponding to V_{IH}, V_{IL}, V_{OL}, V_{OH} parameters. Updated Capacitance (Changed maximum value of C_{IN} and C_{OUT} parameters from 11.5 pF to 8 pF). Updated AC Test Loads and Waveforms: Updated Figure 4.
*C	4260504	01/24/2014	Updated Logic Block Diagram (for more clarity). Updated Device Operation: Updated AutoStore Operation (Power-Down): Updated description (Removed “The HSB signal is monitored by the system to detect if an AutoStore cycle is in progress.”). Updated Sleep Mode: Updated Figure 3 (for more clarity). Updated DC Electrical Characteristics: Splitted I_{SB} parameter to two rows. Updated details in “Test Conditions” column corresponding to I_{SB} parameter (Added “t_{RC} = 30 ns” and “t_{RC} = 45 ns”). Retained the existing values of I_{SB} parameter for “t_{RC} = 30 ns”. Added values of I_{SB} parameter for “t_{RC} = 45 ns”. Updated Note 8. Changed minimum value of V_{CAP} parameter from 20 µF to 19.8 µF. Updated AC Switching Characteristics: Updated Note 17. Updated AutoStore/Power-Up RECALL Characteristics: Updated Figure 10 (for more clarity). Updated Sleep Mode Characteristics: Changed maximum value of t_{ZZH} parameter from 20 ns to 70 ns. Updated Figure 11 (for more clarity). Completing Sunset Review.
*D	4417851	06/24/2014	Updated DC Electrical Characteristics: Added Note 7 and referred the same note in I_{CC4} parameter. Updated maximum value of V_{VCAP} parameter from 4.5 V to 5.0 V. Updated Capacitance: Updated maximum value of C_{IN} and C_{OUT} parameters from 8 pF to 10 pF. Added C_{IO} parameter and its details. Updated Thermal Resistance: Changed value of Θ_{JA} parameter from 22.0 °C/W to 15.6 °C/W corresponding to “165-ball FBGA” package. Changed value of Θ_{JC} parameter from 15.28 °C/W to 2.9 °C/W corresponding to “165-ball FBGA” package.

Document History Page (continued)

Document Title: CY14V116N, 16-Mbit (1024K × 16) nvSRAM Document Number: 001-75791			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
*E	4432183	07/07/2014	Updated DC Electrical Characteristics: Changed maximum value of V_{CAP} parameter from 120.0 µF to 82.0 µF.
*F	4456803	07/31/2014	No technical updates.
*G	4571551	11/17/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*H	4616093	01/07/2015	Changed status from Preliminary to Final. Completing Sunset Review.
*I	6093693	03/09/2018	Updated Package Diagram: spec 51-85195 – Changed revision from *C to *D. Updated to new template.
*J	6681289	09/24/2019	Updated Sales page and Copyright information. Updated Ordering Information: Removed CY14V116N-BZ45XI part number. Added CY14V116N-BZ30XIT part number.

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