LTC6900

# Low Power, 1kHz to 20MHz Resistor Set SOT-23 Oscillator

## FEATURES

- **One External Resistor Sets the Frequency**
- **1kHz to 20MHz Frequency Range**
- **500µA Typical Supply Current, $V_S$ = 3V, 3MHz**
- Frequency Error ≤1.5% Max, 5kHz to 10MHz ($T_A$ = 25°C)
- Frequency Error ≤2% Max, 5kHz to 10MHz ($T_A$ = 0°C to 70°C)
- ±40ppm/°C Temperature Stability
- 0.04%/V Supply Stability
- 50% ±1% Duty Cycle 1kHz to 2MHz
- 50% ±5% Duty Cycle 2MHz to 10MHz
- Fast Start-Up Time: 50µs to 1.5ms
- 100Ω CMOS Output Driver
- Operates from a Single 2.7V to 5.5V Supply
- Low Profile (1mm) ThinSOT™ Package

## APPLICATIONS

- Portable and Battery-Powered Equipment
- PDAs
- Cell Phones
- Low Cost Precision Oscillator
- Charge Pump Driver
- Switching Power Supply Clock Reference
- Clocking Switched Capacitor Filters
- Fixed Crystal Oscillator Replacement
- Ceramic Oscillator Replacement

## DESCRIPTION

The LTC®6900 is a precision, low power oscillator that is easy to use and occupies very little PC board space. The oscillator frequency is programmed by a single external resistor ($R_{SET}$). The LTC6900 has been designed for high accuracy operation (≤1.5% frequency error) without the need for external trim components.

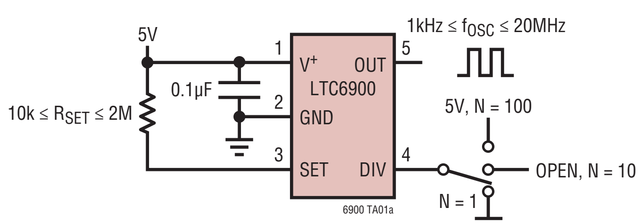
The LTC6900 operates with a single 2.7V to 5.5V power supply and provides a rail-to-rail, 50% duty cycle square wave output. The CMOS output driver ensures fast rise/fall times and rail-to-rail switching. The frequency-setting resistor can vary from 10kΩ to 2MΩ to select a master oscillator frequency between 100kHz and 20MHz (5V supply). The three-state DIV input determines whether the master clock is divided by 1, 10 or 100 before driving the output, providing three frequency ranges spanning 1kHz to 20MHz (5V supply). The LTC6900 features a proprietary feedback loop that linearizes the relationship between $R_{SET}$ and frequency, eliminating the need for tables to calculate frequency. The oscillator can be easily programmed using the simple formula outlined below:

$$f_{OSC} = 10\text{MHz} \bullet \left(\frac{20k}{N \bullet R_{SET}}\right), \quad N = \begin{cases} 100, & \text{DIV Pin} = V^+ \\ 10, & \text{DIV Pin} = \text{Open} \\ 1, & \text{DIV Pin} = \text{GND} \end{cases}$$



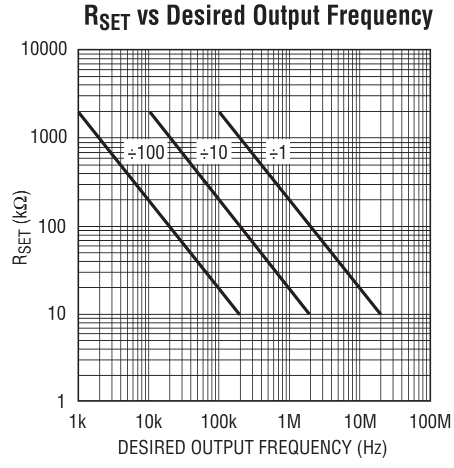
## TYPICAL APPLICATION

**Clock Generator**




$$f_{OSC} = 10\text{MHz} \bullet \left(\frac{20k}{N \bullet R_{SET}}\right)$$

**$R_{SET}$ vs Desired Output Frequency**

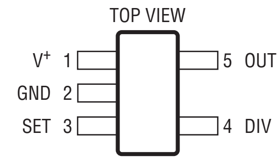


## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

Supply Voltage ($V^+$) to GND ........................ −0.3V to 6V
DIV to GND .................................. −0.3V to ($V^+$ + 0.3V)
SET to GND .................................. −0.3V to ($V^+$ + 0.3V)
Operating Temperature Range (Note 8)
  LTC6900C ........................................... −40°C to 85°C
  LTC6900I ............................................ −40°C to 85°C
Storage Temperature Range .................. −65°C to 150°C
Lead Temperature (Soldering, 10 sec) .................. 300°C

## PIN CONFIGURATION




S5 PACKAGE
5-LEAD PLASTIC TSOT-23
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 256°C/W

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC6900CS5#PBF | LTC6900CS5#TRPBF | LTZM | 5-Lead Plastic TSOT-23 | –40°C to 85°C |
| LTC6900IS5#PBF | LTC6900IS5#TRPBF | LTZM | 5-Lead Plastic TSOT-23 | –40°C to 85°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V^+$ = 2.7V to 5.5V, $R_L$= 5k, $C_L$ = 5pF, Pin 4 = $V^+$ unless otherwise noted. All voltages are with respect to GND.**

| SYMBOL | PARAMETER | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| $\Delta f$ | Frequency Accuracy (Notes 2, 3) | $V^+$ = 5V | 5kHz ≤ f ≤ 10MHz | | | ±0.5 | ±1.5 | % |
| | | | 5kHz ≤ f ≤ 10MHz, LTC6900C | ● | | | ±2.0 | % |
| | | | 5kHz ≤ f ≤ 10MHz, LTC6900I | ● | | | ±2.5 | % |
| | | | 1kHz ≤ f < 5kHz | | | ±2 | | % |
| | | | 10MHz < f ≤ 20MHz | | | ±2 | | % |
| | | $V^+$ = 3V | 5kHz ≤ f ≤ 10MHz | | | ±0.5 | ±1.5 | % |
| | | | 5kHz ≤ f ≤ 10MHz, LTC6900C | ● | | | ±2.0 | % |
| | | | 5kHz ≤ f ≤ 10MHz, LTC6900I | ● | | | ±2.5 | % |
| | | | 1kHz ≤ f < 5kHz | | | ±2 | | % |
| $R_{SET}$ | Frequency-Setting Resistor Range | $\|\Delta f\|$ < 1.5% | $V^+$ = 5V | | 20 | | 400 | kΩ |
| | | | $V^+$ = 3V | | 20 | | 400 | kΩ |
| $\Delta f/\Delta T$ | Frequency Drift Overtemperature (Note 3) | $R_{SET}$ = 63.2k | | ● | | ±0.004 | | %/°C |
| $\Delta f/\Delta V$ | Frequency Drift Over Supply (Note 3) | $V^+$ = 3V to 5V, $R_{SET}$ = 63.2k | | ● | | 0.04 | 0.1 | %/V |
| | Timing Jitter (Note 4) | Pin 4 = $V^+$, 20k ≤ $R_{SET}$ ≤ 400k | | | | 0.1 | | % |
| | | Pin 4 = Open, 20k ≤ $R_{SET}$ ≤ 400k | | | | 0.2 | | % |
| | | Pin 4 = 0V, 20k ≤ $R_{SET}$ ≤ 400k | | | | 0.6 | | % |
| | Long-Term Stability of Output Frequency | | | | | 300 | | ppm/$\sqrt{kHr}$ |
| | Duty Cycle (Note 7) | Pin 4 = $V^+$ or Open (DIV Either by 100 or 10) | | ● | 49 | 50 | 51 | % |
| | | Pin 4 = 0V (DIV by 1), $R_{SET}$ = 20k to 400k | | ● | 45 | 50 | 55 | % |

6900fa

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V^+$ = 2.7V to 5.5V, $R_L$= 5k, $C_L$ = 5pF, Pin 4 = $V^+$ unless otherwise noted. All voltages are with respect to GND.**

| SYMBOL | PARAMETER | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| $V^+$ | Operating Supply Range | | | ● | 2.7 | | 5.5 | V |
| $I_S$ | Power Supply Current | $R_{SET}$ = 400k, Pin 4 = $V^+$, $R_L = \infty$ | $V^+$ = 5V | ● | | 0.32 | 0.42 | mA |
| | | $f_{OSC}$ = 5kHz | $V^+$ = 3V | ● | | 0.29 | 0.38 | mA |
| | | $R_{SET}$ = 20k, Pin 4 = 0V, $R_L = \infty$ | $V^+$ = 5V | ● | | 0.92 | 1.20 | mA |
| | | $f_{OSC}$ = 10MHz | $V^+$ = 3V | ● | | 0.68 | 0.86 | mA |
| $V_{IH}$ | High Level DIV Input Voltage | | | ● | $V^+ - 0.4$ | | | V |
| $V_{IL}$ | Low Level DIV Input Voltage | | | ● | | | 0.5 | V |
| $I_{DIV}$ | DIV Input Current (Note 5) | Pin 4 = $V^+$ | $V^+$ = 5V | ● | | 2 | 4 | μA |
| | | Pin 4 = 0V | $V^+$ = 5V | ● | –4 | –2 | | μA |
| $V_{OH}$ | High Level Output Voltage (Note 5) | $V^+$ = 5V | $I_{OH}$ = –1mA | ● | 4.8 | 4.95 | | V |
| | | | $I_{OH}$ = –4mA | ● | 4.5 | 4.8 | | V |
| | | $V^+$ = 3V | $I_{OH}$ = –1mA | ● | 2.7 | 2.9 | | V |
| | | | $I_{OH}$ = –4mA | ● | 2.2 | 2.6 | | V |
| $V_{OL}$ | Low Level Output Voltage (Note 5) | $V^+$ = 5V | $I_{OL}$ = 1mA | ● | | 0.05 | 0.15 | V |
| | | | $I_{OL}$ = 4mA | ● | | 0.2 | 0.4 | V |
| | | $V^+$ = 3V | $I_{OL}$ = 1mA | ● | | 0.1 | 0.3 | V |
| | | | $I_{OL}$ = 4mA | ● | | 0.4 | 0.7 | V |
| $t_r$ | OUT Rise Time (Note 6) | $V^+$ = 5V | Pin 4 = $V^+$ or Floating, $R_L = \infty$ | | | 14 | | ns |
| | | | Pin 4 = 0V, $R_L = \infty$ | | | 7 | | ns |
| | | $V^+$ = 3V | Pin 4 = $V^+$ or Floating, $R_L = \infty$ | | | 19 | | ns |
| | | | Pin 4 = 0V, $R_L = \infty$ | | | 11 | | ns |
| $t_f$ | OUT Fall Time (Note 6) | $V^+$ = 5V | Pin 4 = $V^+$ or Floating, $R_L = \infty$ | | | 13 | | ns |
| | | | Pin 4 = 0V, $R_L = \infty$ | | | 6 | | ns |
| | | $V^+$ = 3V | Pin 4 = $V^+$ or Floating, $R_L = \infty$ | | | 19 | | ns |
| | | | Pin 4 = 0V, $R_L = \infty$ | | | 10 | | ns |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Frequencies near 100kHz and 1MHz may be generated using two different values of $R_{SET}$ (see the Selecting the Divider Setting Resistor paragraph in the Applications Information section). For these frequencies, the error is specified under the following assumption: 20k < $R_{SET}$ ≤ 200k.

**Note 3:** Frequency accuracy is defined as the deviation from the $f_{OSC}$ equation.

**Note 4:** Jitter is the ratio of the peak-to-peak distribution of the period to the mean of the period. This specification is based on characterization and is not 100% tested. Also, see the Peak-to-Peak Jitter vs Output Frequency curve in the Typical Performance Characteristics section.

**Note 5:** To conform with the Logic IC Standard convention, current out of a pin is arbitrarily given as a negative value.

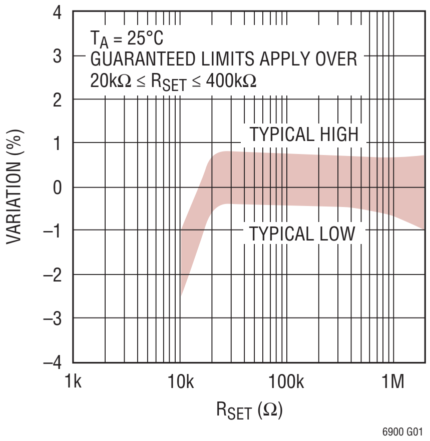
**Note 6:** Output rise and fall times are measured between the 10% and 90% power supply levels. These specifications are based on characterization.

**Note 7:** Guaranteed by 5V test.

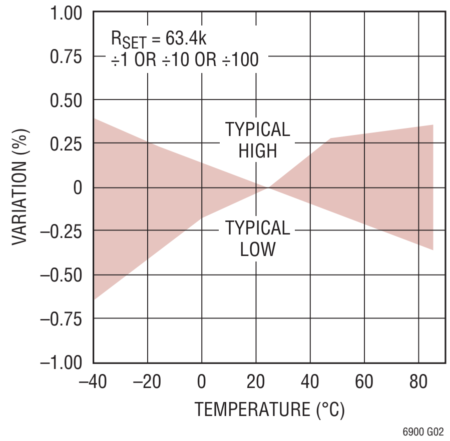
**Note 8:** The LTC6900C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6900C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LTC6900I is guaranteed to meet specified performance from –40°C to 85°C.

## TYPICAL PERFORMANCE CHARACTERISTICS

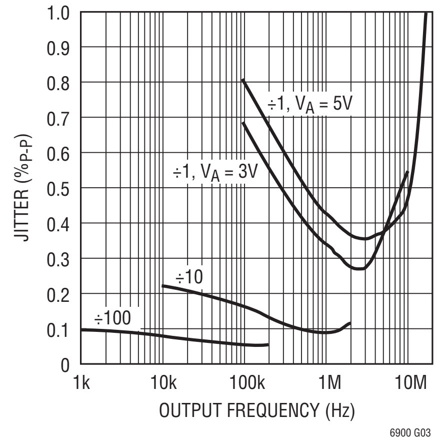
### Frequency Variation vs $R_{SET}$



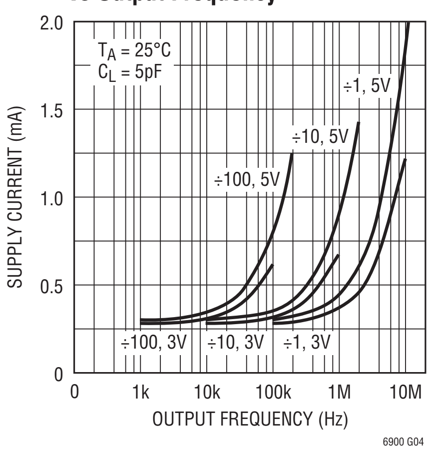

### Frequency Variation Over Temperature



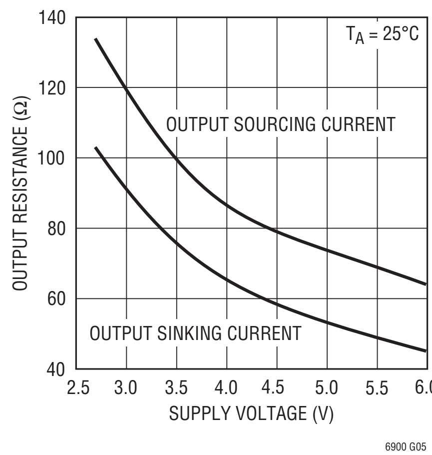

### Peak-to-Peak Jitter vs Output Frequency



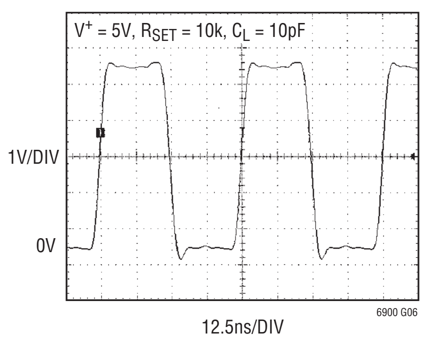

### Supply Current vs Output Frequency



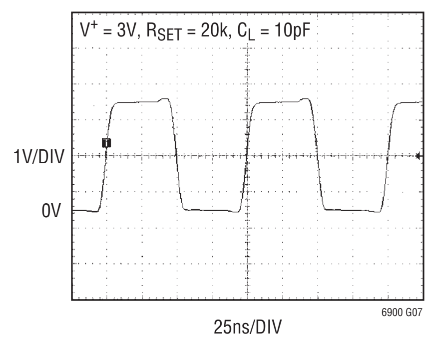

### Output Resistance vs Supply Voltage




### LTC6900 Output Operating at 20MHz, $V_S$ = 5V




### LTC6900 Output Operating at 10MHz, $V_S$ = 3V



## PIN FUNCTIONS

**V⁺ (Pin 1):** Voltage Supply (2.7V ≤ V⁺ ≤ 5.5V). This supply must be kept free from noise and ripple. It should be bypassed directly to a ground plane with a 0.1μF capacitor.

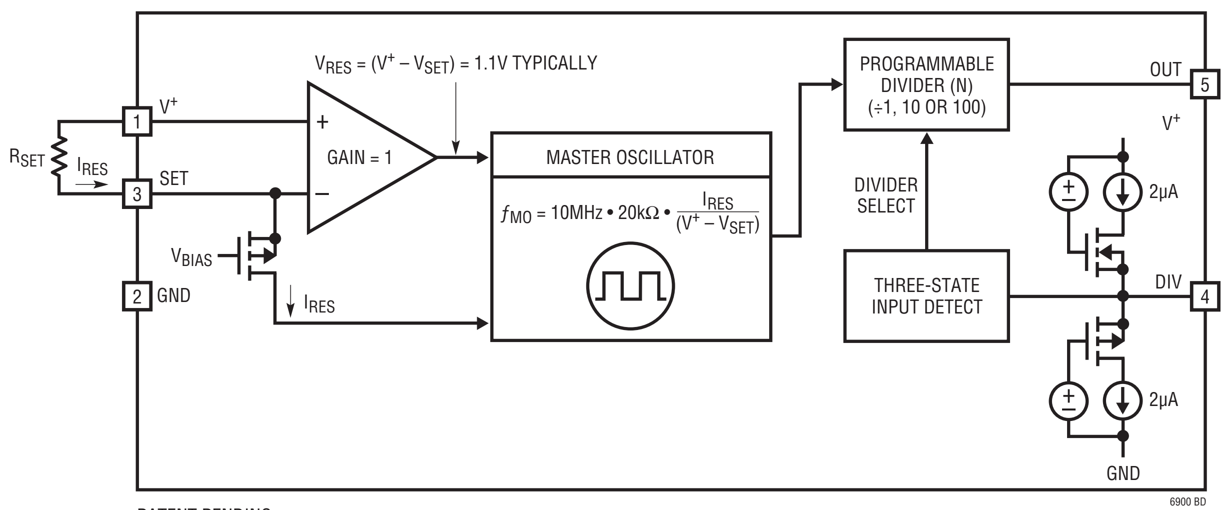
**GND (Pin 2):** Ground. Should be tied to a ground plane for best performance.

**SET (Pin 3):** Frequency-Setting Resistor Input. The value of the resistor connected between this pin and V⁺ determines the oscillator frequency. The voltage on this pin is held by the LTC6900 to approximately 1.1V below the V⁺ voltage. For best performance, use a precision metal film resistor with a value between 10kΩ and 2MΩ and limit the capacitance on this pin to less than 10pF.

**DIV (Pin 4):** Divider-Setting Input. This three-state input selects among three divider settings, determining the value of N in the frequency equation. Pin 4 should be tied to GND for the ÷1 setting, the highest frequency range. Floating Pin 4 divides the master oscillator by 10. Pin 4 should be tied to V⁺ for the ÷100 setting, the lowest frequency range. To detect a floating DIV pin, the LTC6900 attempts to pull the pin toward midsupply. Therefore, driving the DIV pin high requires sourcing approximately 2μA. Likewise, driving DIV low requires sinking 2μA. When Pin 4 is floated, it should preferably be bypassed by a 1nF capacitor to ground or it should be surrounded by a ground shield to prevent excessive coupling from other PCB traces.

**OUT (Pin 5):** Oscillator Output. This pin can drive 5kΩ and/or 10pF loads. Heavier loads may cause inaccuracies due to supply bounce at high frequencies. Voltage transients, coupled into Pin 5, above or below the LTC6900 power supplies will not cause latchup if the current into/out of the OUT pin is limited to 50mA.

## BLOCK DIAGRAM




PATENT PENDING

## OPERATION

As shown in the Block Diagram, the LTC6900's master oscillator is controlled by the ratio of the voltage between the $V^+$ and SET pins and the current ($I_{RES}$) is entering the SET pin. The voltage on the SET pin is forced to approximately 1.1V below $V^+$ by the PMOS transistor and its gate bias voltage. This voltage is accurate to ±8% at a particular input current and supply voltage (see Figure 1).

A resistor $R_{SET}$, connected between the $V^+$ and SET pins, "locks together" the voltage ($V^+ – V_{SET}$) and current, $I_{RES}$, variation. This provides the LTC6900's high precision. The master oscillation frequency reduces to:

$$f_{MO} = 10\text{MHz} \bullet \left( \frac{20k\Omega}{R_{SET}} \right)$$

The LTC6900 is optimized for use with resistors between 10k and 2M, corresponding to master oscillator frequencies between 100kHz and 20MHz.

To extend the output frequency range, the master oscillator signal may be divided by 1, 10 or 100 before driving OUT (Pin 5). The divide-by value is determined by the state of the DIV input (Pin 4). Tie DIV to GND or drive it below 0.5V to select ÷1. This is the highest frequency range, with the master output frequency passed directly to OUT. The DIV pin may be floated or driven to midsupply to select ÷10, the intermediate frequency range. The lowest frequency range, ÷100, is selected by tying DIV to $V^+$ or driving it to within 0.4V of $V^+$. Figure 2 shows the relationship between $R_{SET}$, divider setting and output frequency, including the overlapping frequency ranges near 100kHz and 1MHz.

The CMOS output driver has an on resistance that is typically less than 100Ω. In the ÷1 (high frequency) mode, the rise and fall times are typically 7ns with a 5V supply and 11ns with a 3V supply. These times maintain a clean square wave at 10MHz (20MHz at 5V supply). In the ÷10 and ÷100 modes, where the output frequency is much lower, slew rate control circuitry in the output driver increases the rise/fall times to typically 14ns for a 5V supply and 19ns for a 3V supply. The reduced slew rate lowers EMI (electromagnetic interference) and supply bounce.

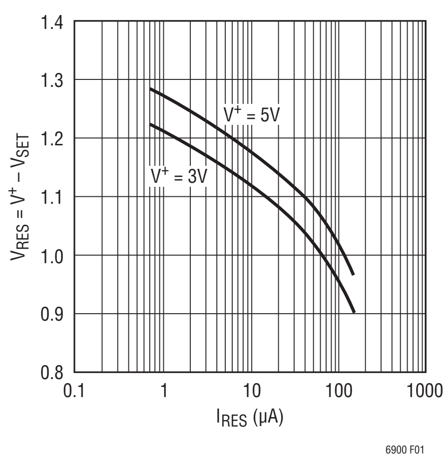



**Figure 1. $V^+ – V_{SET}$ Variation with $I_{RES}$**

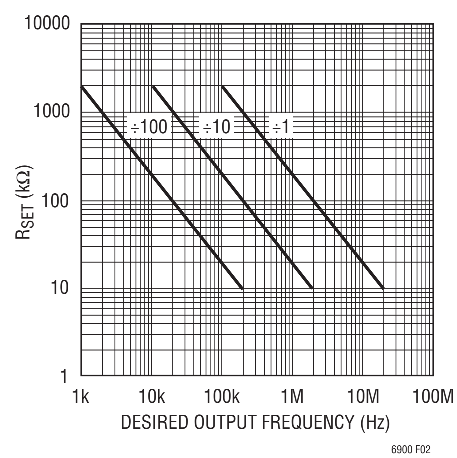



**Figure 2. $R_{SET}$ vs Desired Output Frequency**

# APPLICATIONS INFORMATION

## SELECTING THE DIVIDER SETTING AND RESISTOR

The LTC6900's master oscillator has a frequency range spanning 0.1MHz to 20MHz. However, accuracy may suffer if the master oscillator is operated at greater than 10MHz with a supply voltage lower than 4V. A programmable divider extends the frequency range to greater than three decades. Table 1 describes the recommended frequencies for each divider setting. Note that the ranges overlap; at some frequencies there are two divider/resistor combinations that result in the desired frequency.

In general, any given oscillator frequency ($f_{OSC}$) should be obtained using the lowest master oscillator frequency. Lower master oscillator frequencies use less power and are more accurate. For instance, $f_{OSC}$ = 100kHz can be obtained by either $R_{SET}$ = 20k, N = 100, master oscillator = 10MHz or $R_{SET}$ = 200k, N = 10, master oscillator = 1MHz. The $R_{SET}$ = 200k approach is preferred for lower power and better accuracy.

**Table 1. Frequency Range vs Divider Setting**

| DIVIDER SETTING | FREQUENCY RANGE |
|---|---|
| ÷1 ⇒ DIV (Pin 4) = GND | > 500kHz* |
| ÷10 ⇒ DIV (Pin 4) = Floating | 50kHz to 1MHz |
| ÷100 ⇒ DIV (Pin 4) = V+ | < 100kHz |

*At master oscillator frequencies greater than 10MHz ($R_{SET} < 20k\Omega$), the LTC6900 may experience reduced accuracy with a supply voltage less than 4V.

After choosing the proper divider setting, determine the correct frequency-setting resistor. Because of the linear correspondence between oscillation period and resistance, a simple equation relates resistance with frequency.

$$R_{SET} = 20k \bullet \left(\frac{10MHz}{N \bullet f_{OSC}}\right), N = \begin{cases} 100 \\ 10 \\ 1 \end{cases}$$

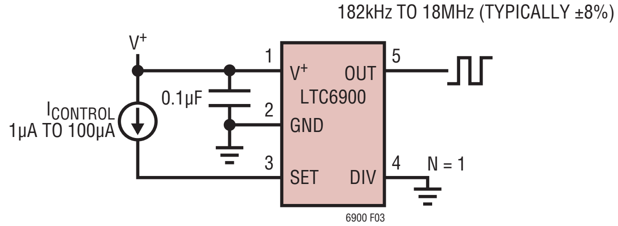
$(R_{SETMIN} = 10k, R_{SETMAX} = 2M)$

Any resistor, $R_{SET}$, tolerance adds to the inaccuracy of the oscillator, $f_{OSC}$.

## ALTERNATIVE METHODS OF SETTING THE OUTPUT FREQUENCY OF THE LTC6900

The oscillator may be programmed by any method that sources a current into the SET pin (Pin 3). The circuit in Figure 3 sets the oscillator frequency using a programmable current source and in the expression for $f_{OSC}$, the resistor $R_{SET}$ is replaced by the ratio of $1.1V/I_{CONTROL}$. As already explained in the Operation section, the voltage difference between $V^+$ and SET is approximately 1.1V, therefore, the Figure 3 circuit is less accurate than if a resistor controls the oscillator frequency.

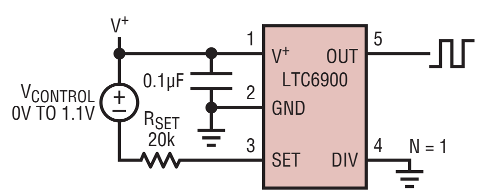
Figure 4 shows the LTC6900 configured as a VCO. A voltage source is connected in series with an external 20k resistor. The output frequency, $f_{OSC}$, will vary with $V_{CONTROL}$, that is the voltage source connected between $V^+$ and the SET pin. Again, this circuit decouples the relationship between the input current and the voltage between $V^+$ and SET; the frequency accuracy will be degraded. The oscillator frequency, however, will monotonically increase with decreasing $V_{CONTROL}$.




$$f_{OSC} \cong \frac{10MHz}{N} \bullet \frac{20k\Omega}{1.1V} \bullet I_{CONTROL}$$

$I_{CONTROL}$ EXPRESSED IN (A)

**Figure 3. Current Controlled Oscillator**




$$f_{OSC} \cong \frac{10MHz}{N} \bullet \frac{20k}{R_{SET}} \bullet \left(1 - \frac{V_{CONTROL}}{1.1V}\right)$$

TYPICAL $f_{OSC}$ ACCURACY
±0.5%, $V_{CONTROL}$ = 0V
±8%, $V_{CONTROL}$ = 0.5V

**Figure 4. Voltage Controlled Oscillator**

# APPLICATIONS INFORMATION

## POWER SUPPLY REJECTION

### Low Frequency Supply Rejection (Voltage Coefficient)

Figure 5 shows the output frequency sensitivity to power supply voltage at several different temperatures. The LTC6900 has a guaranteed voltage coefficient of 0.1%/V but, as Figure 5 shows, the typical supply sensitivity is twice as low.

### High Frequency Power Supply Rejection

The accuracy of the LTC6900 may be affected when its power supply generates significant noise with a frequency content in the vicinity of the programmed value of $f_{OSC}$. If a switching power supply is used to power the LTC6900, and if the ripple of the power supply is more than 20mV, make sure the switching frequency and its harmonics are not related to the output frequency of the LTC6900. Otherwise, the oscillator may show additional frequency error.

If the LTC6900 is powered by a switching regulator and the switching frequency or its harmonics coincide with the output frequency of the LTC6900, the jitter of the oscillator output may be affected. This phenomenon will become noticeable if the switching regulator exhibits ripples beyond 30mV.

## START-UP TIME

The start-up time and settling time to within 1% of the final value can be estimated by $t_{START} \cong R_{SET}(3.7\mu s/k\Omega) + 10\mu s$. Note the start-up time depends on $R_{SET}$ and it is independent from the setting of the divider pin. For instance with $R_{SET}$ = 100k, the LTC6900 will settle with 1% of its 200kHz final value (N = 10) in approximately 380µs. Figure 6 shows start-up times for various $R_{SET}$ resistors.

Figure 7 shows an application where a second set resistor $R_{SET2}$ is connected in parallel with set resistor $R_{SET1}$ via switch S1. When switch S1 is open, the output frequency of the LTC6900 depends on the value of the resistor $R_{SET1}$. When switch S1 is closed, the output frequency of the LTC6900 depends on the value of the parallel combination of $R_{SET1}$ and $R_{SET2}$.

The start-up time and settling time of the LTC6900 with switch S1 open (or closed) is described by $t_{START}$ shown above. Once the LTC6900 starts and settles, and switch S1 closes (or opens), the LTC6900 will settle to its new output frequency within approximately 70µs.

### Jitter

The Peak-to-Peak Jitter vs Output Frequency graph, in the Typical Performance Characteristics section, shows the typical clock jitter as a function of oscillator frequency and power supply voltage. The capacitance from the SET pin, (Pin 3), to ground must be less than 10pF. If this requirement is not met, the jitter will increase.

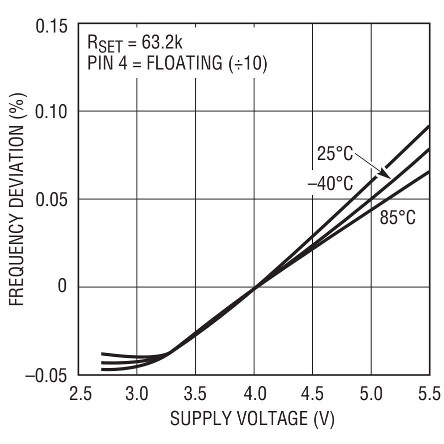



**Figure 5. Supply Sensitivity**

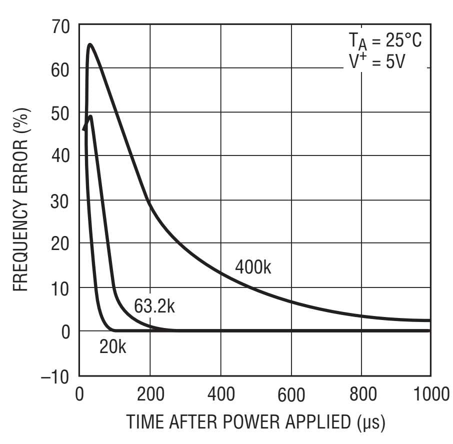



**Figure 6. Start-Up Time**

## APPLICATIONS INFORMATION

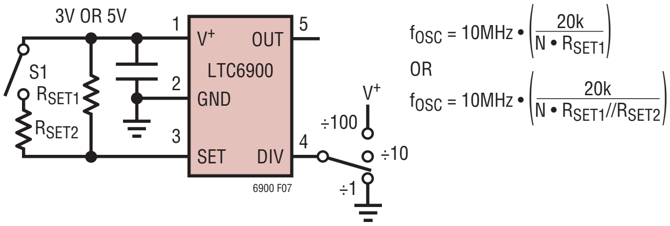



**Figure 7**

### A Ground Referenced Voltage Controlled Oscillator

The LTC6900 output frequency can also be programmed by steering current in or out of the SET pin, as conceptually shown in Figure 8. This technique can degrade accuracy as the ratio of $(V^+ - V_{SET}) / I_{RES}$ is no longer uniquely dependent of the value of $R_{SET}$, as shown in the LTC6900 Block Diagram. This loss of accuracy will become noticeable when the magnitude of $I_{PROG}$ is comparable to $I_{RES}$. The frequency variation of the LTC6900 is still monotonic.

Figure 9 shows how to implement the concept shown in Figure 8 by connecting a second resistor, $R_{IN}$, between the SET pin and a ground referenced voltage source, $V_{IN}$.

For a given power supply voltage in Figure 9, the output frequency of the LTC6900 is a function of $V_{IN}$, $R_{IN}$, $R_{SET}$ and $(V^+ - V_{SET}) = V_{RES}$:

$$f_{OSC} = \frac{10\text{MHz}}{N} \cdot \frac{20k}{R_{IN} \| R_{SET}} \cdot \left[1 + \frac{\left(V_{IN} - V^+\right)}{V_{RES}} \cdot \left(\frac{1}{1 + \frac{R_{IN}}{R_{SET}}}\right)\right] \quad (1)$$

When $V_{IN} = V^+$, the output frequency of the LTC6900 assumes the highest value and it is set by the parallel combination of $R_{IN}$ and $R_{SET}$. Also note, the output frequency, $f_{OSC}$, is independent of the value of $V_{RES} = (V^+ - V_{SET})$ so the accuracy of $f_{OSC}$ is within the data sheet limits.

When $V_{IN}$ is less than $V^+$, and expecially when $V_{IN}$ approaches the ground potential, the oscillator frequency, $f_{OSC}$, assumes its lowest value and its accuracy is affected by the change of $V_{RES} = (V^+ - V_{SET})$. At 25°C $V_{RES}$ varies by ±8%, assuming the variation of $V^+$ is ±5%. The temperature coefficient of $V_{RES}$ is 0.02%/°C.

By manipulating the algebraic relation for $f_{OSC}$ above, a simple algorithm can be derived to set the values of external resistors $R_{SET}$ and $R_{IN}$, as shown in Figure 9.

1. Choose the desired value of the maximum oscillator frequency, $f_{OSC(MAX)}$, occurring at maximum input voltage $V_{IN(MAX)} \le V^+$.
2. Set the desired value of the minimum oscillator frequency, $f_{OSC(MIN)}$, occurring at minimum input voltage $V_{IN(MIN)} \ge 0$.
3. Choose $V_{RES} = 1.1$ and calculate the ratio of $R_{IN}/R_{SET}$ from the following:

$$\frac{R_{IN}}{R_{SET}} = \frac{\left(V_{IN(MAX)} - V^+\right) - \left(\frac{f_{OSC(MAX)}}{f_{OSC(MIN)}}\right)\left(V_{IN(MIN)} - V^+\right)}{V_{RES}\left[\left(\frac{f_{OSC(MAX)}}{f_{OSC(MIN)}}\right) - 1\right]} - 1 \quad (2)$$

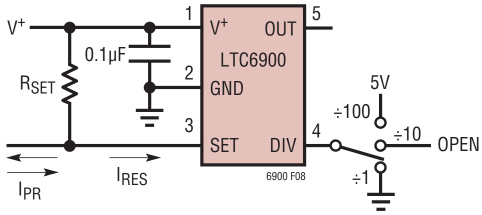



**Figure 8. Concept for Programming via Current Steering**

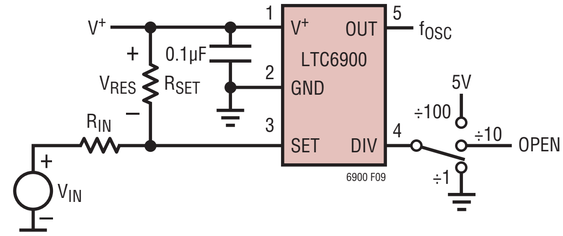



**Figure 9. Implementation of Concept Shown in Figure 8**

## APPLICATIONS INFORMATION

Once $R_{IN}/R_{SET}$ is known, calculate $R_{SET}$ from:

$$R_{SET} = \frac{10\text{MHz}}{N} \bullet \frac{20k}{f_{OSC(MAX)}} \bullet \left[ \frac{\left(V_{IN(MAX)} - V^{+}\right) + V_{RES}\left(1 + \frac{R_{IN}}{R_{SET}}\right)}{V_{RES}\left(\frac{R_{IN}}{R_{SET}}\right)} \right] \quad (3)$$

Example 1:

In this example, the oscillator output frequency has small excursions. This is useful where the frequency of a system should be tuned around some nominal value.

Let $V^+$ = 3V, $f_{OSC(MAX)}$ = 2MHz for $V_{IN(MAX)}$ = 3V and $f_{OSC(MIN)}$ = 1.5MHz for $V_{IN}$ = 0V. Solve for $R_{IN}/R_{SET}$ by Equation (2), yielding $R_{IN}/R_{SET}$ = 9.9/1. $R_{SET}$ = 110.1k by Equation (4). $R_{IN}$ = 9.9$R_{SET}$ = 1.089M. For standard resistor values, use $R_{SET}$ = 110k (1%) and $R_{IN}$ = 1.1M (1%). Figure 10 shows the measured $f_{OSC}$ vs $V_{IN}$. The 1.5MHz to 2MHz frequency excursion is quite limited, so the curve of $f_{OSC}$ vs $V_{IN}$ is linear.

Example 2:

Vary the oscillator frequency by one octave per volt. Assume $f_{OSC(MIN)}$ = 1MHz and $f_{OSC(MAX)}$ = 2MHz, when the input voltage varies by 1V. The minimum input voltage is half supply, that is $V_{IN(MIN)}$ = 1.5V, $V_{IN(MAX)}$ = 2.5V and $V^+$ = 3V.

Equation (2) yields $R_{IN}/R_{SET}$ = 1.273 and Equation (3) yields $R_{SET}$ = 142.8k. $R_{IN}$ = 1.273$R_{SET}$ = 181.8k. For standard resistor values, use $R_{SET}$ = 143k (1%) and $R_{IN}$ = 182k (1%). Figure 11 shows the measured $f_{OSC}$ vs $V_{IN}$. For $V_{IN}$ higher than 1.5V, the VCO is quite linear; nonlinearities occur when $V_{IN}$ becomes smaller than 1V, although the VCO remains monotonic.

### Maximum VCO Modulation Bandwidth

The maximum VCO modulation bandwidth is 25kHz; that is, the LTC6900 will respond to changes in $V_{IN}$ at a rate up to 25kHz. In lower frequency applications however, the modulation frequency may need to be limited to a lower rate to prevent an increase in output jitter. This lower limit is the master oscillator frequency divided by 20, ($f_{OSC}$/20). In general, for minimum output jitter the modulation frequency should be limited to $f_{OSC}$/20 or 25kHz, whichever is less. For best performance at all frequencies, the value for $f_{OSC}$ should be the master oscillator frequency (N = 1) when $V_{IN}$ is at the lowest level.

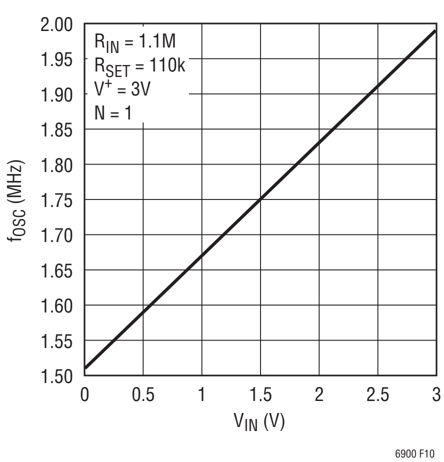



**Figure 10. Output Frequency vs Input Voltage**

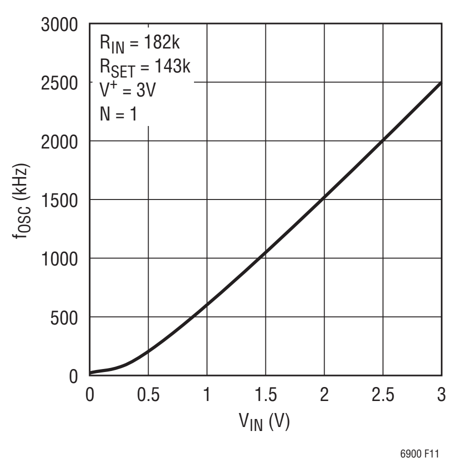



**Figure 11. Output Frequency vs Input Voltage**

## APPLICATIONS INFORMATION

Example 3:

$V^+ = 3V$, $f_{OSC(MAX)} = 5MHz$, $f_{OSC(MIN)} = 4MHz$, $N = 1$

$V_{IN(MAX)} = 2.5V$, $V_{IN(MIN)} = 0.5V$

$R_{IN}/R_{SET} = 8.5$, $R_{SET} = 43.2k$, $R_{IN} = 365k$

Maximum modulation bandwidth is the lesser of 25kHz or $f_{OSC(MIN)}/20$ (4MHz/20 = 200kHz)

Maximum $V_{IN}$ modulation frequency = 25kHz

Example 4:

$V^+ = 3V$, $f_{OSC(MAX)} = 400kHz$, $f_{OSC(MIN)} = 200kHz$, $N = 10$

$V_{IN(MAX)} = 2.5V$, $V_{IN(MIN)} = 0.5V$

$R_{IN}/R_{SET} = 3.1$, $R_{SET} = 59k$, $R_{IN} = 182k$

Maximum modulation bandwidth is the lesser of 25kHz or $f_{OSC(MIN)}/20$ calculated at N =1 (2MHz/20 = 100kHz)

Maximum $V_{IN}$ modulation frequency = 25kHz

**Table 2. Variation of $V_{RES}$ for Various Values of $R_{IN}$ || $R_{SET}$**

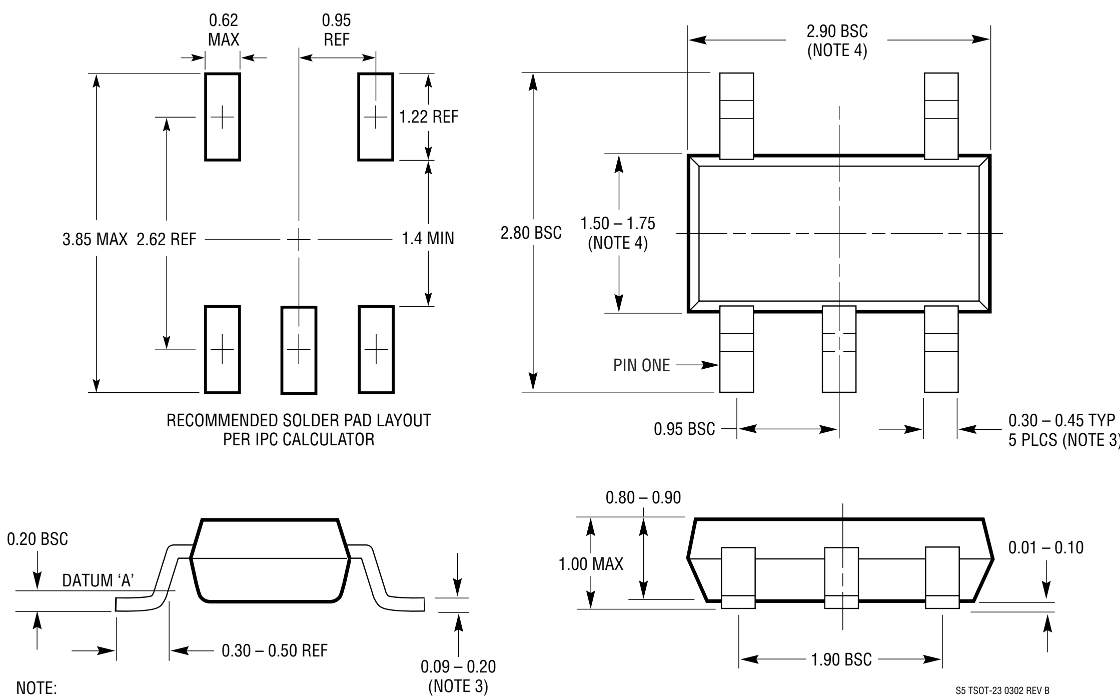
| $R_{IN}$ \|\| $R_{SET}$ ($V_{IN} = V^+$) | $V_{RES}$, $V^+ = 3V$ | $V_{RES}$, $V^+ = 5V$ |
|---|---|---|
| 20k | 0.98V | 1.03V |
| 40k | 1.03V | 1.08V |
| 80k | 1.07V | 1.12V |
| 160k | 1.1V | 1.15V |
| 320k | 1.12V | 1.17V |

$V_{RES}$ = Voltage across $R_{SET}$

**Note:** All of the calculations above assume $V_{RES} = 1.1V$, although $V_{RES} \approx 1.1V$. For completeness, Table 2 shows the variation of VRES against various parallel combinations of $R_{IN}$ and $R_{SET}$ ($V_{IN} = V^+$). Calulate first with $V_{RES} \approx 1.1V$, then use Table 2 to get a better approximation of $V_{RES}$, then recalculate the resistor values using the new value for $V_{RES}$.

## PACKAGE DESCRIPTION

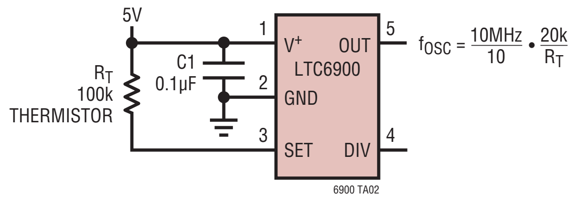
**S5 Package**
**5-Lead Plastic TSOT-23**
(Reference LTC DWG # 05-08-1635)




NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

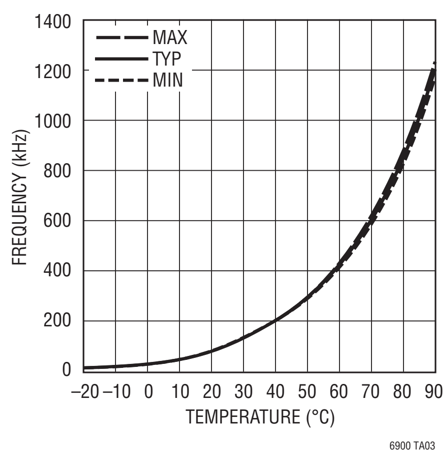
# TYPICAL APPLICATION

**Temperature-to-Frequency Converter**




$R_T$: YSI 44011 800 765-4974

**Output Frequency vs Temperature**




# RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1799 | 1kHz to 30MHz ThinSOT Oscillator | Identical Pinout, Higher Frequency Operation |

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