GaAs, pHEMT, MMIC, 1 W Power Amplifier, 0.1 GHz to 6 GHz

Data Sheet **HMC637ALP5E**

FEATURES

P1dB output power: 29 dBm
Gain: 13 dB
Output IP3: 44 dBm
50 Ω matched input/output
32-lead, 5 mm × 5 mm LFCSP package: 25 mm²

APPLICATIONS

Telecom infrastructure
Microwave radio
Very small aperture terminal (VSAT)
Military and space
Test instrumentation
Fiber optics

FUNCTIONAL BLOCK DIAGRAM

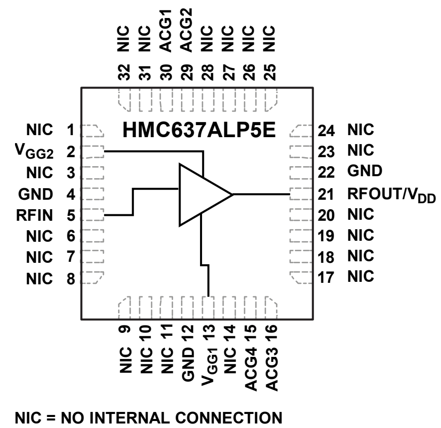

Figure 1.

GENERAL DESCRIPTION

The HMC637ALP5E is a gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), pseudomorphic high electron mobility transistor (pHEMT) distributed power amplifier which operates between 0.1 GHz and 6 GHz. The amplifier provides 13 dB of gain, 44 dBm output third-order intercept (IP3), and 29 dBm of output power at 1 dB gain compression while requiring 400 mA from a 12 V supply. Gain flatness is ±0.75 dB from 100 MHz to 6 GHz making the HMC637ALP5E ideal for electronic warfare (EW), electronic counter-measure (ECM), radar and test equipment applications. The HMC637ALP5E amplifier radio frequency (RF) I/Os are internally matched to 50 Ω, and the 5 mm × 5 mm lead frame chip scale package (LFCSP) is compatible with high volume surface-mount technology (SMT) assembly equipment.

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Technical Support **www.analog.com**

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REVISION HISTORY

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

4/2019—v02.0418 to Rev. C

Updated Format ... Universal
Changed HMC637ALP5 to HMC637ALP5E ... Throughout
Changes to Product Title, Features Section, Applications Section, General Description Section, and Figure 1 ... 1
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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_A = 25°C, drain bias voltage (V_{DD}) = 12 V, gate bias voltage (V_{GG2}) = 5 V, supply current (I_{DD}) = 400 mA (adjust V_{GG1} between −2 V to 0 V to achieve I_{DD} = 400 mA typical), 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Units
FREQUENCY RANGE			0.1		6	GHz
GAIN			12	13		dB
Gain Flatness				±0.75		dB
Gain Variation Over Temperature				0.015		dB/°C
RETURN LOSS						
Input				12		dB
Output				15		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB		27	29		dBm
Saturated Output Power	P_{SAT}			31		dBm
Output Third-Order Intercept	OIP3	P_{OUT} per tone = 10 dBm, 1 MHz spacing		44		dBm
NOISE FIGURE				12		dB
		2.0 GHz to 6.0 GHz		5		dB
SUPPLY CURRENT	I_{DD}		320	400	480	mA
Drain Bias Voltage[1]	V_{DD}	I_{DD} = 400 mA		11.5		V
				12.0		V
				12.5		V

[1] V_{GG1} set initially for nominal bias condition of V_{DD} = 12 V and V_{GG2} = 5 V to achieve I_{DD} = 400 mA typical; then adjusting V_{DD} ±0.5 V from 12 V to measure I_{DD} variation.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Drain Bias Voltage (V_{DD})	14 V_{DC}
Gate Bias Voltage	
V_{GG1}	−3 V_{DC} to 0 V_{DC}
V_{GG2}	4 V_{DC} to 7 V_{DC}
RF Input Power (RFIN), V_{DD} = 12 V_{DC}	25 dBm
Channel Temperature	175°C
Continuous P_{DISS} (T = 85°C, Derate 95 mW/°C Above 85°C)	8.6 W
Maximum Peak Reflow Temperature	260°C (MSL3[1] Rating)
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	Class 1B

[1] MSL3 stands for Moisture Sensitivity Level 3.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

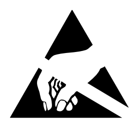
θ_{JC} is the junction to case thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
HCP-32-1	10.5	°C/W

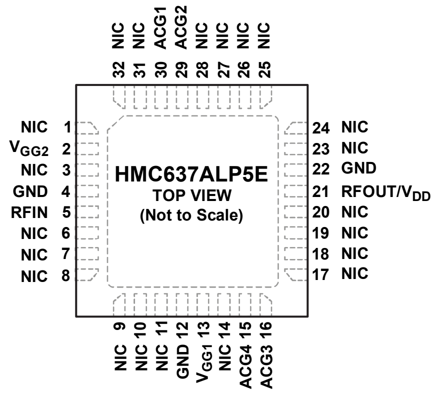
[1] Thermal impedance simulated values are based on a JEDEC 1S0P thermal test board. See JEDEC JESD51.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NO INTERNAL CONNECTION. THESE PINS MAY BE CONNECTED TO RF GROUND. PERFORMANCE IS NOT AFFECTED.
2. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO RF/DC GROUND.

17308-002

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description[1]
1, 3, 6 to 11, 14, 17 to 20, 23 to 28, 31, 32	NIC	No Internal Connection. These pins may be connected to RF ground. Performance is not affected.
2	V_{GG2}	Gate Control 2 for Amplifier. Apply 5 V to V_{GG2} for nominal operation. Attach a bypass capacitor per the application circuit shown in the Applications Information section.
4, 12, 22	GND	Ground. Connect Pin 4, Pin 12, and Pin 22 to RF/dc ground.
5	RFIN	This pad is dc-coupled and matched to 50 Ω.
13	V_{GG1}	Gate Control 1 for Amplifier. Attach a bypass capacitor per the application circuit shown in the Applications Information section. Follow the power up and power down sequences outlines in the Applications Information section.
15	ACG4	Low Frequency Termination. Attach a bypass capacitor per the application circuit shown in the Applications Information section.
16	ACG3	Low Frequency Termination. Attach a bypass capacitor per the application circuit shown in the Applications Information section.
21	RFOUT/V_{DD}	RF Output/Power Supply Voltage for Amplifier. Connect the dc bias (V_{DD}) network to provide drain current (I_{DD}). See the application circuit shown in the Applications Information section.
29	ACG2	Low Frequency Termination. Attach a bypass capacitor per the application circuit shown in the Applications Information section.
30	ACG1	Low Frequency Termination. Attach a bypass capacitor per the application circuit shown in the Applications Information section.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

[1] See the Interface Schematics section for pin interfaces.

INTERFACE SCHEMATICS

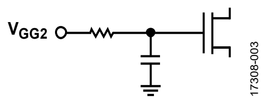


Figure 3. V_{GG2} Interface Schematic

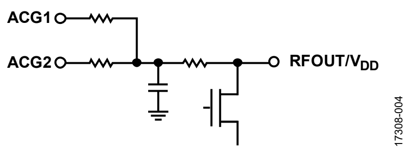


Figure 4. ACG1, ACG2, and RFOUT/V_{DD} Interface Schematic

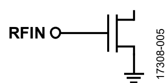


Figure 5. RFIN Interface Schematic

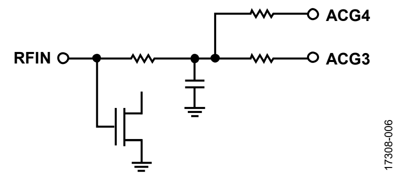


Figure 6. RFIN, ACG4, and ACG3 Interface Schematic

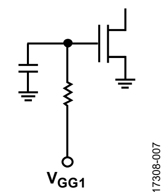


Figure 7. V_{GG1} Interface Schematic

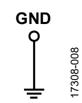


Figure 8. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

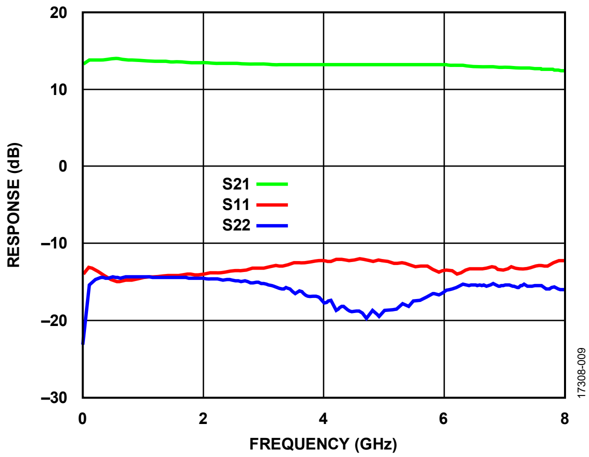


Figure 9. Gain and Return Loss

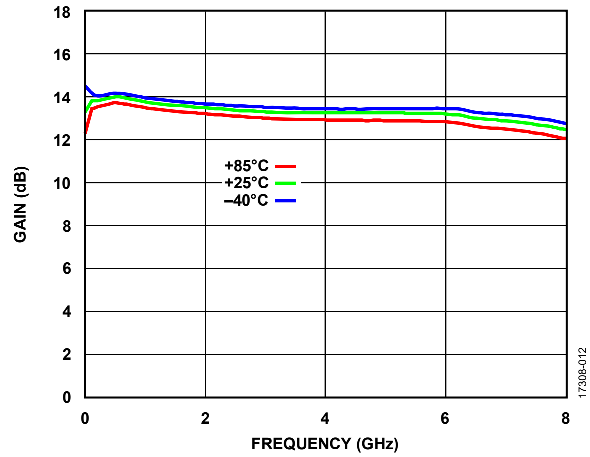


Figure 12. Gain vs. Frequency at Various Temperatures

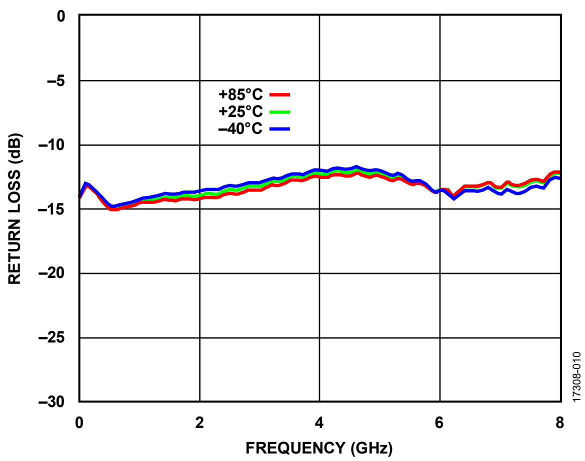


Figure 10. Input Return Loss vs. Frequency at Various Temperatures

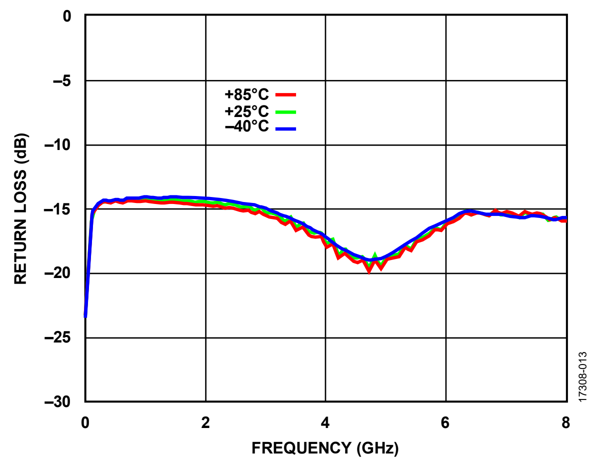


Figure 13. Output Return Loss vs. Frequency at Various Temperatures

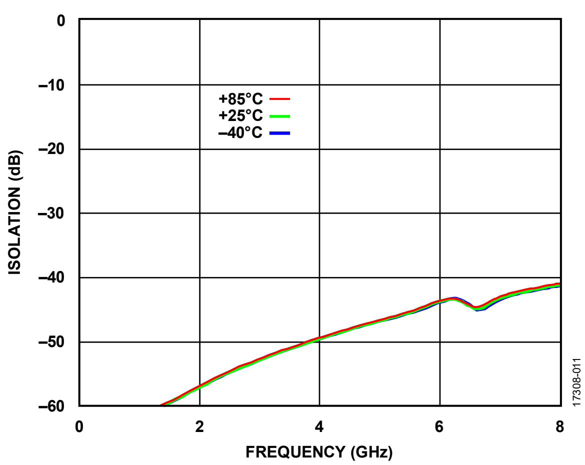


Figure 11. Reverse Isolation vs. Frequency at Various Temperatures

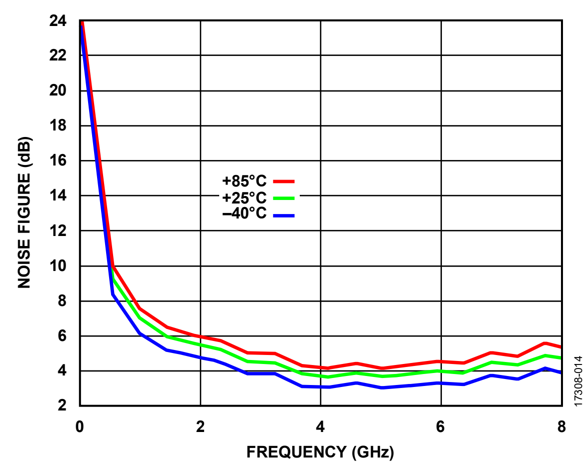


Figure 14. Noise Figure vs. Frequency at Various Temperatures

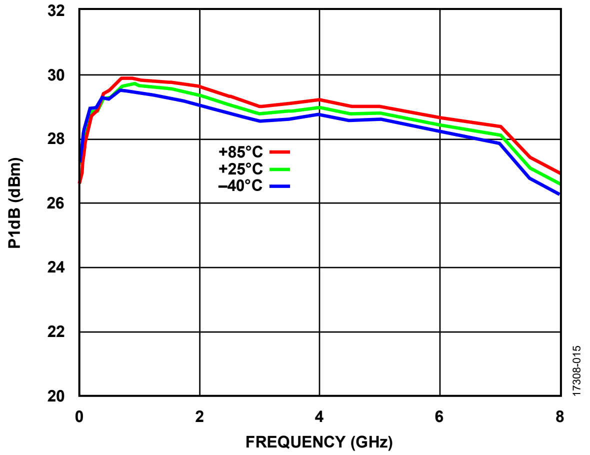


Figure 15. P1dB vs. Frequency at Various Temperatures

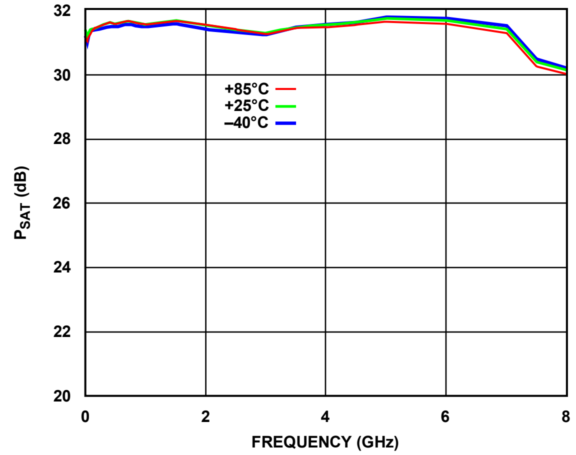


Figure 18. P_{SAT} vs. Frequency at Various Temperatures

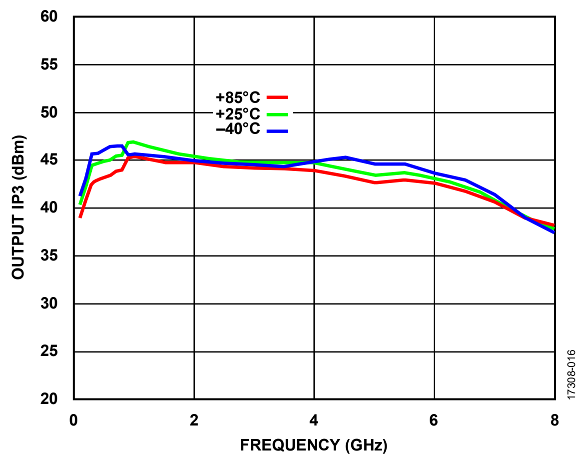


Figure 16. Output IP3 vs. Frequency at Various Temperatures

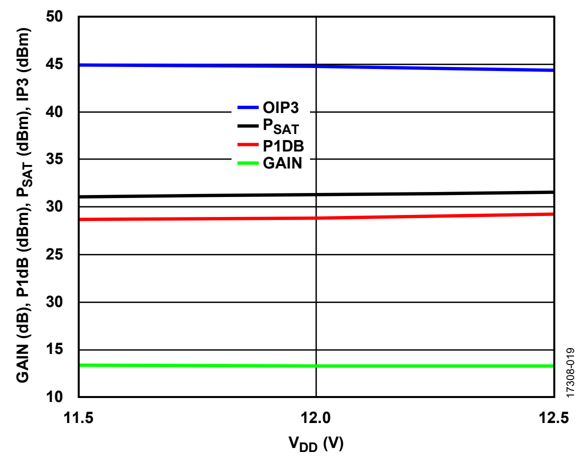


Figure 19. Gain, Power, and Output IP3 vs. Supply Voltage at 3 GHz, Fixed V_{GG}

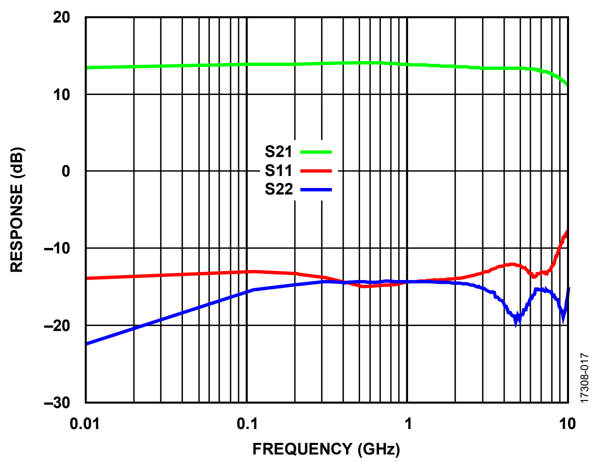


Figure 17. Gain and Return Loss vs. Frequency, Log Scale

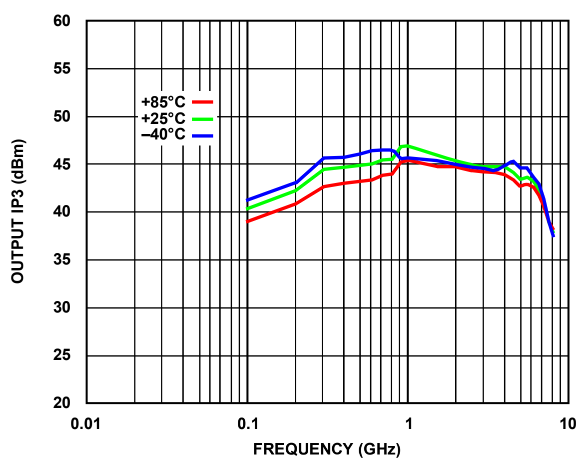


Figure 20. Output IP3 vs. Frequency at Various Temperatures, Log Scale

APPLICATIONS INFORMATION

For the application circuit shown in Figure 21, V_{DD} must be applied through a broadband bias tee or external bias network.

The power-up bias sequence is as follows:

1. Set V_{GG1} to −2 V
2. Set V_{DD} to 12 V
3. Set V_{GG2} to 5 V
4. Adjust V_{GG1} to achieve I_{DD} for 400 mA

The power-down sequence is as follows:

1. Remove V_{GG2} bias
2. Remove V_{DD} bias
3. Remove V_{GG1} bias

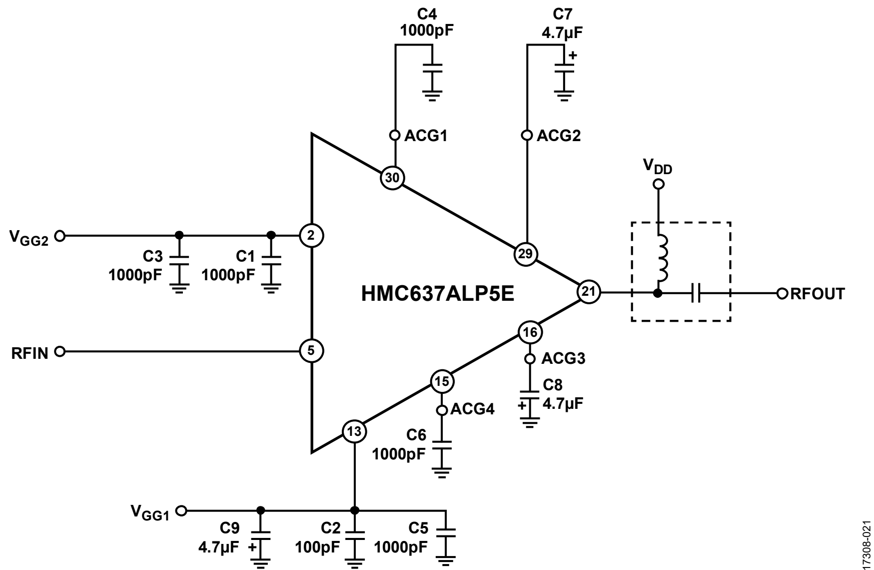


Figure 21. Application Circuit

EVALUATION PCB

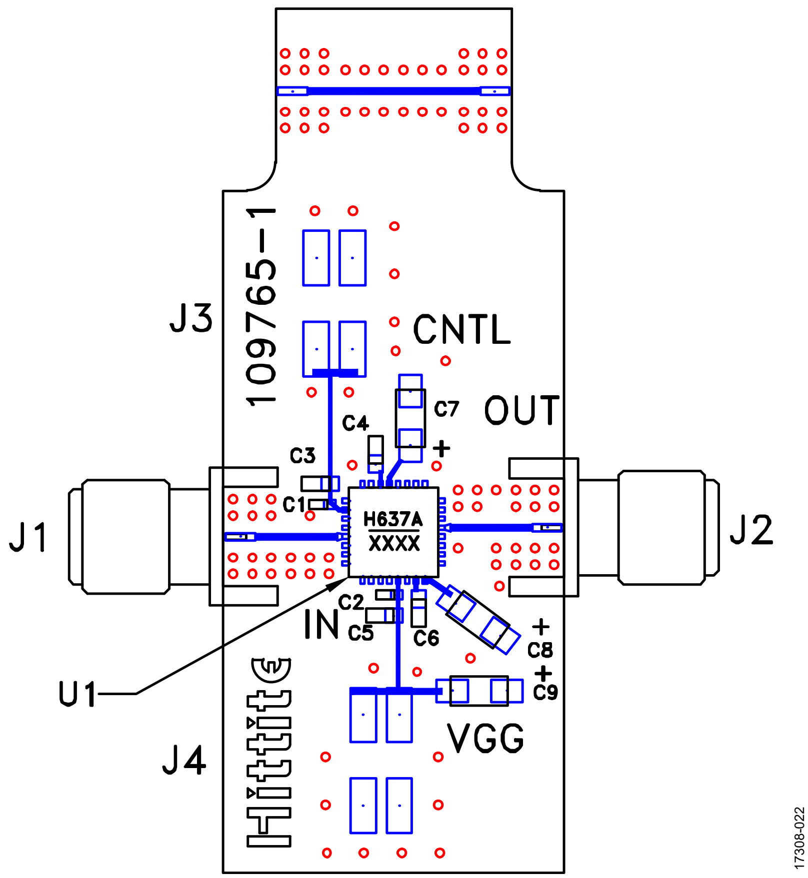


Figure 22. Evaluation Board PCB

LIST OF MATERIALS FOR PCB EV1HMC637ALP5E

It is recommended that the circuit board used in the application follows proper RF circuit design techniques. Signal lines must have 50 Ω impedance while the package ground leads and package bottom are connected directly to the ground plane similar to that shown in Figure 22. Ensure that a sufficient number of via holes are used to connect the top and bottom ground planes. The evaluation board thermal design must also be considered and mounted to an appropriate heat sink. The evaluation circuit board shown is available from Analog Devices, Inc. upon request.

Table 5. Bill of Materials for Evaluation PCB EV1HMC637ALP5E

Item	Description
J1, J2	SRI SMA connector
J3, J4	2 mm Molex header
C1, C2	100 pF capacitor, 0402 package
C3 to C6	1000 pF capacitor, 0603 package
C7 to C9	4.7 µF capacitor, tantalum
U1	HMC637ALP5E
PCB[1]	109765 evaluation PCB

[1] Circuit board material: Rogers 4350.

OUTLINE DIMENSIONS

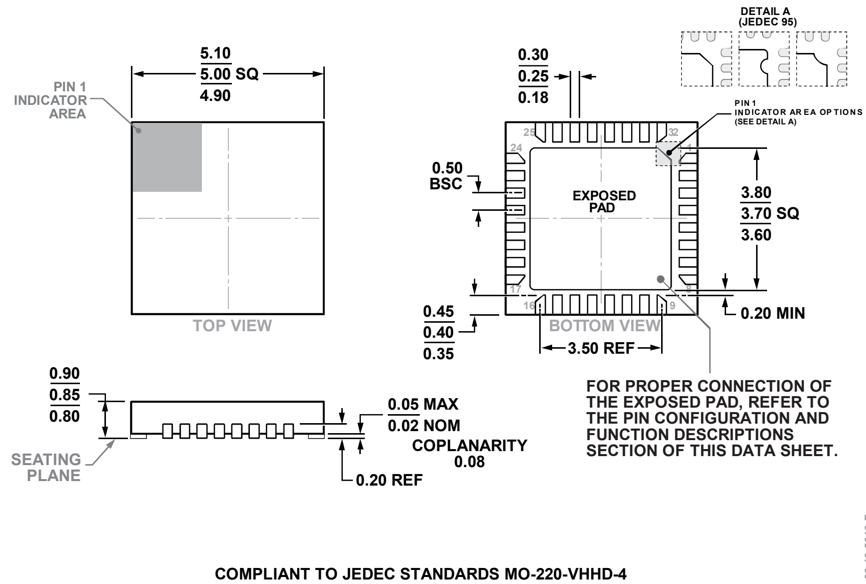


Figure 23. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm and 0.85 mm Package Height
(HCP-32-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option
HMC637ALP5E	−40°C to +85°C	MSL3	32-Lead Lead Frame Chip Scale Package [LFCSP]	HCP-32-1
HMC637ALP5ETR	−40°C to +85°C	MSL3	32-Lead Lead Frame Chip Scale Package [LFCSP]	HCP-32-1
EV1HMC637ALP5			Evaluation Board	

[1] All devices are RoHS compliant.
[2] See the Absolute Maximum Ratings section.