MB39C022G/J/L/N

Buck DC/DC Converter + Low Noise LDO

The MB39C022 is a 2 channels power supply IC. It consists of one channel Buck DC/DC Converter and one channel LDO regulator. The DC/DC converter has fast transient response with current mode control topology. Moreover, the integrated LDO provides an auxiliary output supply for noise sensitive circuit.

Features

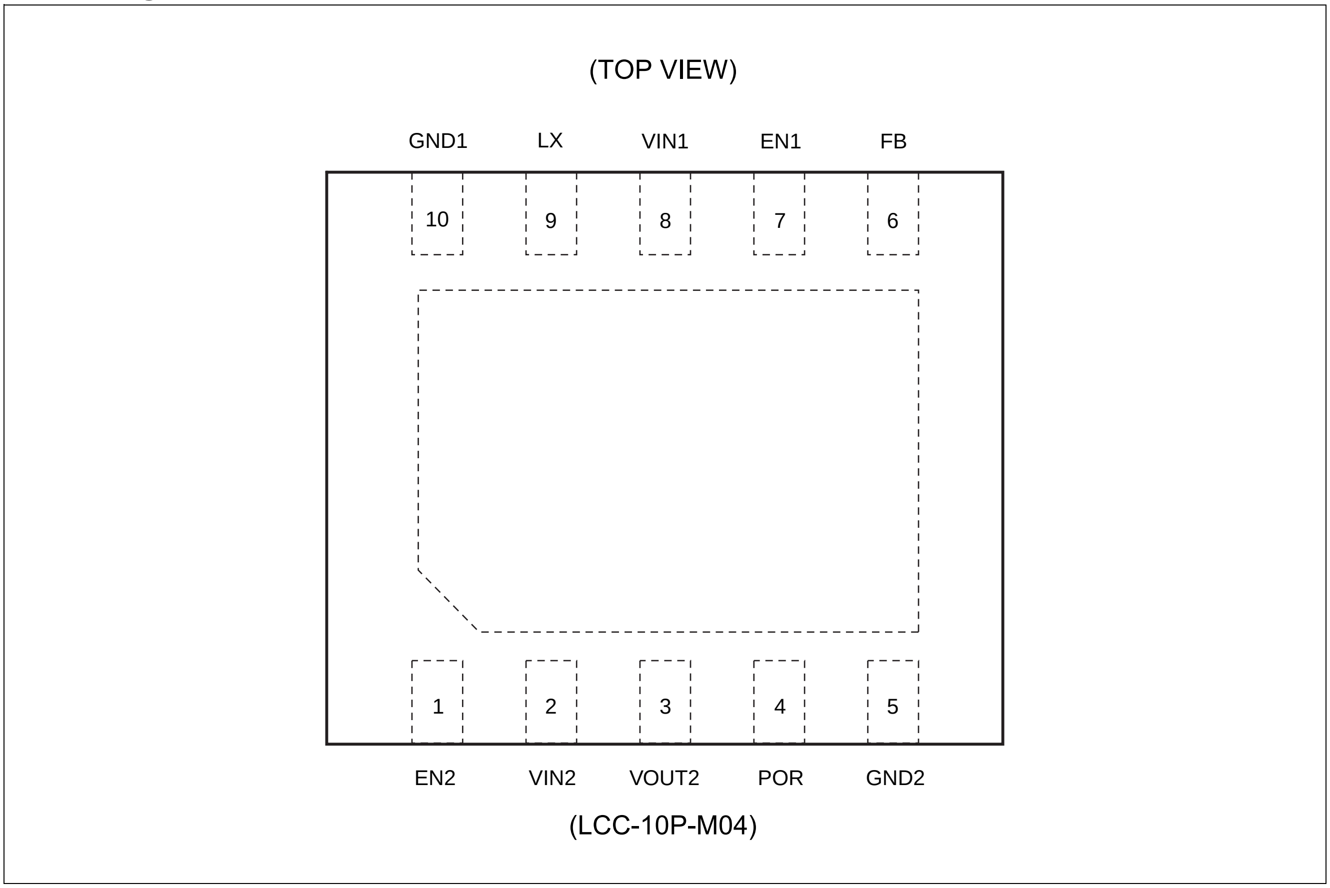
- Power supply voltage range : 2.5 V to 5.5 V
- For Buck DC/DC included SW FET (CH1) : output 0.8 V to 4.5 V, 600 mA Max DC
- For LDO (CH2) : output 3.30 V (MB39C022G) 300 mA Max DC
  : output 2.85 V (MB39C022J) 300 mA Max DC
  : output 1.80 V (MB39C022L) 300 mA Max DC
  : output 1.20 V (MB39C022N) 300 mA Max DC
- Error amplifier threshold voltage : 0.3 V ± (2.5%) (CH1)
- Fast line transient response with current mode topology (CH1)
- PFM mode at light load current with VO1/VIN1 ≤ 80% (IO1 ≤ 10 mA) (CH1)
- Power-on-reset with 66 ms delay (CH1)
- Built-in short circuit protect (CH2)
- Built-in over current protect (CH1, CH2)
- Built-in thermal protection function
- Small size plastic SON-10 (3 mm × 3 mm) package

Applications

- Portable Equipment
- PND, GPS
- PMP
- Mobile TV, USB-dongle (CMMB, DVB-T, DMB-T)
- Smart-phone
- MP3

Contents

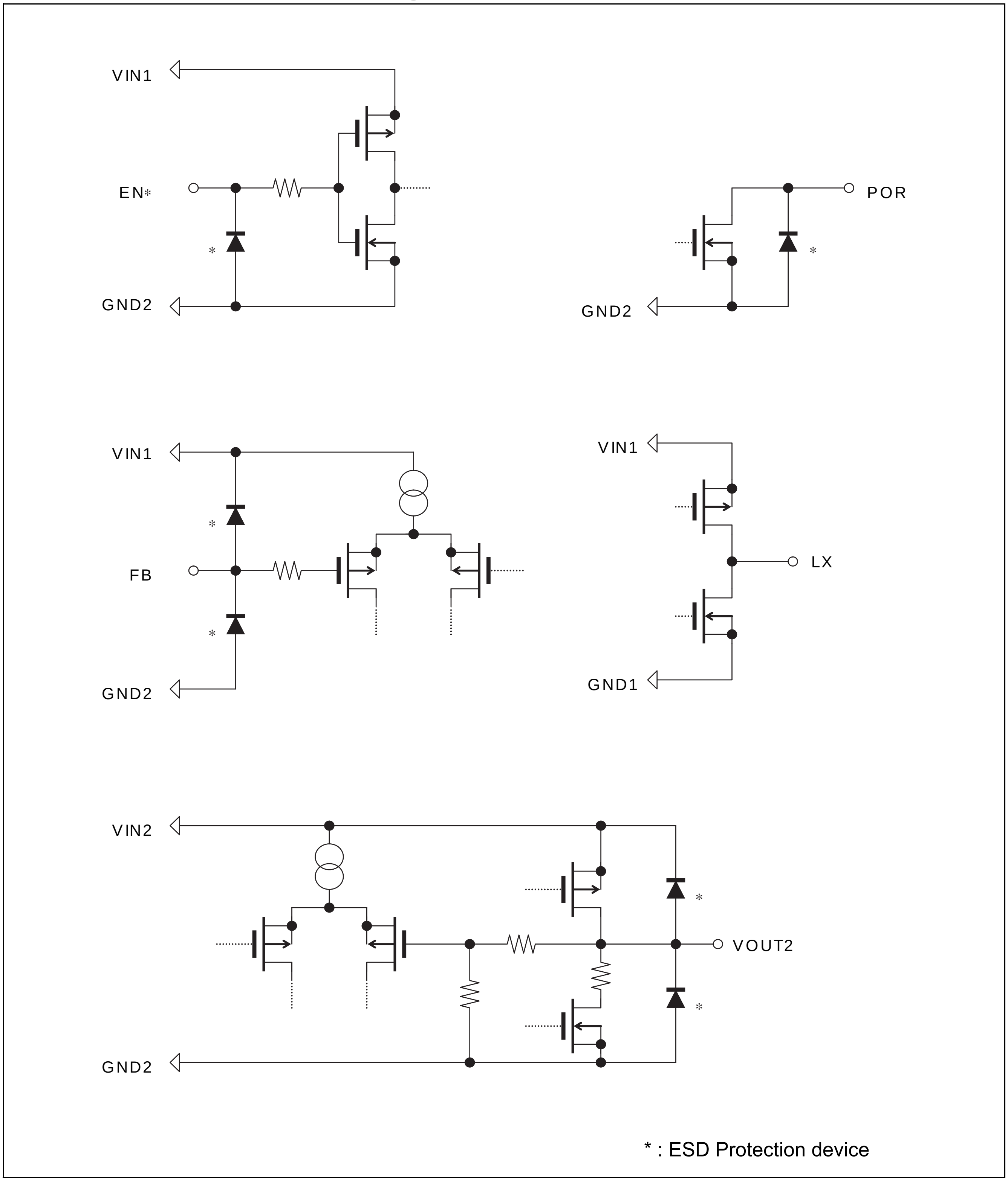
1. Pin Assignment



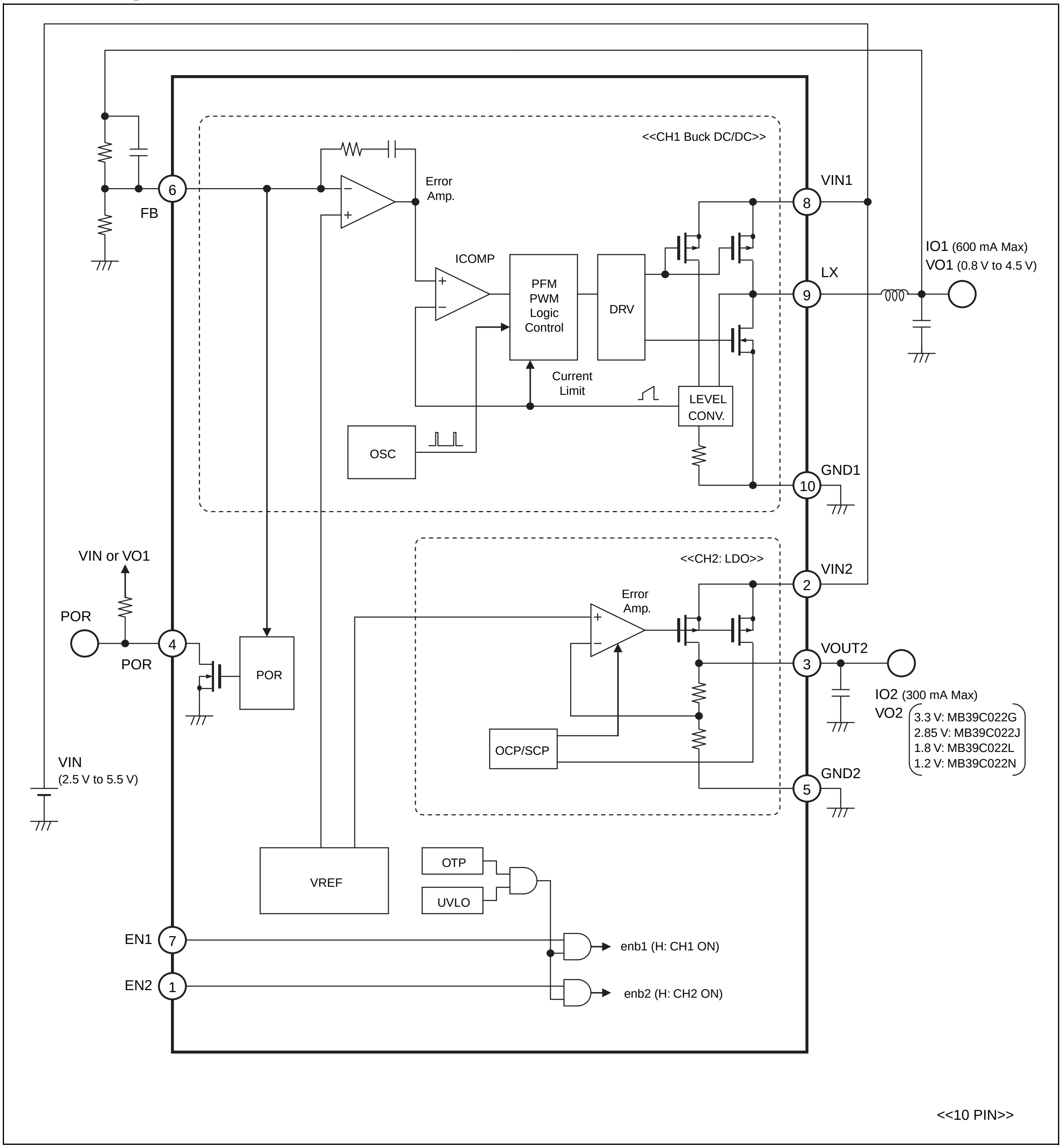
2. Pin Descriptions

Block	Pin No.	Pin name	I/O	Descriptions
CH1 (Buck DC/DC)	6	FB	I	CH1 Error Amplifier input pin
	9	LX	O	CH1 Inductor connection pin
CH2 (LDO)	3	VOUT2	O	CH2 LDO output pin
Control	7	EN1	I	CH1 Control pin (L : shutdown / H : operation)
	1	EN2	I	CH2 Control pin (L : shutdown / H : operation)
Power	8	VIN1	–	CH1 Power supply pin
	2	VIN2	–	CH2 Power supply pin
	10	GND1	–	CH1 Ground pin
	5	GND2	–	CH2 Ground pin
Power-on Reset	4	POR	O	CH1 Power on reset output pin (NMOS open drain)

3. I/O Terminal Equivalent Circuit Diagram



4. Block Diagram



5. Function Descriptions

5.1 PFM/PWM Logic Control Block (CH1)

The built-in P-ch and N-ch MOS FETs are controlled for synchronization rectification according to the frequency (2.0 MHz) oscillated from the built-in oscillator (square wave oscillation circuit). Under light load, it operates intermittently.

This circuit protects the through current caused by synchronous rectification and the reverse current in Discontinuous Conduction Mode.

Since the PWM control circuit of this IC is in the control method in current mode, the current peak value is monitored and controlled as required.

5.2 Level converter and Iout Comparator circuit (CH1)

The Level converter circuit detects the current (ILX) which flows to the external inductor from the built-in P-ch MOS FET. By comparing VIDET obtained through I-V conversion of peak current I_{PK} of ILX with the Error Amp. output, the Iout Comparator turns off the built-in P-ch MOS FET via the PWM Logic Control circuit.

5.3 Error Amp. circuit (CH1)

The error amplifier (Error Amp.) detects the output voltage from the DC/DC converter and output to the current comparators (ICOMP). The output voltage setting resistor externally connected to FB allows an arbitrary output voltage to be set.

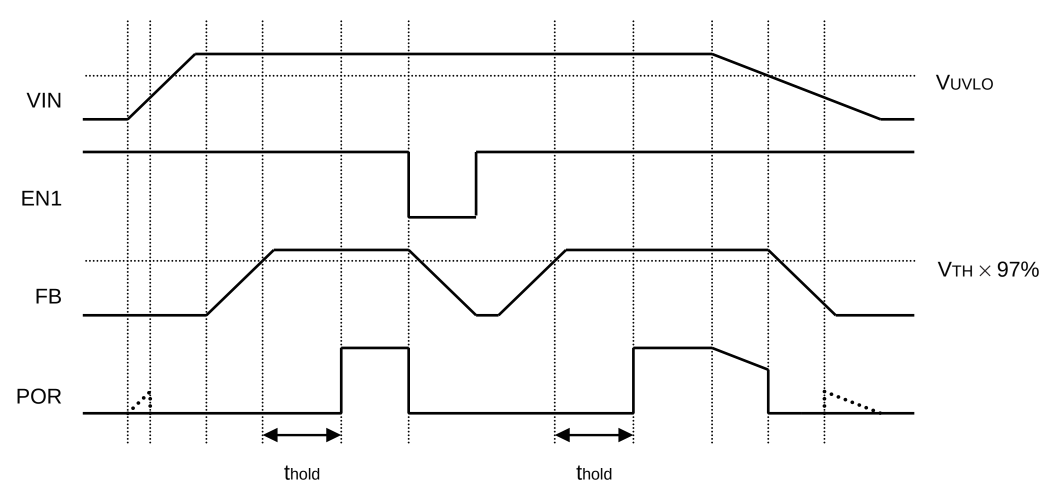
5.4 LDO Block (CH2)

The integrated low noise low dropout regulator (LDO) is available up to 300 mA current capability and 700 mA over current protection (OCP) 350 mA short circuit protection (SCP). The LDO output VOUT2 requires a 4.7 µF capacitor for MB39C022G and MB39C022N and a 1.0 µF capacitor for MB39C022J and MB39C022L for stability. MB39C022G, MB39C022J, MB39C022L and MB39C022N have fixed 3.3 V, 2.85 V, 1.8 V and 1.2 V output voltages respectively, eliminating the need for an external resistor divider.

5.5 POR Block

The POR circuit monitors the VO1 through the FB pin voltage. When the FB pin voltage reaches 97% of V_{FBTH}, POR pin becomes high level after the hold time of 66 ms. The POR pin is an open-drain output and pulled up to VIN or VO1 with an external resistor.

Timing Chart : (POR pin pulled up to VIN with resistor)



V_{UVLO} : UVLO threshold voltage (VT_{LH} = 2.050 V)
V_{TH} : FB pin threshold voltage (V_{TH} = 0.3 V)

5.6 Reference Voltage Block (VREF)

A high accuracy reference voltage is generated with BGR (bandgap reference) circuit.

5.7 Under Voltage Lockout Protection Circuit Block (UVLO)

The circuit protects against IC malfunction and system destruction/deterioration in a transitional state or a momentary drop of when the internal reference voltage starts. It detects a voltage drop at the VIN1 pin and stops IC operation. When voltages at the VIN1 pin exceed the threshold voltage of the under voltage lockout protection circuit, the system is restored.

5.8 Over Temperature Protection Block (OTP)

The circuit protects an IC from heat-destruction. If the junction temperature reaches 135°C, the circuit turns off the CH1 and CH2 operation, When the junction temperature comes down to ＋110°C, the CH1 and CH2 are returned to the normal operation.

5.9 Control Block (CTL)

■ Control function table

EN1	EN2	CH1 and POR	CH2	VREF, UVLO, OTP
L	L	OFF	OFF	OFF
H	L	ON	OFF	ON
L	H	OFF	ON	ON
H	H	ON	ON	ON

6. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	VIN1	VIN1 pin	− 0.3	+ 6.0	V
	VIN2	VIN2 pin	− 0.3	VIN1 + 0.3	V
Input voltage	VFB	FB pin	− 0.3	VIN1 + 0.3	V
	VEN1	EN1 pin	− 0.3	+ 6.0	V
	VEN2	EN2 pin	− 0.3	+ 6.0	V
POR pull-up voltage	VPOR	POR pin	− 0.3	+ 6.0	V
LX voltage	VLX	LX pin	− 0.3	VIN1 + 0.3	V
LX peak current	ILX	LX pin AC	–	1.6	A
VOUT2 peak current	IO2	VOUT2 pin AC	–	0.8	A
Power dissipation	PD	Ta ≤ + 25°C	–	2632[*1, *2]	mW
			–	980[*1, *3]	
		Ta = + 85°C	–	1053[*1, *2, *4]	
			–	392[*1, *3, *4]	
Storage temperature	T_{STG}	–	− 55	+ 125	°C

[*1]: When mounted on four layer epoxy board of 11.7 cm × 8.4 cm

[*2]: At connect the exposure pad and with thermal via (Thermal via 4 pcs).

[*3]: At connect the exposure pad and not thermal via.

[*4]: Power dissipation value between + 25°C and + 85°C is obtained by connecting these two points with a straight line

Notes:
- The use of negative voltages below − 0.3 V to the GND pin may create parasitic transistors on LSI lines, which can cause abnormal operation.
- If LX terminal is short-circuited to VIN1 or VIN2 or GND line, there is a possibility to destroy it. Such usage is prohibit

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

7. Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	VIN1	VIN1 pin*1, *3, *4, *5	2.5	3.7	5.5	V
	VIN2	VIN2 pin*2, *3				
Input voltage	VFB	FB pin	–	0.30	–	V
	VEN1	EN1 pin	0	–	5.5	V
	VEN2	EN2 pin	0	–	5.5	V
Output voltage	VO1	CH1 : Buck DC/DC*1, *5	0.8	–	4.5	V
Output current	ILX	LX pin DC	–	–	0.6	A
	IVOUT2	VOUT2 pin DC	–	–	0.3	A
Operating ambient temperature	Ta	–	− 40	+ 25	+ 85	°C

*1 : The minimum VIN1 has to meet two conditions : VIN1 ≥ (VIN1 Min) and VIN1 ≥ VO1 + 0.5 V

*2 : The minimum VIN2 has to meet two conditions : VIN2 ≥ (VIN2 Min) and VIN2 ≥ VO2 + Vdrop (VO2 and Vdrop values are specified in “Electrical Characteristics”)

*3 : VIN1 ≥ VIN2

*4 : VIN1 startup rise time ≤ 1 ms is recommended

*5 : PFM mode at light load current with VO1/VIN1 ≤ 80% (IO1 ≤ 10 mA)

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

8. Electrical Characteristics

(Ta = ＋25°C, VIN1 = VIN2 = 3.7 V)

Parameter		Symbol	Pin No.	Condition		Value Min	Value Typ	Value Max	Unit
CH1 [Buck DC/DC]	Threshold voltage	VTH	6	FB pin		−2.5%	0.3	＋2.5%	V
	Input Bias current	IFB	6	FB = 0 V		−100	0	＋100	nA
	SW PMOS-Tr On resistor	RPON	8,9	ILX = −100 mA		–	0.35	–	Ω
	SW NMOS-Tr On resistor	RNON	9,10	ILX = 100 mA		–	0.25	–	Ω
	Line regulation	Vline1	–	VIN1 = 2.5 V to 5.5 V*1		–	10	–	mV
	Load regulation	Vload1	–	IO1 = 100 mA to 600 mA		–	10	–	mV
	Over current protect	ILIM1	9	VOUT1 × 0.9		0.9	1.2	1.5	A
CH2 [LDO]	Output voltage	VO2	3	IO2 = 0 mA to −300 mA MB39C022G		−2.5%	3.30	＋2.5%	V
				IO2 = 0 mA to −300 mA MB39C022J		−2.5%	2.85	＋2.5%	V
				IO2 = 0 mA to −300 mA MB39C022L		−2.5%	1.80	＋2.5%	V
				IO2 = 0 mA to −300 mA MB39C022N		−2.5%	1.20	＋2.5%	V
	Line regulation	Vline2	3	VIN2 = 2.5 V to 5.5 V*2		–	–	10	mV
	Load regulation	Vload2	3	IO2 = 0 mA to −300 mA		–	–	25	mV
	Drop out voltage	Vdrop	3	IO2 = −300 mA, VIN2 = VO2 : MB39C022G, MB39C022J		–	200	–	mV
	Power supply rejection ratio	PSRR	3	MB39C022G*3	f = 1 kHz	–	70*4	–	dB
					f = 10 kHz	–	70*4	–	dB
				MB39C022J*3	f = 1 kHz	–	65*4	–	dB
					f = 10 kHz	–	65*4	–	dB
				MB39C022L*3	f = 1 kHz	–	60*4	–	dB
					f = 10 kHz	–	60*4	–	dB
				MB39C022N*3	f = 1 kHz	–	55*4	–	dB
					f = 10 kHz	–	55*4	–	dB
	Output noise voltage	Vnoise	3	f = 10 Hz to 100 kHz, EN1 = 0 V		–	55*4	–	μVrms
	Over current protect	ILIM2	3	VO2 × 0.9		500	700	980	mA
	Short circuit protect	ISCP2	3	VO2 = 0 V		150	350	700	mA

(Continued)

(Continued)

(Ta = ＋25°C, VIN1 = VIN2 = 3.7 V)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Power On Reset [POR]	Hold time	Thold	4	fosc = 2 MHz	52.8	66	79.2	ms
	Output voltage	VPOR	4	POR = 250 µA	–	–	0.1	V
	Output current	IPOR	4	POR = 5.5 V	–	–	1	µA
Under Voltage Lockout Protection Circuit Block [UVLO]	Threshold voltage	VTHL	2, 8	VIN1	1.95	2.10	2.25	V
	Hysteresis width	VH	2, 8	–	–	0.20	–	V
Over Temperature Protection Block [OTP]	Stop temperature	TOTPH	–	–	–	＋135	–	°C
	Hysteresis width	TOTPHYS	–	–	–	＋25	–	°C
Oscillator Block [OSC]	Output frequency	fosc	9	–	1.6	2.0	2.4	MHz
Control Block [CTL]	Input voltage	VIH	1, 7	EN1, EN2 ON	1.5	–	–	V
		VIL	1, 7	EN1, EN2 OFF	–	–	0.4	V
	Input current	IEN	1, 7	EN1, EN2 = 0 V	− 100	0	＋100	nA
General	Shut down power supply current	ICC1	8	EN1, EN2 = 0 V	–	0	1	µA
		ICC1	2	EN1, EN2 = 0 V	–	0	1	µA
	Standby power supply current (DC/DC)	ICC2	8	EN1 = VIN1, EN2 = 0 V IO1 = 0 mA, VFB = VIN1	–	30	60	µA
		ICC2	2		–	0	1	
	Standby power supply current (LDO)	ICC3	8	EN1 = 0 V, EN2 = VIN1 IO2 = 0 mA	–	10	18	µA
		ICC3	2		–	60	120	
	Power-on invalid current	ICC4	8	EN1, EN2 = VIN1, VFB = 0.2 V	–	0.9	1.5	mA
		ICC4	2		–	60	120	µA

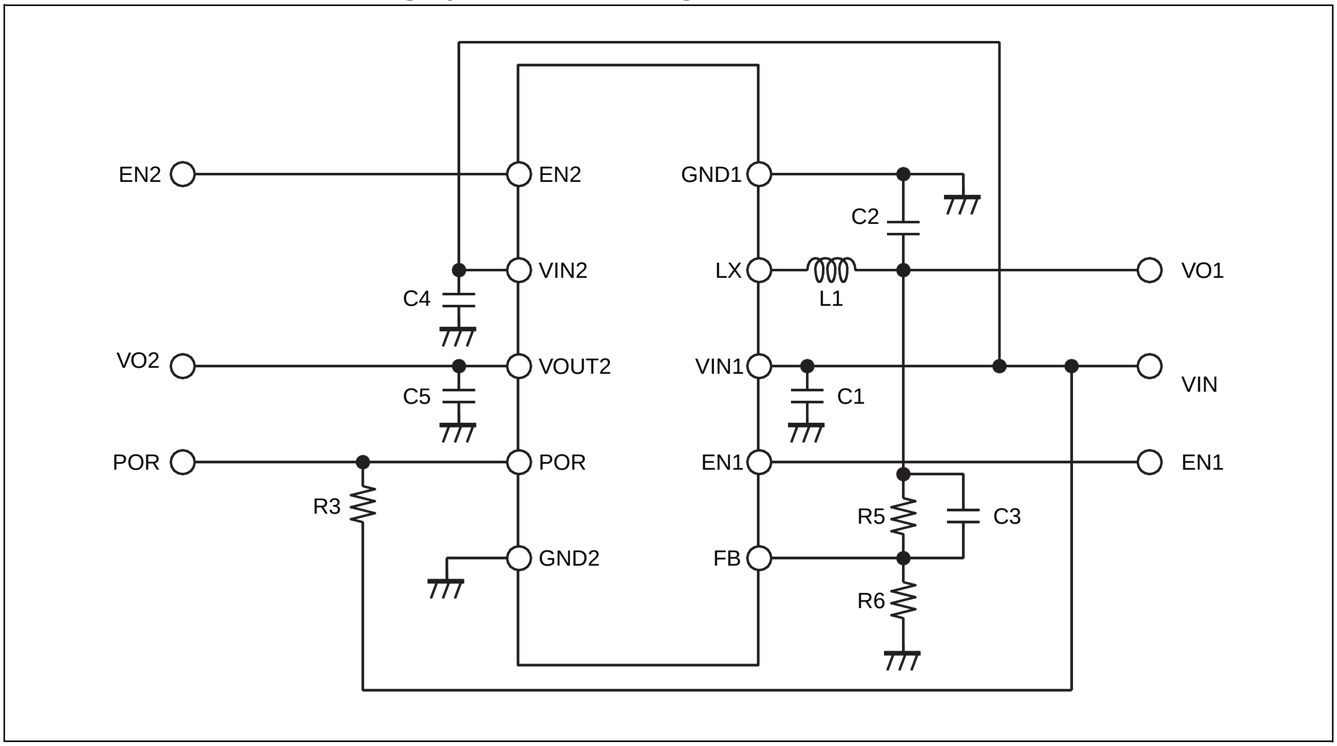
*1 : The minimum VIN1 has to meet two conditions : VIN1 ≥ (VIN1 Min) and VIN1 ≥ VO1 ＋ 0.5 V

*2 : The minimum VIN2 has to meet two conditions : VIN2 ≥ (VIN2 Min) and VIN2 ≥ VO2 ＋ Vdrop (VO2 and Vdrop values are specified in “ Electrical Characteristics”)

*3 : VIN2 = VO2 ＋ 1 V, (MB39C022N: VIN2 = 2.5 V), IO2 = 100 mA

*4 : This value is not be specified. This should be used as a reference to support designing the circuits.

9. Test Circuit For Measuring Typical Operating Characteristics



Component	Item	Specification	Remarks
C1	Ceramic capacitor	10 µF	
C2	Ceramic capacitor	4.7 µF	
C3	Ceramic capacitor	22 pF	
C4	Ceramic capacitor	4.7 µF	
C5	Ceramic capacitor	1 µF	for MB39C022J, MB39C022L
		4.7 µF	for MB39C022G, MB39C022N
L1	Inductor	2.2 µH	
R3	Resistor	1 MΩ	
R5	Resistor	600 kΩ	at VO1 = 1.2 V*
R6	Resistor	200 kΩ	

* : The output voltage of VO1 can be adjusted by the external resistor divider R5.

$$V_{O1} = V_{ref} \times \frac{(R5 + R6)}{R6} = 0.3\text{ V} \times \frac{(600\text{ k}\Omega + 200\text{ k}\Omega)}{200\text{ k}\Omega} = 1.2\text{ V}$$

10. Application Notes

10.1 Selection of components

Selection of an external inductor for DC/DC

This IC is designed to operate well with a 2.2 μH inductor. Choosing larger values would lead to larger overshoot/undershoot during load transient. Choosing a smaller value would lead to larger ripple voltage.
The inductor should be rated for a saturation current higher than the LX peak current value during normal operating conditions, and should have a minimal DC resistance. (100 mΩ or less is recommended to improve efficiency.)

LX peak current value I_{PK} is obtained by the following formula.

$$I_{PK} = I_{OUT} + \frac{V_{IN} - V_{OUT}}{L} \times \frac{D}{fosc} \times \frac{1}{2} = I_{OUT} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times fosc \times V_{IN}}$$

L : External inductor value

I_{OUT} : Load current (DC)

V_{IN} : Power supply voltage

V_{OUT} : Output setting voltage

D : ON- duty to be switched (= V_{OUT}/V_{IN})

fosc : Switching frequency (2.0 MHz)

ex) At V_{IN} = 3.7 V, V_{OUT} = 1.2 V, I_{OUT} = 0.6 A, L = 2.2 μH, fosc = 2.0 MHz
The maximum peak current value I_{PK};

$$I_{PK} = I_{OUT} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times fosc \times V_{IN}} = 0.6\text{ A} + \frac{(3.7\text{ V} - 1.2\text{ V}) \times 1.2\text{ V}}{2 \times 2.2\ \mu\text{H} \times 2\text{ MHz} \times 3.7\text{ V}} = 0.69\text{ A}$$

I/O capacitor selection

- DC/DC's output capacitor's finite equivalent series resistance (ESR) causes ripple voltages on output equal to the amount of current variation multiplied by the ESR value. The output capacitor value also has a significant impact on the operating stability of the device when used as a DC/DC converter. Therefore, Cypress generally recommends C2 = 4.7 μF as DC/DC output capacitor, or a larger capacitor value can be used if ripple voltages are not suitable.

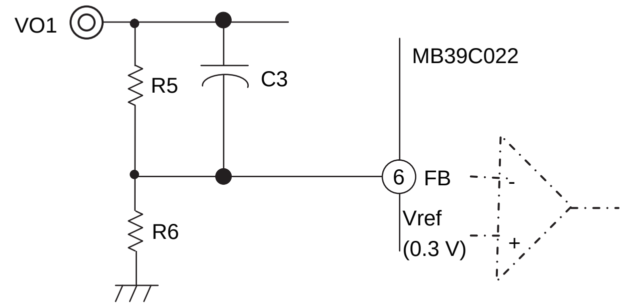
- For DC/DC, select a low ESR for the VIN1/VIN2 input capacitor to suppress dissipation from ripple currents. In addition, to reduce startup overshoot for DC/DC and LDO, it is recommended that larger ceramic capacitor be used for input capacitors C1 and C4. Recommended values are C1 = 10 μF, C4 = 4.7 μF.

- Types of capacitors
  Ceramic capacitors are effective for reducing the ESR and afford smaller DC/DC converter circuit. However, power supply functions as a heat generator, therefore avoid using capacitor with the F-temperature rating (−80% to +20%). Cypress recommends capacitors with the B-temperature rating (±10% to ±20%).
  Normal electrolytic capacitors are not recommended due to their high ESR.
  Tantalum capacitor will reduce ESR, however, it is dangerous to use because it turns into short mode when damaged. If you insist on using a tantalum capacitor, Cypress recommends the type with an internal fuse.

10.2 DC/DC Output voltage setting

The output voltage V_{O1} of this IC is defined by the external resistive divider R5 & R6. Note that C3 is a capacitor used for improving stability. Use a 22 pF cap for C3 should be suitable in all cases.

$$V_{O1} = V_{ref} \times \frac{R5 + R6}{R6} = 0.3\ V \times \frac{600\ k\Omega + 200\ k\Omega}{200\ k\Omega} = 1.2\ V$$



10.3 Power On Reset (POR)

R3 and R4 are the pull-up resistors for POR (Pin 4). A 1 MΩ resistor is required to placed at either R3 or R4. When R3 has a 1 MΩ resistor and R4 is open; the POR will be connected VIN. When R4 has a 1 MΩ resistor and R3 is open; the POR pin will be connected to VO1.

By default, only R3 require a 1 MΩ resistor while R4 is open.

10.4 Power dissipation and heat considerations

The DC/DC is so efficient that no consideration is required in most cases. The LDO, on the other hand, would be the dominant heat generator due to its inherent efficiency loss. Thus, if the IC is used at a high power supply voltage, heavy load, and low LDO output voltage, or high temperature, it requires further consideration.

The internal loss (Pc) is roughly obtained from the following formula :

$$P_C = P_{C1} + P_{C2} = I_{O1}^2 \times (RDC + D \times R_{ONP} + (1 - D) \times R_{ONN}) + I_{O2} \times V_{drop}$$

P_{C1}	: DC/DC continuity loss
P_{C2}	: LDO continuity loss
RDC	: External inductor series resistance ($<$ 100 mΩ recommended)
D	: Switching ON-duty cycle (= V_{OUT} / V_{IN})
R_{ONP}	: Internal P-ch SW FET ON resistance
R_{ONN}	: Internal N-ch SW FET ON resistance
I_{O1}	: DC/DC Load current
I_{O2}	: LDO Load current
V_{drop}	: LDO Dropout voltage

The loss expressed by the above formula is continuity loss. The internal loss includes the switching loss and the control circuit loss as well but they are so small compared to the continuity loss they can be ignored.

For P_{C1}, consider the scenario with high temperature and heavy load (VIN = 3.7 V, V_{O1} = 1.2 V, I_{O1} = 0.6 A, Ta = +70°C). Here, $R_{ONP} \fallingdotseq 0.4\ \Omega$ and $R_{ONN} \fallingdotseq 0.3\ \Omega$ according to the graph “MOS FET ON resistance vs. Operating ambient temperature”.
P_{C1} = 156 mW.

For P_{C2}, consider the scenario with low output voltage (MB39C022N), high temperature and heavy load (VIN = 3.7 V, V_{O2} = 1.2 V, I_{O2} = 0.3 A, Ta = +70°C). Here, P_{C2} = 0.75 W. Note that $P_{C2} >> P_{C1}$.

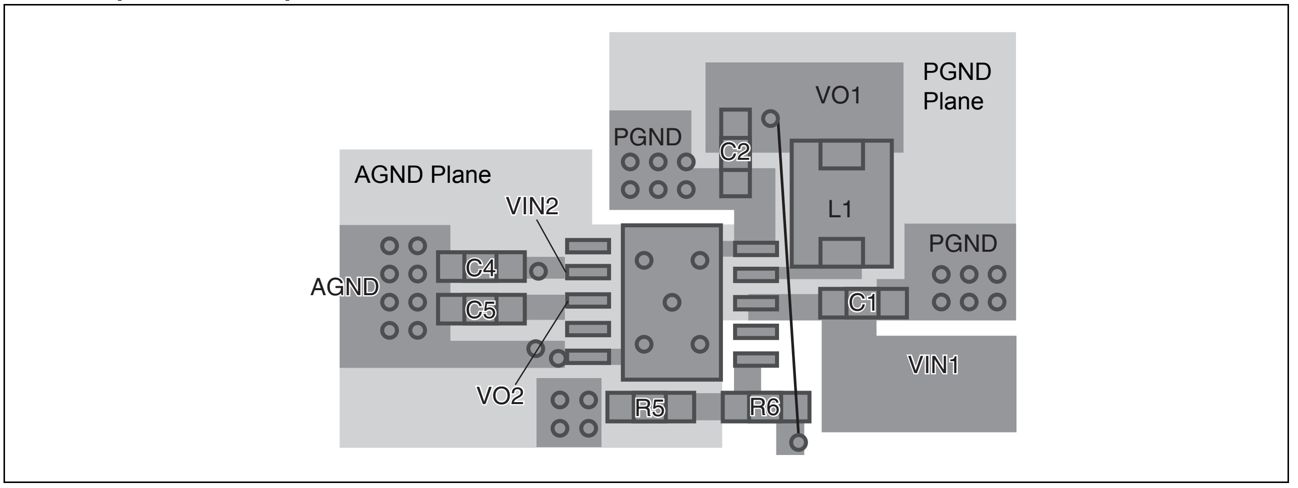
According to the graph “Power dissipation vs. Operating ambient temperature”, the maximum permissible power dissipation at an operating ambient temperature Ta of +70°C is 1.4 W. The internal loss is lower than the maximum permissible power dissipation.

10.5 Board layout, design example

Some basic design guidelines should be used when physically placing the MB39C022 on a Printed Circuit Board (PCB).

- Regarding to GND pattern of PCB layout of MB39C022, It needs to separate like AGND (analog ground) and PGND (power ground). By separating grounds, it is possible to minimize the switching frequency noise on the LDO output.
- Arrange the input capacitor C1 and C4 as close as possible between VIN1 & PGND pins and VIN2 & AGND pins. Make a through hole near the pins of this capacitor if the board has planes for power and GND.
- Large AC currents flow between this IC and the input capacitor (C1), output capacitor (C2), and external inductor (L1). Group these components as close as possible to this IC to reduce the overall loop area occupied by this group. Also try to mount these components on the same surface and arrange wiring without through hole wiring. Use thick, short, and straight routes to wire the net (The layout by planes is recommended.).
- The C1 and C2 capacitor returns are connected closely together at the PGND plane.
- The LDO input capacitor (C4) and LDO output capacitor (C5) are returned to the AGND plane.
- The analog ground plane and power ground plane are connected at one point.
- All other signals (EN1, EN2, FB) should be referenced to AGND and have the AGND plane underneath them.
- The feedback wiring to the V_{O1} and the V_{O1} pin should be wired closest to the output capacitor (C2). The resistive divider and FB pin is extremely sensitive and should thus be kept wired away from the LX pin of this IC as far as possible.
- Try to make a GND plane on the surface to which this IC will be mounted. For efficient heat dissipation when using the SON-10 package, Cypress recommends providing a thermal via in the footprint of the thermal pad.

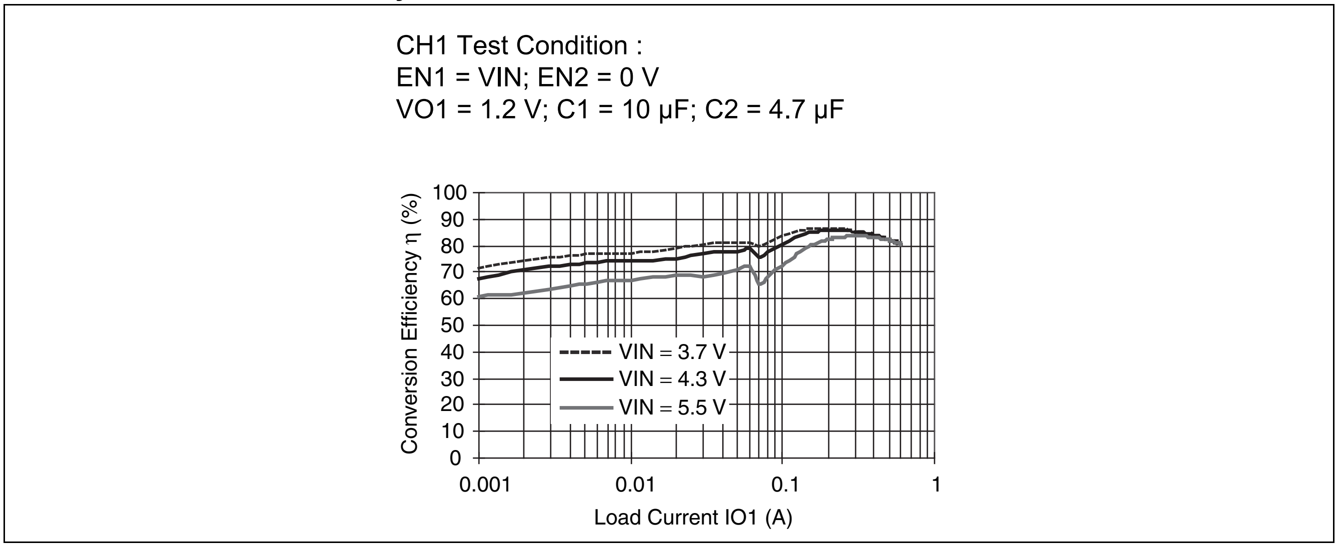
Layout Example of IC components



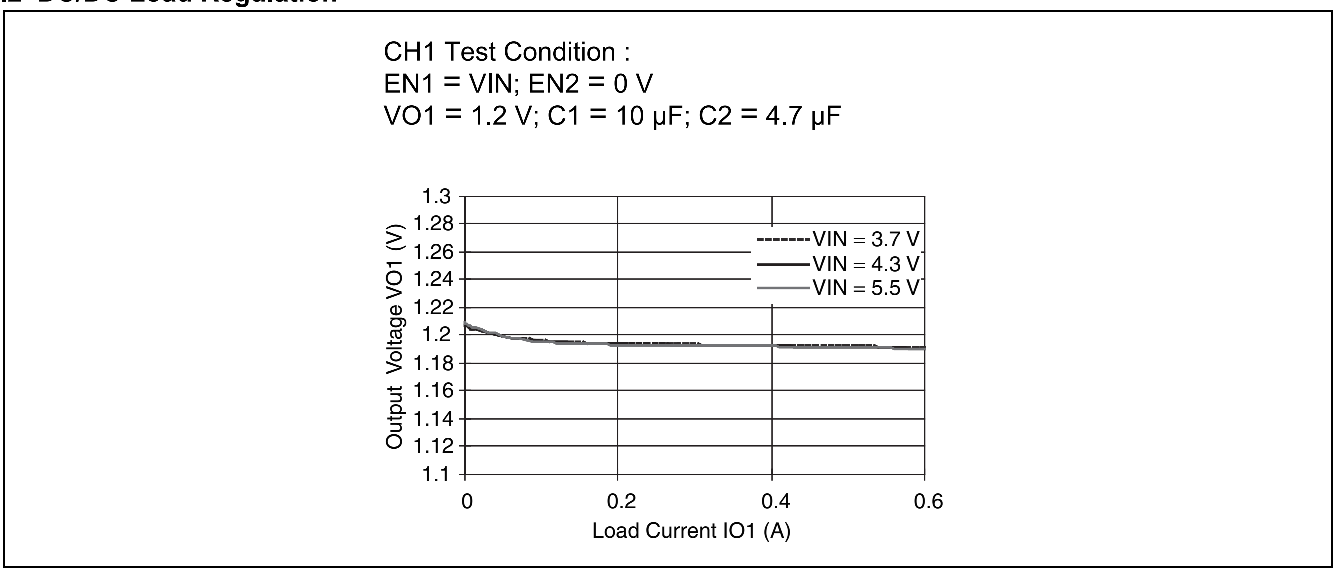
11. Example Of Standard Operation Characteristics

(Shown below is an example of characteristics for connection according to " Test Circuit For Measuring Typical Operating Characteristics".)

11.1 DC/DC Conversion Efficiency

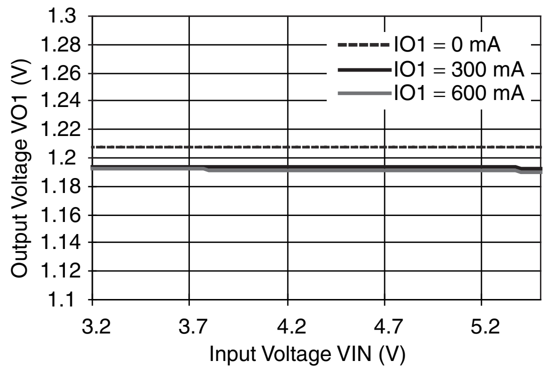


11.2 DC/DC Load Regulation



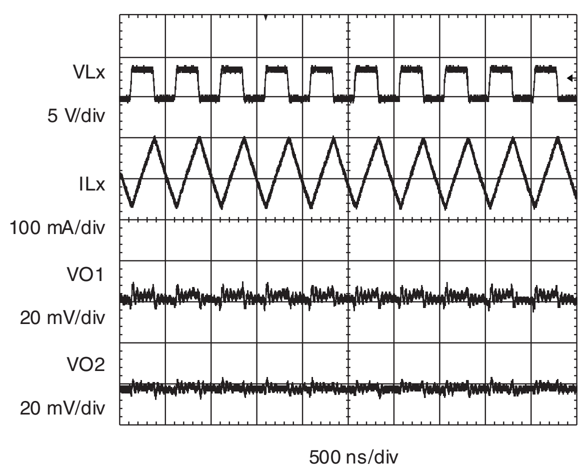
11.3 DC/DC Line Regulation

CH1 Test Condition :
EN1 = VIN; EN2 = 0 V
VO1 = 1.2 V; C1 = 10 μF; C2 = 4.7 μF

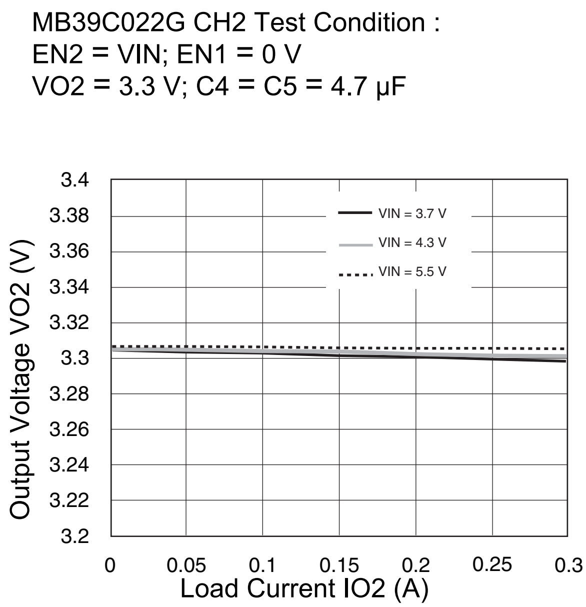


11.4 DC/DC Switching Waveform

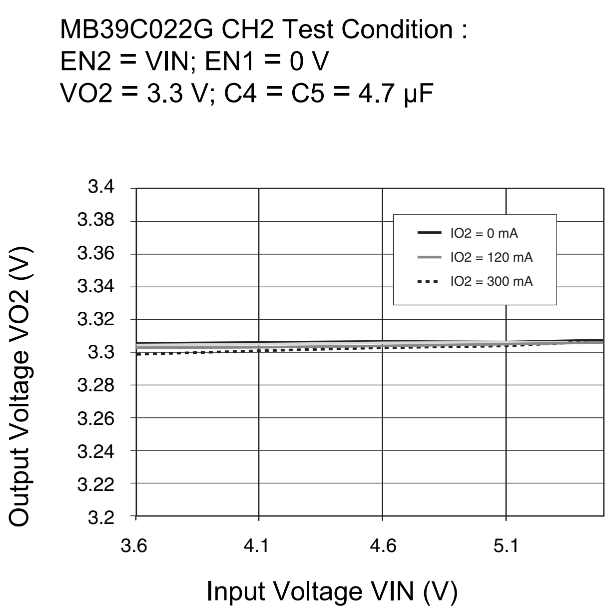
CH1 Test Condition :
EN1 = EN2 = VIN = 3.7 V;
VO1 = 1.8 V; IO1 = 250 mA; C1 = 10 μF; C2 = 4.7 μF
VO2 = 3.3 V; IO2 = 150 mA; C4 = C5 = 4.7 μF



11.5 LDO Load Regulation

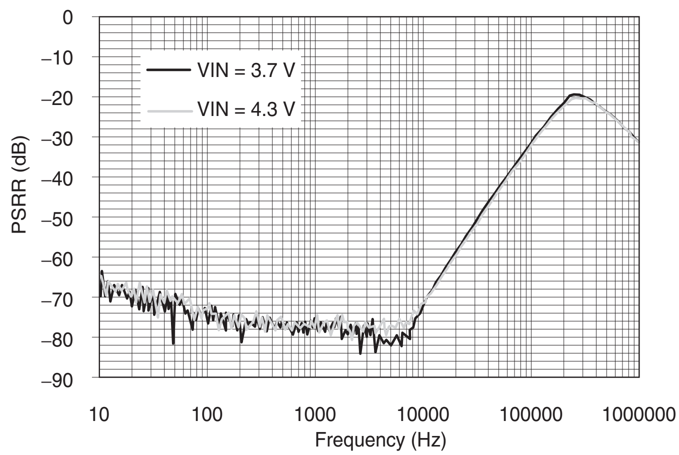


11.6 LDO Line Regulation



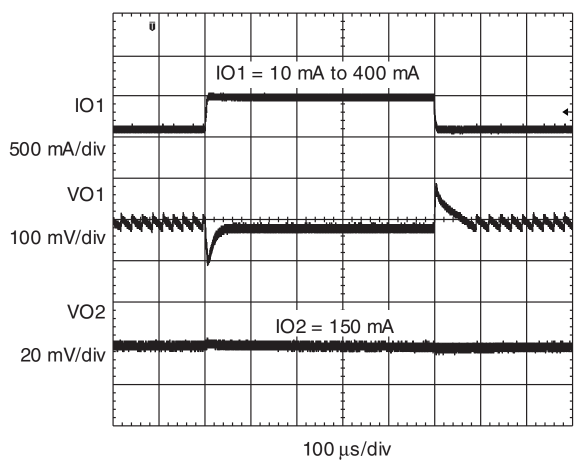
11.7 LDO Power Supply Rejection Ratio

MB39C022G CH2 Test Condition :
EN2 = VIN = 3.7 V; EN1 = 0 V
VO2 = 3.3 V; IO2 = 100 mA; C1 = C4 = 0 µF



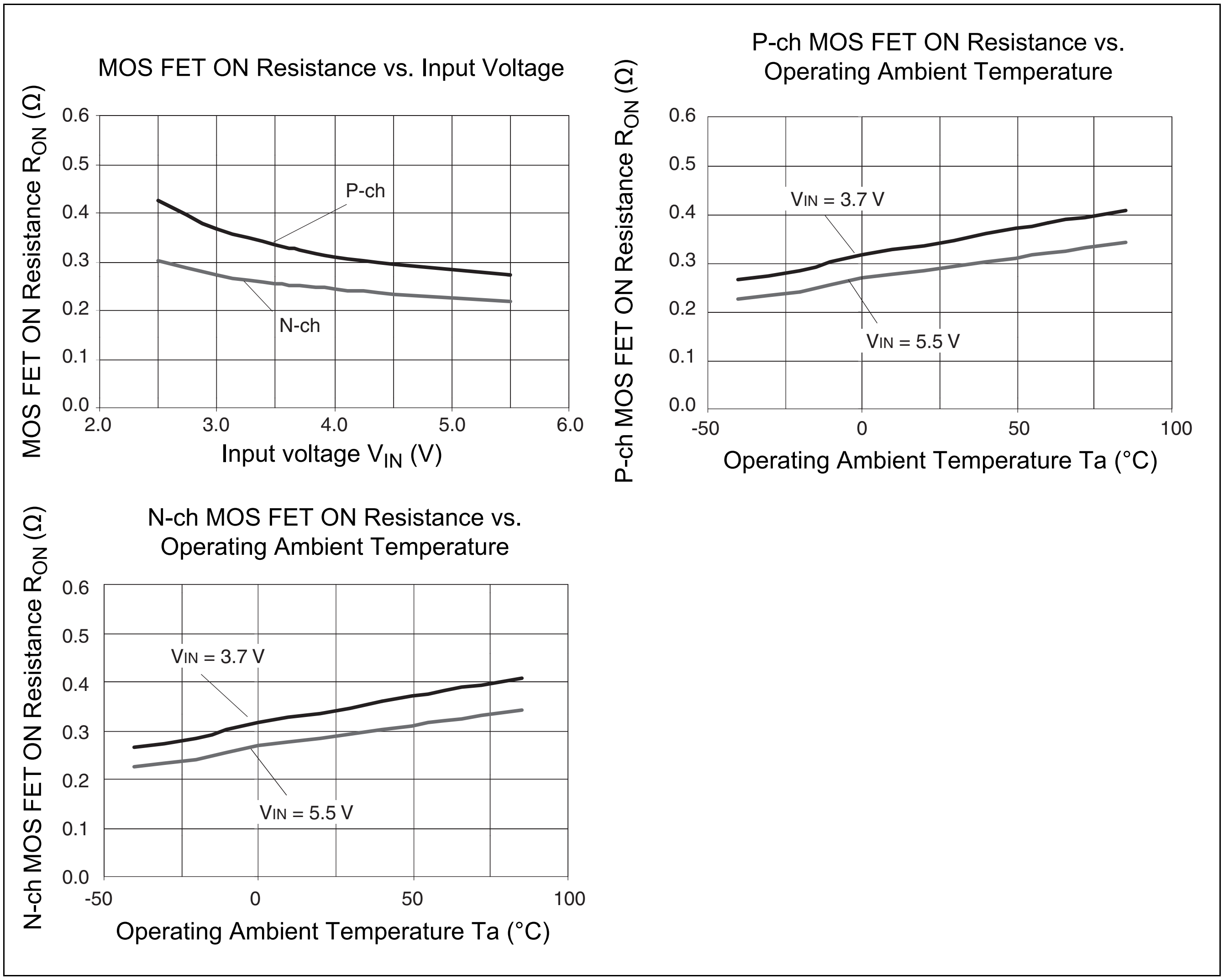
11.8 DC/DC Load Transient Waveforms

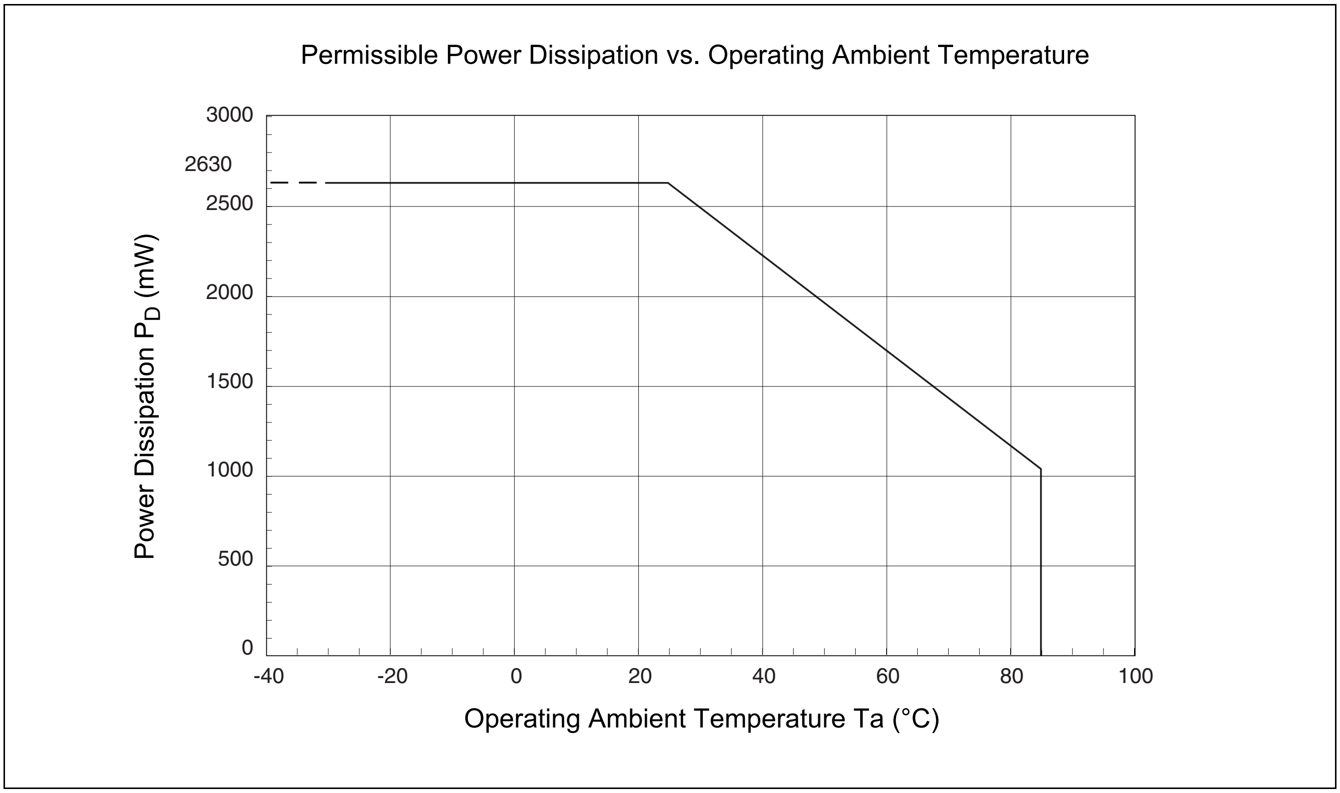
Test Condition :
VIN = EN1 = EN2 = 3.7 V; VO1 = 1.2 V; C1 = 10 µF; C2 = 4.7 µF; VO2 = 3.3 V; C4 = C5 = 4.7 µF



CH1 Load Transient Waveforms

11.9 DC/DC Power MOS FET ON Resistance



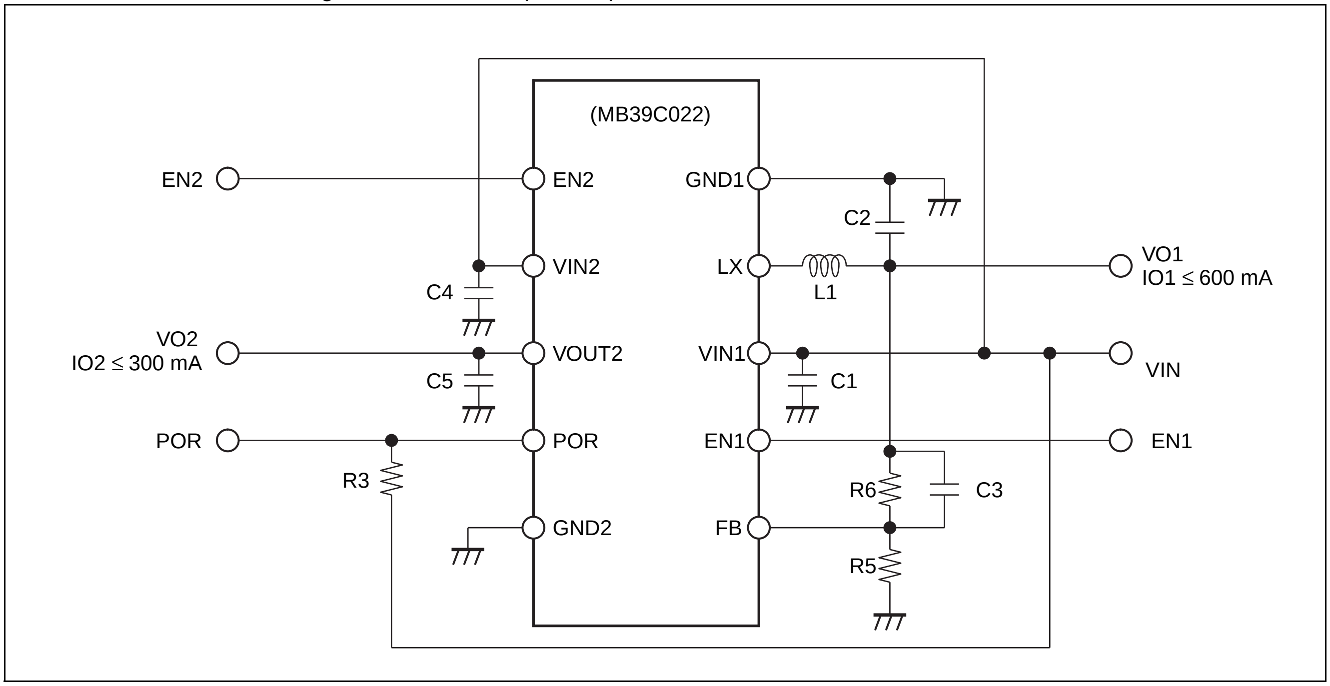


Permissible Power Dissipation vs. Operating Ambient Temperature
3000
2630
2500
2000
1500
1000
500
0
Power Dissipation P_D (mW)
-40
-20
0
20
40
60
80
100
Operating Ambient Temperature Ta (°C)

12. Application Circuits Examples

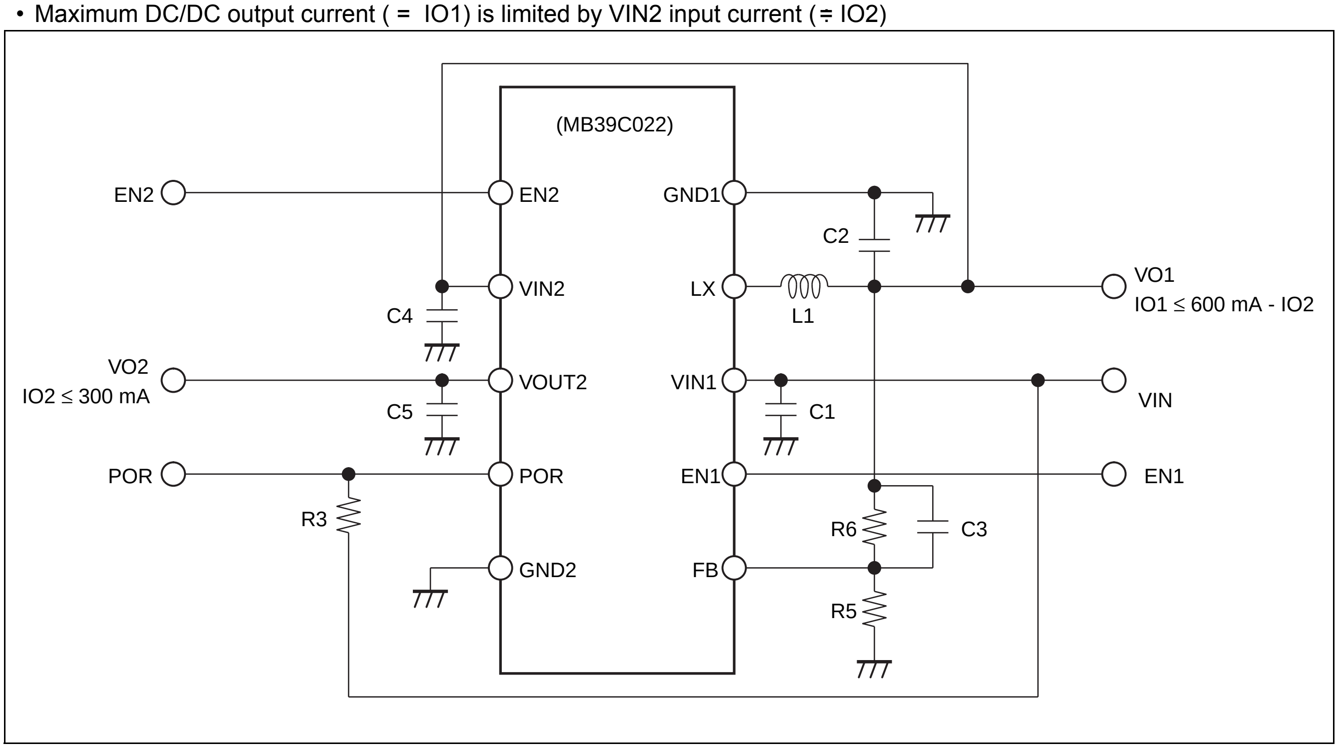
Example 1 (VIN1 = VIN2)

VIN1 and VIN2 are connected together and POR is pulled up to VIN



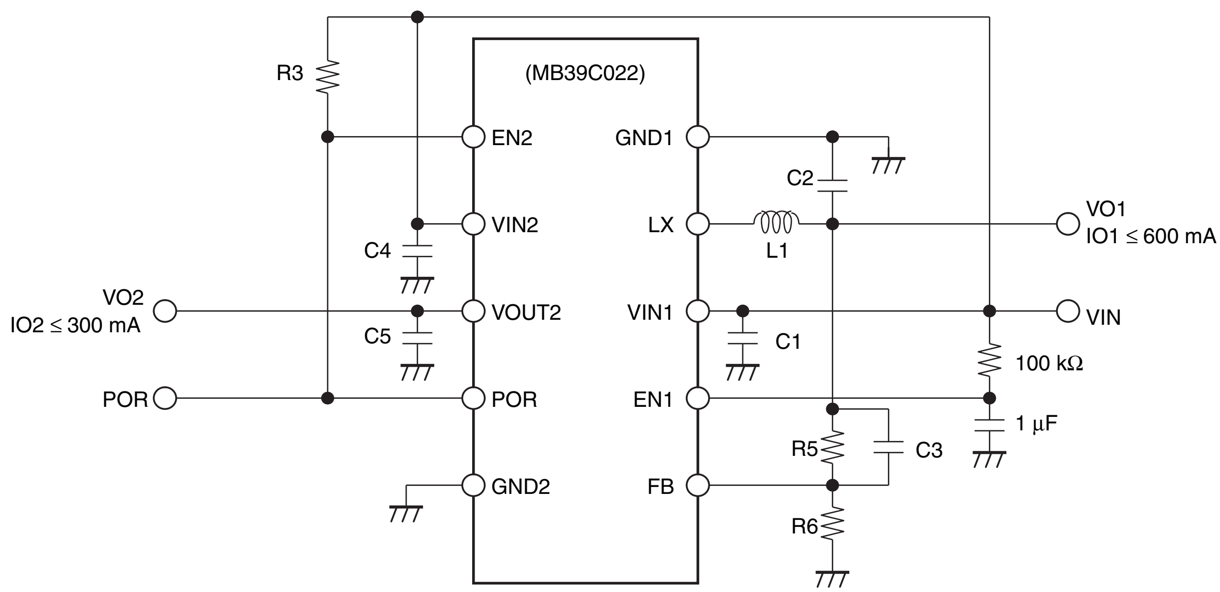
Example 2 (VIN2 = VO1)

- VIN2 is connected to VO1 and POR is pulled up to VIN
- It is possible to maximize LDO efficiency by connecting DC/DC Output to LDO supply.
- Maximum DC/DC output current (= IO1) is limited by VIN2 input current (≒ IO2)

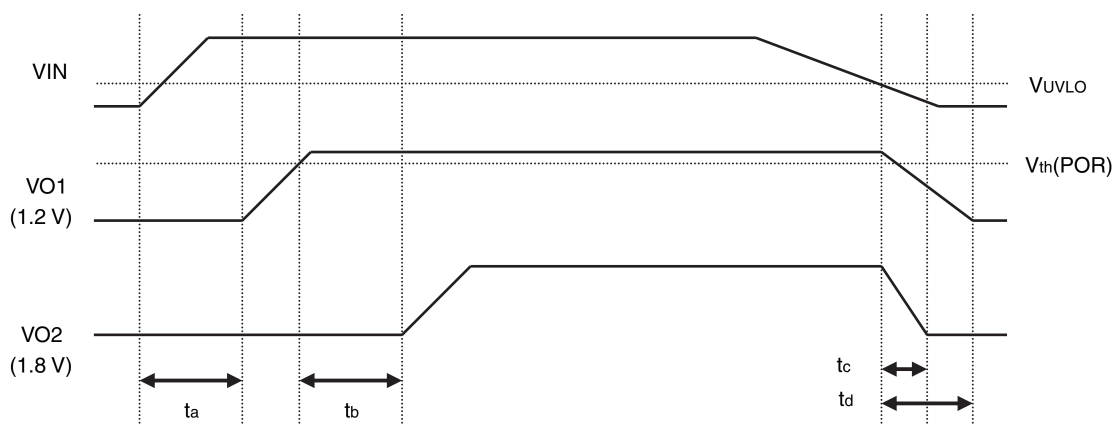


Example 3 (POR and RC delay channel control)

- EN1 is controlled by RC delay and EN2 is controlled by POR output.
- It is possible to control each channel without signal from MCU



Timing chart



Start up control

t_a : RC delay time (28 ms at VIN = 3.7 V, R = 100 kΩ, C = 1 µF)

t_b : POR hold time (66 ms fixed)

Power down control

t_c, t_d : depend on internal discharge path and output loading

13. Usage Precautions

1. **Never use setting exceeding maximum rated conditions**.

   Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. **Use the devices within recommended conditions**

   It is recommended that devices be operated within recommended conditions.
   Exceeding the recommended operating condition may adversely affect devices reliability.
   Nominal electrical characteristics are warranted within the range of recommended operating conditions otherwise specified on each parameter in the section of electrical characteristics.

3. **Design the ground line on printed circuit boards with consideration of common impedance.**

4. **Take appropriate measures against static electricity.**

   The LX pin has less built-in ESD protection than other pins.
   LX pin : 150 V (MM), 1500 V (HBM), Other pins : 200 V (MM), 2000 V (HBM)
   Containers for semiconductor materials should have anti-static protection or be made of conductive material.
   After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
   Work platforms, tools, and instruments should be properly grounded.
   Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.

5. **Do not apply negative voltages**

   The use of negative voltages below −0.3 V may activate parasitic transistors on the device, which can cause abnormal operation.

14. Ordering Information

Part number	Package	Remarks
MB39C022GPN	10-pin plastic SON (LCC-10P-M04)	
MB39C022JPN		
MB39C022LPN		
MB39C022NPN		

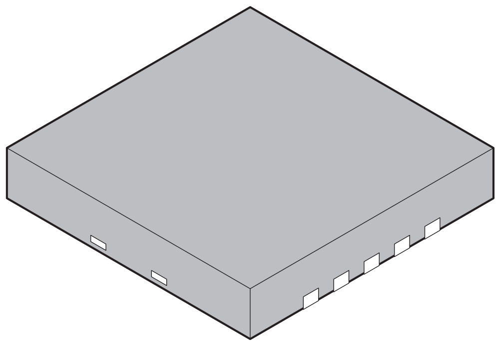
15. RoHS Compliance Information Of Lead(Pb) Free Version

The LSI products of Cypress with “E1” are compliant with RoHS Directive, and has observed the standard of lead, cadmium, mercury, chromium, polybrominated biphenyls (PBB), and polybrominated diphenylethers (PBDE).

A product whose part number has trailing characters “E1” is RoHS compliant.

16. Package Dimension

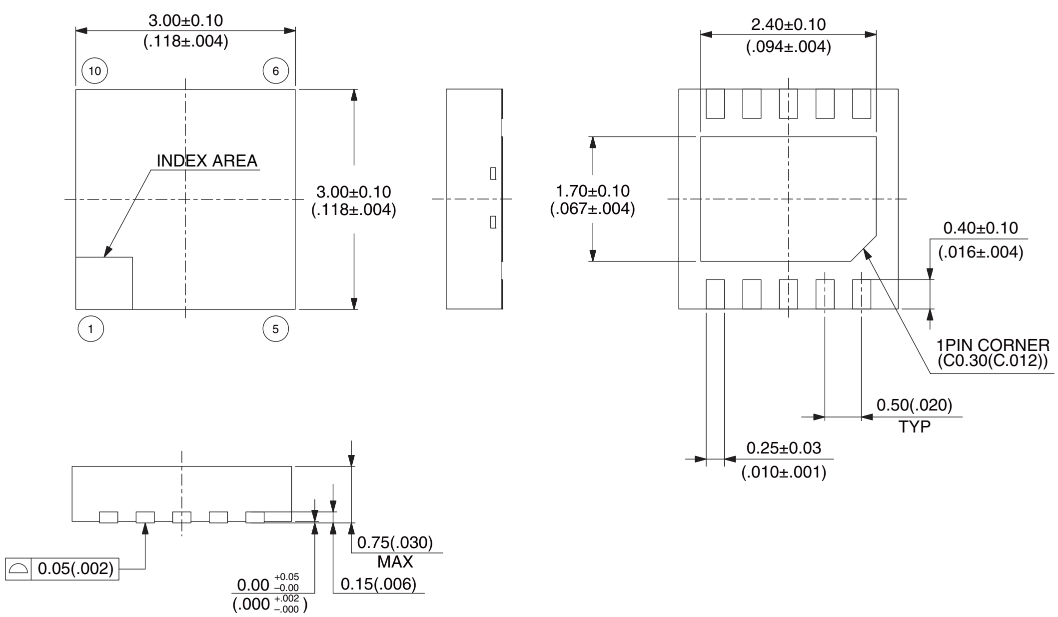
10-pin plastic SON



(LCC-10P-M04)

Lead pitch	0.50 mm
Package width × package length	3.00 mm × 3.00 mm
Sealing method	Plastic mold
Mounting height	0.75 mm MAX
Weight	0.018 g

10-pin plastic SON
(LCC-10P-M04)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Document History Page

Document Title: MB39C022G/J/L/N Buck DC/DC Converter + Low Noise LDO Document Number: 002-08460				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	TAOA	04/13/2009	Initial release
*A	5150068	TAOA	02/24/2016	Migrated Spansion Datasheet from DS04-27271-2E to Cypress format

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Lighting & Power Control	cypress.com/powerpsoc
Memory	cypress.com/memory
PSoC	cypress.com/psoc
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/RF	cypress.com/wireless

PSoC® Solutions

cypress.com/psoc

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/support