12.7 GHz to 15.4 GHz, GaAs, MMIC, Upper Sideband, Differential Upconverter

Data Sheet **ADMV1009**

FEATURES

RF output frequency range: 12.7 GHz to 15.4 GHz
IF input frequency range: 2.8 GHz to 4 GHz
LO input frequency range: 9 GHz to 12.6 GHz
Matched 50 Ω RF output, LO input, and IF input
20 dB of image rejection
32-terminal, 4.9 mm × 4.9 mm LCC package

APPLICATIONS

Point to point microwave radios
Radars and electronic warfare systems
Instrumentation, automatic test equipment

FUNCTIONAL BLOCK DIAGRAM

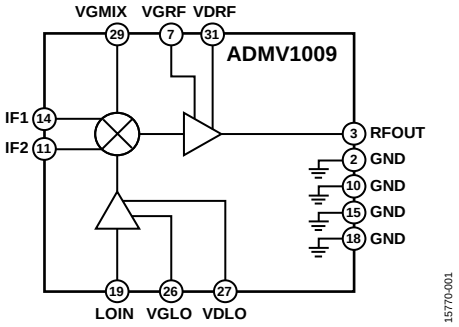

Figure 1.

GENERAL DESCRIPTION

The ADMV1009 is a compact, gallium arsenide (GaAs) design, monolithic microwave integrated circuit (MMIC), upper sideband (USB), differential, upconverter in a RoHS compliant package optimized for point to point microwave radio designs that operate in the 12.7 GHz to 15.4 GHz frequency range.

The ADMV1009 provides 21 dB of conversion gain with 20 dB of sideband rejection. The ADMV1009 uses a radio frequency (RF) amplifier preceded by a passive, double balanced mixer, where a driver amplifier drives the local oscillator (LO). IF1 and IF2 mixer inputs are provided, and an external 180° balun is needed to drive the IF pins differentially. The ADMV1009 is a much smaller alternative to hybrid style single sideband (SSB) upconverter assemblies and eliminates the need for wire bonding by allowing the use of surface-mount manufacturing assemblies.

The ADMV1009 upconverter comes in a compact, thermally enhanced, 4.9 mm × 4.9 mm LCC package. The ADMV1009 operates over the −40°C to +85°C temperature range.

Rev. B Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

4/2018—Rev. A to Rev. B

Changes to Thermal Resistance Section and Table 3 ... 4

1/2018—Rev. 0 to Rev. A

Change to Product Title ... 1
Changes to General Description and Figure 1 ... 1
Changes to Table 1 ... 3
Changes to Table 2 ... 4
Added Thermal Resistance Section and Table 3; Renumbered Sequentially ... 4
Changes to Figure 2 and Table 4 ... 5
Changes to Figure 4, Figure 7, Figure 4 Caption, and Figure 7 Caption ... 6
Changes to Figure 14, Figure 17, Figure 14 Caption, and Figure 17 Caption ... 8
Changes to Figure 24, Figure 27, Figure 24 Caption, and Figure 27 Caption ... 10
Changes to Figure 35 and Figure 36 ... 12
Changes to Figure 37 through Figure 40 ... 13
Changes to Figure 47 through Figure 52 ... 15
Changes to Figure 53 through Figure 58 ... 16
Changes to Table 5 and M × N Spurious Performance Section ... 17
Change to Theory of Operation Section ... 18
Changes to Figure 59 ... 19
Changes to Power On Sequence Section and Power Off Sequence Section ... 20
Change to Table 6 ... 22
Changes to Ordering Guide ... 23

10/2017—Revision 0: Initial Version

SPECIFICATIONS

VDRF = 5 V, VDLO = 5 V, IDLO = 60 mA, IDRF = 250 mA, LO = −4 dBm ≤ LO ≤ +4 dBm, −40°C ≤ T_A ≤ +85°C; data taken with Mini-Circuits NCS1-422+, RF transformer as upper sideband, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
RF OUTPUT FREQUENCY RANGE			12.7		15.4	GHz
INPUT FREQUENCY RANGE						
Local Oscillator	LO		9		12.6	GHz
Intermediate Frequency	IF		2.8		4	GHz
LO AMPLITUDE			−4	0	+4	dBm
IF INPUT POWER			−25		0	dBm
PERFORMANCE		With balun				
Conversion Gain			15	21	25	dB
Noise Figure	NF			14	16.5	dB
Output Third-Order Intercept	IP3	At output power (P_{OUT}) = 8 dBm	31	35		dBm
Output 1 dB Compression Point	P1dB		23	25		dBm
Sideband Rejection			20	60		dBc
Leakage						
LO to RF				−30	−10	dBm
LO to IF				−25	−20	dBm
RF Output		IF = 0 dBm				
2× LO − 2× IF Spur			45	52		dBc
4× IF Spur			70	75		dBc
Return Loss						
RF Output				12	10	dB
LO Input		−4 dBm ≤ LO ≤ +4 dBm		12	10	dB
IF Input				11	10	dB
POWER INTERFACE						
Amplifier Voltage						
RF	VDRF			5		V
LO	VDLO			5		V
Gate Voltage						
RF	VGRF		−1.5		−0.5	V
LO	VGLO		−1.5		−0.5	V
Mixer Voltage	VGMIX			−1.1		V
Amplifier Current						
RF	IDRF	Adjust VGRF between −1.5 V and −0.5 V to achieve IDRF		250	300	mA
LO	IDLO	Adjust VGLO between −1.5 V and −0.5 V to achieve IDLO		60		mA
Gate Current						
RF	IGRF			< 3		mA
LO	IGLO			< 1		mA
Total Power				1.55		W

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	
VDRF	6 V
VDLO	6 V
VGLO	−2 V to 0 V
VGRF	−2 V to 0 V
VGMIX	−2 V to 0 V
Maximum Junction Temperature	175°C
Lifetime at Maximum Junction Temperature	>1 million hours
Maximum Power Dissipation	2.9 W
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Moisture Sensitivity Level (MSL) Rating	MSL3
Input Power	
LO	15 dBm
IF	15 dBm
Lead Temperature Range (Soldering 60 sec)	260°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	750 V
Field Induced Charged Device Model (FICDM)	750 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is thermal resistance, junction to ambient (°C/W), and θ_{JC} is thermal resistance, junction to case (°C/W).

Table 3.

Package Type	θ_{JA}[1]	θ_{JC}[1]	Unit
E-32-1	33.4	31	°C/W

[1] See JEDEC standard JESD51-2 for additional information on optimal thermal impedance (printed circuit board (PCB) within 3 × 3 vias)

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

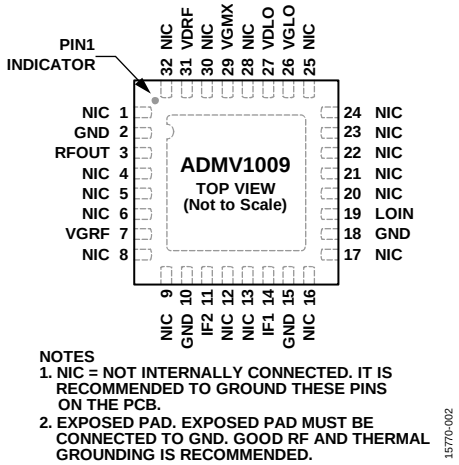

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4 to 6, 8, 9, 12, 13, 16, 17, 20 to 25, 28, 30, 32	NIC	Not Internally Connected. It is recommended to ground these pins on the PCB.
2, 10, 15, 18	GND	Ground. These pins are grounded internally and must also be grounded on the PCB.
3	RFOUT	RF Output. This pin is ac-coupled internally and matched to 50 Ω, single-ended.
7	VGRF	Power Supply Voltage for the Gate of the RF Amplifier. Refer to the Applications Information section for the required external components and biasing.
11, 14	IF2, IF1	Differential IF Inputs. These pins are matched to 50 Ω and are ac-coupled. No external dc block is required.
19	LOIN	Local Oscillator Input. This pin is ac-coupled and matched to 50 Ω.
26	VGLO	Power Supply Voltage for the Gate of the LO Amplifier. Refer to the Applications Information section for the required external components and biasing.
27	VDLO	Power Supply Voltage for the LO Amplifier. Refer to the Applications Information section for the required external components and biasing.
29	VGMIX	Power Supply Voltage for the Mixer. This pin is a high impedance port. Refer to the Applications Information section for the required external components and biasing.
31	VDRF	Power Supply Voltage for the RF Amplifier. Refer to the Applications Information section for the required external components and biasing.
	EPAD	Exposed pad. The exposed pad must be connected to GND. Good RF and thermal grounding is recommended.

TYPICAL PERFORMANCE CHARACTERISTICS

IF FREQUENCY = 2.8 GHz

VDRF = 5 V, VDLO = 5 V, IDLO = 60 mA, IDRF = 250 mA, LO = −4 dBm ≤ LO ≤ +4 dBm, −40°C ≤ T_A ≤ +85°C, data taken with Mini-Circuits NCS1-422+, RF transformer as upper sideband, unless otherwise noted.

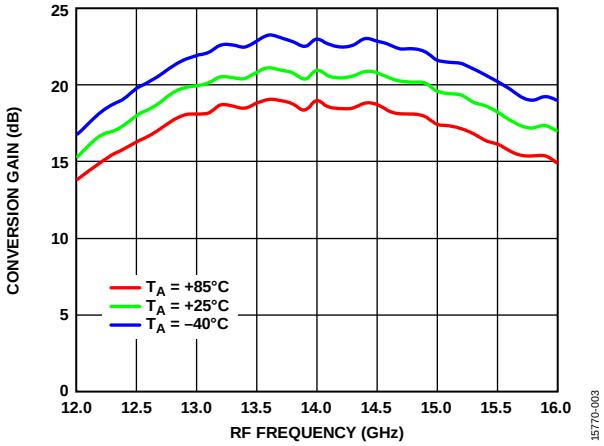

Figure 3. Conversion Gain vs. RF Frequency at Various Temperatures

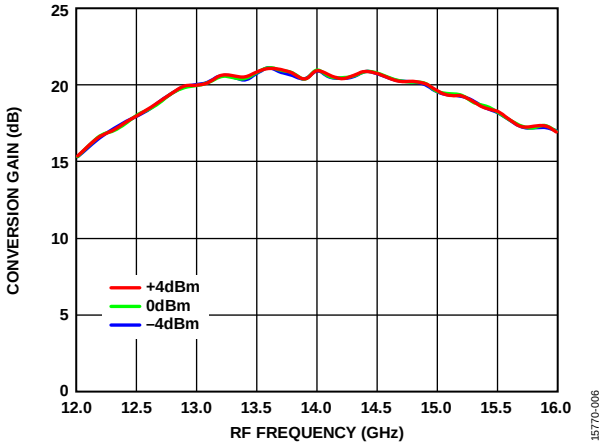

Figure 6. Conversion Gain vs. RF Frequency at Various LO Powers

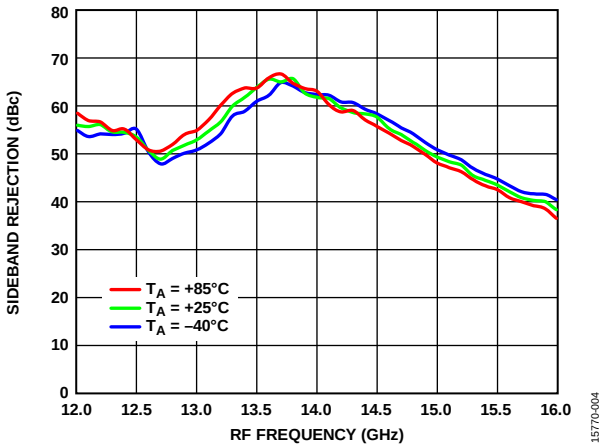

Figure 4. Sideband Rejection vs. RF Frequency at Various Temperatures

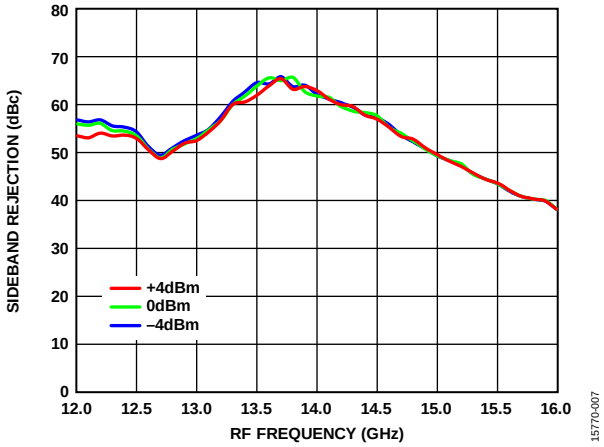

Figure 7. Sideband Rejection vs. RF Frequency at Various LO Powers

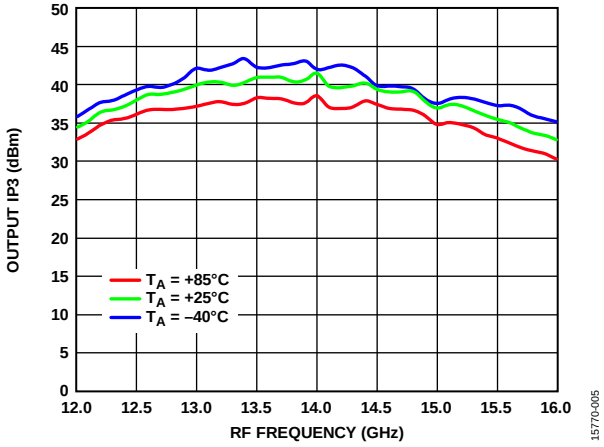

Figure 5. Output IP3 vs. RF Frequency at Various Temperatures

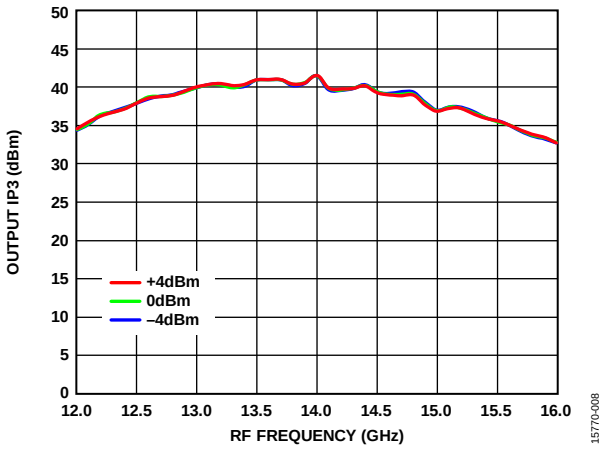

Figure 8. Output IP3 vs. RF Frequency at Various LO Powers

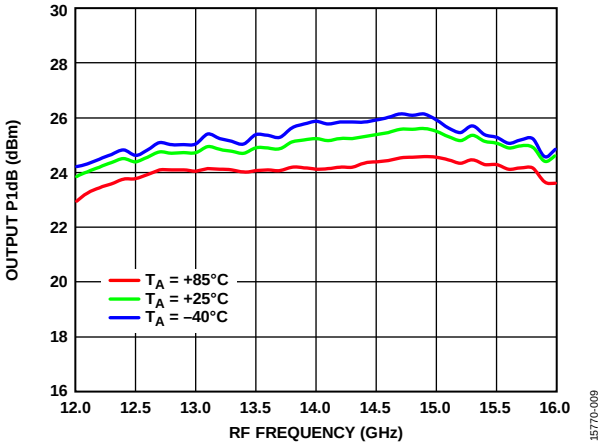

Figure 9. Output P1dB vs. RF Frequency at Various Temperatures

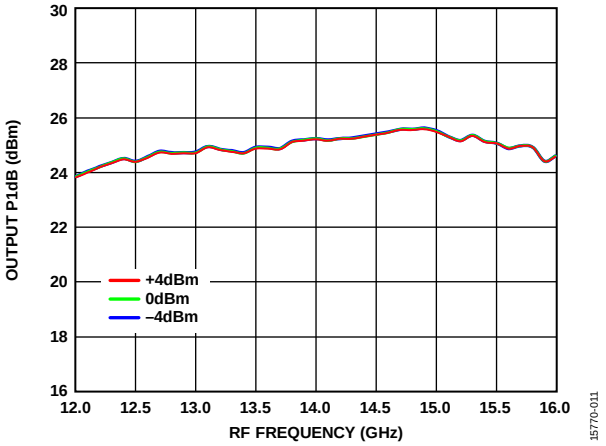

Figure 11. Output P1dB vs. RF Frequency at Various LO Powers

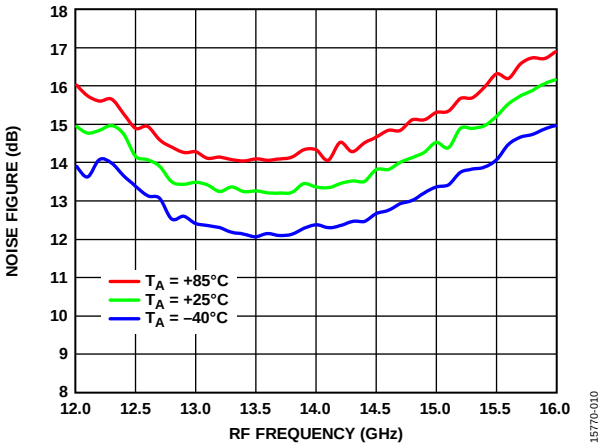

Figure 10. Noise Figure vs. RF Frequency at Various Temperatures

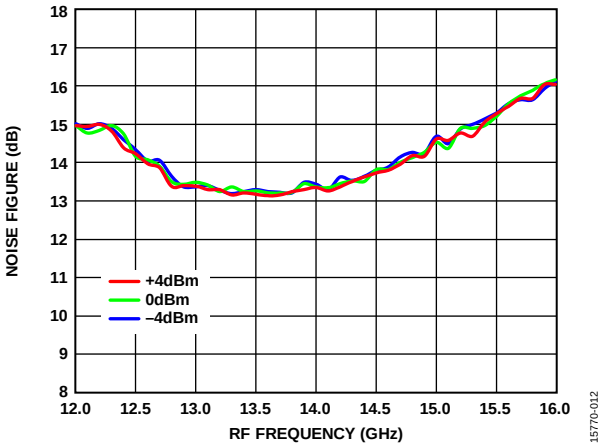

Figure 12. Noise Figure vs. RF Frequency at Various LO Powers

IF FREQUENCY = 3.4 GHz

VDRF = 5 V, VDLO = 5 V, IDLO = 60 mA, IDRF = 250 mA, LO = −4 dBm ≤ LO ≤ +4 dBm, −40°C ≤ T_A ≤ +85°C, data taken with Mini-Circuits NCS1-422+, RF transformer as upper sideband, unless otherwise noted.

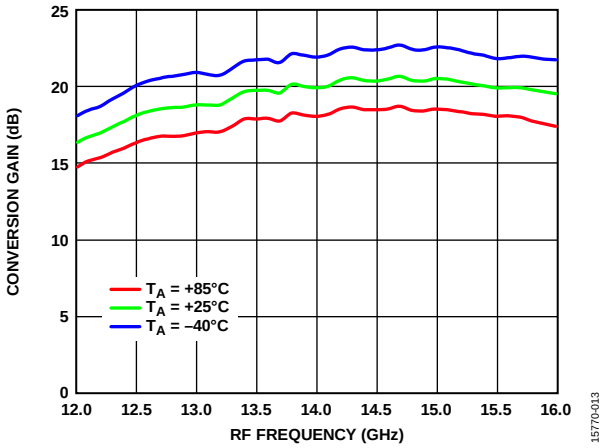

Figure 13. Conversion Gain vs. RF Frequency at Various Temperatures

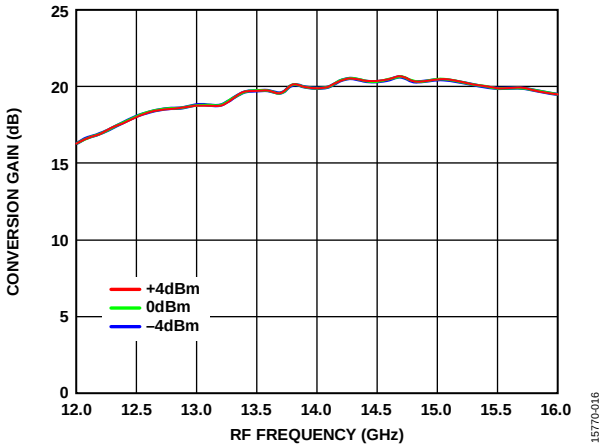

Figure 16. Conversion Gain vs. RF Frequency at Various LO Powers

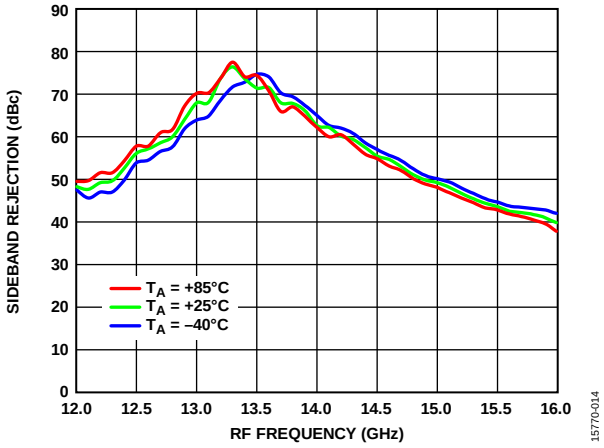

Figure 14. Sideband Rejection vs. RF Frequency at Various Temperatures

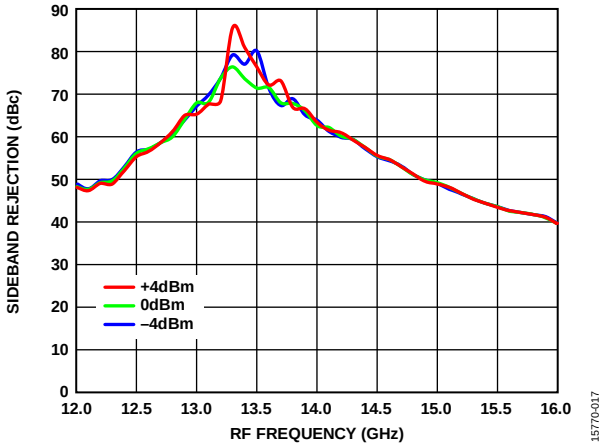

Figure 17. Sideband Rejection vs. RF Frequency at Various LO Powers

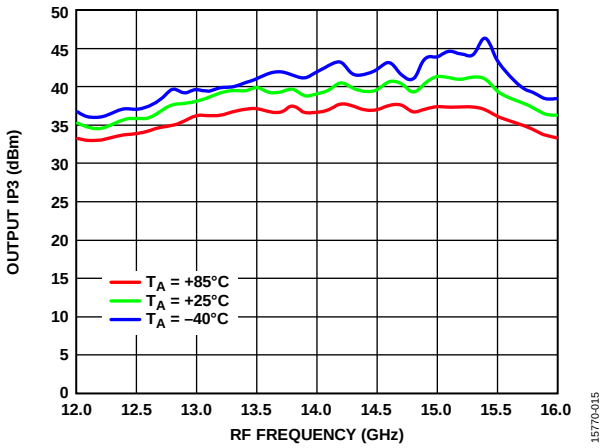

Figure 15. Output IP3 vs. RF Frequency at Various Temperatures

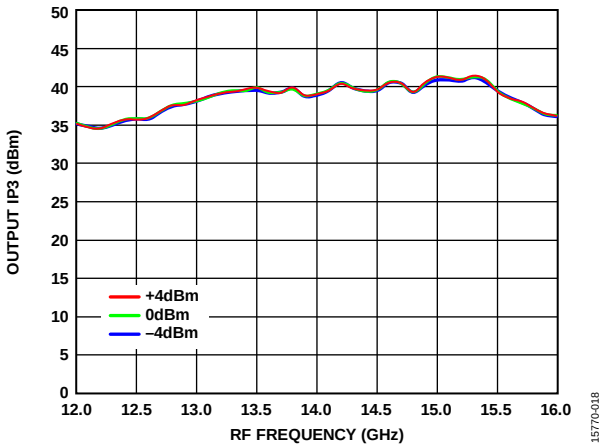

Figure 18. Output IP3 vs. RF Frequency at Various LO Powers

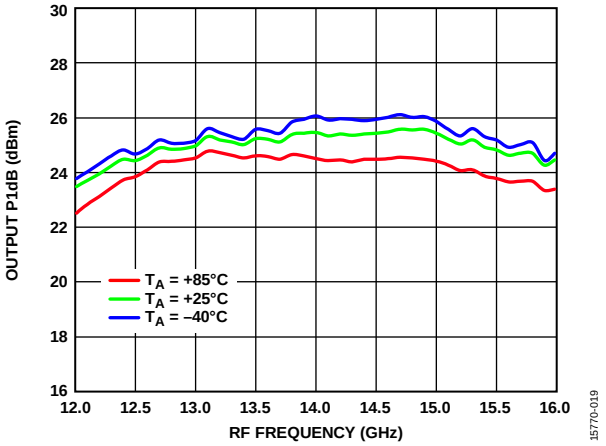

Figure 19. Output P1dB vs. RF Frequency at Various Temperatures

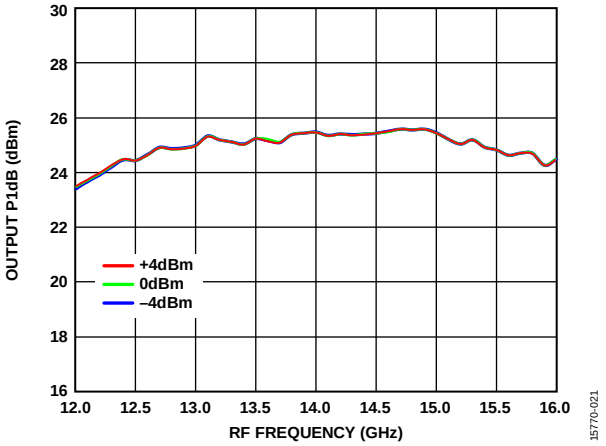

Figure 21. Output P1dB vs. RF Frequency at Various LO Powers

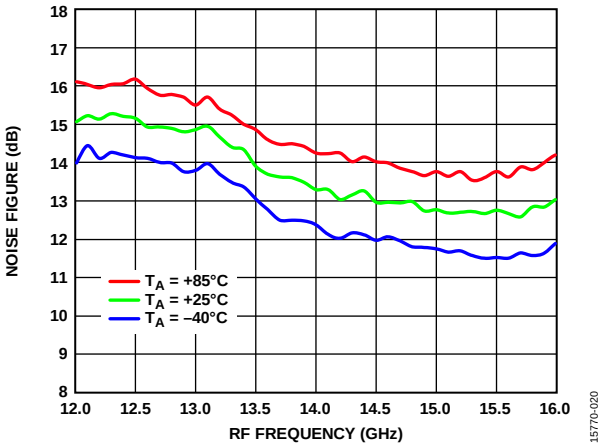

Figure 20. Noise Figure vs. RF Frequency at Various Temperatures

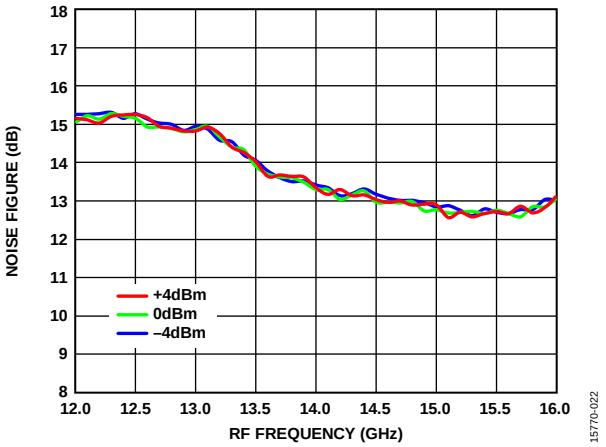

Figure 22. Noise Figure vs. RF Frequency at Various LO Powers

IF FREQUENCY = 4 GHz

VDRF = 5 V, VDLO = 5 V, IDLO = 60 mA, IDRF = 250 mA, LO = −4 dBm ≤ LO ≤ +4 dBm, −40°C ≤ T_A ≤ +85°C, data taken with Mini-Circuits NCS1-422+, RF transformer as upper sideband, unless otherwise noted.

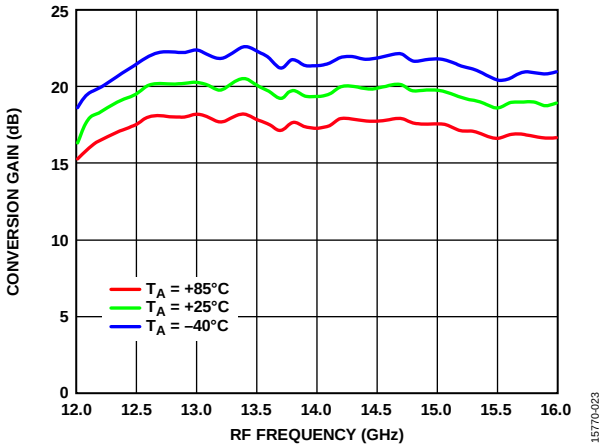

Figure 23. Conversion Gain vs. RF Frequency at Various Temperatures

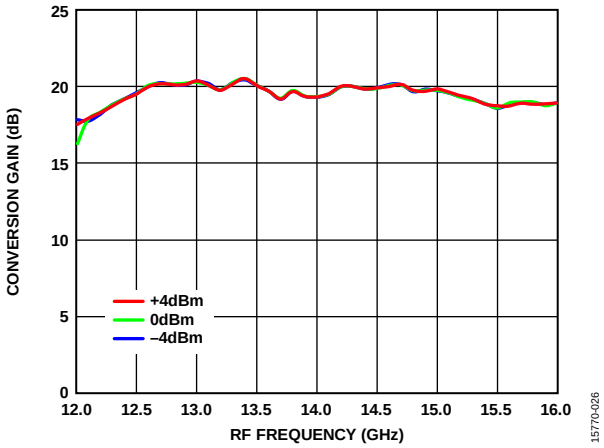

Figure 26. Conversion Gain vs. RF Frequency at Various LO Powers

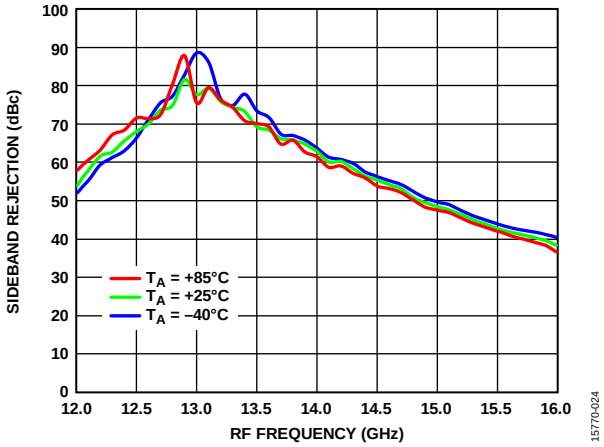

Figure 24. Sideband Rejection vs. RF Frequency at Various Temperatures

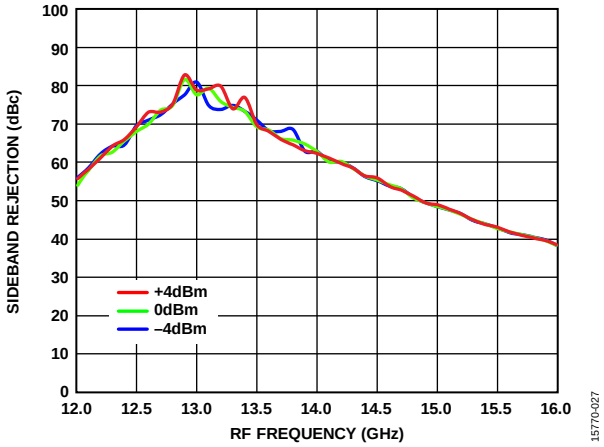

Figure 27. Sideband Rejection vs. RF Frequency at Various LO Powers

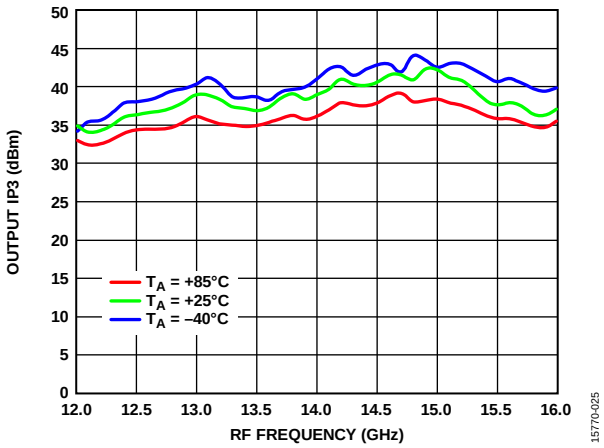

Figure 25. Output IP3 vs. RF Frequency at Various Temperatures

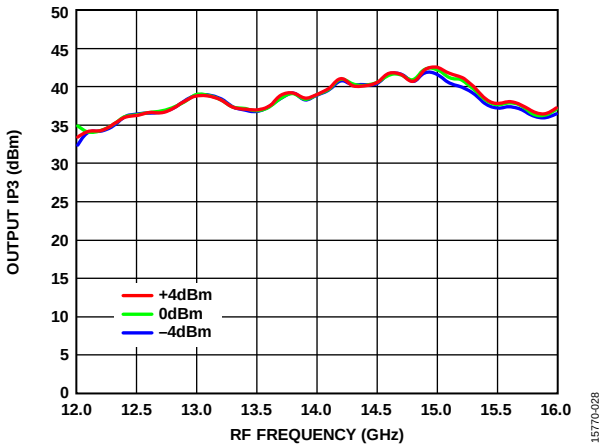

Figure 28. Output IP3 vs. RF Frequency at Various LO Powers

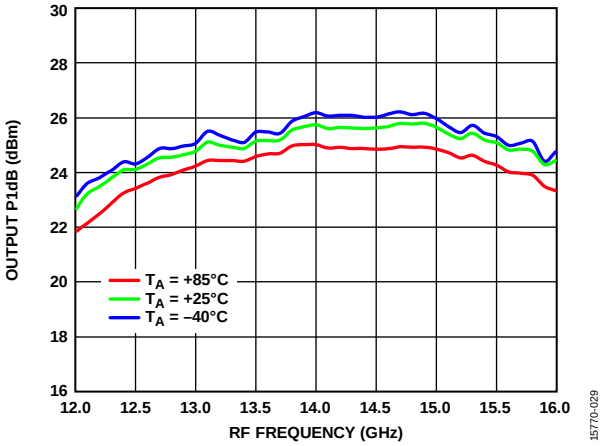

Figure 29. Output P1dB vs. RF Frequency at Various Temperatures

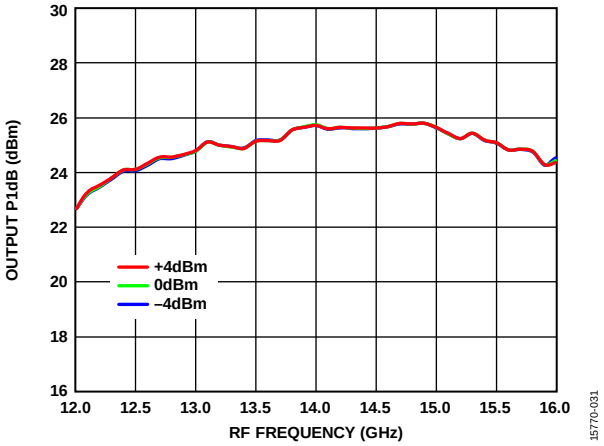

Figure 31. Output P1dB vs. RF Frequency at Various LO Powers

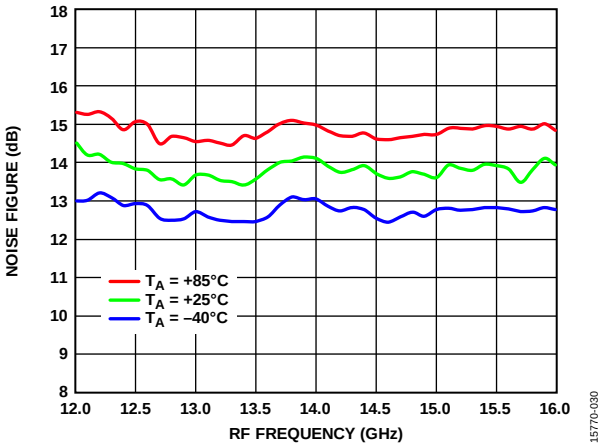

Figure 30. Noise Figure vs. RF Frequency at Various Temperatures

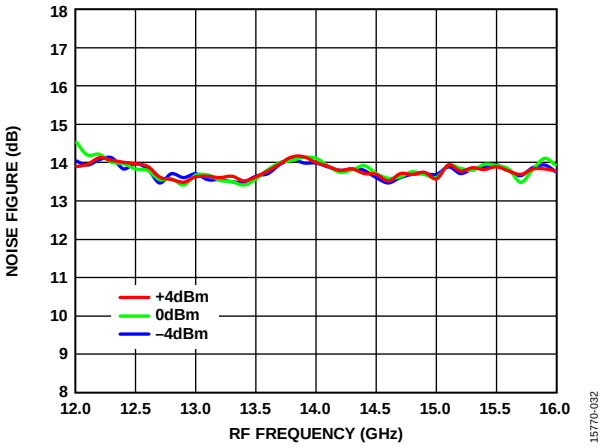

Figure 32. Noise Figure vs. RF Frequency at Various LO Powers

IF BANDWIDTH

VDRF = 5 V, VDLO = 5 V, IDLO = 60 mA, IDRF = 250 mA, LO = −4 dBm ≤ LO ≤ +4 dBm at 10.2 GHz, −40°C ≤ T_A ≤ +85°C, data taken with Mini-Circuits NCS1-422+, RF transformer as upper sideband, unless otherwise noted.

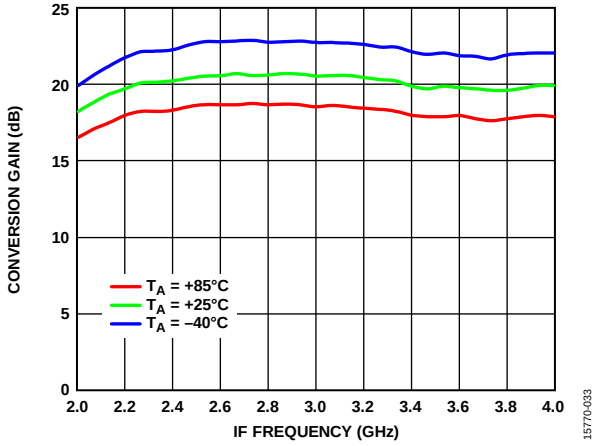

Figure 33. Conversion Gain vs. IF Frequency at Various Temperatures

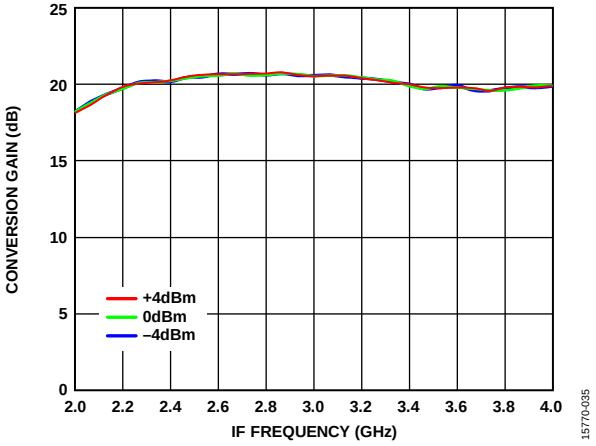

Figure 35. Conversion Gain vs. IF Frequency at Various LO Powers

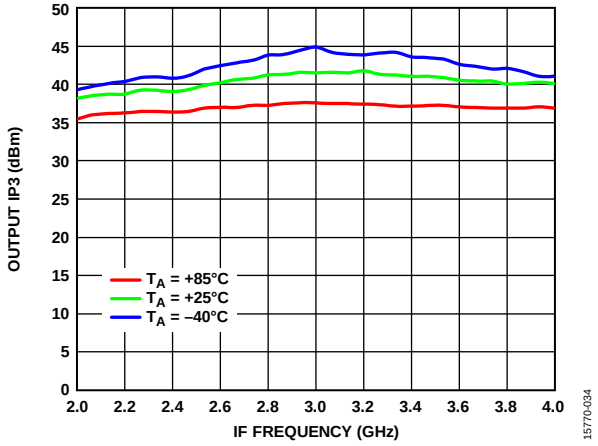

Figure 34. Output IP3 vs. IF Frequency at Various Temperatures

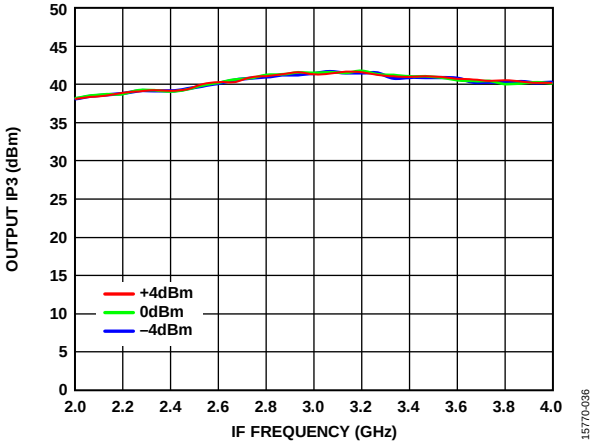

Figure 36. Output IP3 vs. IF Frequency at Various LO Powers

LEAKAGE PERFORMANCE

VDRF = 5 V, VDLO = 5 V, IDLO = 60 mA, IDRF = 250 mA, LO = −4 dBm ≤ LO ≤ +4 dBm, −40°C ≤ T_A ≤ +85°C, data taken with Mini-Circuits NCS1-422+, RF transformer as upper sideband, unless otherwise noted.

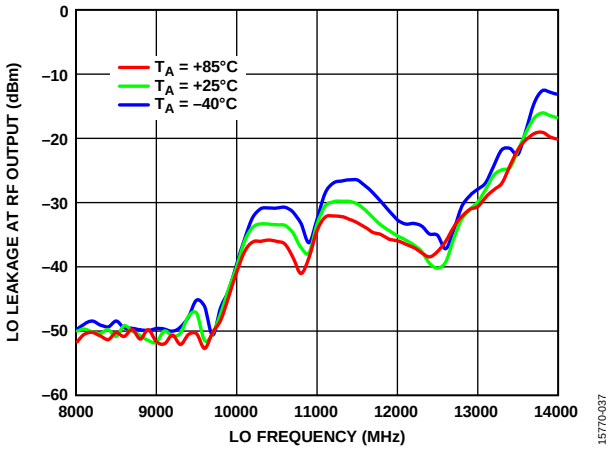

Figure 37. LO Leakage at RFOUT vs. LO Frequency at Various Temperatures

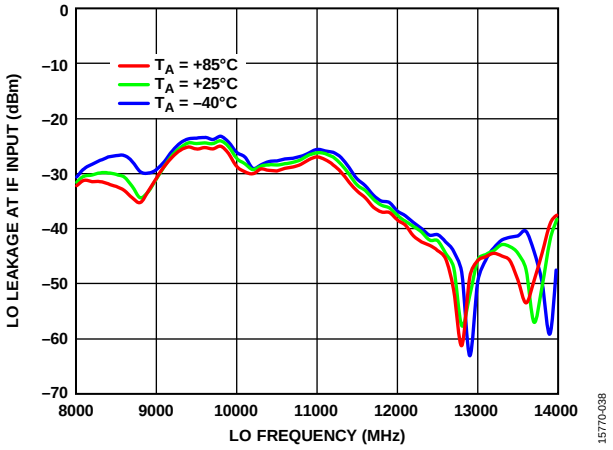

Figure 38. LO Leakage at IF Input vs. LO Frequency at Various Temperatures

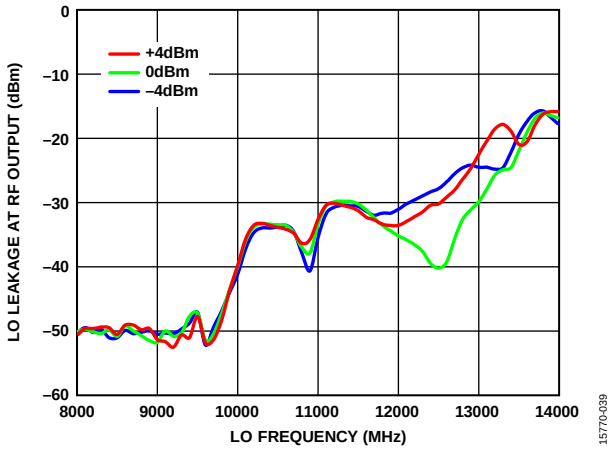

Figure 39. LO Leakage at RFOUT vs. LO Frequency at Various LO Powers

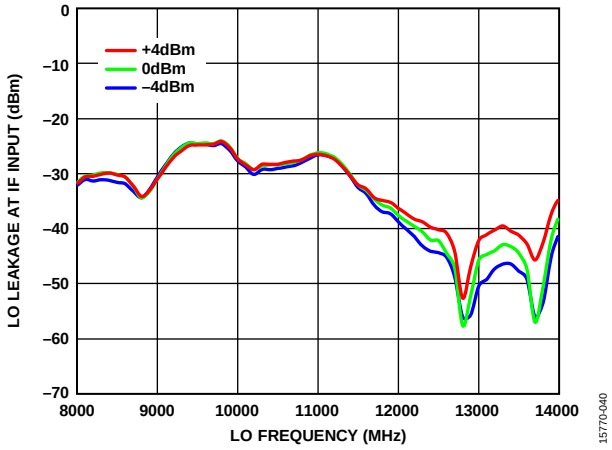

Figure 40. LO Leakage at IF Input vs. LO Frequency at Various LO Powers

RETURN LOSS PERFORMANCE

VDRF = 5 V, VDLO = 5 V, IDLO = 60 mA, IDRF = 250 mA, LO = −4 dBm ≤ LO ≤ +4 dBm, −40°C ≤ T_A ≤ +85°C, data taken with Mini-Circuits NCS1-422+, RF transformer as upper sideband, unless otherwise noted. Measurement includes trace loss and RF connector loss.

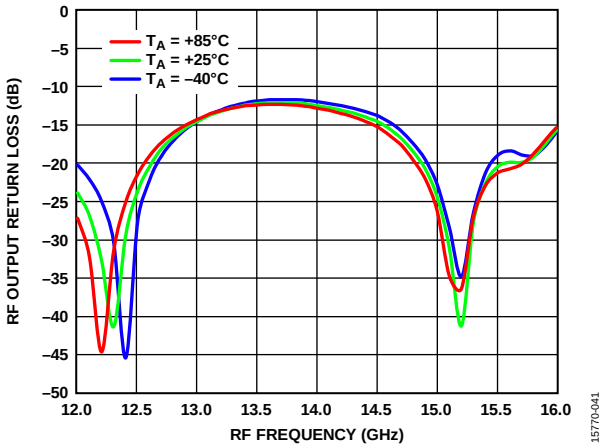

Figure 41. RF Output Return Loss vs. RF Frequency at Various Temperatures

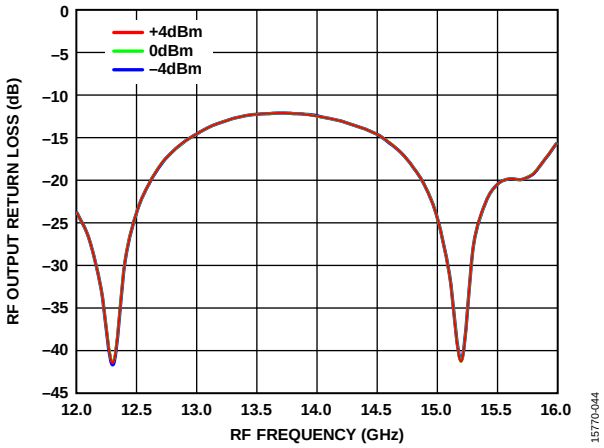

Figure 44. RF Output Return Loss vs. RF Frequency at Various LO Powers

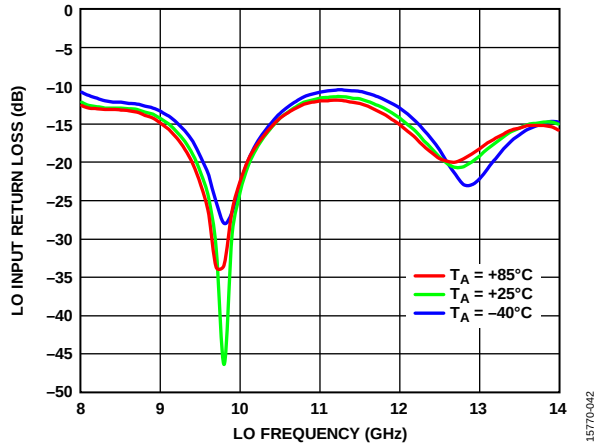

Figure 42. LO Input Return Loss vs. LO Frequency at Various Temperatures

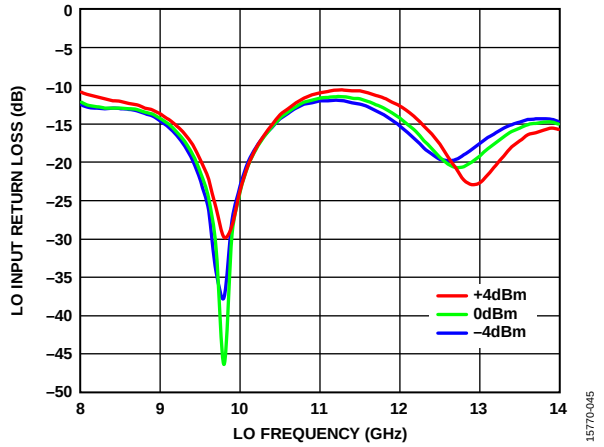

Figure 45. LO Input Return Loss vs. LO Frequency at Various LO Powers

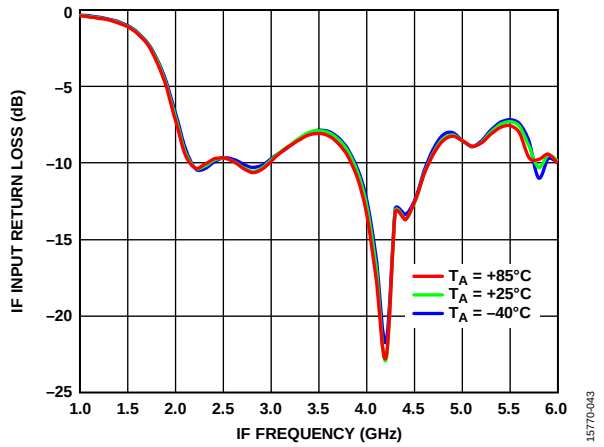

Figure 43. IF Input Return Loss vs. IF Frequency at Various Temperatures

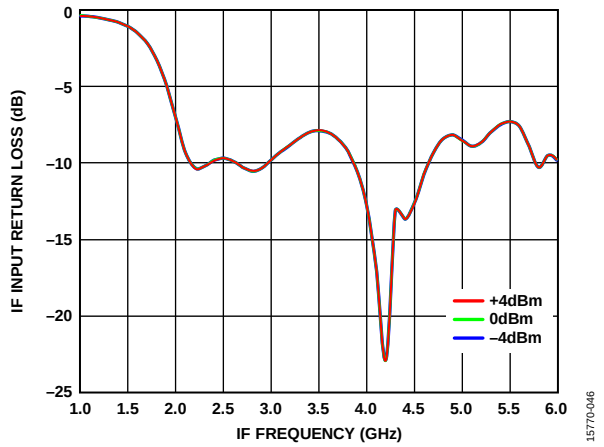

Figure 46. IF Input Return Loss vs. IF Frequency at Various LO Powers

SPURIOUS PERFORMANCE

VDRF = 5 V, VDLO = 5 V, IDLO = 60 mA, IDRF = 250 mA, LO = 0 dBm, −40°C ≤ T_A ≤ +85°C, data taken with Mini-Circuits NCS1-422+, RF transformer as upper sideband, unless otherwise noted.

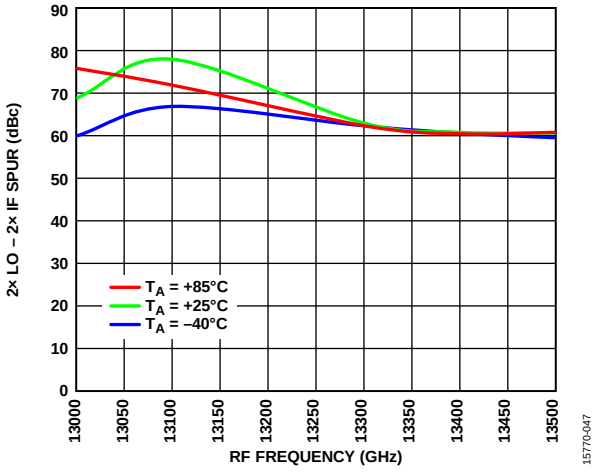

Figure 47. 2× LO – 2× IF Leakage vs. RF Frequency at Various Temperatures, IF = 3.1 GHz, −10 dBm

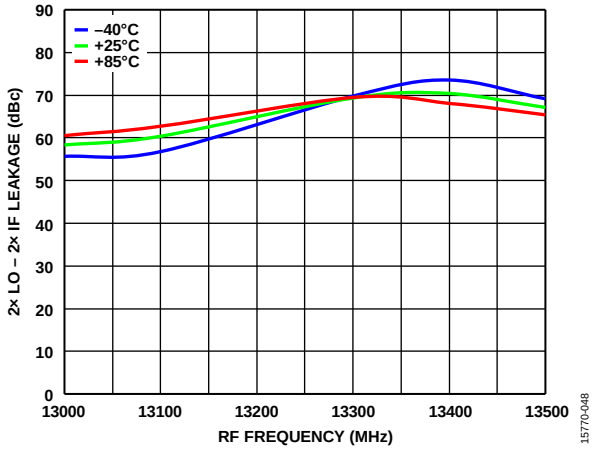

Figure 48. 2× LO – 2× IF Leakage vs. RF Frequency at Various Temperatures, IF = 3.3 GHz, −10 dBm

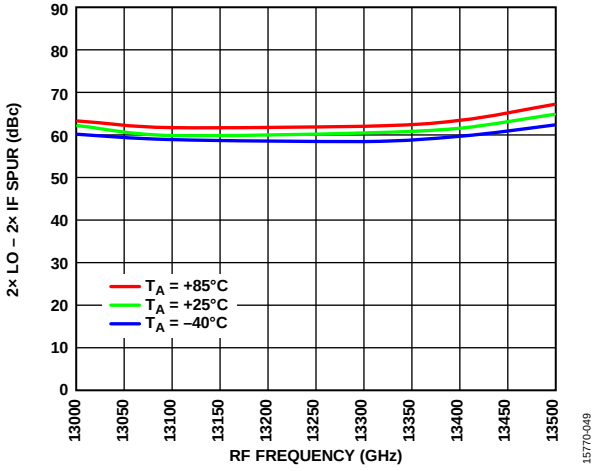

Figure 49. 2× LO – 2× IF Leakage vs. RF Frequency at Various Temperatures, IF = 3.5 GHz, −10 dBm

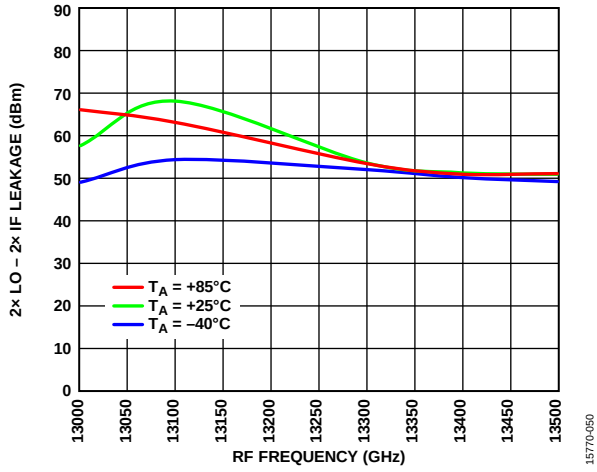

Figure 50. 2× LO – 2× IF Leakage vs. RF Frequency at Various Temperatures, IF = 3.1 GHz, 0 dBm

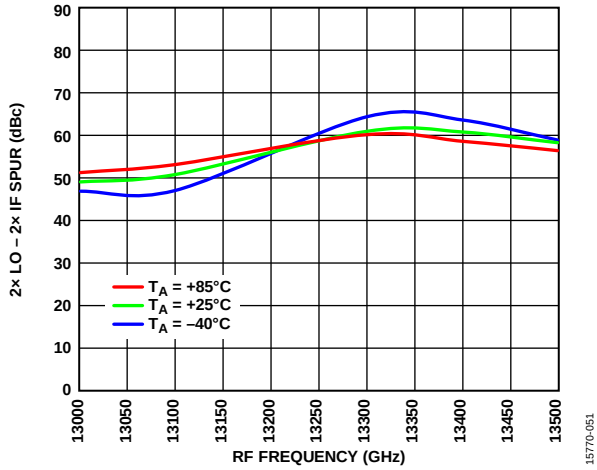

Figure 51. 2× LO – 2× IF Leakage vs RF Frequency at Various Temperatures, IF = 3.3 GHz, 0 dBm

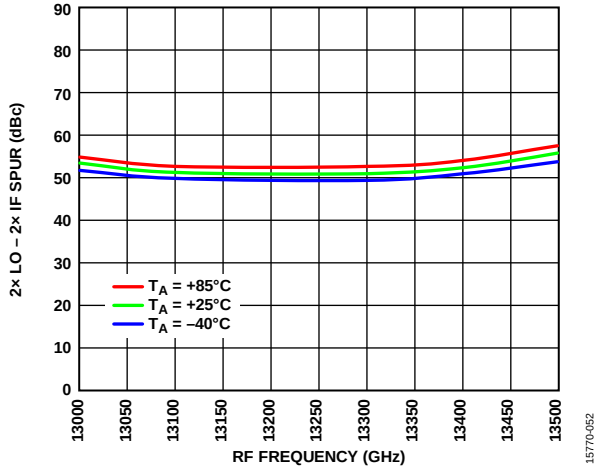

Figure 52. 2× LO – 2× IF Leakage vs RF Frequency at Various Temperatures, IF = 3.5 GHz, 0 dBm

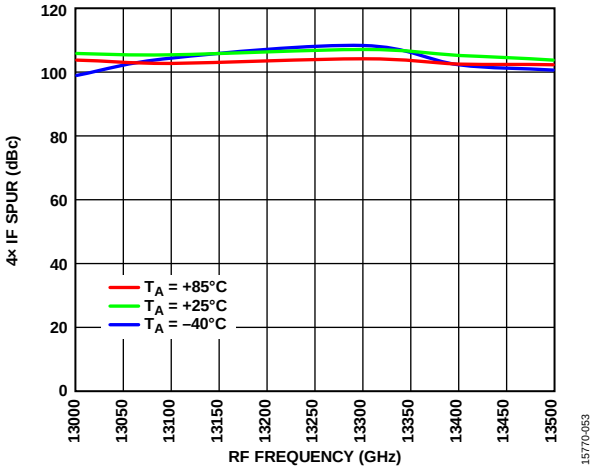

Figure 53. 4× IF Leakage vs. RF Frequency at Various Temperatures, IF = 3.1 GHz, −10 dBm

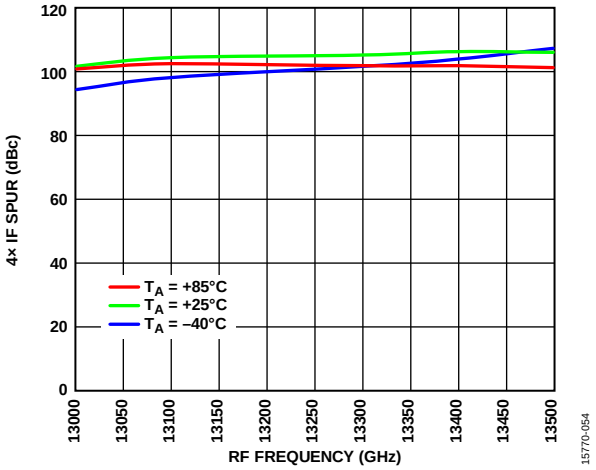

Figure 54. 4× IF Leakage vs. RF Frequency at Various Temperatures, IF = 3.3 GHz, −10 dBm

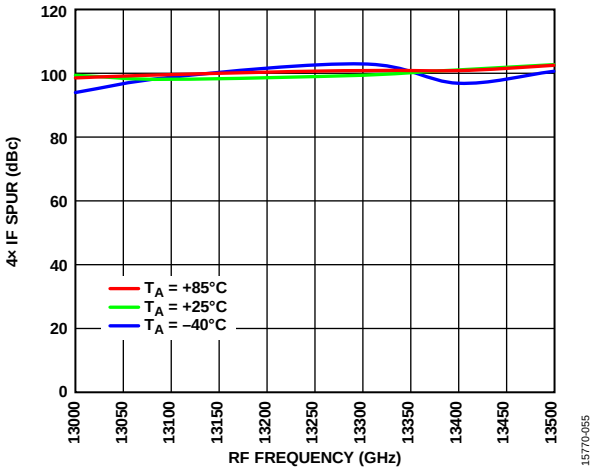

Figure 55. 4× IF Leakage vs. RF Frequency at Various Temperatures, IF = 3.5 GHz, −10 dBm

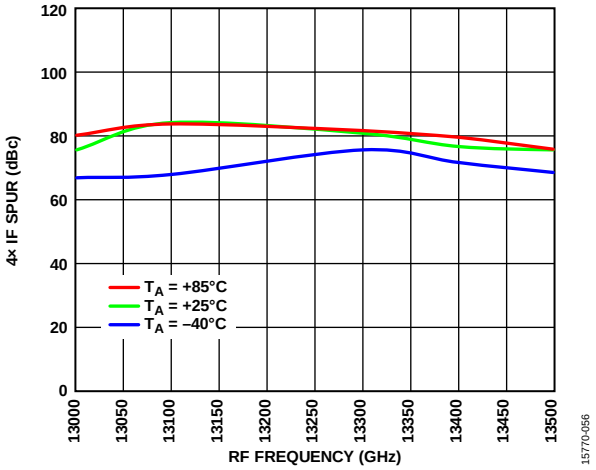

Figure 56. 4× IF Leakage vs. RF Frequency at Various Temperatures, IF = 3.1 GHz, 0 dBm

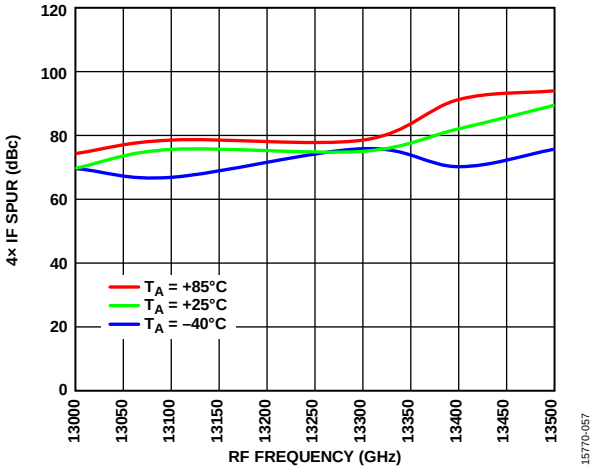

Figure 57. 4× IF Leakage vs. RF Frequency at Various Temperatures, IF = 3.3 GHz, 0 dBm

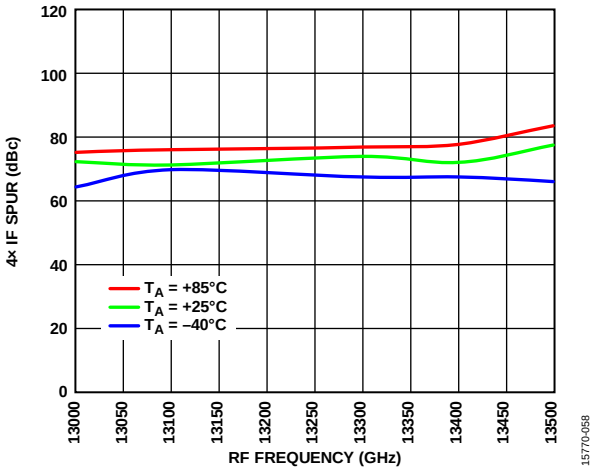

Figure 58. 4× IF Leakage vs. RF Frequency at Various Temperatures, IF = 3.5 GHz, 0 dBm

Table 5. LO Harmonic Leakage at RFOUT

	Harmonics			
LO Frequency (MHz)[1]	**1.0**	**2.0**	**3.0**	**4.0**
9000	−51	−14	−50	−72
9500	−48	−5	−55	−67
10000	−40	−15	−51	−63
10500	−33	−28	−67	−62
11000	−33	−44	−74	−75
11500	−30	−44	−63	−77
12000	−35	−44	−73	−76
12600	−39	−40	−63	−75

[1] All values are in dBm. LO Input Power = 0 dBm.

M × N SPURIOUS PERFORMANCE

LO = 0 dBm, Upper Sideband

IF = 3100 MHz at 0 dBm and RF = 13300 MHz. All values in dBc below RF power level. N/A means not applicable.

		N × LO				
		0	**1**	**2**	**3**	**4**
M × IF	**−4**	N/A	98	83	83	105
	−3	N/A	99	66	75	104
	−2	N/A	60	52	77	89
	−1	N/A	61	27	80	97
	0	N/A	53	38	68	85
	1	77	0	68	70	75
	2	65	43	31	86	86
	3	50	67	77	64	78
	4	77	58	83	96	N/A

IF = 3300 MHz at 0 dBm and RF = 13300 MHz. All values in dBc below RF power level. N/A means not applicable.

		N × LO				
		0	**1**	**2**	**3**	**4**
M × IF	**−4**	N/A	92	92	78	100
	−3	N/A	100	85	67	101
	−2	N/A	67	58	76	95
	−1	N/A	57	29	76	99
	0	N/A	58	32	60	80
	1	74	0	73	60	79
	2	64	43	32	86	82
	3	57	63	79	67	91
	4	78	67	80	96	N/A

IF = 3500 MHz at 0 dBm and RF = 13300 MHz. All values in dBc below RF power level. N/A means not applicable.

		N × LO				
		0	**1**	**2**	**3**	**4**
M × IF	**−4**	N/A	92	92	78	100
	−3	N/A	100	85	67	101
	−2	N/A	67	50	76	95
	−1	N/A	50	28	72	97
	0	N/A	64	27	58	74
	1	71	0	73	60	79
	2	59	43	32	86	82
	3	57	63	79	67	91
	4	78	67	80	96	N/A

THEORY OF OPERATION

The ADMV1009 is a GaAs, MMIC, SSB, upper side band upconverter in a RoHS compliant package optimized for upper sideband point to point microwave radio applications operating in the 12.7 GHz to 15.4 GHz output frequency range. The ADMV1009 supports LO input frequencies of 9 GHz to 12.6 GHz and IF frequencies of 2.8 GHz to 4 GHz.

The ADMV1009 uses a RF amplifier preceded by a passive, double balanced mixer, where a driver amplifier drives the LO (see Figure 59). The combination of design, process, and packaging technology allows the functions of these subsystems to be integrated into a single die, using mature packaging and interconnection technologies to provide a high performance, low cost design with excellent electrical, mechanical, and thermal properties. In addition, the need for external components is minimized, optimizing cost and size.

LO DRIVER AMPLIFIER

The LO driver amplifier takes a single LO input and amplifies it to the desired LO signal level for the mixer to operate optimally. The LO driver amplifier requires a single dc bias voltage (VDLO) and a single dc gate bias (VGLO) to operate. Starting at −2 V at the gate supply (VGLO), the LO amplifier is biased at +5 V (VDLO). Then, the gate bias (VGLO) is varied until the desired LO amplifier bias current (IDLO) is achieved. The desired LO amplifier bias current is 60 mA under the LO input drive of −4 dBm to +4 dBm. The LO drive range of −4 dBm to +4 dBm makes it compatible with Analog Devices, Inc., wideband synthesizer portfolio without the requirement for an external LO driver amplifier.

MIXER

The mixer has two differential inputs, IF1 and IF2, and an external 180° balun is required to drive the IF ports differentially. The ADMV1009 is optimized to work with the Mini-Circuit NCS1-422+ RF balun. The mixer must be biased at −1.1 V (VGMIX) to operate.

RF AMPLIFIER

The RF amplifier requires a single dc bias voltage (VDRF) and a single dc gate bias (VGRF) to operate. Starting at −2 V at the gate supply (VGRF), the RF amplifier is biased at +5 V (VDRF). Then, the gate bias (VGRF) is varied until the desired RF amplifier bias current (IDRF) is achieved. The desired RF amplifier bias current is 250 mA under small signal conditions.

The ADMV1009 has an internal band-pass filter between the mixer and the RF driver amplifier that reduces LO leakage and filters out the lower sideband at the RF output. The balanced input drive allows exceptional linearity performance compared to similar single-ended solutions.

The typical application circuit (see Figure 59) shows the necessary external components on the bias lines to eliminate any undesired stability problems for the RF amplifier and the LO amplifier.

The ADMV1009 upconverter comes in a compact, thermally enhanced, 4.9 mm × 4.9 mm, 32-terminal ceramic leadless chip carrier (LCC) package. The ADMV1009 operates over the −40°C to +85°C temperature range.

APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUIT

The typical applications circuit is shown in Figure 59. The application circuit shown has been replicated for the evaluation board circuit.

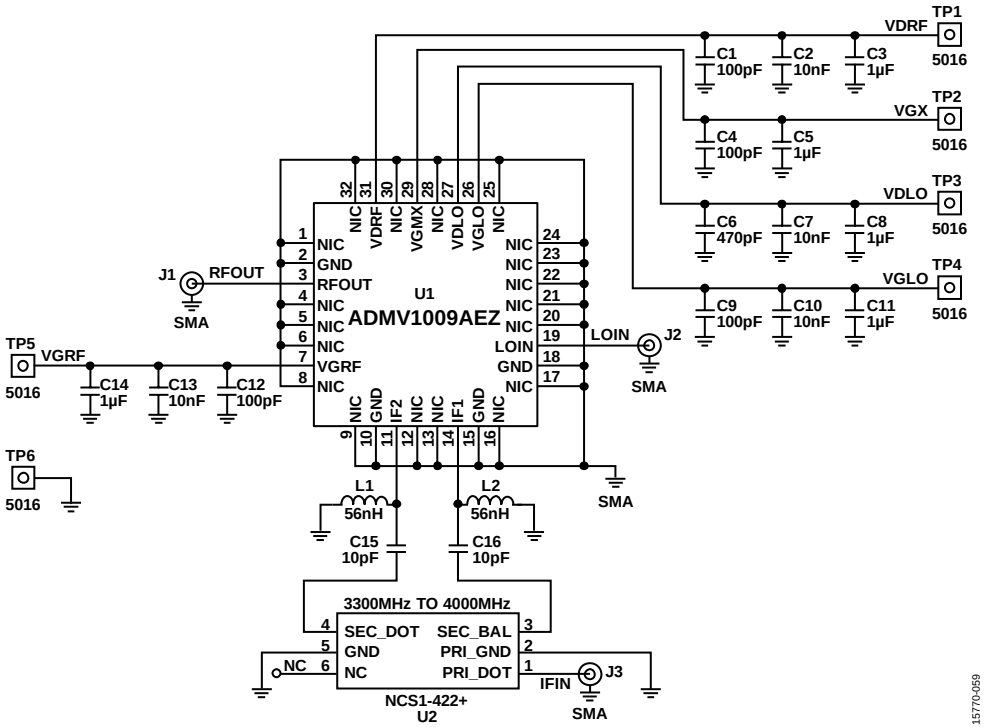

Figure 59. Typical Application Circuit

EVALUATION BOARD INFORMATION

The circuit board used in the application must use RF circuit design techniques. Signal lines must have 50 Ω impedance, and the package ground leads and exposed pad must be connected directly to the ground plane, similar to what is shown in Figure 60 and Figure 61. Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation circuit board shown in Figure 59 is available from Analog Devices, Inc., upon request.

Layout

Solder the exposed pad on the underside of the ADMV1009 to a low thermal and electrical impedance ground plane. This pad is typically soldered to an exposed opening in the solder mask on the evaluation board. Connect these ground vias to all other ground layers on the evaluation board to maximize heat dissipation from the device package. Figure 60 shows the PCB land pattern footprint for the ADMV1009-EVALZ, and Figure 61 shows the solder paste stencil for the ADMV1009-EVALZ evaluation board.

Power-On Sequence

To set up the ADMV1009-EVALZ, take the following steps:

1. Power up the VGLO with a −1.5 V supply.
2. Power up the VDLO with a 5 V supply.
3. Adjust VGLO from −1.5 V to −0.5 V such that IDLO = 60 mA.
4. Power up VGRF with a −1.5 V supply.
5. Power up VDRF with a 5 V supply.
6. Adjust VGRF from −1.5 V to −0.5 V such that IDLO = 250 mA
7. Power up VGMIX with a −1.5 V supply.
8. Apply an LO signal.
9. Apply an IF signal.

Power Off Sequence

To turn off the ADMV1009-EVALZ, take the following steps:

1. Turn off the LO and IF signals.
2. Set VGRF and VGLO to −1.5 V.
3. Set the VDRF and VDLO supplies to 0 V and then turn off the VDRF and VDLO supplies.
4. Turn off the VGRF and VGLO supplies.

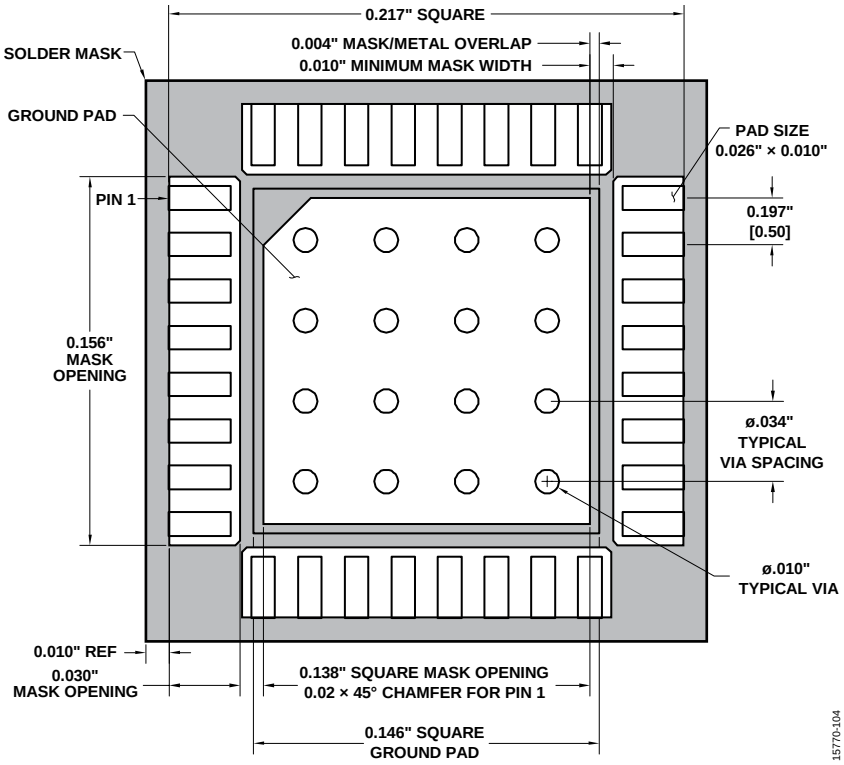

Figure 60. PCB Land Pattern Footprint of the ADMV1009-EVALZ

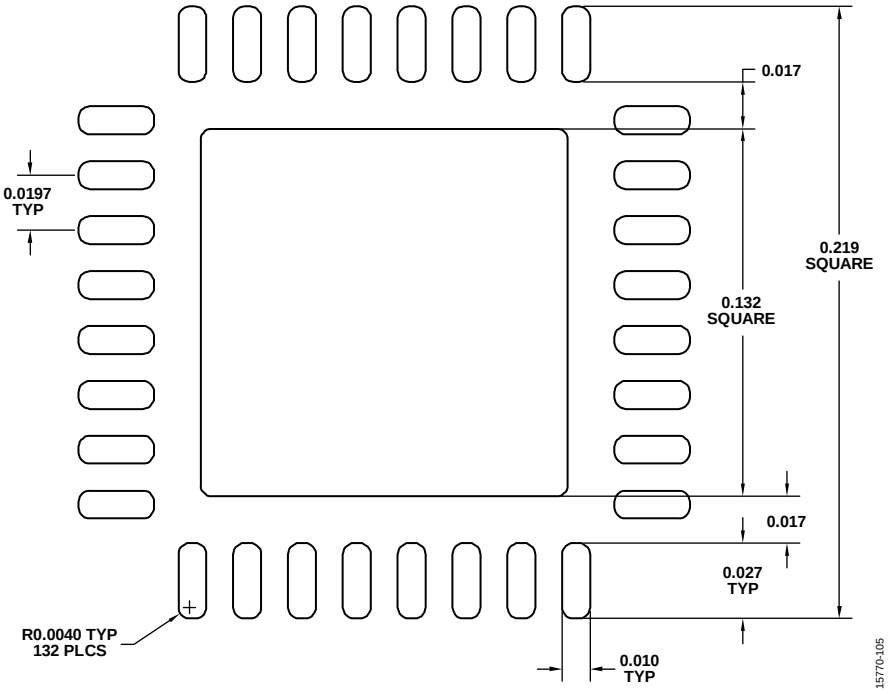

Figure 61. Solder Paste Stencil of the ADMV1009-EVALZ

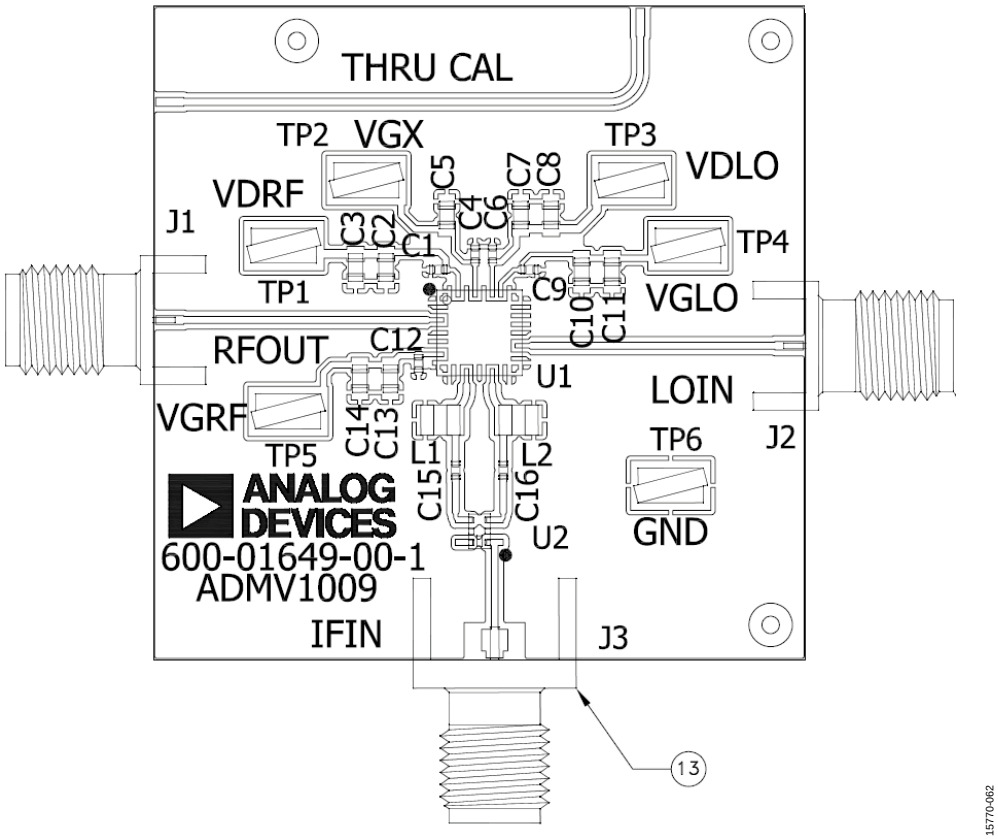

Figure 62. ADMV1009-EVALZ Evaluation Board Top Layer

BILL OF MATERIALS

Table 6.

Qty.	Reference Designator	Description	Manufacturer/Part No.
1	Not applicable	PCB	Analog Devices/600-01649-00
1	U1	ADMV1009AEZ	Analog Devices/ADMV1009AEZ
4	C1, C4, C9, C12	100 pF ceramic capacitors, 5%, 50 V, C0G, 0402	Murata/GRM1555C1H101JA01D
4	C2, C7, C10, C13	10 nF ceramic capacitors, 50 V, 10%, X7R, 0603	Panasonic/ECJ-1VB1H103K
5	C3, C5, C8, C11, C14	1 µF ceramic capacitors, 50 V, 10%, X7R, 0603	Taiyo Yuden/UMK107AB7105KA-T
1	C6	470 pF ceramic capacitor, 5%, 50 V, COG, 0402, SMD	Murata/GRM1555C1H471JA01D
2	C15, C16	10 pF ceramic capacitors, 5%, 25 V, C0G, 0402	Kemet/C0402C100J3GAL
2	J1, J2	SCD, COMP, SMA connectors, SRI	SRI Connector Gage Co./21-141-1000-01
1	J3	SCD, COMP, SMA connector	Johnson Components/142-0701-851
2	L1, L2	56 nH inductors, 0805, 5%, 500 mA	Coilcraft/0805CS-560XJLB
6	TP1 to TP6	Test points, PC compact SMT	Keystone Electronics/5016
1	U2	50 Ω RF transformer, 3300 MHz to 4000 MHz	Mini-Circuits/NCS1-422+
1	Heatsink	Aluminum heatsink	Analog Devices/111332

OUTLINE DIMENSIONS

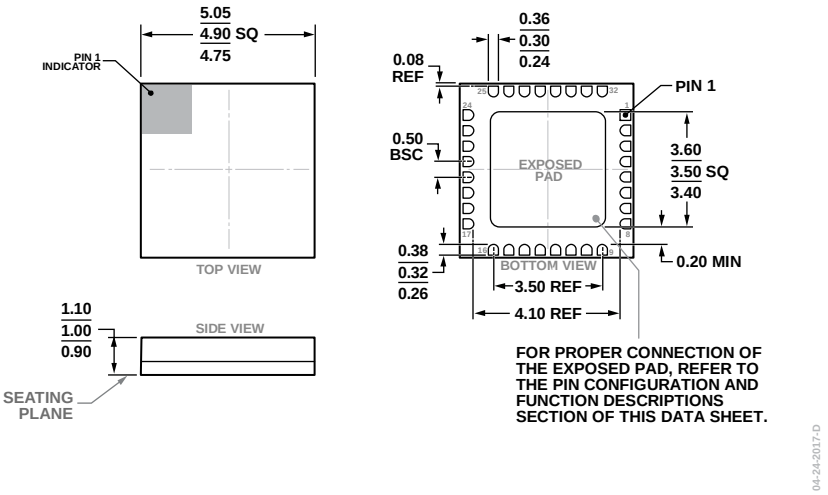

Figure 63. 32-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-32-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Body Material	Lead Finish	Package Description	Package Option
ADMV1009AEZ	−40°C to +85°C	Alumina Ceramic	Gold Over Nickel	32-Terminal Ceramic LCC	E-32-1
ADMV1009AEZ-R7	−40°C to +85°C	Alumina Ceramic	Gold Over Nickel	32-Terminal Ceramic LCC	E-32-1
ADMV1009-EVALZ				Evaluation Board	

[1] Z = RoHS Compliant Part.