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THIS SPEC IS OBSOLETE

Spec No: 002-08550

Spec Title: MB3793-27A Power Voltage Monitoring IC with Watchdog Timer

Replaced by: None

MB3793-27A

Power Voltage Monitoring IC with Watchdog Timer

Description

The MB3793 is an integrated circuit to monitor power voltage; it incorporates a watchdog timer. A reset signal is output when the power is cut or falls abruptly. When the power recovers normally after resetting, a power-on reset signal is output to microprocessor units (MPUs). An internal watchdog timer with two inputs for system operation diagnosis can provide a fall-safe function for various application systems.

Features

- Precise detection of power voltage fall: ±2.5%
- Detection voltage with hysteresis
- Low power dispersion: I_{CC} = 31 µA (reference)
- Internal dual-input watchdog timer
- Watchdog-timer halt function (by inhibition pin)
- Independently-set watchdog and reset times
- Three types of packages (SOP-8pin : 2 types)

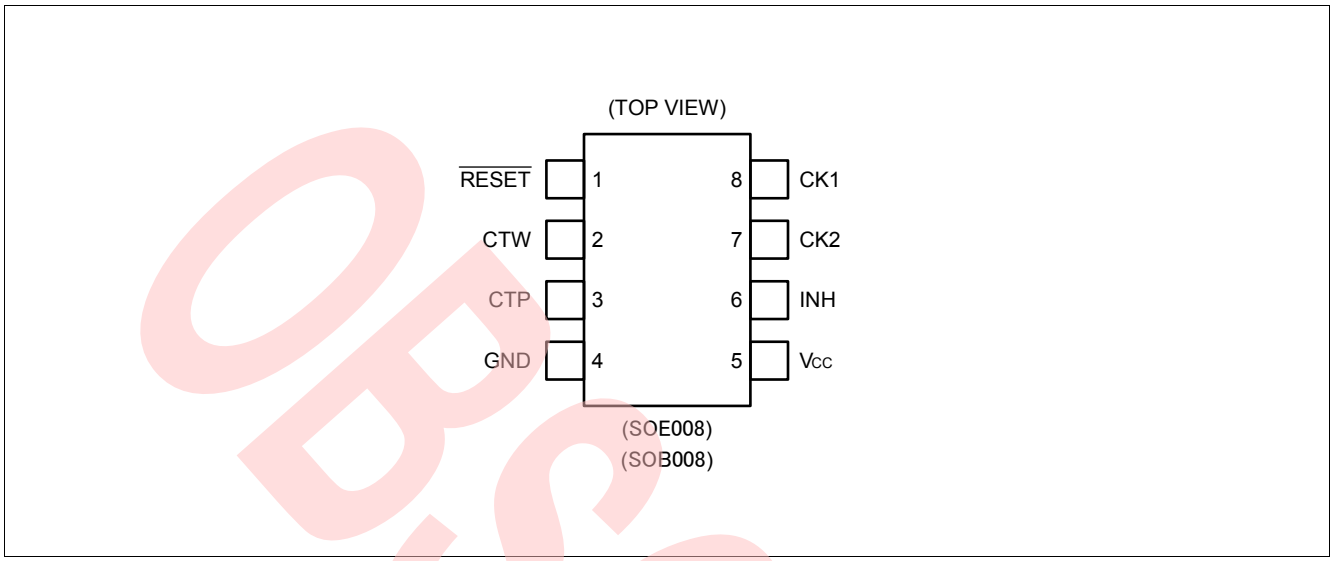
Application

- Arcade Amusement etc.

Contents

Description **1**
Features **1**
Application **1**
Contents **2**
1. Pin Assignment **3**
2. Pin Description **3**
3. Block Diagram **4**
4. Block Description **5**
5. Absolute Maximum Ratings **5**
6. Recommended Operating Conditions **6**
7. Electrical Characteristics **7**
7.1 DC Characteristics 7
7.2 AC Characteristics 7
8. Diagram **8**
8.1 Basic operation (Positive clock pulse) 8
8.2 Basic operation (Negative clock pulse) 9
8.3 Single-clock input monitoring (Positive clock pulse) . 10
8.4 Inhibition operation (Positive clock pulse) 11
8.5 Clock pulse input supplementation (Positive clock pulse) 12
9. Operation Sequence **13**
9.1 Positive clock pulse input 13
9.2 Negative clock pulse input 13
9.3 Clock monitoring 13
9.4 Description of Operations 13
10. Typical Characteristics **15**
11. Application Example **18**
11.1 Supply voltage monitor and watchdog timer (1-clock monitor) 18
11.2 Supply voltage monitor and watchdog timer stop ... 19
12. Typical Application **20**
13. Notes On Use **21**
14. Ordering Information **21**
15. RoHS Compliance Information **21**
16. Package Dimensions **22**
17. Major Changes **24**
Document History **24**
Sales, Solutions, and Legal Information **25**

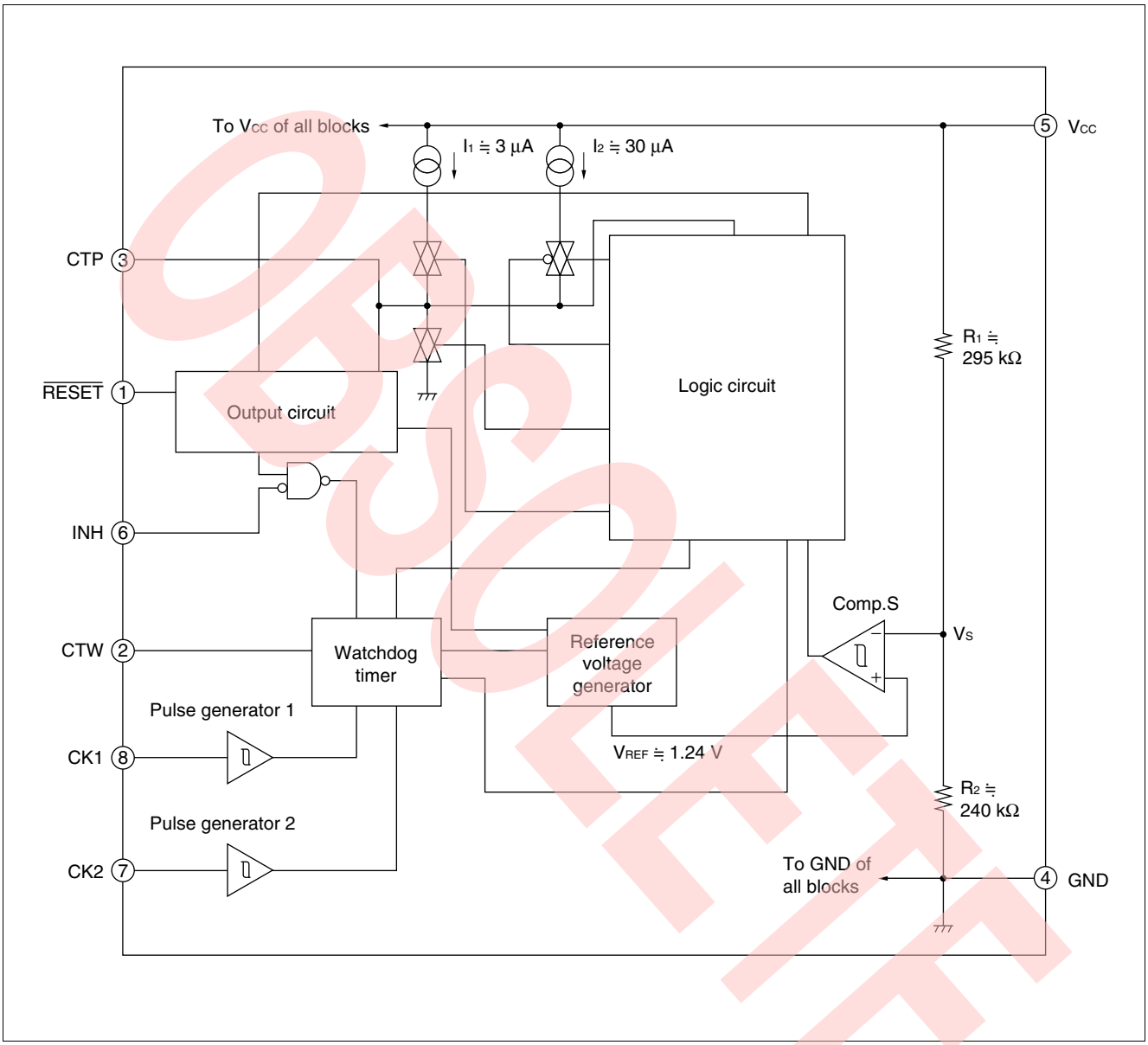
1. Pin Assignment



2. Pin Description

Pin no.	Symbol	Descriptions	Pin no.	Symbol	Descriptions
1	$\overline{\text{RESET}}$	Outputs reset pin	5	V_{CC}	Power supply pin
2	CTW	Watchdog timer monitor time setting pin	6	INH	Inhibit pin
3	CTP	Power-on reset hold time setting pin	7	CK2	Inputs clock 2 pin
4	GND	Ground pin	8	CK1	Inputs clock 1 pin

3. Block Diagram



4. Block Description

1. Comp. S

Comp. S is a comparator with hysteresis to compare the reference voltage with a voltage (V_S) that is the result of dividing the power voltage (V_{CC}) by resistors 1 and 2. When V_S falls below 1.24 V, a reset signal is output.
This function enables the MB3793 to detect an abnormality within 1 µs when the power is cut or falls abruptly.

2. Output circuit

The output circuit contains a $\overline{\text{RESET}}$ output control comparator that compares the voltage at the CTP pin to the threshold voltage to release the $\overline{\text{RESET}}$ output if the CTP pin voltage exceeds the threshold value.

Since the reset ($\overline{\text{RESET}}$) output buffer has CMOS organization, no pull-up resistor is needed.

3. Pulse generator

The pulse generator generates pulses when the voltage at the CK1 and CK2 clock pins changes to High from Low level (positive-edge trigger) and exceeds the threshold voltage; it sends the clock signal to the watchdog timer.

4. Watchdog timer

The watchdog timer can monitor two clock pulses. Short-circuit the CK1 and CK2 clock pins to monitor a single clock pulse.

5. Inhibition pin

The inhibition (INH) pin forces the watchdog timer on/off. When this pin is High level, the watchdog timer is stopped.

6. Logic circuit

The logic circuit contains flip-flops.

Flip-flop RSFF1 controls the charging and discharging of the power-on reset hold time setting capacitor (C_{TP}).

Flip-flop RSFF2 turns on/off the circuit that accelerates charging of the power-on reset hold time setting capacitor (C_{TP}) at a reset. The RSFF2 operates only at a reset; it does not operate at a power-on reset when the power is turned on.

5. Absolute Maximum Ratings

Parameter		Symbol	Conditions	Rating		Unit
				Min	Max	
Power supply voltage*		V_{CC}	—	–0.3	+7	V
Input voltage*	CK1	V_{CK1}	—	–0.3	+7	V
	CK2	V_{CK2}	—			
	INH	I_{INH}	—			
Reset output current	$\overline{\text{RESET}}$	I_{OL} I_{OH}	—	–10	+10	mA
Power dissipation		P_D	Ta ≤ +85°C	—	200	mW
Storage temperature		Tstg	—	–55	+125	°C

*: The voltage is based on the ground voltage (0 V).

WARNING:

1. Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.Do not exceed any of these ratings.

6. Recommended Operating Conditions

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{CC}	—	1.2	—	6.0	V
Reset ($\overline{RESET}$) output current	I_{OL} I_{OH}	—	–5	—	+5	mA
Power-on reset hold time setting capacity	C_{TP}	—	0.001	—	10	µF
Watchdog-timer monitoring time setting capacity*	C_{TW}	—	0.001	—	1	µF
Operating ambient temperature	Ta	—	–40	—	+85	°C

*: The watchdog timer monitor time range depends on the rating of the setting capacitor.

WARNING:

1. The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

2. Any use of semiconductor devices will be under their recommended operating condition.

3. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

4. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

7. Electrical Characteristics

7.1 DC Characteristics

(V_{CC} = +3.3 V, Ta = +25°C)

Parameter	Symbol	Conditions		Value			Unit
				Min	Typ	Max	
Power supply current	I_{CC}	After exit from reset		—	31	55	µA
Detection voltage	V_{SL}	V_{CC} falling	Ta = +25 °C	2.63	2.70	2.77	V
			Ta = –40 °C to +85 °C	(2.59)*	2.70	(2.81)*	
	V_{SH}	V_{CC} rising	Ta = +25 °C	2.69	2.76	2.87	V
			Ta = –40 °C to +85 °C	(2.65)*	2.76	(2.87)*	
Detection voltage hysteresis difference	V_{SHYS}	$V_{SH} - V_{SL}$		35	65	95	mV
Clock-input threshold voltage	V_{CIH}	CK rising		(0.7)*	1.3	1.9	V
	V_{CIL}	CK falling		0.5	1.0	(1.5)*	V
Clock-input hysteresis	V_{CHTS}	—		(0.1)*	0.3	(0.6)*	V
Inhibition-input voltage	V_{IIH}	—		2.2	—	—	V
	V_{IIL}	—		—	0	0.8	
Input current (CK1, CK2, INH)	I_{IH}	V_{CK} = 5 V		—	0	1.0	µA
	I_{IL}	V_{CK} = 0 V		–1.0	0	—	µA
Reset output voltage	V_{OH}	$I_{\overline{RESET}}$ = –5 mA		2.8	3.10	—	V
	V_{OL}	$I_{\overline{RESET}}$ = +5 mA		—	0.12	0.4	V
Reset-output minimum power voltage	V_{CCL}	$I_{\overline{RESET}}$ = +50 µA		—	0.8	1.2	V

*: The values enclosed in parentheses ( ) are setting assurance values.

7.2 AC Characteristics

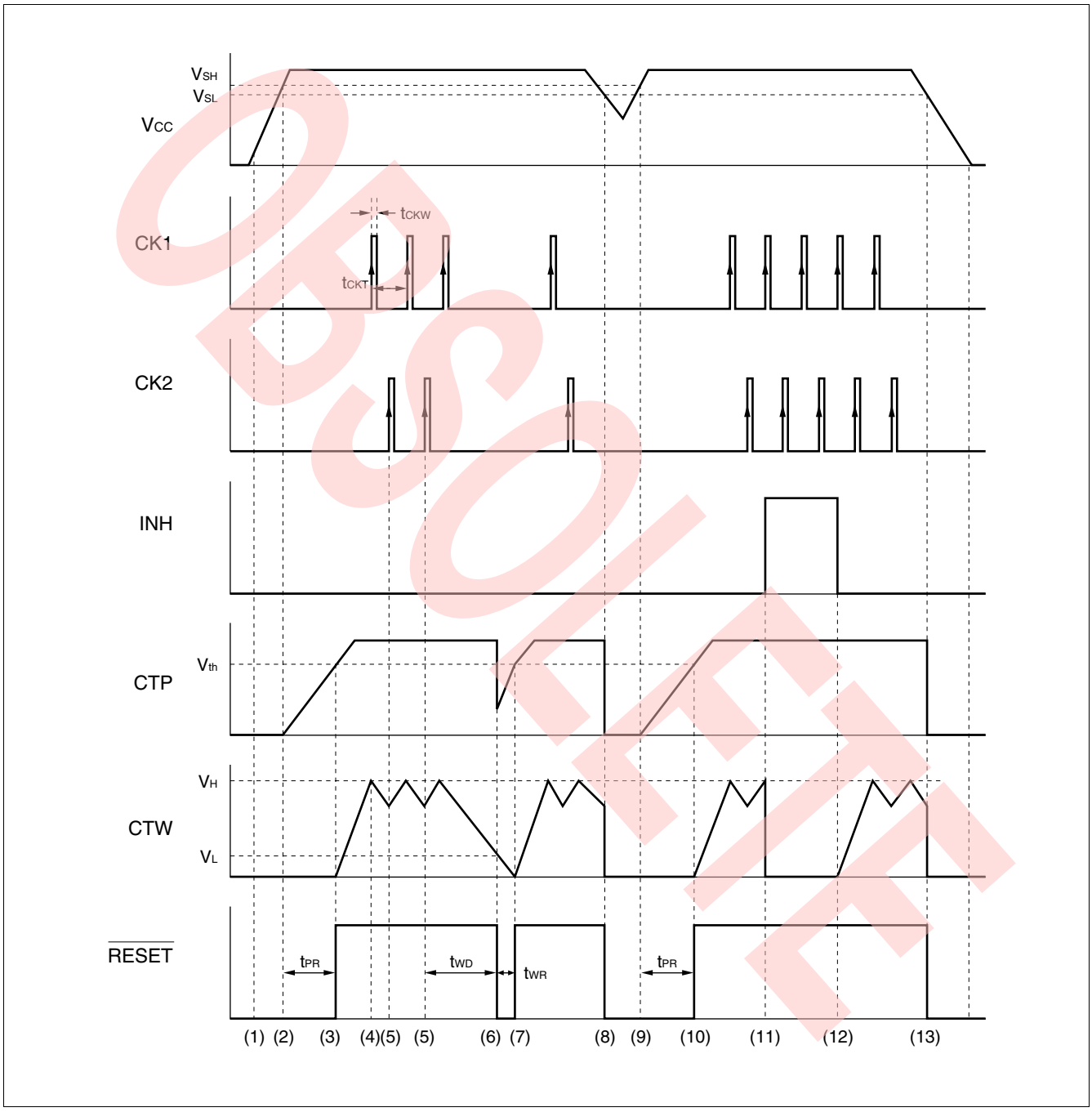
(V_{CC} = +3.3 V, Ta = +25°C)

Parameter		Symbol	Conditions	Value			Unit
				Min	Typ	Max	
Power-on reset hold time		t_{PR}	C_{TP} = 0.1 µF	30	75	120	ms
V_{CC} input pulse width		t_{PI}	C_{TP} = 0.1 µF	(8)*2	—	—	µs
V_{CC} delay time		t_{PD}	C_{TP} = 0.1 µF	—	2	(10)*2	µs
Watchdog timer monitor time		t_{WD}	C_{TW} = 0.01 µF, C_{TP} = 0.1 µF	8	16	24	ms
Watchdog timer reset time		t_{WR}	C_{TP} = 0.1 µF	2	5.5	9	ms
Clock input pulse width		t_{CKW}	—	500	—	—	ns
Clock input pulse cycle		t_{CKT}	—	20	—	—	µs
Reset ($\overline{RESET}$) output transition time	Rising	t_r*1	C_L = 50 pF	—	—	500	ns
	Falling	t_f*1	C_L = 50 pF	—	—	500	ns

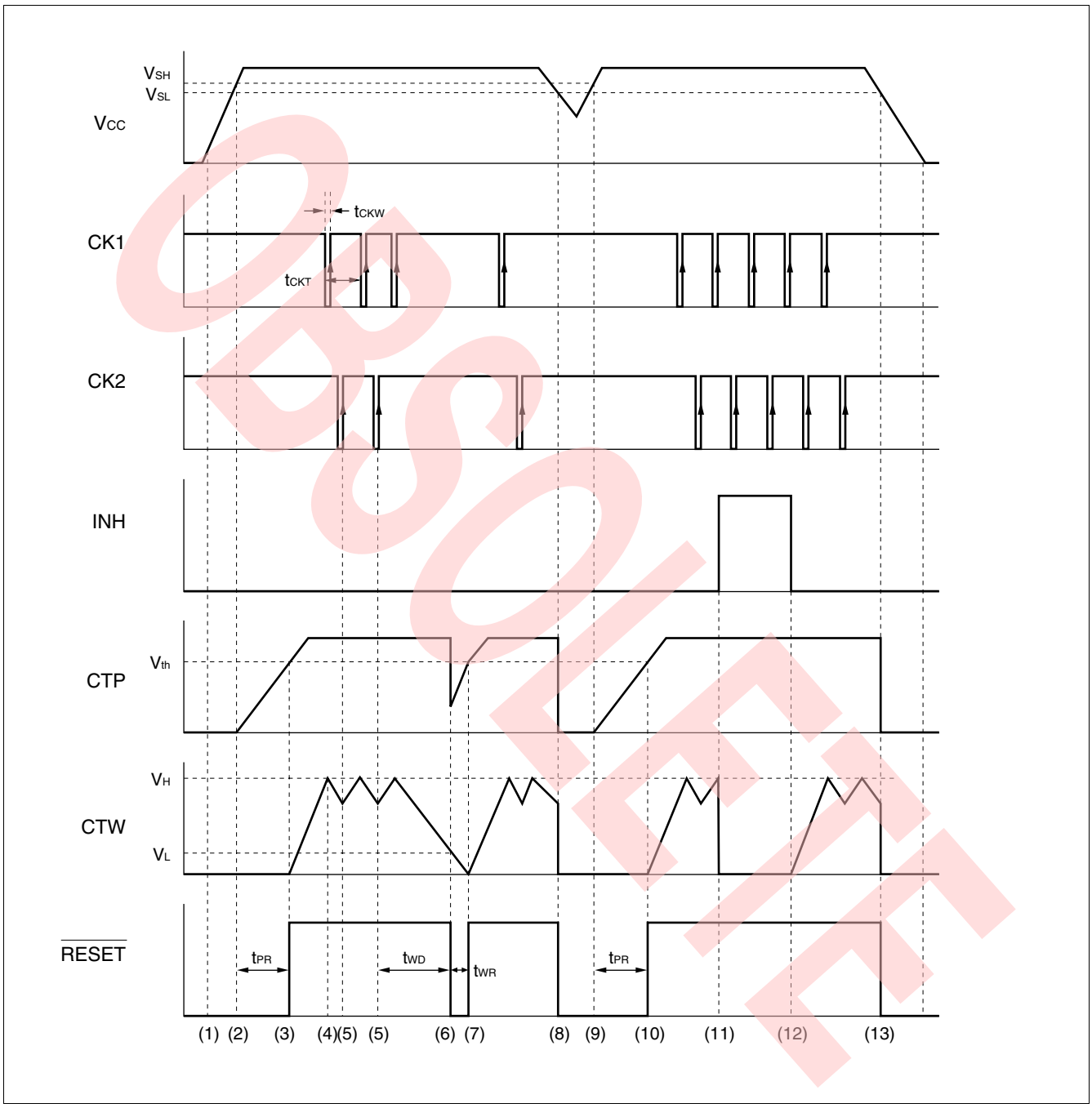
*1:The voltage range is 10% to 90% at testing the reset output transition time.
*2:The values enclosed in parentheses ( ) are setting assurance values.

8. Diagram

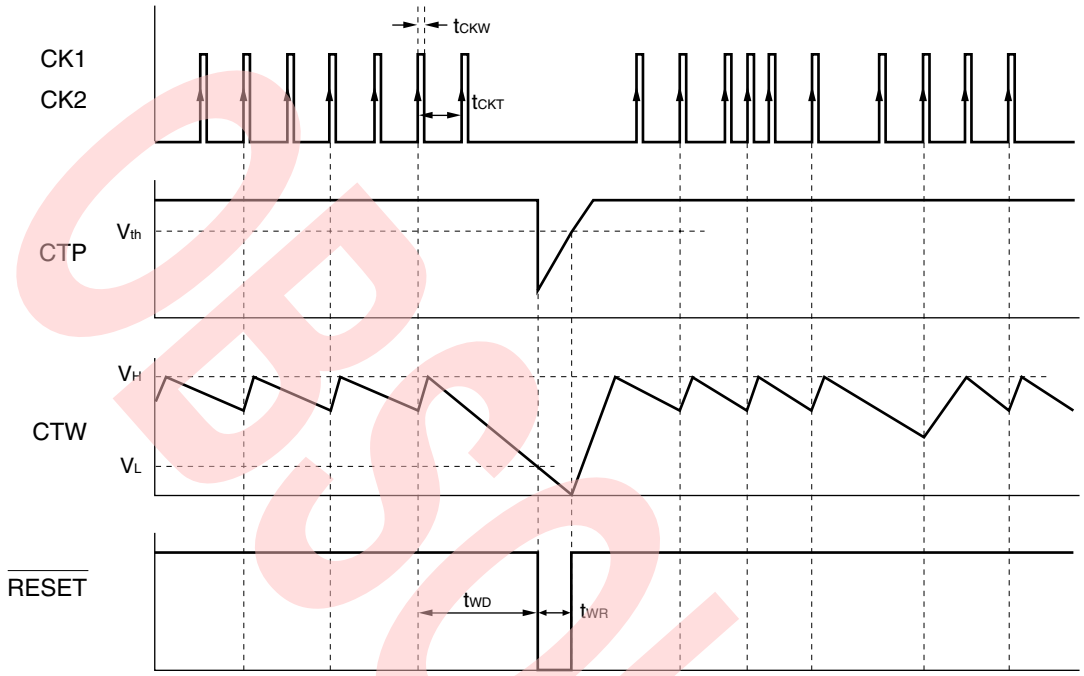
8.1 Basic operation (Positive clock pulse)



8.2 Basic operation (Negative clock pulse)

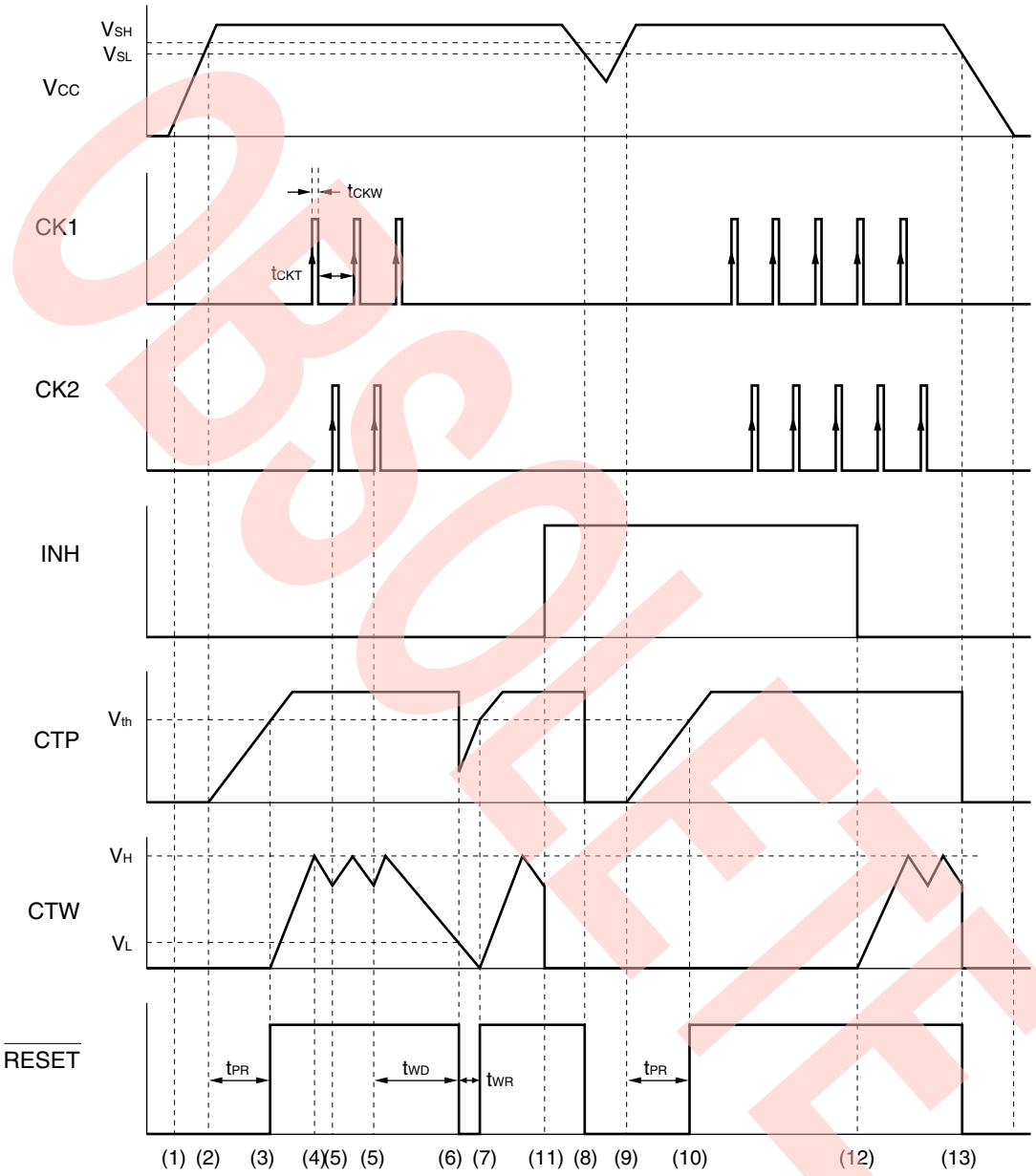


8.3 Single-clock input monitoring (Positive clock pulse)

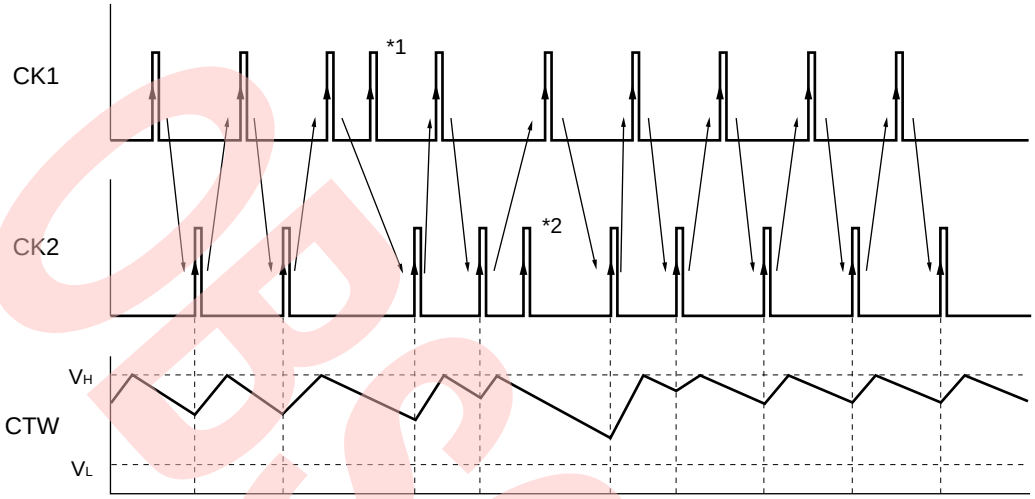


Note : The MB3793 can monitor only one clock.
The MB3793 checks the clock signal at every other input pulse. Therefore, set watchdog timer monitor time t_{WD} to the time that allows the MB3793 to monitor the period twice as long as the input clock pulse.

8.4 Inhibition operation (Positive clock pulse)



8.5 Clock pulse input supplementation (Positive clock pulse)



Note : The MB3793 watchdog timer monitors Clock1 (CK1) and Clock2 (CK2) pulses alternately.
When a CK2 pulse is detected after detecting a CK1 pulse, the monitoring time setting capacity (C_{TW}) switches to charging from discharging.
When two consecutive pulses occur on one side of this alternation before switching, the second pulse is ignored.
In the above figure, pulse *1 and *2 are ignored.

9. Operation Sequence

9.1 Positive clock pulse input

See “1. Basic operation (positive clock pulse)” under “Diagram.”

9.2 Negative clock pulse input

See “2. Basic operation (negative clock pulse)” under “Diagram.”

The MB3793 operates in the same way whether it inputs positive or negative pulses.

9.3 Clock monitoring

To use the MB3793 while monitoring only one clock, connect clock pins CK1 and CK2.

Although the MB3793 operates basically in the same way as when monitoring two clocks, it monitors the clock signal at every other input pulse.

See “3. Single-clock input monitoring (positive clock pulse)” under “Diagram.”

9.4 Description of Operations

The numbers given to the following items correspond to numbers (1) to (13) used in “Diagram.”

(1) The MB3793 outputs a reset signal when the supply voltage (V_{CC}) reaches about 0.8 V (V_{CCL})

(2) If V_{CC} reaches or exceeds the rise-time detected voltage V_{SH}, the MB3793 starts charging the power-on reset hold time setting capacitor C_{TP}. At this time, the output remains in a reset state. The V_{SH} value is about 2.76 V.

(3) When C_{TP} has been charged for a certain period of time T_{PR} (until the CTP pin voltage exceeds the threshold voltage (V_{th}) after the start of charging), the MB3793 cancels the reset (setting the $\overline{\text{RESET}}$ pin to “H” level from “L” level).
The V_{th} value is about 2.4 V with V_{CC} = 3.3 V

The power-on reset hold time t_{PR} is set with the following equation:
t_{PR} (ms) ≈ A × C_{TP} (µF)
The value of A is about 750 with V_{CC} = 3.3 V and about 700 with V_{CC} = 3.0 V. The MB3793 also starts charging the watchdog time setting capacitor (C_{TW}).

(4) When the voltage at the watchdog timer monitor time setting pin CTW reaches the “H” level threshold voltage V_H, the C_{TW} switches from the charge state to the discharge state.
The value of V_H is always about 1.24 V regardless of the detected voltage.

(5) If the CK2 pin inputs a clock pulse (positive edge trigger) when the C_{TW} is being discharged in the CK1-CK2 order or simultaneously, the C_{TW} switches from the discharge state to the charge state.
The MB3793 repeats operations (4) and (5) as long as the CK1/CK2 pin inputs clock pulses with the system logic circuit operating normally.

(6) If no clock pulse is fed to the CK1 or CK2 pin within the watchdog timer monitor time t_{WD} due to some problem with the system logic circuit, the CTW pin is set to the “L” level threshold voltage V_L or less and the MB3793 outputs a reset signal (setting the $\overline{\text{RESET}}$ pin to “L” level from “H” level).
The value of V_L is always about 0.24 V regardless of the detected voltage.

The watchdog timer monitor time t_{WD} is set with the following equation:
t_{WD} (ms) ≈ B × C_{TW} (µF)
The value of B is hardly affected by the power supply voltage; it is about 1600 with V_{CC} = 3.0 V to 3.3 V.

(7) When a certain period of time t_{WR} has passed (until the CTP pin voltage reaches or exceeds Vth again after recharging the C_{TP}), the MB3793 cancels the reset signal and starts operating the watchdog timer.
The watchdog timer monitor reset time t_{WR} is set with the following equation:
t_{WR} (ms) ≈ D x C_{TP} (µF)
The value of D is 55 with V_{CC} = 3.3 V and about 50 with V_{CC} = 3.0 V.
The MB3793 repeats operations (4) and (5) as long as the CK1/CK2 pin inputs clock pulses. If no clock pulse is input, the MB3793 repeats operations (6) and (7).

(8) If V_{CC} is lowered to the fall-time detected voltage (V_{SL}) or less, the CTP pin voltage decreases and the MB3793 outputs a reset signal (setting the $\overline{\text{RESET}}$ pin to “L” level from “H” level).
The value of V_{SL} is 2.7 V

(9) When V_{CC} reaches or exceeds V_{SH} again, the MB3793 starts charging the C_{TP}.

(10) When the CTP pin voltage reaches or exceeds V_{th}, the MB3793 cancels the reset and restarts operating the watchdog timer. It repeats operations (4) and (5) as long as the CK1/CK2 pin inputs clock pulses.

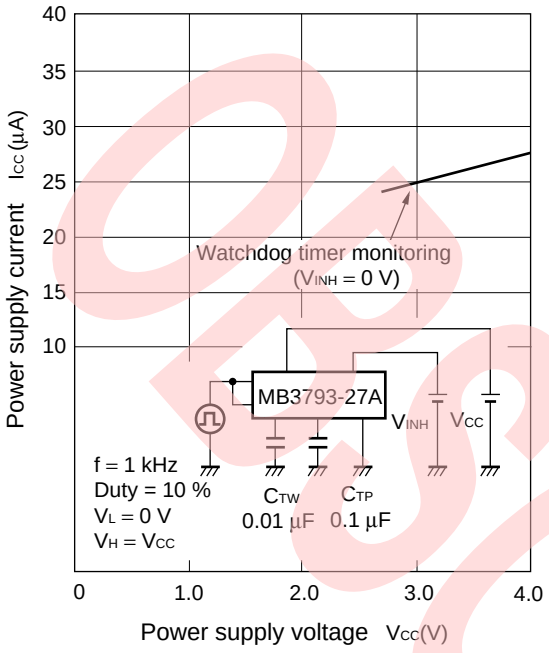
(11) Making the inhibit pin active (setting the INH pin to “H” from “L”) forces the watchdog timer to stop operation.
This stops only the watchdog timer, leaving the MB3793 monitoring V_{CC} (operations (8) to (10)).
The watchdog timer remains inactive unless the inhibit input is canceled.

(12) Canceling the inhibit input (setting the INH pin to “L” from “H”) restarts the watchdog timer.

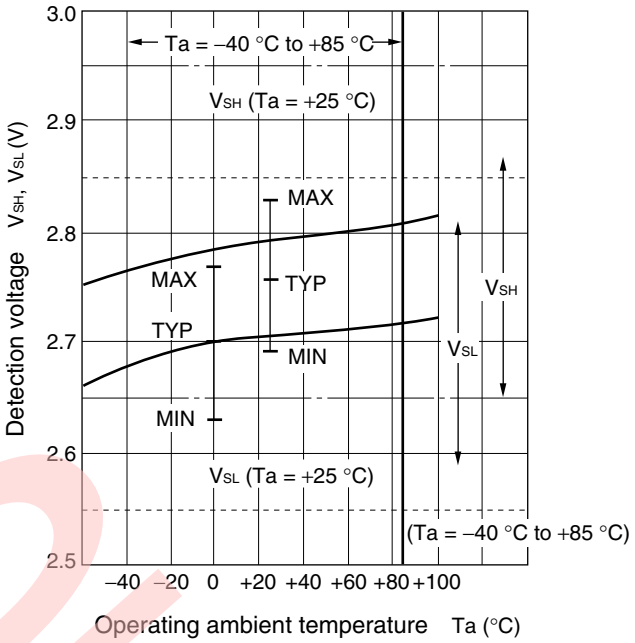
(13) The reset signal is output when the power supply is turned off to set V_{CC} to V_{SL} or less.

10. Typical Characteristics

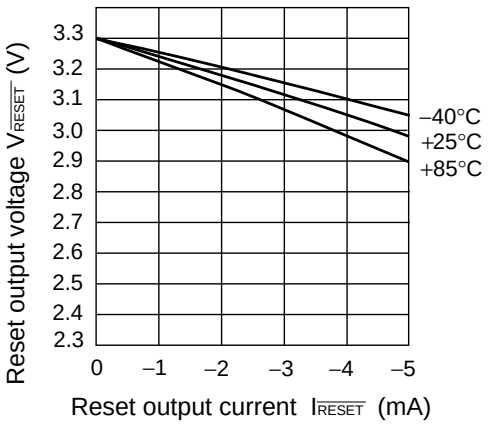
Power supply current vs. power supply voltage



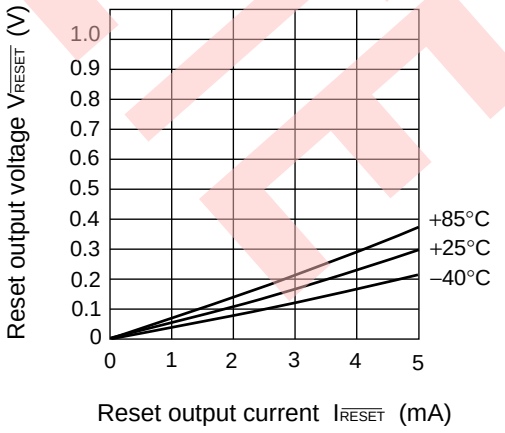
Detection voltage vs.
Operating ambient temperature



Reset output voltage vs. reset output current
(P-MOS side)

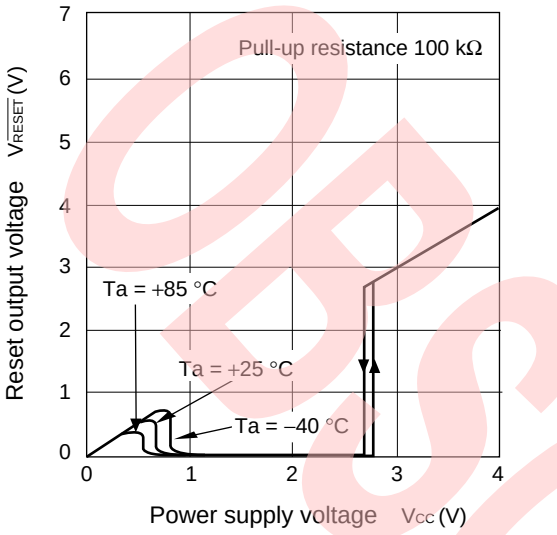


Reset output voltage vs. reset output current
(N-MOS side)

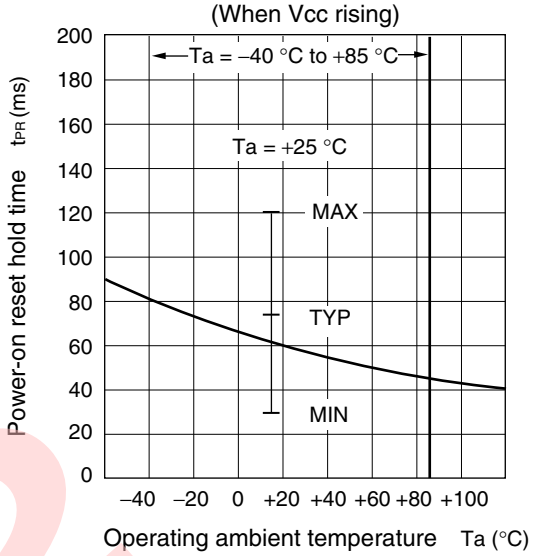


Note: Without writing the value clearly, V_{CC} = 3.3 (V), C_{TP} = 0.1 (µF), C_{TW} = 0.01 (µF).

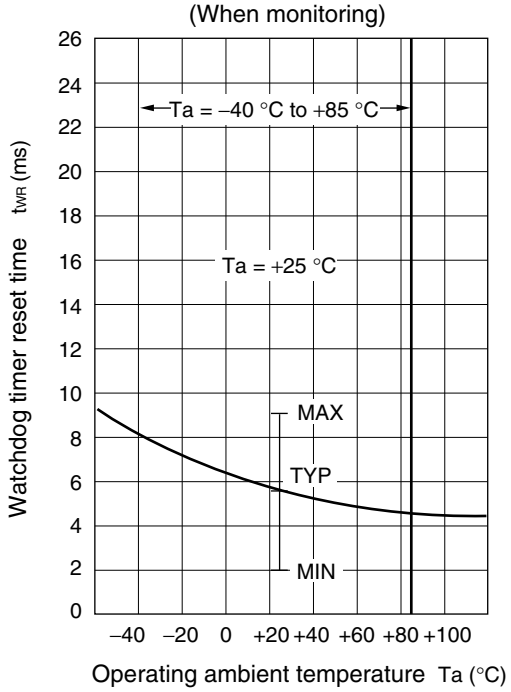
Reset output voltage vs. power supply voltage



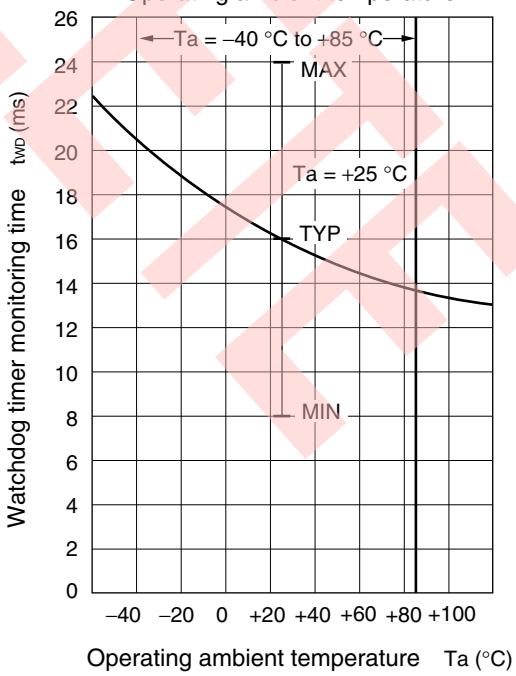
Power-on reset hold time vs.
Operating ambient temperature
(When Vcc rising)



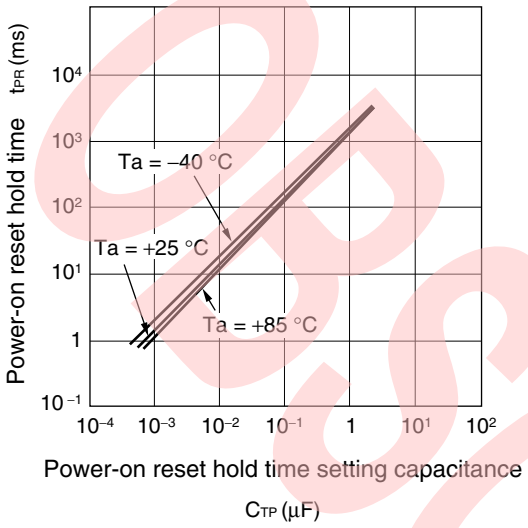
Watchdog timer reset time vs.
Operating ambient temperature
(When monitoring)



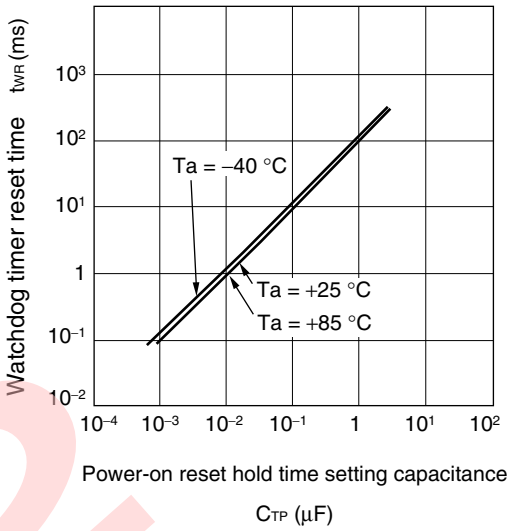
Watchdog timer monitoring time vs.
Operating ambient temperature



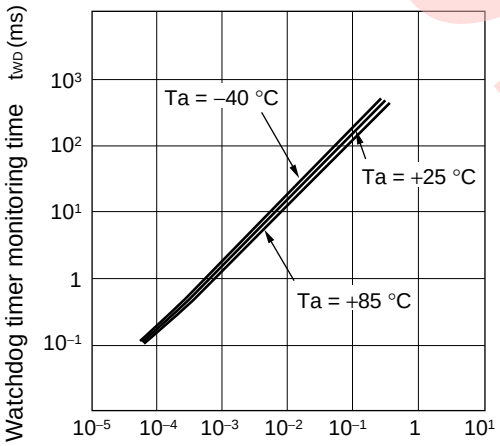
Power-on reset hold time vs. C_{TP} capacitance



Watchdog timer reset time vs. C_{TP} capacitance

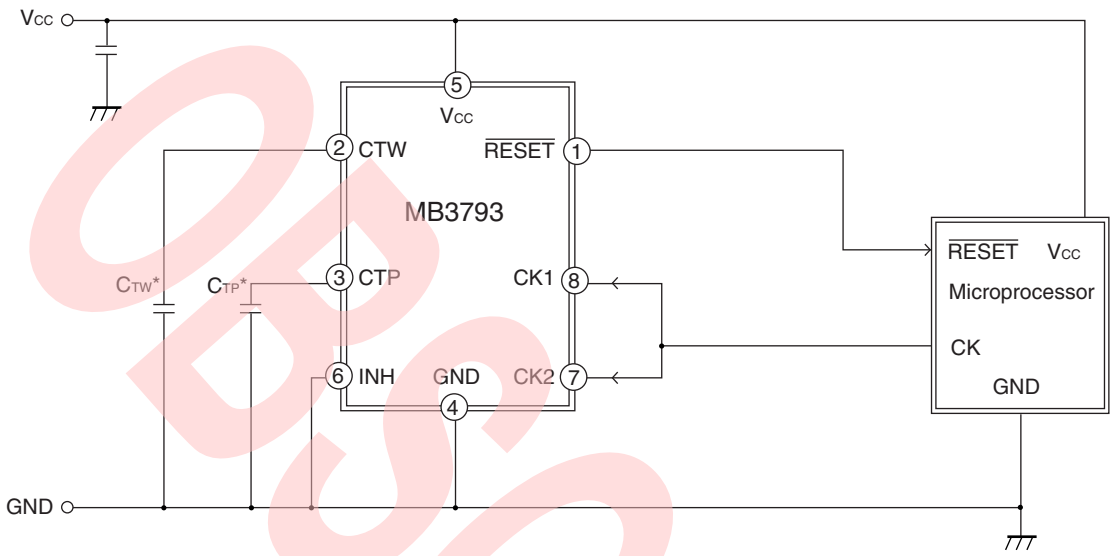


Watchdog timer monitoring time vs. C_{TW} capacitance



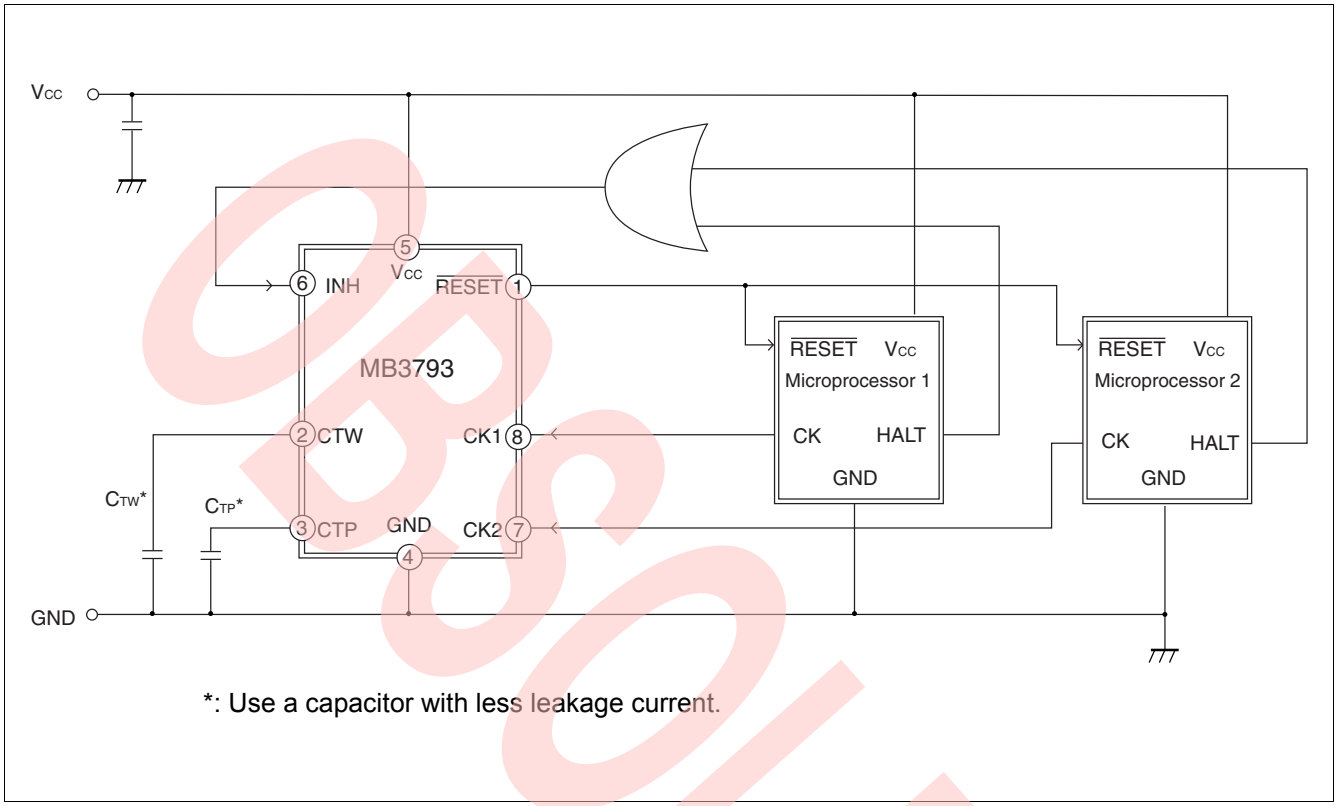
11. Application Example

11.1 Supply voltage monitor and watchdog timer (1-clock monitor)

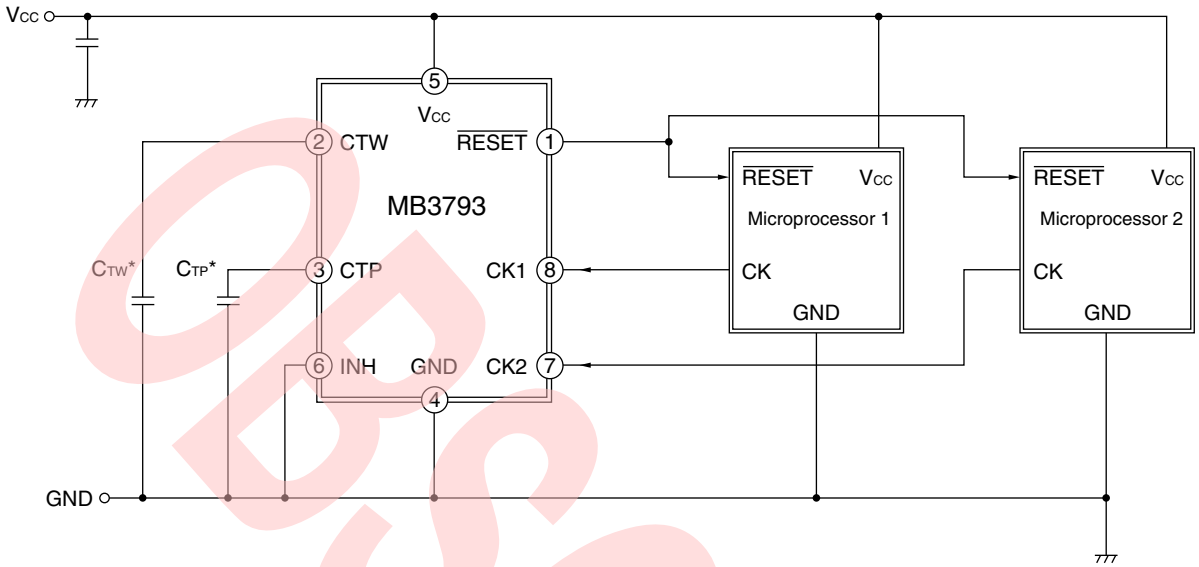


*: Use a capacitor with less leakage current.
The MB3793 monitors the clock (CK1, CK2) at every other input pulse.

11.2 Supply voltage monitor and watchdog timer stop



12. Typical Application



*: Use a capacitor with less leakage current.

1. Equation of time-setting capacitances (C_{TP} and C_{TW}) and set time

t_{PR} [ms] ≈ A × C_{TP} [µF]

t_{WD} [ms] ≈ B × C_{TW} [µF]

t_{WR} [ms] ≈ D × C_{TP} [µF]

Values of A, B, C, and D

A	B	C	D	Remark
750	1600	0	55	V_{CC} = 3.3 V
700	1600	0	50	V_{CC} = 3.0 V

2. Example (when C_{TP} = 0.1 µF and C_{TW} = 0.01 µF)

	Symbol	V_{CC} = 3.3 V	V_{CC} = 3.0 V
time (ms)	t_{PR}	≈ 75	≈ 70
	t_{WD}	≈ 16	≈ 16
	t_{WR}	≈ 5.5	≈ 5

13. Notes On Use

- Take account of common impedance when designing the earth line on a printed wiring board.

- Take measures against static electricity.
  - For semiconductors, use antistatic or conductive containers.
  - When storing or carrying a printed circuit board after chip mounting, put it in a conductive bag or container.
  - The work table, tools and measuring instruments must be grounded.
  - The worker must put on a grounding device containing 250 kΩ to 1 MΩ resistors in series.

- Do not apply a negative voltage
  - Applying a negative voltage of –0.3 V or less to an LSI may generate a parasitic transistor, resulting in malfunction.

14. Ordering Information

Part number	Package	Marking	Remarks
MB3793-27APF-❑❑❑E1	8-pin Plastic SOP (SOE008)	3793-Y	–
MB3793-27APNF-❑❑❑E1	8-pin Plastic SOP (SOB008)	3793-Y	–

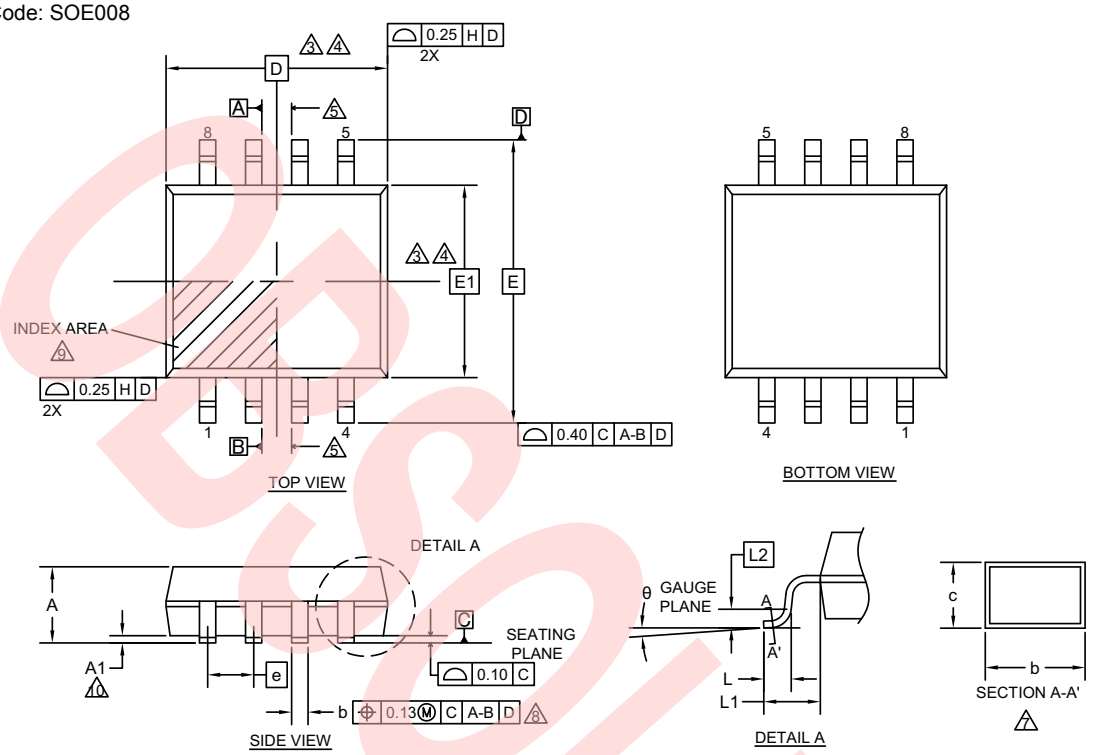
15. RoHS Compliance Information

The LSI products of Cypress with “E1” are compliant with RoHS Directive , and has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB) , and polybrominated diphenyl ethers (PBDE) .

The product that conforms to this standard is added “E1” at the end of the part number.

16. Package Dimensions

Package Code: SOE008



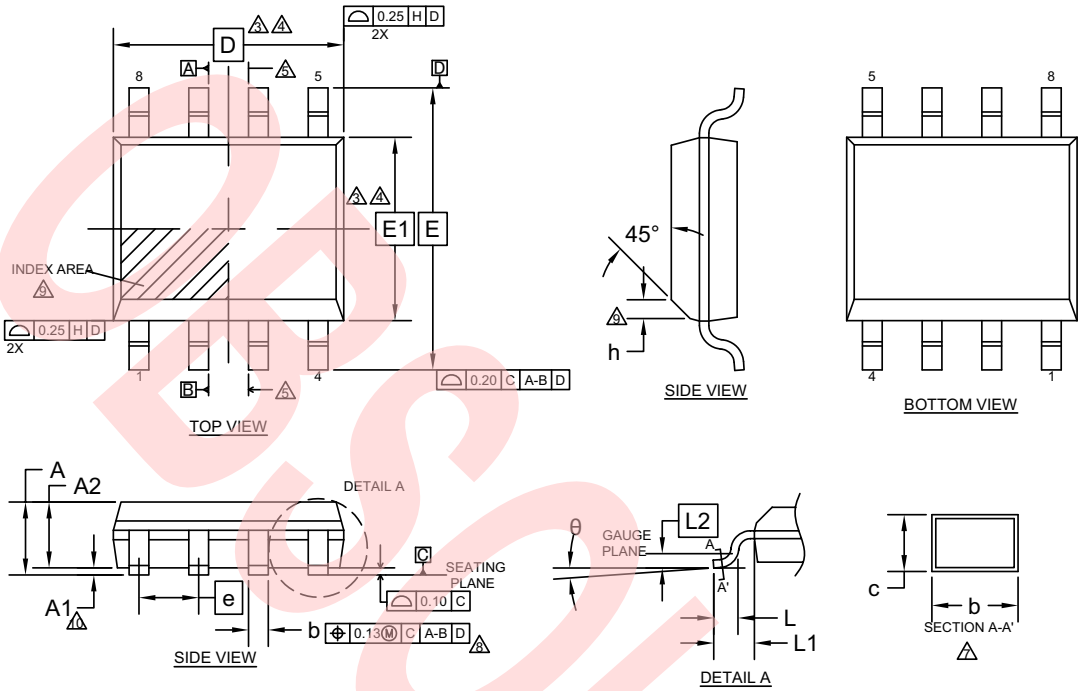
SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	——	——	2.25
A1	0.05	——	0.20
D	6.35 BSC		
E	7.80 BSC		
E1	5.30 BSC		
θ	0°	——	8°
c	0.13	——	0.20
b	0.39	0.47	0.55
L	0.45	0.60	0.75
L 1	1.25 REF		
L 2	0.25 BSC		
e	1.27 BSC		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A & B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION.
THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. LF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
10. "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
11. JEDEC SPECIFICATION NO. REF : N/A

002-15857 Rev. **

Package Code: SOB008



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.75
A1	0.05	——	0.25
A2	1.30	1.40	1.50
D	5.05 BSC.		
E	6.00 BSC.		
E1	3.90 BSC		
θ	0°	——	8°
c	0.15	——	0.25
b	0.36	0.44	0.52
L	0.45	0.60	0.75
L 1	1.05 REF		
L 2	0.25 BSC		
e	1.27 BSC.		
h	0.40 BSC.		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
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6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. LF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
10. "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
11. JEDEC SPECIFICATION NO. REF : N/A

002-15856 Rev. **

17. Major Changes

Spansion Publication Number: MB3793-27A_DS04-27404

Page	Section	Change Results
Revision 4.0		
-	-	Company name and layout design change
1	DESCRIPTION	Deleted "There is also a mask option that can detect voltages of 4.9 V to 2.4 V in 0.1-V steps."

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: MB3793-27A Power Voltage Monitoring IC with Watchdog Timer
Document Number: 002-08550

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	TAOA	01/30/2015	Migrated to Cypress and assigned document number 002-08550. No change to document contents or format.
*A	5169535	TAOA	04/01/2016	Updated to Cypress template
*B	5592786	HIXT	01/23/2017	Updated Pin Assignment: Change the package name from FPT-8P-M01 to SOE008 Change the package name from FPT-8P-M02 to SOB008 Updated Ordering Information: Change the package name from FPT-8P-M01 to SOE008 Change the package name from FPT-8P-M02 to SOB008 Updated Package Dimensions: Updated to Cypress format Deleted "Marking Format (Lead Free version)" Deleted "Labeling Sample (Lead free version)" Deleted "MB3793-27APF- ❑❑❑ E1, MB3793-27APNF- ❑❑❑ E1 Recommended Conditions of Moisture Sensitivity Level" Deleted the part numbers, MB3793-27APF- ❑❑❑ and MB3793-27APNF- ❑❑❑ , from Ordering Information Deleted the words in the Remarks, "Lead Free version", from Ordering Information
*C	5790102	MASG	06/29/2017	Adapted Cypress new logo.
*D	6406322	YOST	12/10/2018	Obsoleted.

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