ANALOG DEVICES

Dual-Mode, Ka Band Upconverter with Integrated Fractional-N PLL and VCO

Data Sheet **ADMV4530**

FEATURES

- **RF output frequency range: 27 GHz to 31 GHz**
- **Two upconversion modes**
  - **Direct upconversion from differential baseband I/Q (I/Q mode)**
  - **Single upper sideband upconversion (IF mode)**
- **1 dB bandwidth: 500 MHz (I/Q mode)**
- **Input frequency range: 2 GHz to 3 GHz (IF mode)**
- **Matched, 50 Ω, single-ended RF output**
- **Matched, 50 Ω, single-ended IF input**
- **Programmable baseband I/Q common mode-voltage**
- **Sideband rejection and carrier feedthrough optimization**
- **Combined RF and IF gain dynamic range: 70 dB**
- **Programmable automatic IF gain control**
- **Programmable via 3-wire or 4-wire SPI**
- **40-terminal, 6 mm × 6 mm, RoHS compliant LGA**

APPLICATIONS

- **Satellite communication**
- **Point to point microwave communication**

GENERAL DESCRIPTION

The ADMV4530 is a highly integrated upconverter with an inphase/quadrature (I/Q) mixer that is ideally suited for next generation Ka band satellite communications.

An integrated low phase noise, fractional-N phase-locked loop (PLL) with a voltage controlled oscillator (VCO) and internal 2× multiplier generate the necessary on-chip local oscillator (LO) signal for the I/Q mixer, eliminating the need for external frequency synthesis. The VCO uses an internal autocalibration routine that allows the PLL to select the necessary settings and locks in approximately 100 µs.

The single-ended reference input to the PLL operates up to 500 MHz and features internal reference dividers and a multiplier for added flexibility. Additionally, the phase frequency detector (PFD) comparison frequency can be up to 250 MHz for integer mode and 160 MHz for fraction-N mode.

The upconverter consists of an I/Q mixer that can operate in either I/Q mode with 500 MHz of bandwidth or in IF mode up to 3 GHz of bandwidth, which allows various radio architectures and backward compatibility with legacy systems.

Immediately following the I/Q mixer are stages of gain and variable attenuation. The configuration can achieve a minimum 1 dB compression point (P1dB) compression point of 19 dBm, eliminating the need for external stages of gain.

A programmable 4-wire serial port interface (SPI) allows adjustment of the quadrature phase for optimum sideband suppression. In addition, the SPI allows nulling of LO feedthrough in IF mode. In I/Q mode, the LO feedthrough can be nulled by applying external dc offset to the differential baseband I/Q inputs.

An IF automatic gain control (AGC) adjusts the IF variable gain amplifier (VGA) to compensate for input power variations. During normal operation, this AGC feature can be enabled or disabled via the SPI. When disabled during normal operation, the AGC feature only works on a test tone during power-down mode to track temperature variations.

The ADMV4530 upconverter comes in a RoHs compliant, 6 mm × 6 mm, 40-terminal land grid array (LGA) package. The ADMV4530 operates over the −40°C to +85°C case temperature range.

Rev. A **Document Feedback**

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REVISION HISTORY

3/2020—Rev. 0 to Rev. A

Change to Data Sheet Title ... 1

3/2020—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

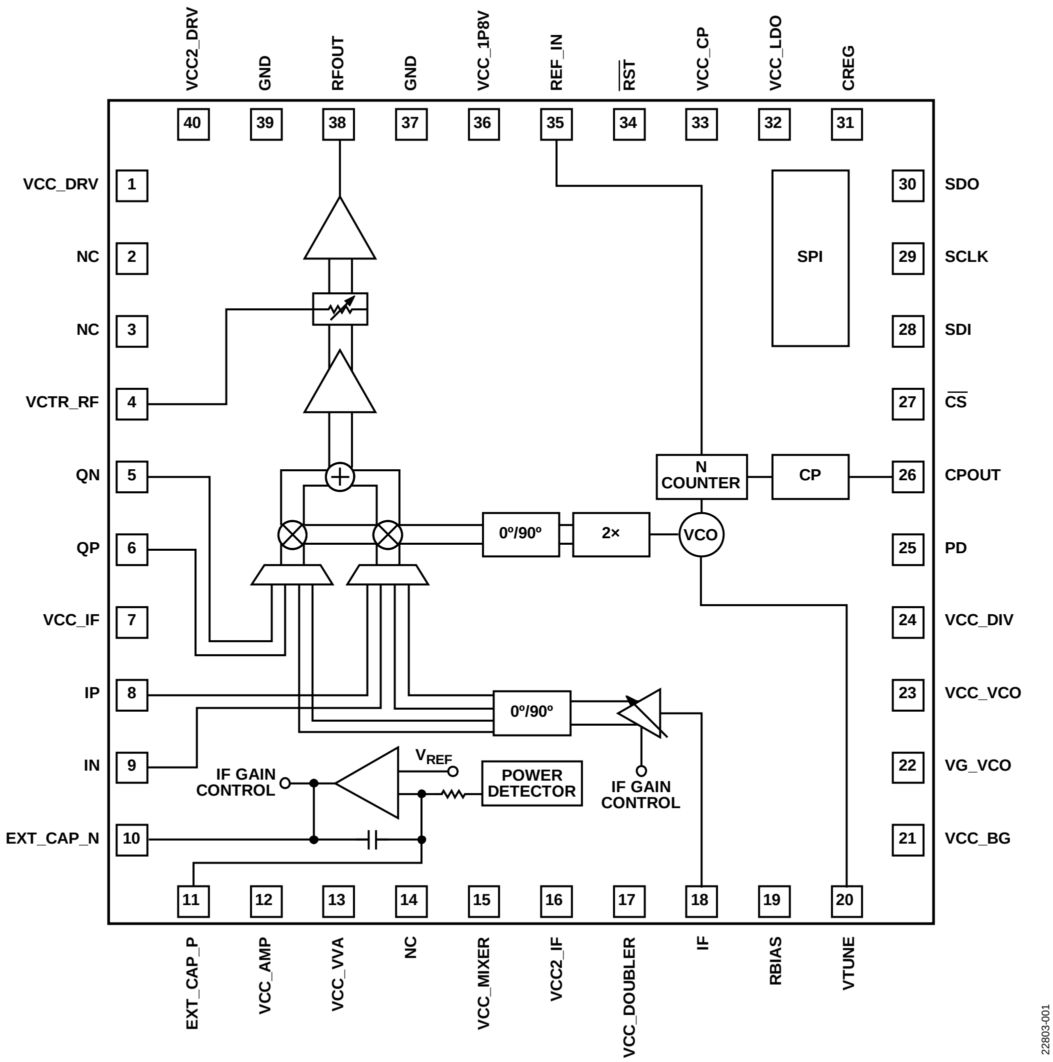


Figure 1.

SPECIFICATIONS

VCC_DRV = VCC_AMP = VCC2_DRV = 4 V, VCC_IF = VCC2_IF = VCC_VVA = VCC_MIXER = VCC_DOUBLER = VCC_VCO = VCC_DIV = VCC_LDO = VCC_CP = 3.3 V, VCC_1P8V = 1.8 V, and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LO FREQUENCY RANGE	25.6		30	GHz	
VCO					
Frequency Range	12.8		15	GHz	
Voltage Range (V_{TUNE})	0.5		2.8	V	
Tuning Sensitivity (K_{VCO})		165		MHz/V	At VCO frequency
Open-Loop Phase Noise					
1 kHz Offset		−49		dBc/Hz	
10 kHz Offset		−76		dBc/Hz	
100 kHz Offset		−102		dBc/Hz	
1 MHz Offset		−125		dBc/Hz	
10 MHz Offset		−145		dBc/Hz	
40 MHz Offset		−150		dBc/Hz	
PLL					
Reference Input					
Voltage	0		1.8	V p-p	
Capacitance		7		pF	
Reference Frequency		200		MHz	
PFD Frequency					
Integer Mode		250		MHz	
Fractional-N Mode		160		MHz	
PFD In Band Phase Noise		−147		dBc/Hz	PFD frequency (f_{PFD}) = 200 MHz
Lock Detect					
Locked			3.3	V	
Unlocked	0.1	0.3	0.5	V	

I/Q MODE

I/Q frequency = 25 MHz, I/Q input power = −10 dBm, RF frequency = 29 GHz, 1 MHz tone spacing, upper sideband, R_WORD = 2, CP_CURRENT = 4.20 mA, REF_IN power = 8 dBm, REF_IN frequency = 200 MHz, loop filter bandwidth = 540 kHz, VCC_DRV = VCC_AMP = VCC2_DRV = 4 V, VCC_IF = VCC2_IF = VCC_VVA = VCC_MIXER = VCC_DOUBLER = VCC_VCO = VCC_DIV = VCC_LDO = VCC_CP = 3.3 V, VCC_1P8V = 1.8 V, T_A = 25°C, common-mode voltage (V_{CM}) = 0.5 V, VCTR_RF = 1.8 V, and board losses de-embedded to the device, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT FREQUENCY RANGE	27		31	GHz	
OUTPUT RETURN LOSS		−4		dB	
RF GAIN	17	21		dB	
Flatness		±1		dB	
Dynamic Range		30		dB	
VCTR_RF Control					
Range	0		1.8	V	
Slope		32		dB/V	VCTR_RF = 0.6 V to 1.5 V
1 dB COMPRESSION POINT (P1dB)	17	19		dBm	Maximum gain
OUTPUT THIRD-ORDER DISTORTION (IP3)		29		dBm	Maximum gain, −10 dBm per tone, 1 MHz tone spacing
NOISE DENSITY		−139		dBm/Hz	Maximum gain
OUTPUT SPURIOUS					Spurs at maximum gain
Reference Spurs		−65		dBm	
VCO Feedthrough		−75		dBm	
1 dB BANDWIDTH		500		MHz	Per differential I and Q inputs
I/Q COMMON-MODE VOLTAGE (V_{CM})	0	0.5	2.5	V	
DIFFERENTIAL INPUT IMPEDANCE		100		Ω	
SIDEBAND REJECTION		−27		dBc	Uncalibrated
LO TO RF LEAKAGE					
Minimum Gain		−41		dBm	Uncalibrated
Maximum Gain		−15		dBm	Uncalibrated
		−45		dBm	Calibrated
SUPPLY VOLTAGE					
	3.8	4.0	4.2	V	VCC_DRV, VCC_AMP, and VCC2_DRV pins
	3.2	3.3	3.4	V	VCC_IF, VCC2_IF, VCC_VVA, VCC_MIXER, VCC_DOUBLER, VCC_BG, VCC_VCO, VCC_DIV, VCC_LDO, and VCC_CP pins
	1.7	1.8	1.9	V	VCC_1P8V
SUPPLY CURRENT					
		200		mA	VCC_DRV, VCC_AMP, and VCC2_DRV pins
		320		mA	VCC_IF, VCC2_IF, VCC_VVA, VCC_MIXER, VCC_DOUBLER, VCC_BG, VCC_VCO, VCC_DIV, VCC_LDO, and VCC_CP pins
		2		mA	VCC_1P8V

IF MODE

IF frequency = 2.7 GHz, IF power = −41 dBm, RF frequency = 29 GHz, 1 MHz tone spacing, upper sideband, R_WORD = 4, CP_CURRENT = 2.10 mA, REF_IN power = 8 dBm, REF_IN frequency = 200 MHz, loop filter bandwidth = 100 kHz, VCC_DRV = VCC_AMP = VCC2_DRV = 4 V, VCC_IF = VCC2_IF = VCC_VVA = VCC_MIXER = VCC_DOUBLER = VCC_VCO = VCC_DIV = VCC_LDO = VCC_CP = 3.3 V, VCC_1P8V = 1.8 V, T_A = 25°C, VCTR_RF = 1.8 V, VCTR_IF = 0 V, and board losses de-embedded to the device, unless otherwise noted. Note that VCTR_IF is the voltage applied to the EXT_CAP_x pins.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT FREQUENCY RANGE	28		30	GHz	
OUTPUT RETURN LOSS		−4		dB	
GAIN		50		dB	VCTR_IF = 0 V
Flatness		0.25		dB	Within a bandwidth of 50 MHz
Dynamic Range		70		dB	VCTR_RF and VCTR_IF combined dynamic range
VCTR_RF Control					
Range	0		1.8	V	
Slope		32		dB/V	VCTR_RF = 0.6 V to 1.5 V
VCTR_IF Control					
AGC Set Voltage	0		2.5	V	Accessed via SPI map
Range	0		3.3	V	When bypassing AGC
Slope		−32		dB/V	VCTR_IF = 0.9 V to 2.2 V for both AGC or external control voltage
P1dB	17	19		dBm	Maximum gain
OUTPUT IP3		29		dBm	Maximum gain, −41 dBm per tone, 1 MHz tone spacing
NOISE DENSITY		−139		dBm/Hz	Maximum gain
OUTPUT SPURIOUS					Spurs at maximum gain
Reference Spurs		−65		dBm	
VCO Feedthrough		−75		dBm	
LO TO RF LEAKAGE		−10		dBm	Uncalibrated
		−35		dBm	Calibrated
SIDEBAND REJECTION	−24	−35		dBc	Uncalibrated
INPUT RANGE					
Frequency	2	2.5	3	GHz	
Power			0	dBm	
INPUT RETURN LOSS		12		dB	
SUPPLY VOLTAGE					
	3.8	4.0	4.2	V	VCC_DRV, VCC_AMP, and VCC2_DRV pins
	3.2	3.3	3.4	V	VCC_IF, VCC2_IF, VCC_VVA, VCC_MIXER, VCC_DOUBLER, VCC_BG, VCC_VCO, VCC_DIV, VCC_LDO, and VCC_CP pins
	1.7	1.8	1.9	V	VCC_1P8V
SUPPLY CURRENT					
		190		mA	VCC_DRV, VCC_AMP, and VCC2_DRV pins
		470		mA	VCC_IF, VCC2_IF, VCC_VVA, VCC_MIXER, VCC_DOUBLER, VCC_BG, VCC_VCO, VCC_DIV, VCC_LDO, and VCC_CP pins
		2		mA	VCC_1P8V

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VCC_DRV, VCC_AMP, and VCC2_DRV	5 V
VCC_IF, VCC2_IF, VCC_VVA, VCC_MIXER, VCC_DOUBLER, VCC_BG	4.3 V
VCC_VCO, VCC_DIV, VCC_LDO, VCC_CP	3.6 V
VCC_1P8V	2.3 V
REF_IN to GND	−0.3 V to +2.1 V
Input Power	
IF	10 dBm
I/Q	5 dBm
Temperature	
Junction	125°C
Lifetime at Maximum Junction (T_J)	10^6 hours
Operating Range	−40°C to +85°C
Storage Range	−55°C to +150°C
Lead Range (Soldering 60 sec)	260°C
Moisture Sensitivity Level (MSL) Rating	MSL3
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	1000 V
Field Induced Charged Device Model (FICDM)	1000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.
θ_{JC} is the junction to case thermal resistance.

Only use θ_{JA} and θ_{JC} to compare the thermal performance of different packages when all test conditions listed are similar to JEDEC specifications. Otherwise, use Ψ_{JT} and Ψ_{JB} to calculate the device junction temperature using the following equations:

$$T_J = (P \times \Psi_{JT}) + T_{TOP} \quad (1)$$

where:
P is the total power dissipation in the chip (W).
Ψ_{JT} is the junction to top thermal characterization number.
T_{TOP} is package top temperature (°C). T_{TOP} is measured at the top center of the package.

$$T_J = (P \times \Psi_{JB}) + T_{BOARD} \quad (2)$$

where:
P is the total power dissipation in the chip (W).
Ψ_{JB} is the junction to board thermal characterization number.
T_{BOARD} is the board temperature measured on the midpoint of the longest side of the package, no more than 1 mm from the edge of the package body (°C).

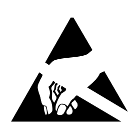
As stated in JEDEC51-12, only use Equation 1 and Equation 2 when no heat sink or heat spreader is present. When a heat sink or heat spreader is added, use θ_{JC_TOP} or θ_{JC_BOT} to estimate or calculate the junction temperature.

Table 5. Thermal Resistance

Package Type	θ_{JC_BOT}[1]	θ_{JC_TOP}[1]	Ψ_{JT}	Ψ_{JB}	θ_{JA}	Unit
CC-40-8	5.9	12.8	3.0	8.5	28.2	°C/W

[1] See JEDEC Standard JESD51-2 for additional information on optimizing the thermal impedance.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

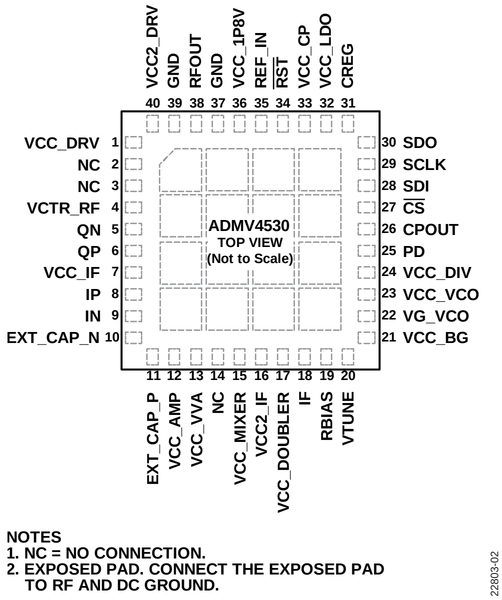


Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 12, 40	VCC_DRV, VCC_AMP, VCC2_DRV	Supply Voltages for the RF Output Driver, 4.0 V. Place a 1 µF decoupling capacitor close to each pin.
2, 3, 14	NC	No Connection.
4	VCTR_RF	RF Gain Control, 0 V to 1.8 V.
5, 6, 8, 9	QN, QP, IP, IN	Differential Quadrature Baseband Inputs. These 50 Ω differential impedance inputs can be common-mode dc biased from 0 V to 2.5 V.
7, 16	VCC_IF, VCC2_IF	Supply Voltages for the IF and Baseband Inputs, 3.3 V. Place a 1 µF decoupling capacitor close to each pin.
10	EXT_CAP_N	IF Gain Control Capacitor Negative Terminal. To adjust the IF gain manually, this pin must be driven externally when the AGC functionality is disabled, 0 V to 3.3 V. Note that VCTR_IF is the voltage applied to the EXT_CAP_x pins.
11	EXT_CAP_P	IF Gain Control Capacitor Positive Terminal. Note that VCTR_IF is the voltage applied to the EXT_CAP_x pins.
13	VCC_VVA	Supply Voltage for the Variable Gain Amplifier, 1.8 V. Place a 1 µF decoupling capacitor close to this pin.
15	VCC_MIXER	Supply Voltage for the Mixer, 3.3 V. Place a 1 µF decoupling capacitor close to this pin.
17	VCC_DOUBLER	Supply Voltage for the Internal 2× Multiplier, 3.3 V. Place a 1 µF decoupling capacitor close to this pin.
18	IF	IF Input. This pin has a 50 Ω input impedance.
19	RBIAS	Resistor Band Gap Reference Bias. Place a precision 680 Ω resistor to ground at this pin.
20	VTUNE	VCO Tune Port, 0.5 V to 2.8 V. This pin is driven by the output of the loop filter.
21	VCC_BG	Supply Voltage for the Internal Band Gap, 3.3 V. Place a 1 µF decoupling capacitor close to this pin.
22	VG_VCO	VCO Gate Decoupling. Place a 10 µF decoupling capacitor at this pin.
23	VCC_VCO	Supply Voltage for the VCO, 3.3 V. Place a 1 µF decoupling capacitor close to this pin.
24	VCC_DIV	Supply Voltage for Fractional-N PLL, 3.3 V. Place a 1 µF decoupling capacitor close to this pin.

Pin No.	Mnemonic	Description
25	PD	Power-Down, 3.3 V Logic. Active high.
26	CPOUT	Charge Pump Output. Connect this pin to VTUNE (Pin 20) through the loop filter.
27	$\overline{CS}$	SPI Chip Select. 3.3 V logic. Active low.
28	SDI	SPI Data Input. 3.3 V logic.
29	SCLK	SPI Clock. 3.3 V logic.
30	SDO	SPI Data Output. 3.3 V logic.
31	CREG	External Capacitor for the Low Dropout (LDO) Regulator Output. Place a 0.1 μF decoupling capacitor close to this pin.
32	VCC_LDO	Supply Voltage for the Internal LDO Regulator, 3.3 V. Place a 1 μF decoupling capacitor close to this pin.
33	VCC_CP	Supply Voltage for the Charge Pump, 3.3 V. Place a 1 μF decoupling capacitor close to this pin.
34	$\overline{RST}$	Reset. 3.3 V logic. Active low.
35	REF_IN	PLL Reference Input. Apply an external reference signal to this pin with a 0.01 μF, dc blocking capacitor. Refer to Figure 91 for the external reference input configuration.
36	VCC_1P8V	Supply Voltage for the SPI Block, 1.8 V. Place a 1 μF decoupling capacitor close to this pin.
37, 39	GND	Ground. Connect these pins to RF and dc ground.
38	RFOUT	RF Output. This pin has a 50 Ω output impedance.
	EPAD	Exposed Pad. Connect the exposed pad to RF and dc ground.

TYPICAL PERFORMANCE CHARACTERISTICS

I/Q MODE

I/Q frequency = 25 MHz, I/Q input power = −10 dBm, RF frequency = 29 GHz, 1 MHz tone spacing, upper sideband, R_WORD = 2, CP_CURRENT = 4.20 mA, REF_IN power = 8 dBm, REF_IN frequency = 200 MHz, loop filter bandwidth = 540 kHz, VCC_DRV = VCC_AMP = VCC2_DRV = 4 V, VCC_IF = VCC2_IF = VCC_VVA = VCC_MIXER = VCC_DOUBLER = VCC_VCO = VCC_DIV = VCC_LDO = VCC_CP = 3.3 V, VCC_1P8V = 1.8 V, T_A = +25°C, −40°C, and +85°C, V_{CM} = 0.5 V, VCTR_RF = 1.8 V, and board losses de-embedded to the device, unless otherwise noted.

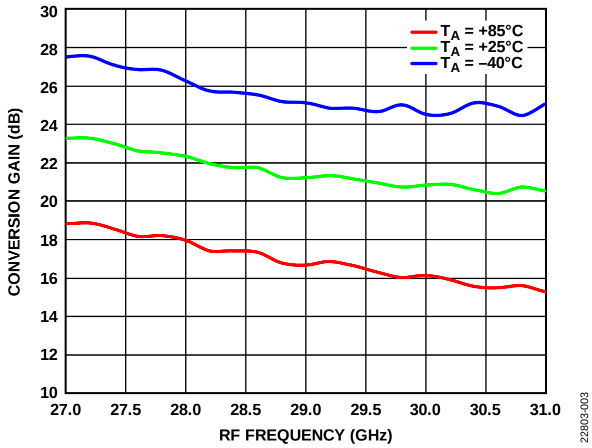


Figure 3. Conversion Gain vs. RF Frequency over Temperature

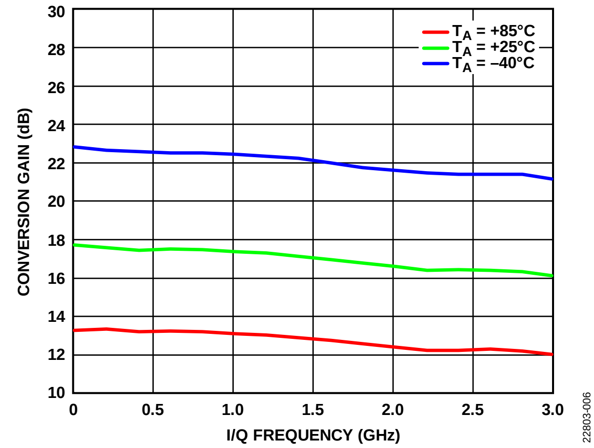


Figure 6. Conversion Gain vs. I/Q Frequency, Single Side Input over Temperature

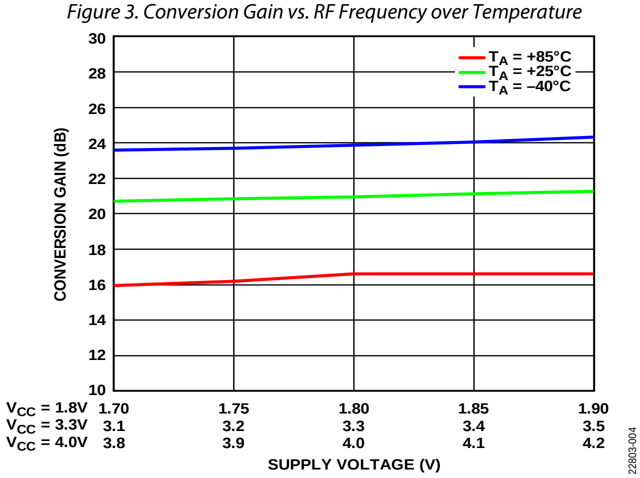


Figure 4. Conversion Gain vs. Supply Voltage over Temperature

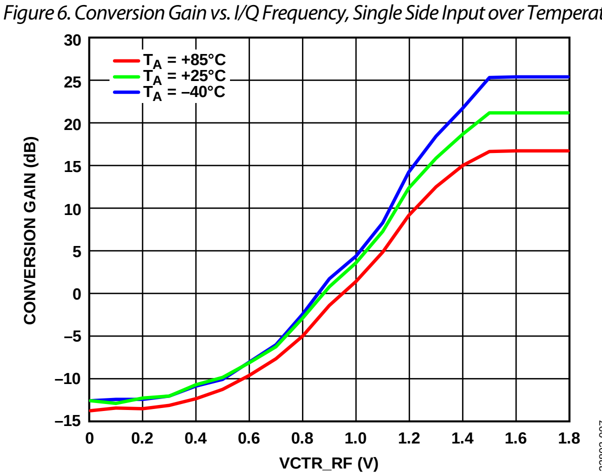


Figure 7. Conversion Gain vs. VCTR_RF over Temperature

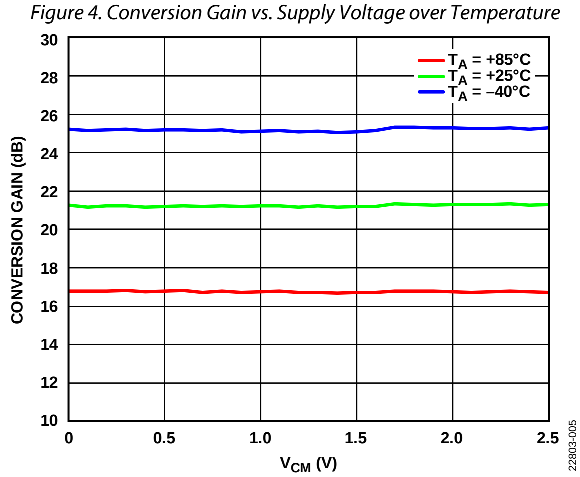


Figure 5. Conversion Gain vs. V_{CM} over Temperature

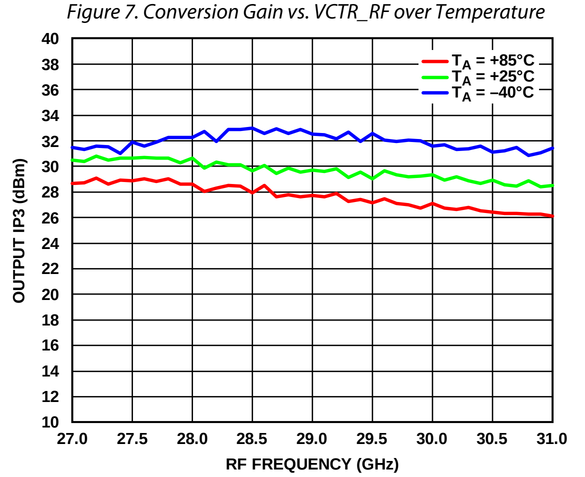


Figure 8. Output IP3 vs. RF Frequency over Temperature

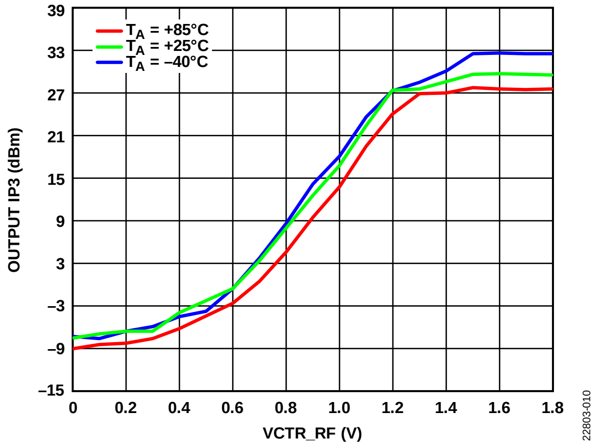


Figure 9. Output IP3 vs. VCTR_RF over Temperature

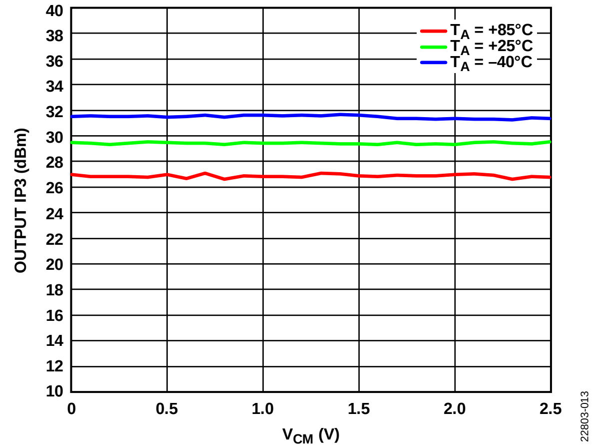


Figure 12. Output IP3 vs. V_{CM} over Temperature

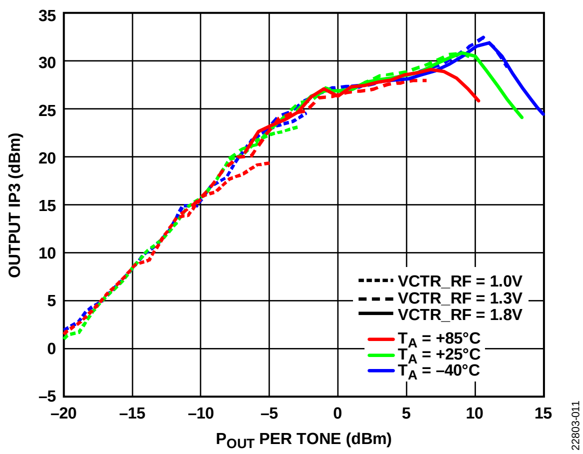


Figure 10. Output IP3 vs. Output Power (P_{OUT}) per Tone over Temperature

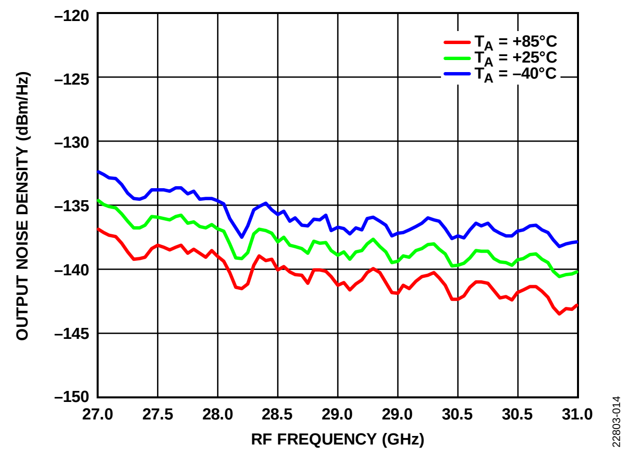


Figure 13. Output Noise Density vs. RF Frequency over Temperature

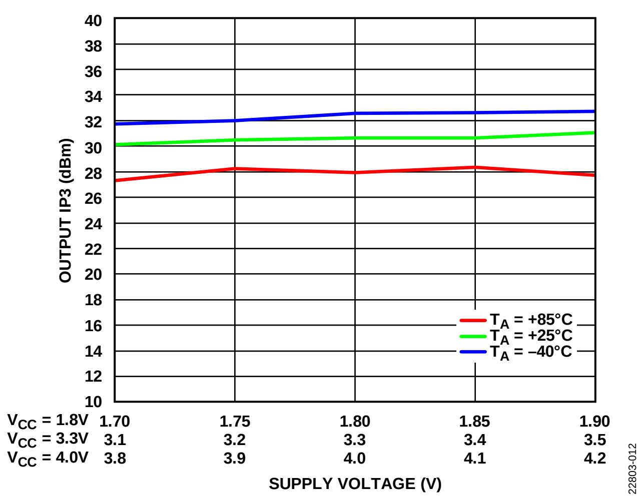


Figure 11. Output IP3 vs. Supply Voltage over Temperature

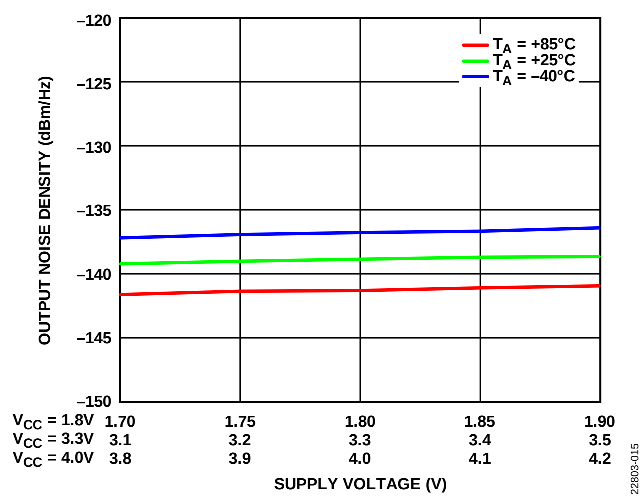


Figure 14. Output Noise Density vs. Supply Voltage over Temperature

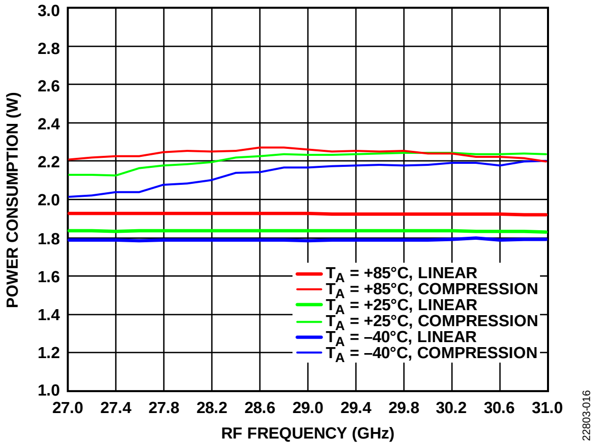


Figure 15. Power Consumption vs. RF Frequency over Temperature at Linear and Compression P_{OUT}

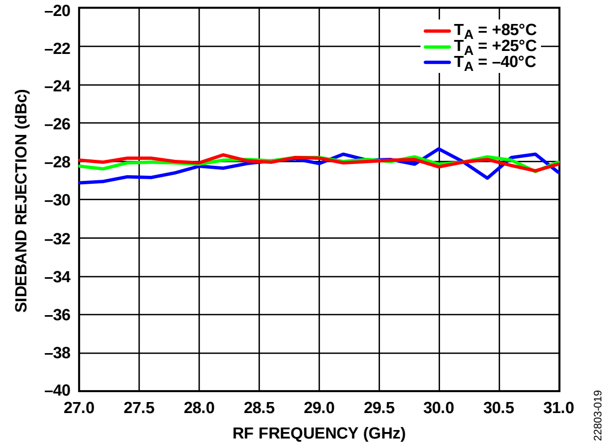


Figure 18. Sideband Rejection vs. RF Frequency over Temperature, Uncalibrated

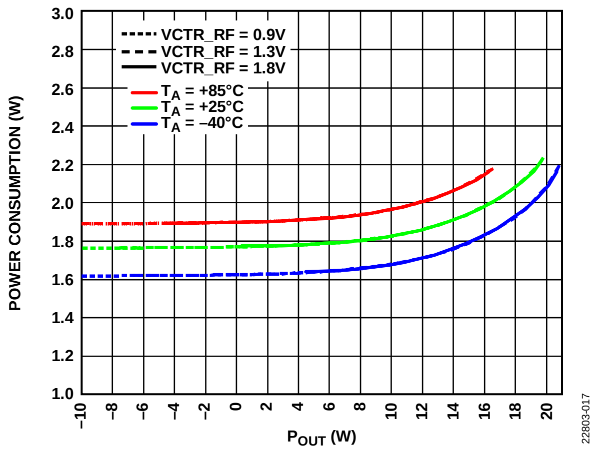


Figure 16. Power Consumption vs. P_{OUT} over Temperature

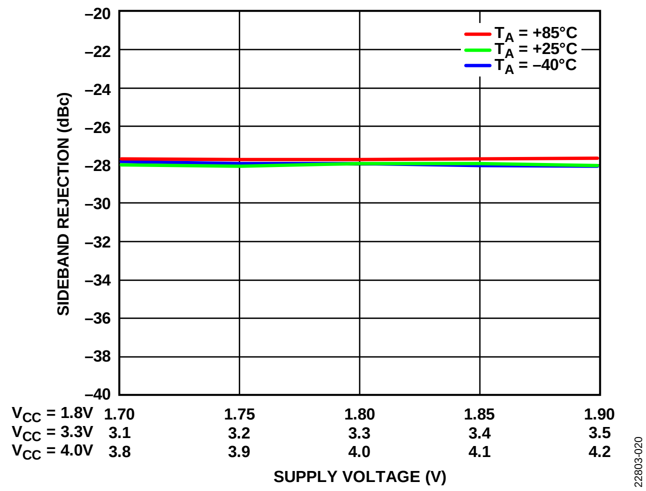


Figure 19. Sideband Rejection vs. Supply Voltage over Temperature, Uncalibrated

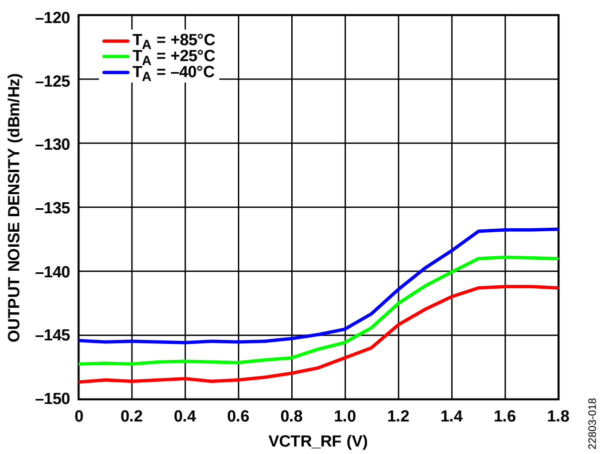


Figure 17. Output Noise Density vs. VCTR_RF over Temperature

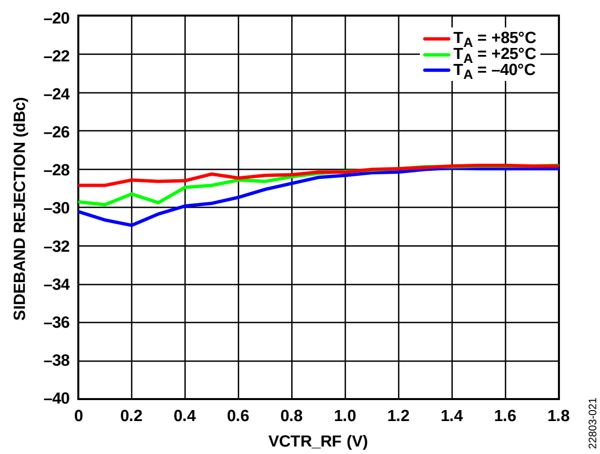


Figure 20. Sideband Rejection vs. VCTR_RF over Temperature, Uncalibrated

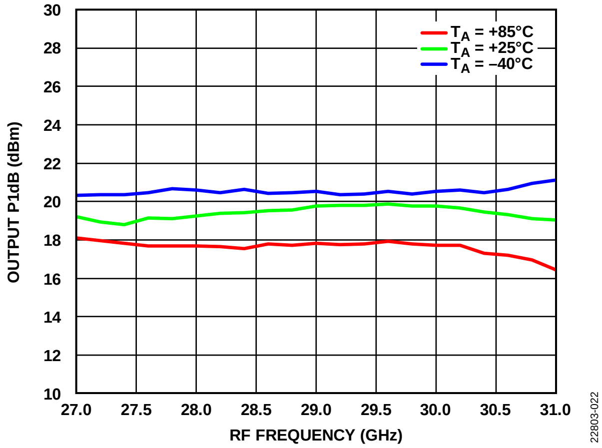


Figure 21. Output P1dB vs. RF Frequency over Temperature

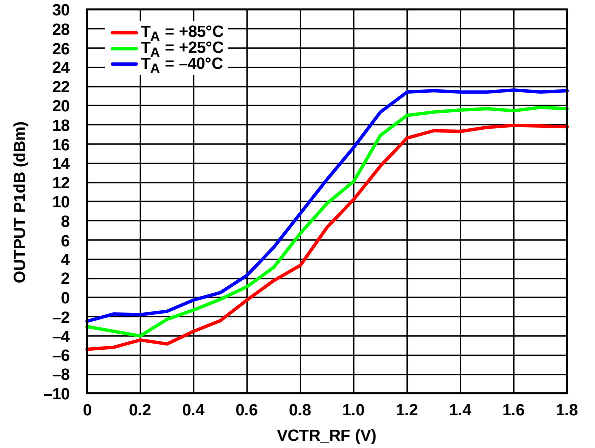


Figure 24. Output P1dB vs. VCTR_RF over Temperature

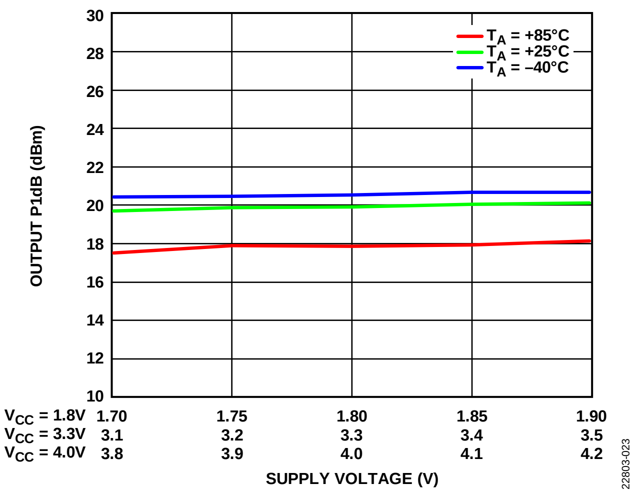


Figure 22. Output P1dB vs. Supply Voltage over Temperature

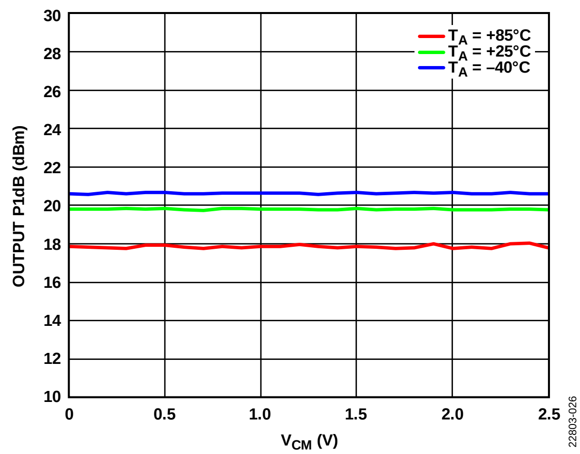


Figure 25. Output P1dB vs. V_{CM} over Temperature

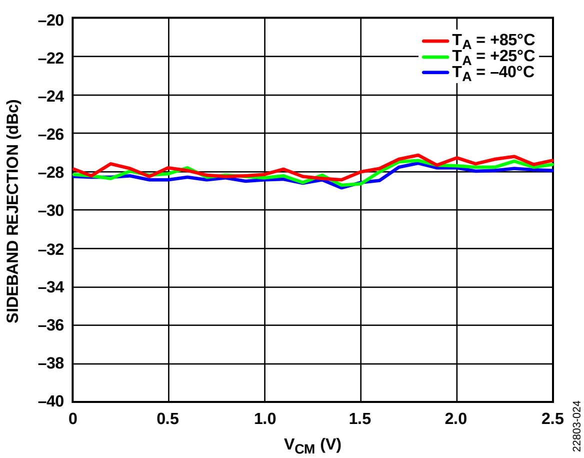


Figure 23. Sideband Rejection vs. V_{CM} over Temperature, Uncalibrated

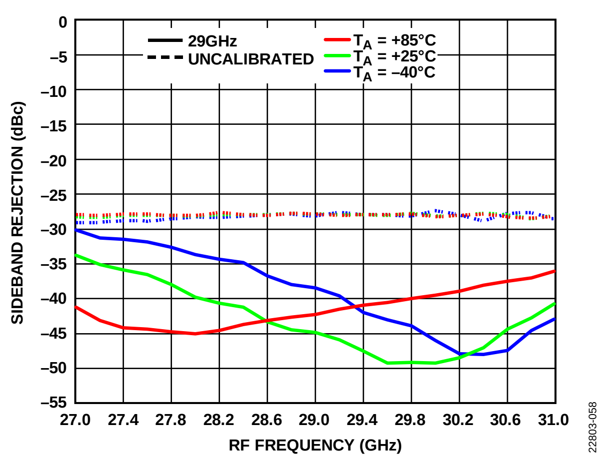


Figure 26. Sideband Rejection vs. RF Frequency over Temperature, Uncalibrated and Calibrated with RF Frequency = 29 GHz, VCTR_RF = 1.8 V at T_A = 25°C, I/Q Mode

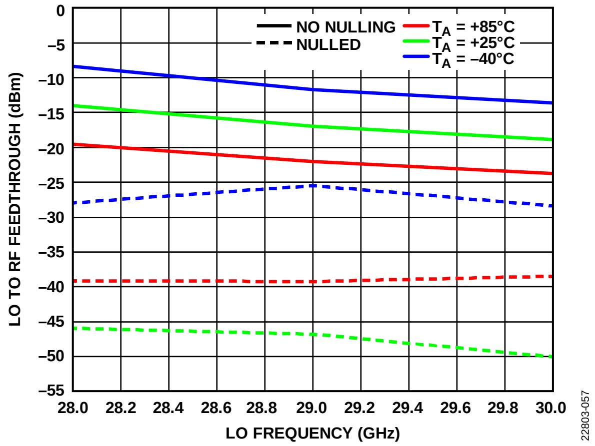


Figure 27. LO to RF Feedthrogh vs. LO Frequency over Temperature, Uncalibrated and Calibrated with LO Frequency = 28 GHz, 29 GHz, and 30 GHz, VCTR_RF = 1.8 V at T_A = 25°C, I/Q Mode

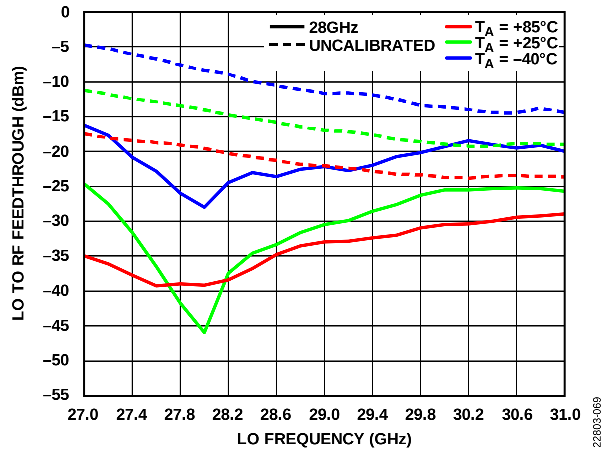


Figure 30. LO to RF Feethrough vs. LO Frequency, over Temperature, Not Calibrated and Calibrated with LO Frequency = 28 GHz at T_A = 25°C, I/Q Mode

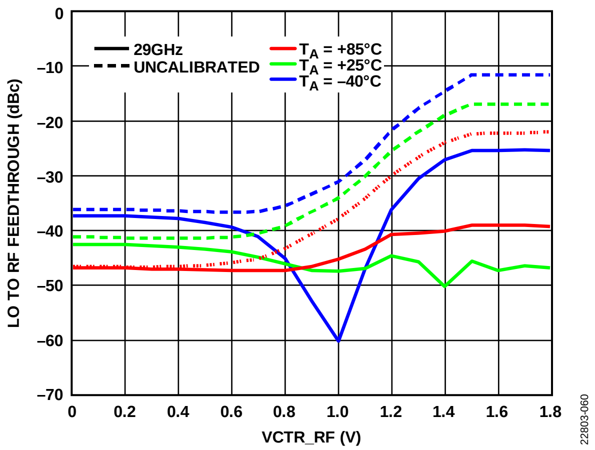


Figure 28. LO to RF Feedthrogh vs. VCTR_RF over Temperature, Uncalibrated and Calibrated with LO Frequency = 29 GHz at T_A = 25°C, I/Q Mode

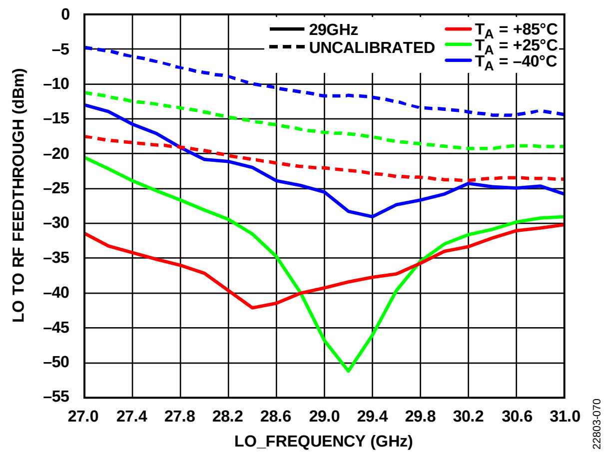


Figure 31. LO to RF Feethrough vs. LO Frequency, over Temperature, Not Calibrated and Calibrated with LO Frequency = 29 GHz at T_A = 25°C, I/Q Mode

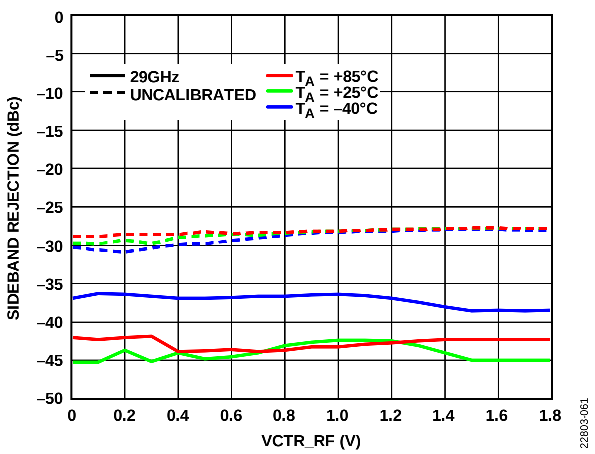


Figure 29. Sideband Rejection vs. VCTR_RF over Temperature, Uncalibrated and Calibrated with RF Frequency = 29 GHz at T_A = 25°C, I/Q Mode

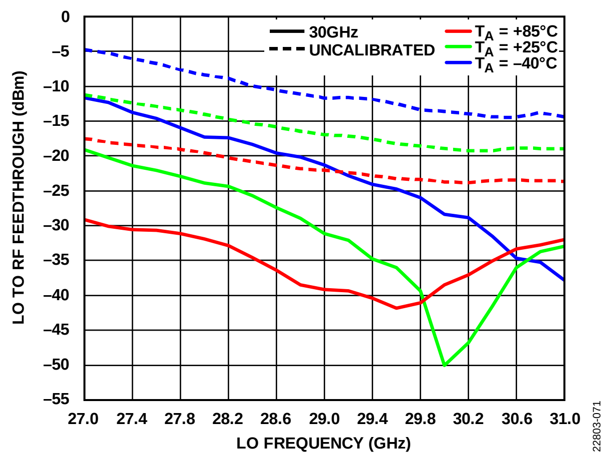


Figure 32. LO to RF Feethrough vs. LO Frequency, over Temperature, Not Calibrated and Calibrated with LO Frequency = 30 GHz at T_A = 25°C, I/Q Mode

IF MODE

IF frequency = 2.7 GHz, IF power = −41 dBm, RF frequency = 29 GHz, 1 MHz tone spacing, upper sideband, R_WORD = 4, CP_CURRENT = 2.10 mA, REF_IN power = 8 dBm, REF_IN frequency = 200 MHz, loop filter bandwidth = 100 kHz, VCC_DRV = VCC_AMP = VCC2_DRV = 4 V, VCC_IF = VCC2_IF = VCC_VVA = VCC_MIXER = VCC_DOUBLER = VCC_VCO = VCC_DIV = VCC_LDO = VCC_CP = 3.3 V, VCC_1P8V = 1.8 V, T_A = +25°C, −40°C, and +85°C, VCTR_RF =1.8 V, VCTR_IF = 0 V, and board losses de-embedded to the device, unless otherwise noted. Note that VCTR_IF is the voltage applied to the EXT_CAP_x pins.

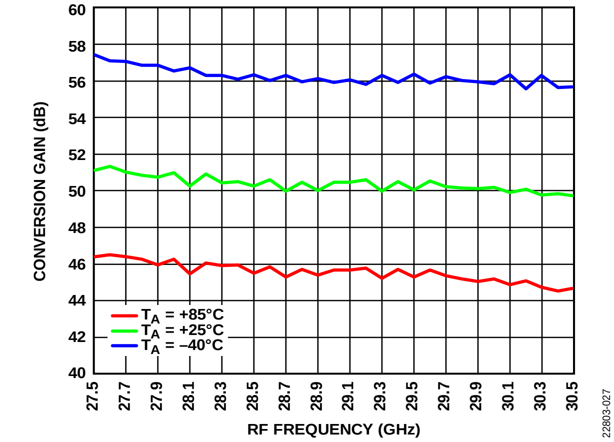


Figure 33. Conversion Gain vs. RF Frequency over Temperature

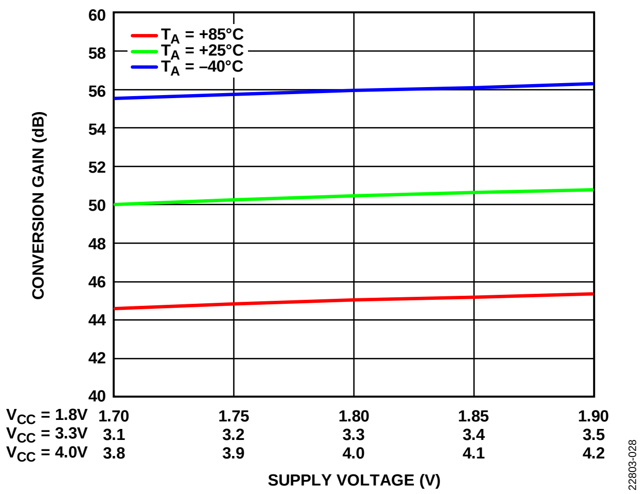


Figure 34. Conversion Gain vs. Supply Voltage over Temperature

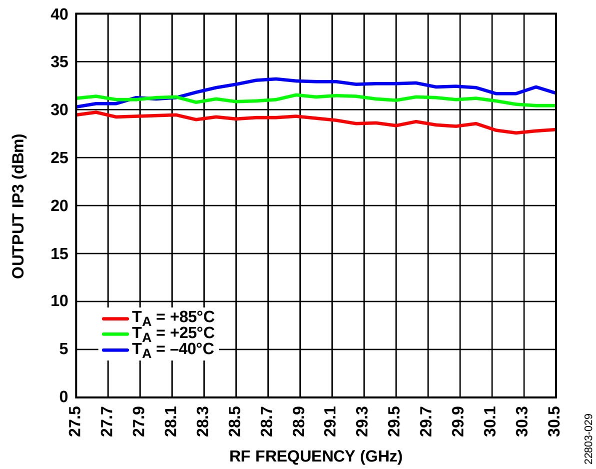


Figure 35. Output IP3 vs. RF Frequency over Temperature

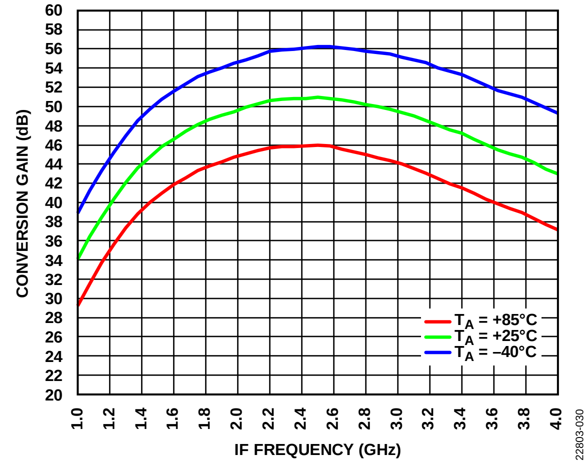


Figure 36. Conversion Gain vs. IF Frequency over Temperature

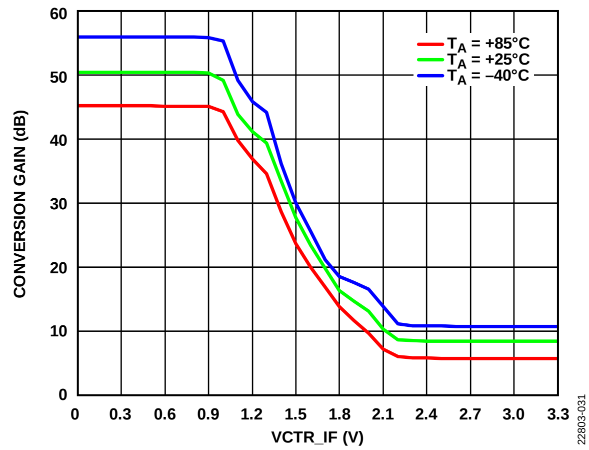


Figure 37. Conversion Gain vs. VCTR_IF over Temperature

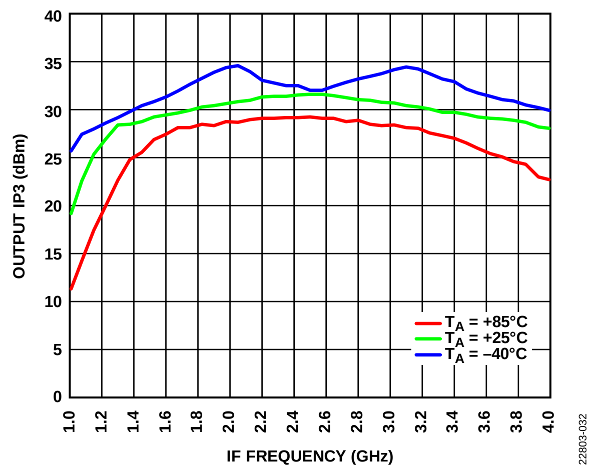


Figure 38. Output IP3 vs. IF Frequency over Temperature

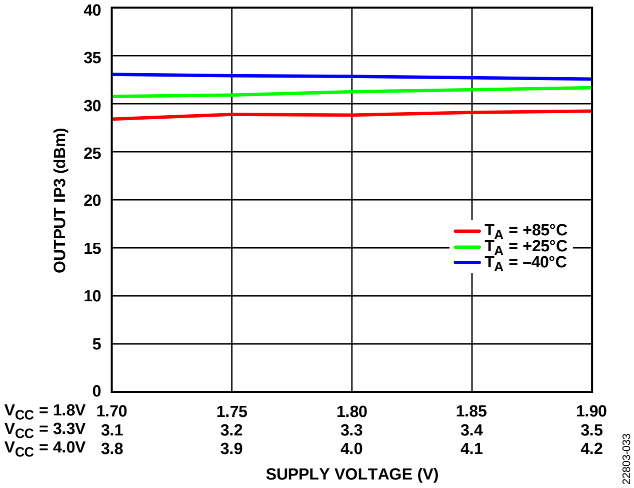


Figure 39. Output IP3 vs. Supply Voltage over Temperature

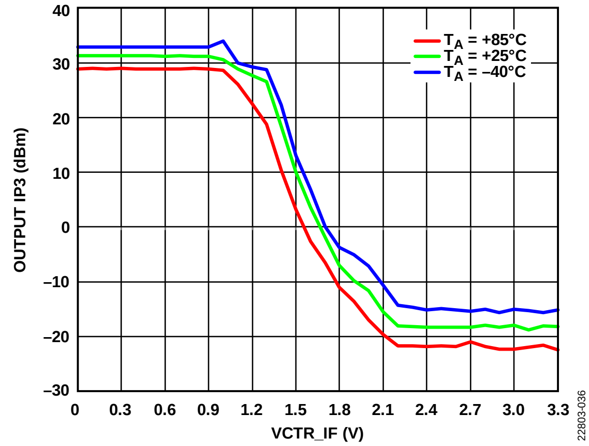


Figure 42. Output IP3 vs. VCTR_IF over Temperature

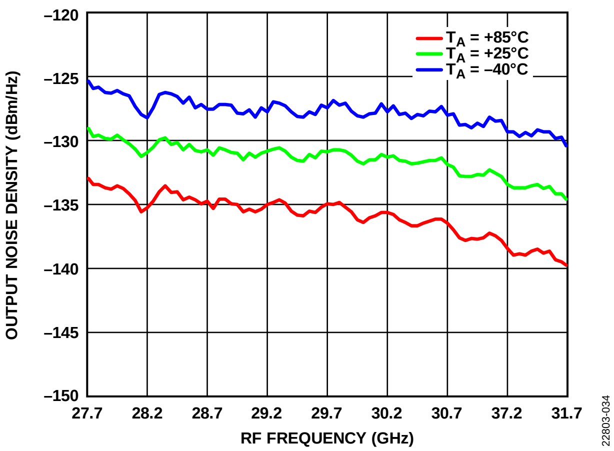


Figure 40. Output Noise Density vs. RF Frequency over Temperature

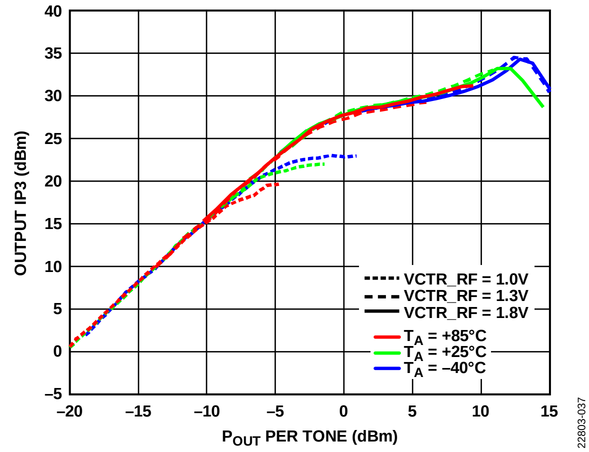


Figure 43. Output IP3 vs. P_{OUT} per Tone over Temperature and VCTR_RF

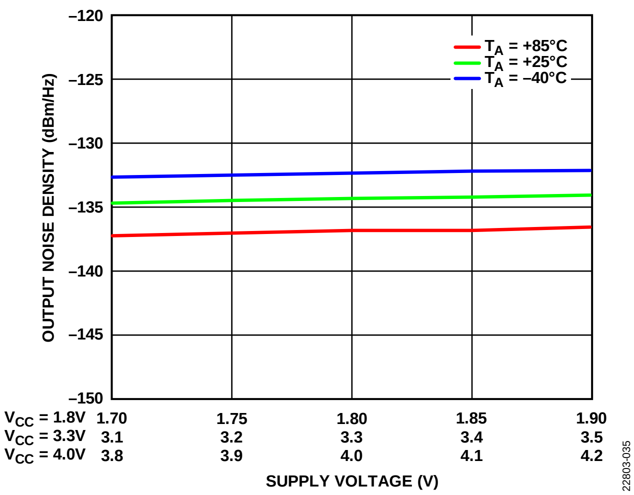


Figure 41. Output Noise Density vs. Supply Voltage over Temperature

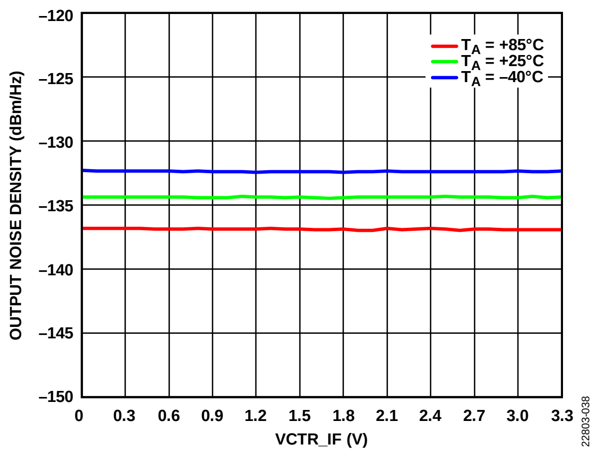


Figure 44. Output Noise Density vs. VCTR_IF over Temperature

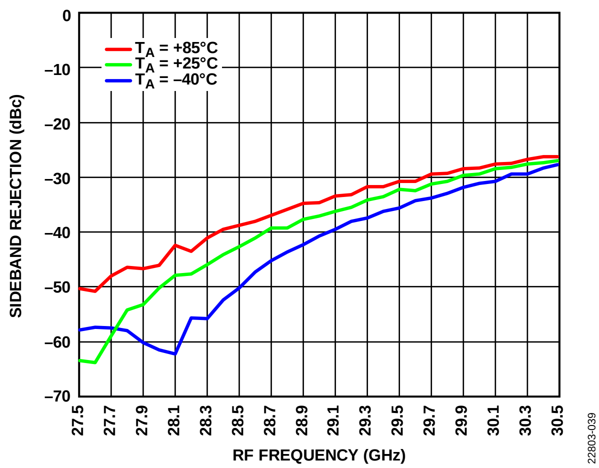


Figure 45. Sideband Rejection vs. RF Frequency over Temperature, Uncalibrated

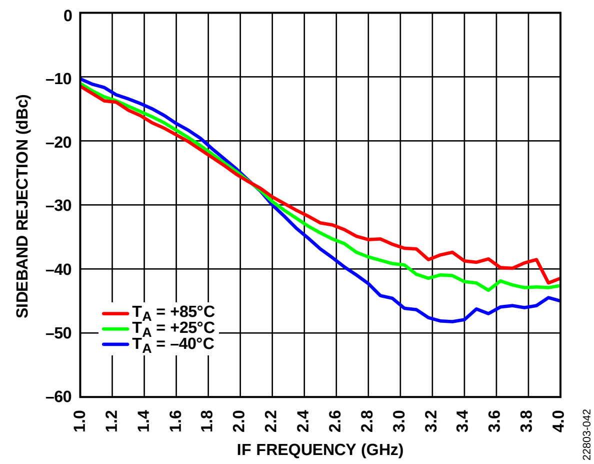


Figure 48. Sideband Rejection vs. IF Frequency over Temperature, Uncalibrated

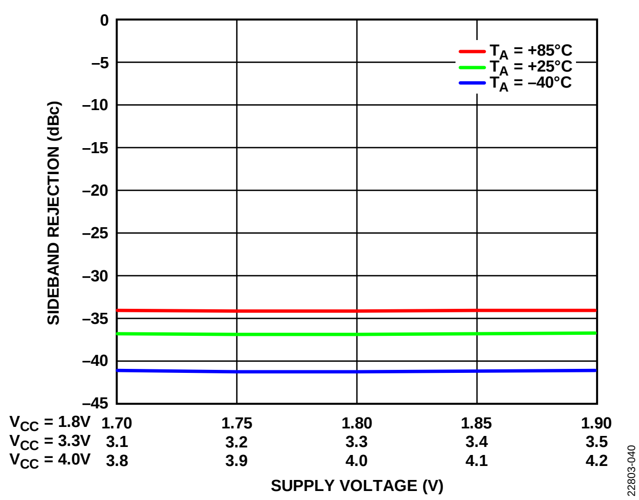


Figure 46. Sideband Rejection vs. Supply Voltage over Temperature, Uncalibrated

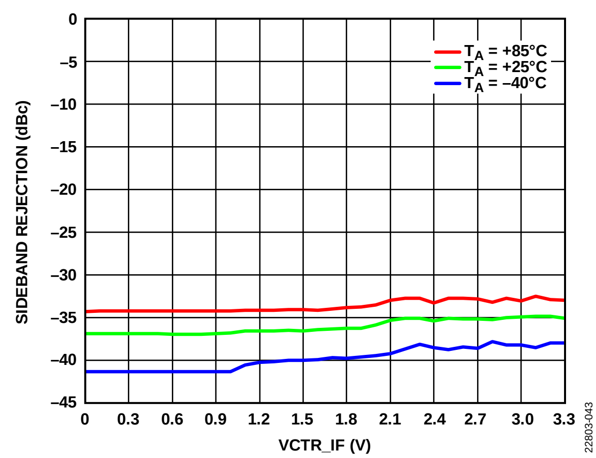


Figure 49. Sideband Rejection vs. VCTR_IF over Temperature, Uncalibrated

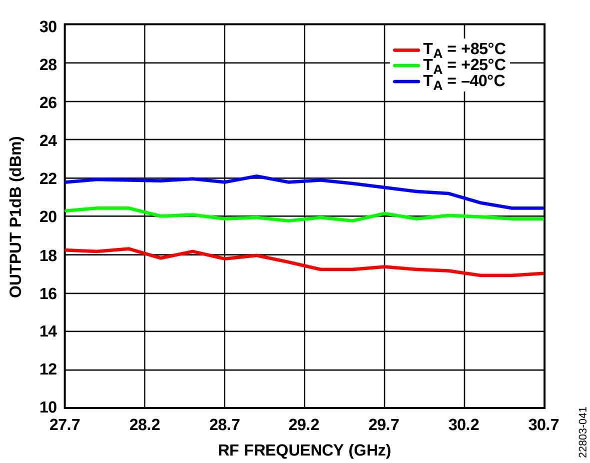


Figure 47. Output P1dB vs. RF Frequency over Temperature

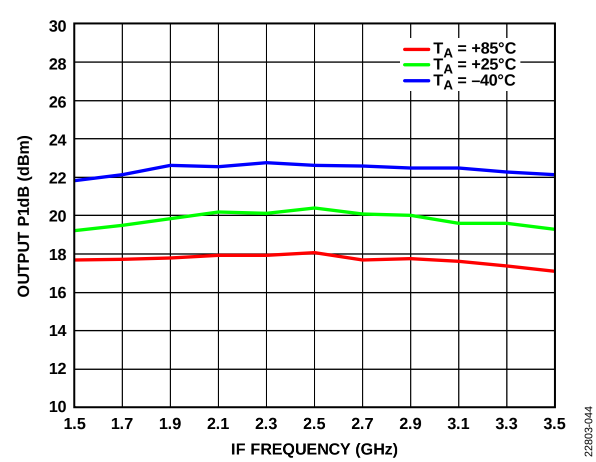


Figure 50. Output P1dB vs. IF Frequency over Temperature

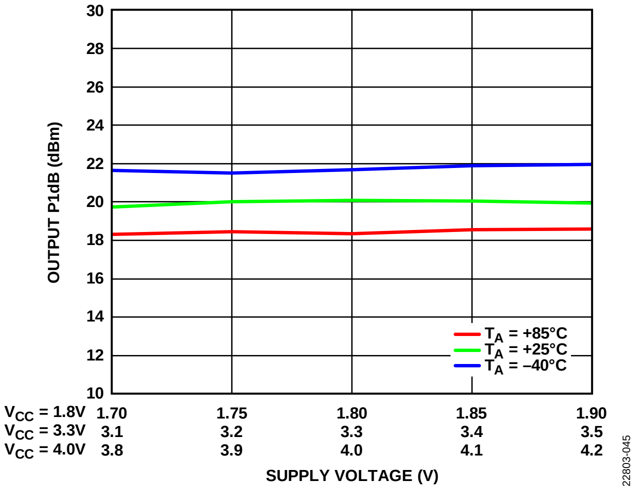


Figure 51. Output P1dB vs. Supply Voltage over Temperature

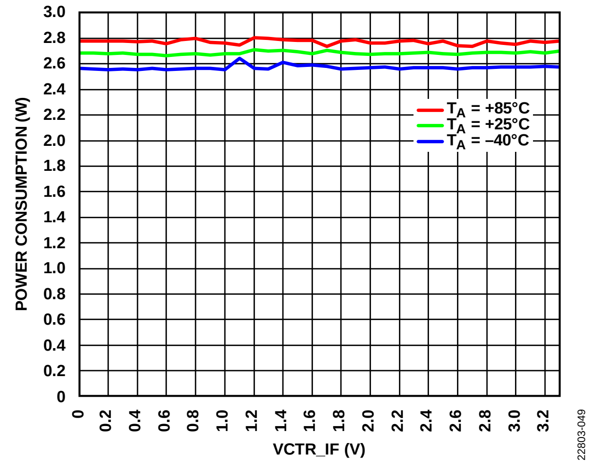


Figure 54. Power Consumption vs. VCTR_IF over Temperature at Compression P_{OUT}

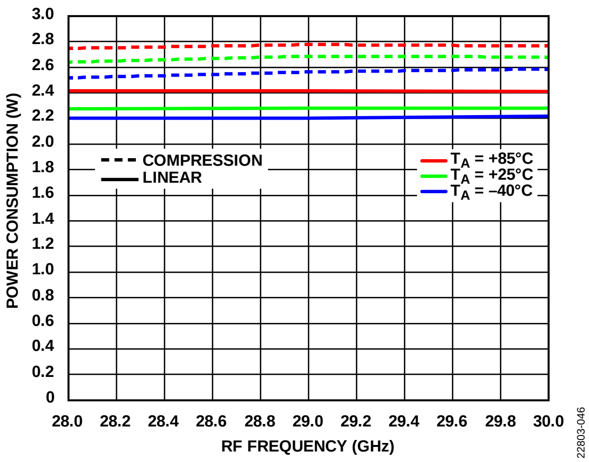


Figure 52. Power Consumption vs. RF Frequency over Temperature at Linear and Compression P_{OUT}

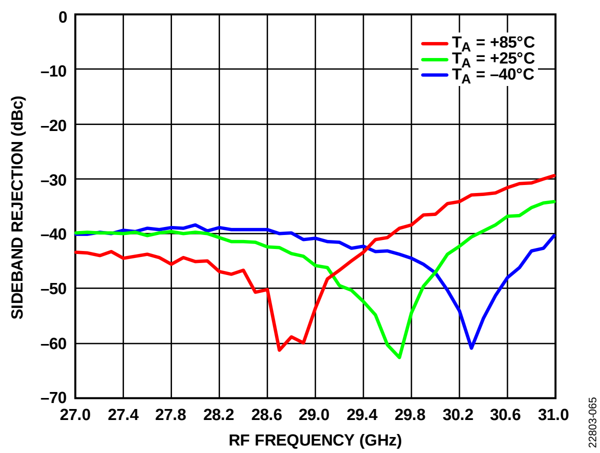


Figure 55. Sideband Rejection vs. RF Frequency over Temperature, Calibrated with RF Frequency = 30 GHz, IF Mode, VCTR_RF = 1.8 V, T_A = 25°C

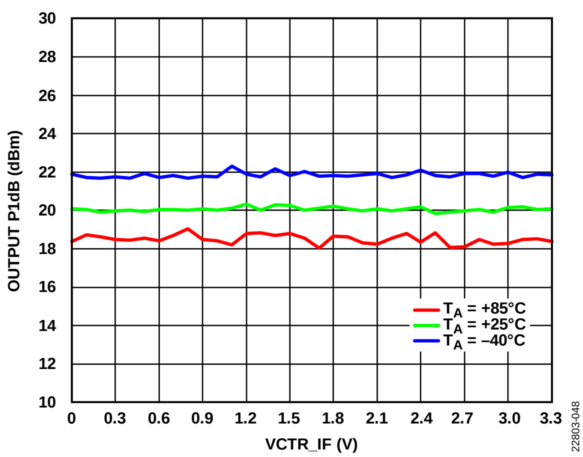


Figure 53. Output P1dB vs. VCTR_IF over Temperature

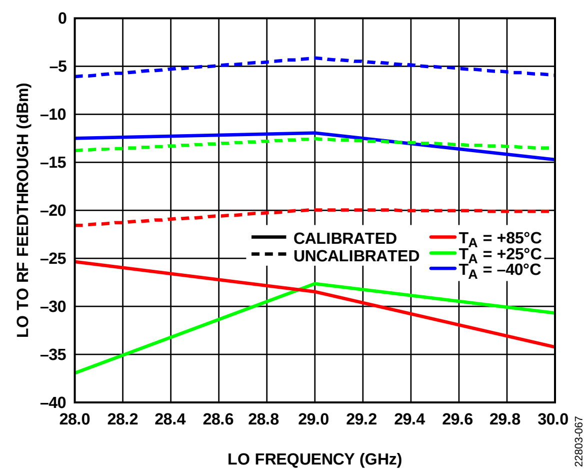


Figure 56. LO to RF Feethrough vs. LO Frequency, Calibrated at T_A = 25°C and Not Calibrated, over Temperature

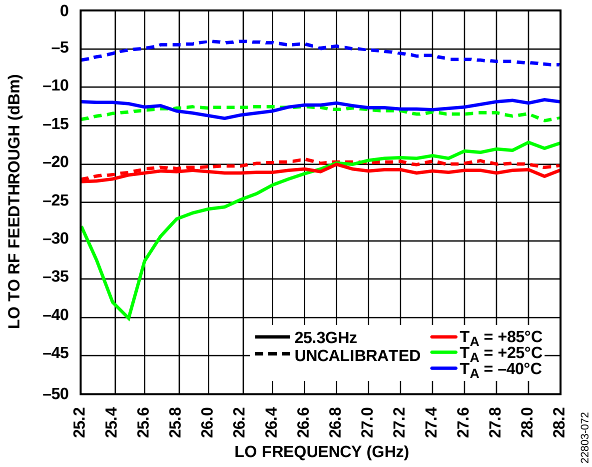


Figure 57. LO to RF Feethrough vs. LO Frequency, over Temperature, Not Calibrated and Calibrated with LO Frequency = 25.3 GHz at T_A = 25°C, IF Mode

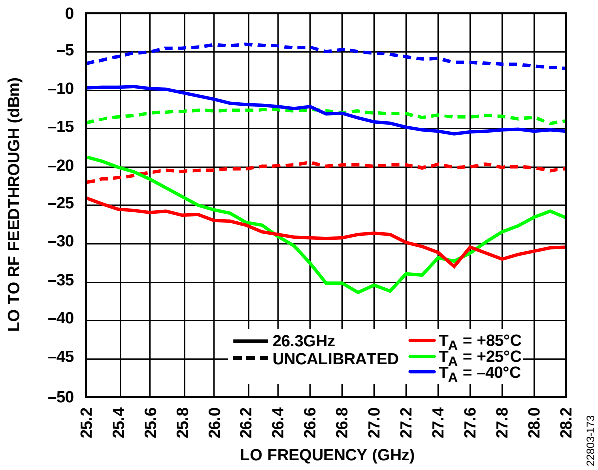


Figure 58. LO to RF Feethrough vs. LO Frequency, over Temperature, Not Calibrated and Calibrated with LO Frequency = 26.3 GHz at T_A = 25°C, IF Mode

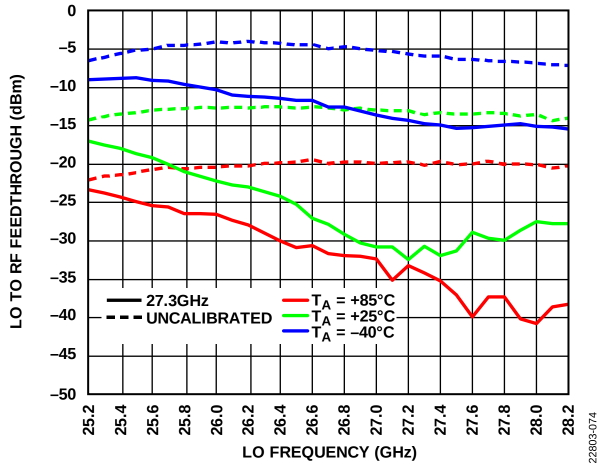


Figure 59. LO to RF Feethrough vs. LO Frequency, over Temperature, Not Calibrated and Calibrated with LO Frequency = 27.3 GHz at T_A = 25°C, IF Mode

RETURN LOSS AND LEAKAGES

VCC_DRV = VCC_AMP = VCC2_DRV = 4 V, VCC_IF = VCC2_IF = VCC_VVA = VCC_MIXER = VCC_DOUBLER = VCC_VCO = VCC_DIV = VCC_LDO = VCC_CP = 3.3 V, VCC_1P8V = 1.8 V, T_A = +25°C, −40°C, and +85°C, VCTR_RF = 1.8 V, and VCTR_IF = 0 V, unless otherwise noted.

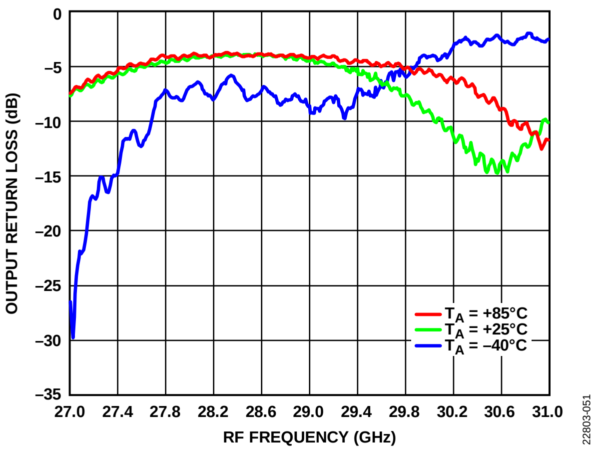


Figure 60. Output Return Loss vs. RF Frequency over Temperature

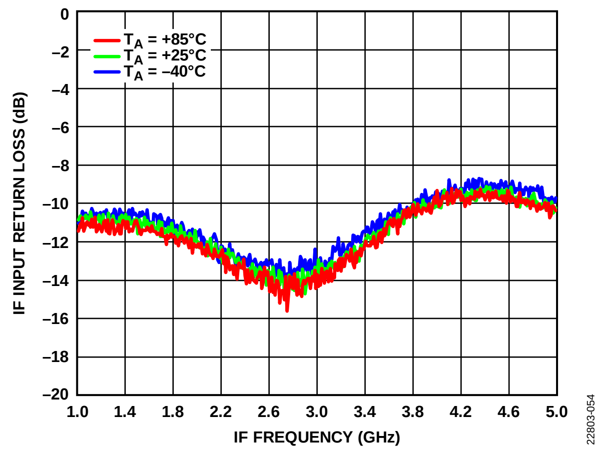


Figure 63. IF Input Return Loss vs. IF Frequency over Temperature

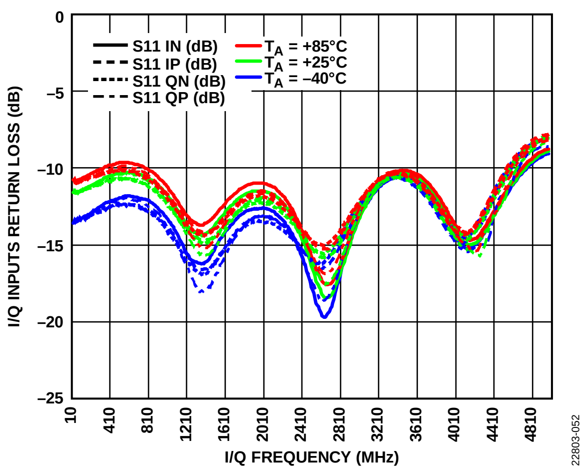


Figure 61. I/Q Inputs Return Loss vs. I/Q Frequency, Single-Ended over Temperature (S11 Is Return Loss)

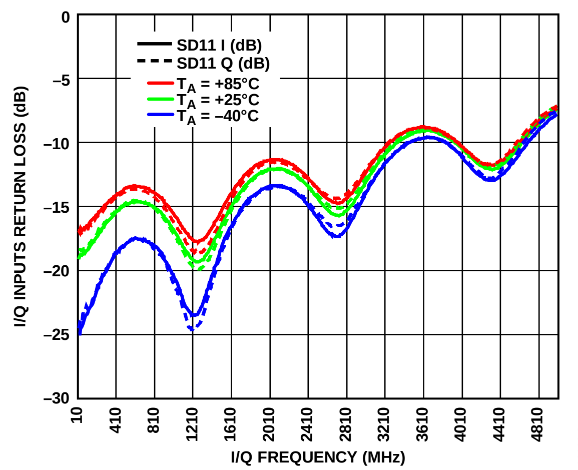


Figure 64. I/Q Inputs Return Loss vs. I/Q Frequency, Differential over Temperature (SD11 Is Differential Return Loss)

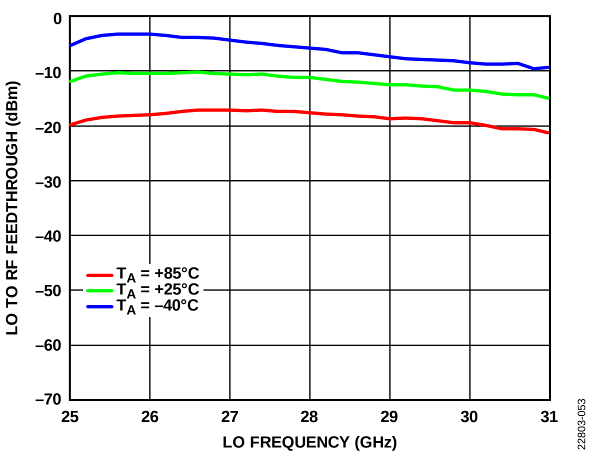


Figure 62. LO to RF Feedthrough vs. LO Frequency, Uncalibrated over Temperature

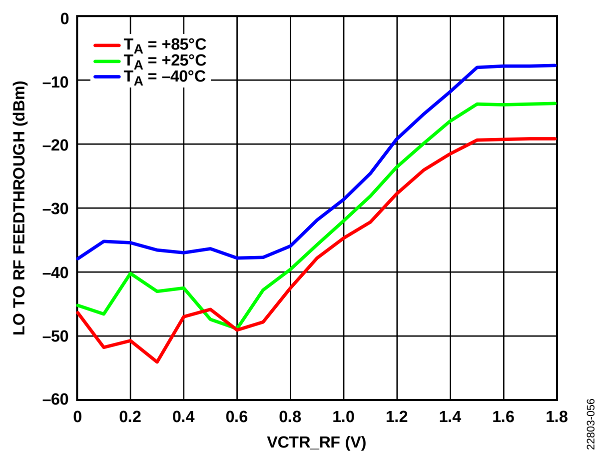


Figure 65. LO to RF Feedthrough vs. VCTR_RF, Uncalibrated over Temperature, LO Frequency = 29 GHz

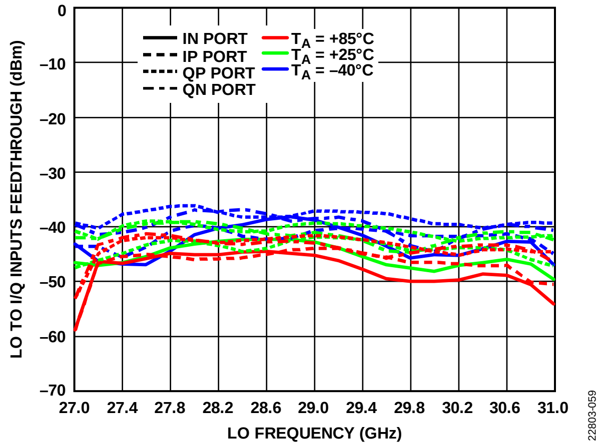


Figure 66. LO to I/Q Inputs Feedthrough vs. LO Frequency, Uncalibrated over Temperature

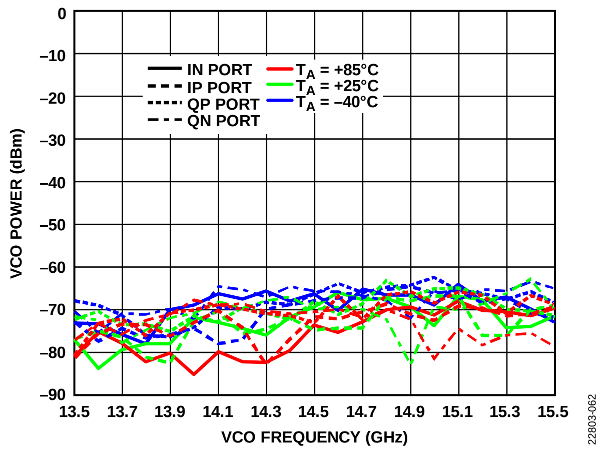


Figure 67. VCO Power vs. VCO Frequency over Temperature, Uncalibrated

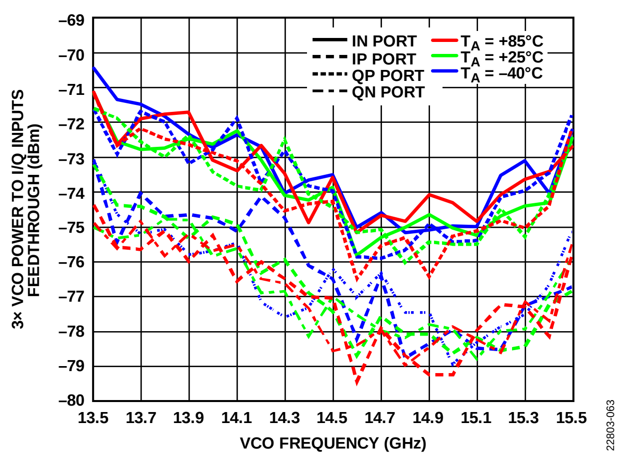


Figure 68. 3× VCO to I/Q Inputs Feedthrough vs. VCO Frequency over Temperature, Uncalibrated

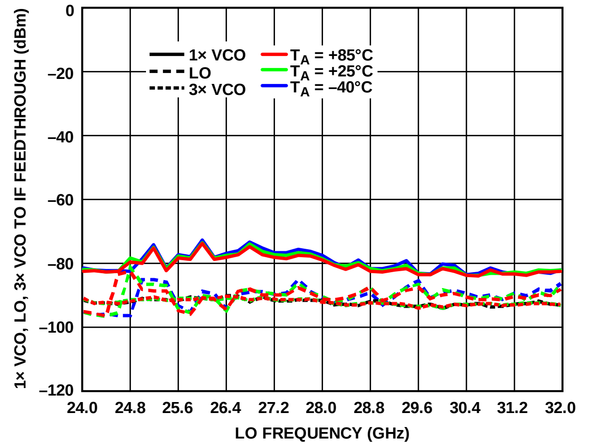


Figure 69. 1× VCO, LO, 3× VCO to IF Feedthrough vs. LO Frequency over Temperature

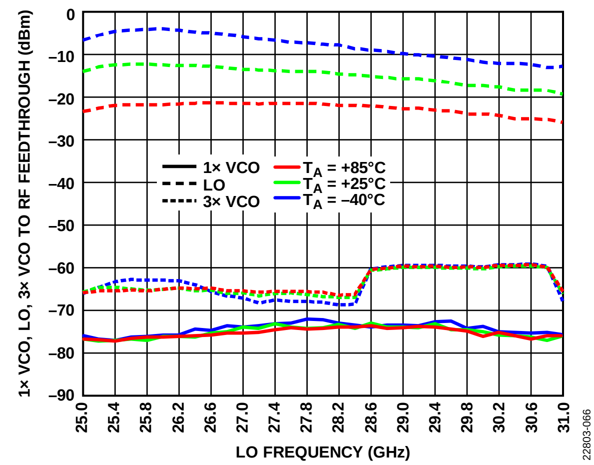


Figure 70. 1× VCO, LO, 3× VCO to RF Feedthrough vs. LO Frequency over Temperature, Uncalibrated

VCO AND PLL

VCC_DRV = VCC_AMP = VCC2_DRV = 4 V, VCC_IF = VCC2_IF = VCC_VVA = VCC_MIXER = VCC_DOUBLER = VCC_VCO = VCC_DIV = VCC_LDO = VCC_CP = 3.3 V, VCC_1P8V = 1.8 V, REF_IN power = 8 dBm, REF_IN frequency = 200 MHz T_A = +25°C, −40°C, and +85°C, VCTR_RF = 1.8 V, and VCTR_IF = 0 V, unless otherwise noted.

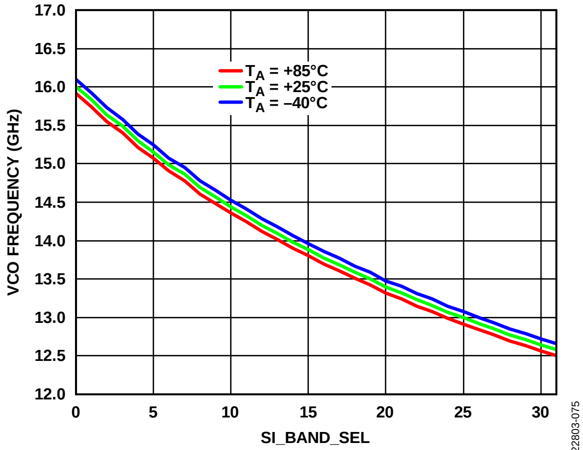


Figure 71. VCO Frequency vs. SI_BAND_SEL, Open Loop, over Temperature, VTUNE = 1.4 V

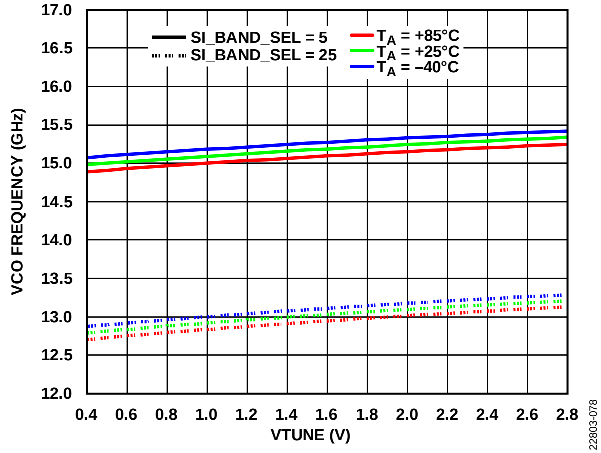


Figure 74. VCO Frequency vs. VTUNE, Open Loop over Temperature, SI_BAND_SEL = 5 and 25

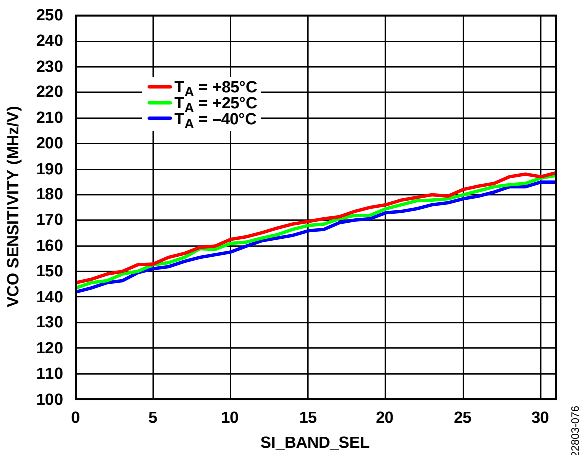


Figure 72. VCO Sensitivity vs. SI_BAND_SEL, Open Loop, over Temperatures, VTUNE = 1.4 V

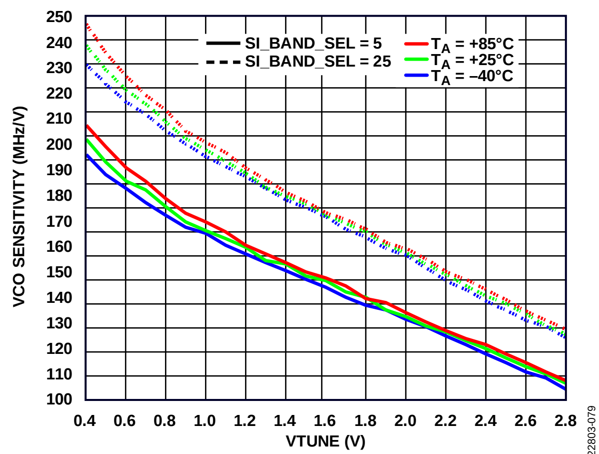


Figure 75. VCO Sensitivity vs. VTUNE, Open Loop over Temperature, SI_BAND_SEL = 5 and 25

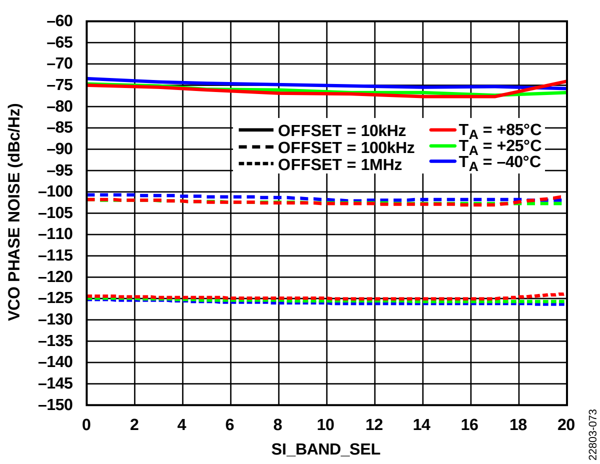


Figure 73. VCO Phase Noise vs. SI_BAND_SEL, over Temperature, Open Loop, VTUNE = 1.4 V

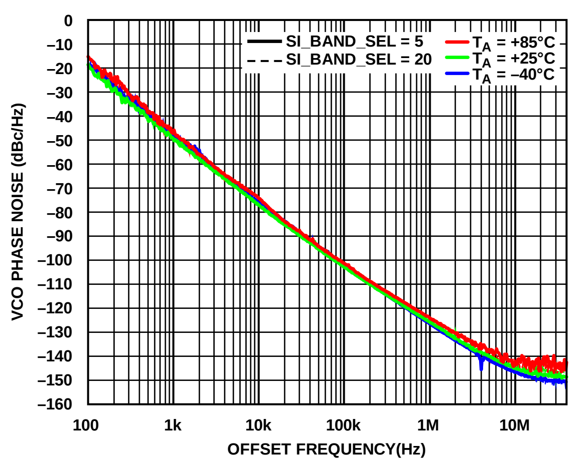


Figure 76. VCO Phase Noise vs. Offset Frequency over Temperature, Open Loop, VTUNE = 1.4 V, SI_BAND_SEL = 5 and 20

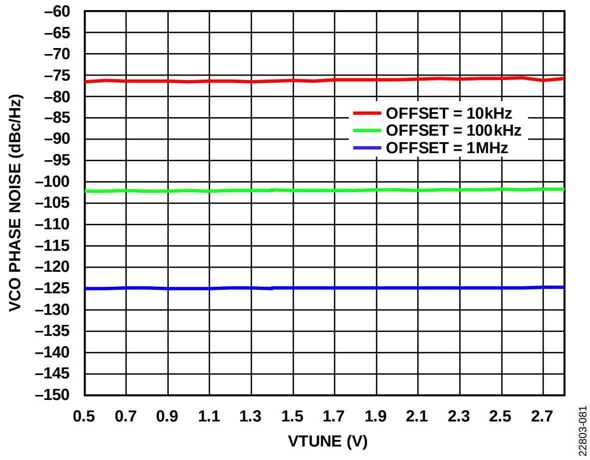


Figure 77. VCO Phase Noise vs. VTUNE for Various Offsets, Open Loop, T_A = 25°C

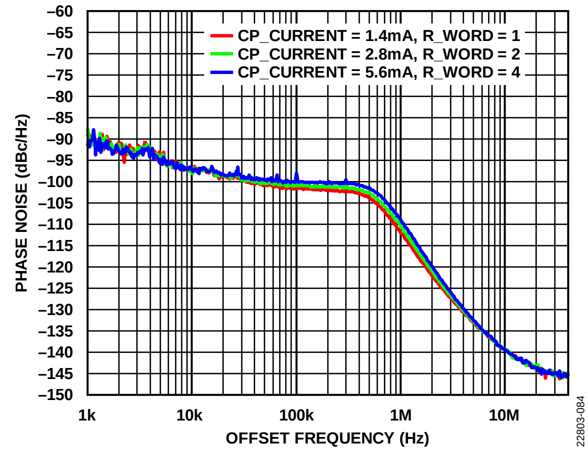


Figure 80. Phase Noise vs. Offset Frequency, LO Frequency = 27.2 GHz for Various CP_CURRENT and R_WORD Settings

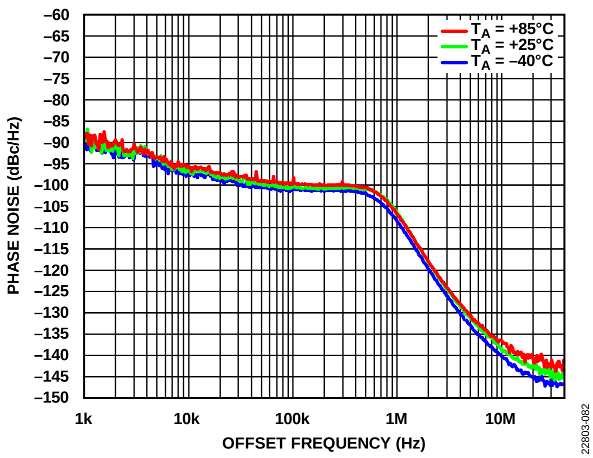


Figure 78. Phase Noise vs. Offset Frequency over Temperature, R_WORD = 2, CP_CURRENT = 4.2 mA, LO Frequency = 30 GHz

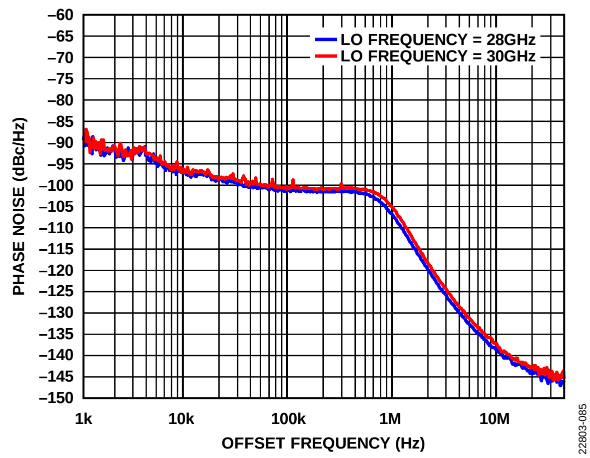


Figure 81. Phase Noise vs. Offset Frequency, R_WORD = 2, CP_CURRENT = 4.2 mA, LO Frequency = 28 GHz and 30 GHz

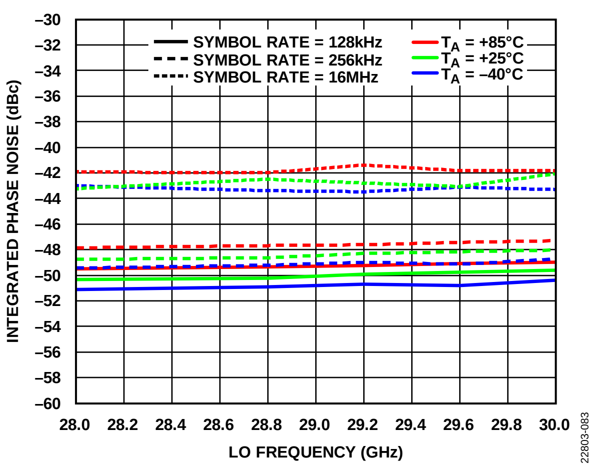


Figure 79. Integrated Phase Noise vs. LO Frequency over Temperature, R_WORD = 2, CP_CURRENT = 4.2 mA, Integrated from 1% to 50% of the Symbol Rate

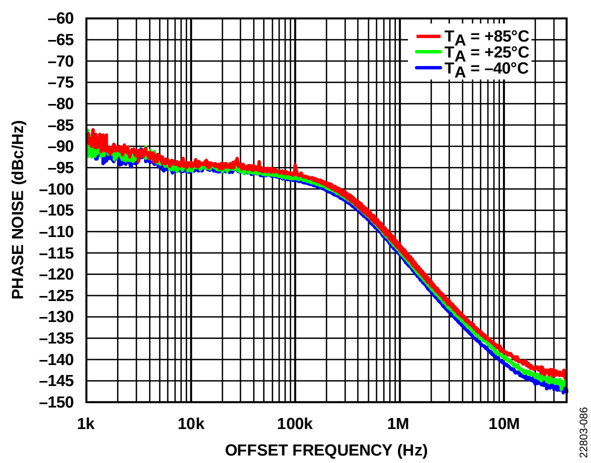


Figure 82. Phase Noise vs. Offset Frequency over Temperature, LO Frequency = 26.8 GHz, R_WORD = 4, CP_CURRENT = 2.1 mA

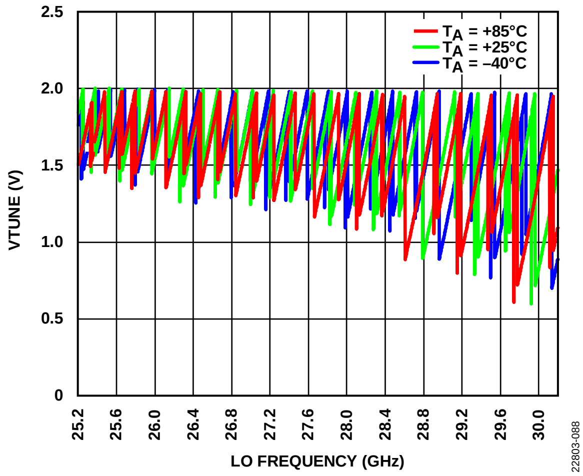


Figure 83. VTUNE vs. LO Frequency over Temperature, VTUNE Temperature Calibration Disabled

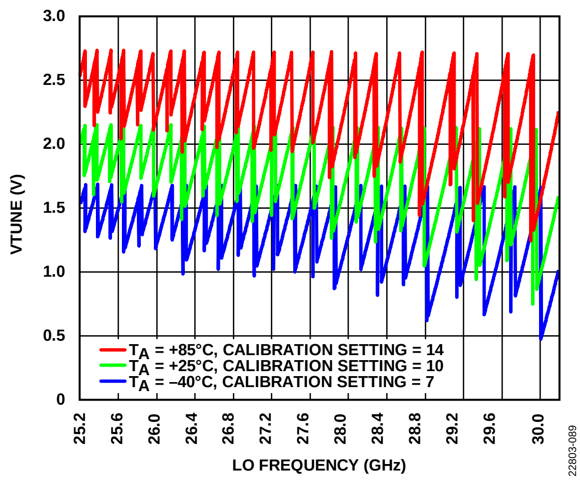


Figure 84. VTUNE vs. LO Frequency over Temperature and Various Calibration Settings, VTUNE Temperature Calibration Enabled

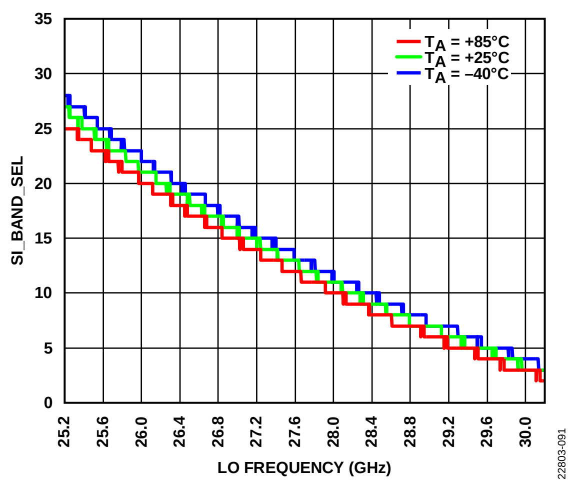


Figure 85. SI_BAND_SEL vs. LO Frequency over Temperature, VTUNE Temperature Calibration Disabled

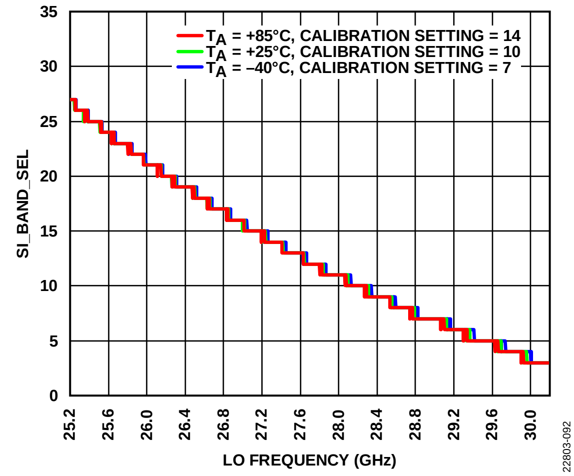


Figure 86. SI_BAND_SEL vs. LO Frequency over Temperature and Various Calibration Settings, VTUNE Temperature Calibration Enabled

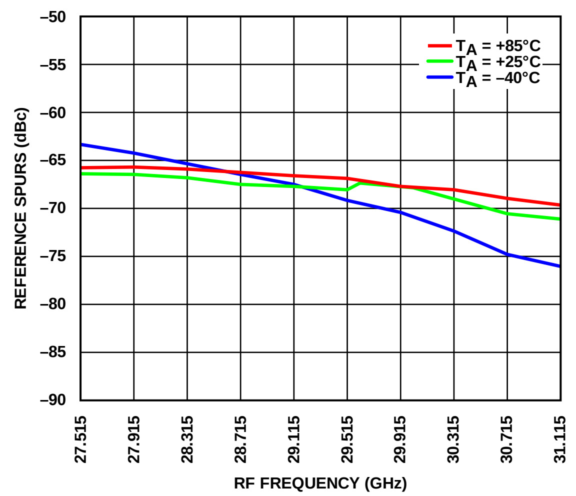


Figure 87. Reference Spurs vs. RF Frequency over Temperature, IF Mode, R_WORD = 4, CP_CURRENT = 2.1 mA, VCTR_IF = 0 V, P_{OUT} = 10 dBm

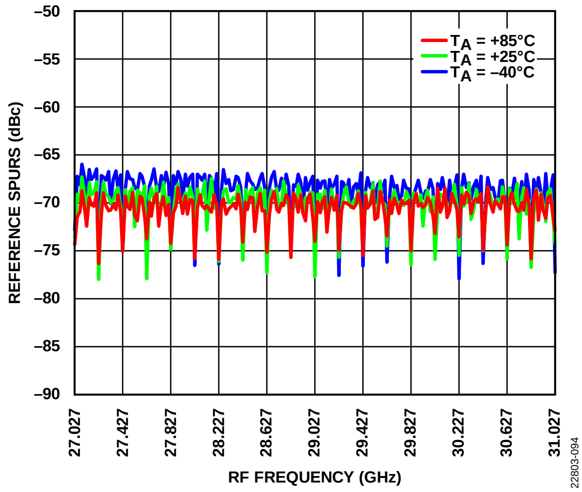


Figure 88. Reference Spurs vs. RF Frequency over Temperature, I/Q Mode, R_WORD = 2, CP_CURRENT = 2.1 mA, P_{OUT} = 10 dBm

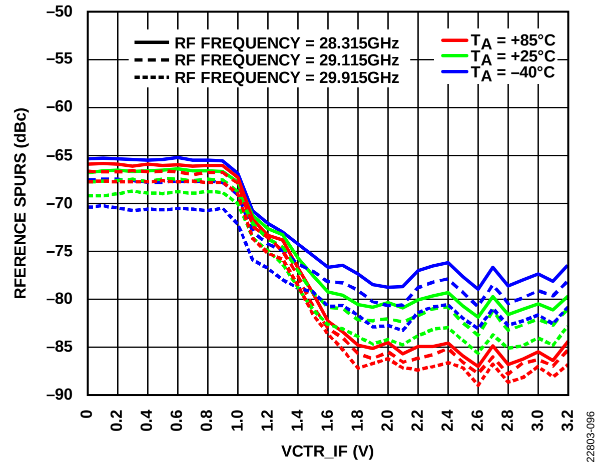


Figure 89. Reference Spurs vs. VCTR_IF over Temperature and Various RF Frequencies, IF Mode, R_WORD = 4, CP_CURRENT = 2.1 mA

UPCONVERTER M × N SPURIOUS PERFORMANCE

Mixer spurious products are measured in dBc from the RF output power level.

For IF mode, spurious frequencies are calculated by

$$|(M \times IF) + (N \times LO)|$$

For I/Q mode, spurious frequencies are calculated by

$$|(M \times I/Q) + (N \times LO)|$$

IF Mode

IF frequency = 2715 MHz, RF frequency = 29 GHz, RF output power = 10 dBm, VCTR_RF = 1.8 V, and VCTR_IF = 0 V. N/A means not applicable.

		N × VCO			
		0	**1**	**2**	**3**
M × IF	**−2**	N/A	−85.4	−79.5	−77.7
	−1	N/A	−84.1	−36.9	−79.0
	0	−74.3	−82.8	−20.1	−83.7
	+1	−83.7	−82.4	0.0	−79.3
	+2	−82.8	−83.6	−64.1	−78.8

I/Q Mode

I/Q frequency = 25 MHz, RF frequency = 29 GHz, RF output power = 10 dBm, and VCTR_RF = 1.8 V. N/A means not applicable.

		N × VCO			
		0	**1**	**2**	**3**
M × I/Q	**−3**	N/A	−100.1	−69.5	−84.9
	−2	N/A	−95.6	−85.8	−96.5
	−1	N/A	−91.8	−27.6	−88.0
	0	N/A	−89.4	−31.3	−80.9
	+1	−76.1	−84.1	0.0	−94.4
	+2	−96.9	−94.6	−51.2	−92.4
	+3	−94.4	−98.3	−64.0	−93.0

THEORY OF OPERATION

The ADMV4530 integrates a fractional-N PLL, VCO, internal 2× multiplier, and I/Q mixer. The fractional-N PLL locks the VCO to a precise reference input signal for low noise operation. The VCO signal is then multiplied by the internal 2× multiplier to generate the necessary LO signal for the I/Q mixer. The I/Q mixer can operate with either differential baseband I/Q inputs or a single-ended IF input. The functionality of the various blocks within the ADMV4530 follows within this section.

SPI CONFIGURATION

The SPI of the ADMV4530 allows configuration of the device for specific functions or operations via the 4-pin SPI port. This interface provides users with added flexibility and customization. The SPI consists of four control lines: SCLK, SDI, SDO, and $\overline{\text{CS}}$. The ADMV4530 protocol consists of a write/read bit followed by 15 register address bits and 8 data bits. The address field and data field are organized MSB first and end with the LSB.

For a write operation, set the MSB to 0, and for a read operation, set the MSB to 1. The write cycle must be sampled on the rising edge of SCLK. The 24 bits of the serial write address and data are shifted in on the SDI control line, MSB to LSB. The ADMV4530 input logic level for the write cycle supports a 3.3 V interface.

For a read cycle, the R/W bit and the 15 bits of address shift in on the rising edge of SCLK on the SDI control line. Then, 8 bits of serial read data shift out on the SDO control line, MSB first, on the falling edge of SCLK. The output logic level for a read cycle is 3.3 V. The output drivers of the SDO are enabled after the last rising edge of SCLK of the instruction cycle and remain active until the end of the read cycle. In a read operation, when $\overline{\text{CS}}$ is deasserted, SDO returns to high impedance until the next read transaction. The $\overline{\text{CS}}$ is active low and must be deasserted at the end of the write or read sequence.

An active low input on $\overline{\text{CS}}$ starts and gates a communication cycle. The $\overline{\text{CS}}$ pin allows more than one device to be used on the same serial communications lines. The SDO pin goes to a high impedance state when the $\overline{\text{CS}}$ input is high. During the communication cycle, the chip select must stay low. The SPI communications protocol follows the Analog Devices, Inc., SPI standard. For more information, see the ADI-SPI Serial Control Interface Standard (Rev 1.0).

REGISTER MAP SECTIONS

The ADMV4530 consists of three register map sections. The first section spans from Register 0x000 through Register 0x00D and follows the standard Analog Devices SPI protocol, which includes protocol setup and device identification registers. The second register map section starts at Register 0x010 through Register 0x07C and contains all of the relevant PLL control registers. The third register map section starts at Register 0x100 through Register 0x119 and contains all of the mixer and baseband control registers. To read back the register values from the first and third sections, the REG_PAGE_SEL bits in Register 0x117 must be set to 1, and to read back from the PLL section, the REG_PAGE_SEL bits in Register 0x117 must be set to 0.

DOUBLE BUFFERED REGISTERS

The PLL inside the ADMV4530 contains several double buffered bit fields that take effect only after a write to the lower portion of the N counter integer value (Register 0x010). This register applies any changes to these double buffered bit fields and initiates the autocalibration routine. The following is a list of the double buffered bit fields and their corresponding registers:

- REF_X2_EN (Register 0x022)
- RDIV2 (Register 0x022)
- R_WORD (Register 0x01F)
- CP_CURRENT (Register 0x01E)
- FRAC2WORD (Register 0x017 and Register 0x018)
- FRAC1WORD (Register 0x014 through Register 0x017)
- MOD2WORD (Register 0x019 and Register 0x01A)
- BIT_INTEGER_WORD (Register 0x010 and Register 0x011)

START-UP INITIALIZATION SEQUENCE

Upon powering up or resetting the ADMV4530, it is recommended to program the register map in reverse order, starting with the highest register number first. The reverse order ensures that the double buffered registers are programmed prior to initiating the autocalibration routine and that all PLL control settings are in their correct state. The recommended values of each register are shown in both the Register Summary section and the Register Details section. The following describes the recommended programming sequence:

1. Program Register 0x000 to a value of 0x18 to enable the SDO pin.
2. Program Register 0x117 to a value of 0x4C to enable reading from the mixer section of the register map.
3. Program Register 0x100 through Register 0x119 in reverse order based upon the desired mixer settings.
4. Program Register 0x117 to a value of 0x0C to enable reading from the PLL section of the register map.
5. Program Register 0x010 through Register 0x07C in reverse order based upon the desired PLL settings.

FREQUENCY UPDATE SEQUENCE

After the initialization sequence is performed, the output frequency can be updated by programming Register 0x010 through Register 0x01A in reverse order.

REFERENCE INPUT

Figure 91 shows the single-ended reference input stage. There is an internal reference multiply by 2 block (×2 doubler) that allows generation of higher f_{PFD}. A higher f_{PFD} is useful for improving overall system phase noise performance. Typically, doubling the f_{PFD} improves the in band phase noise performance by up to 3 dBc/Hz. Use the REF_X2_EN bit (Register 0x022, Bit 5) to enable the reference doubler, which toggles the SW1 switch, shown in Figure 91.

Following the reference doubler block, there are two frequency dividers: a 5-bit R counter (1 to 32 allowed) and a divide by 2 block. These dividers allow the input REF frequency to be divided down to produce lower f_{PFD} that helps minimize fractional-N integer boundary spurs at the output.

Use the R_WORD bits (Bits[4:0]) in Register 0x01F to set the R counter. If the R_WORD = 1, the SW2 switch is in the position shown in Figure 91. Otherwise, the SW2 switch toggles to use the R counter. Additionally, R_WORD = 0 corresponds to a divide by 32 value for the R counter. To enable the reference divide by 2 block, use the RDIV2 bit (Register 0x022, Bit 4) which toggles the SW3 switch, shown in Figure 91.

N COUNTER

The N counter allows a division ratio in the PLL feedback path from the VCO. Note that the VCO signal is multiplied by 2 to achieve the LO frequency at the input of the mixer. The division ratio is determined by using the Integer N (INT), fractional-N (FRAC), and modulus (MOD) values that this counter comprises. The applicable registers for setting the INT, FRAC, and MOD values are Register 0x010 to Register 0x01A.

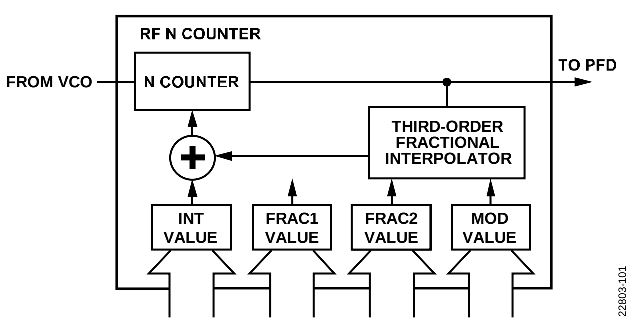


Figure 90. N Counter Functional Block Diagram

INT, FRAC, MOD, AND R COUNTER RELATIONSHIP

The INT, FRAC, and MOD values, in conjunction with the reference path, make it possible to generate VCO frequencies spaced by fractions of the f_{PFD}. To calculate f_{PFD}, use the REF_IN frequency and the reference path configuration parameters as follows:

$$f_{PFD} = REF\_IN\ Frequency \times \frac{1 + D}{R \times (1 + T)}$$

where:
D is the reference doubler bit (0 or 1).
R is the reference divide ratio of the binary, 5-bit programmable counter (1 to 32).
T is the reference divide by 2 bit (0 or 1).

To calculate the VCO frequency (f_{VCO}), use the following equation:

$$f_{VCO} = f_{LO}/2 = f_{PFD} \times N$$

where:
f_{LO} is the frequency of the LO driving the mixer.
N is the desired value of the N counter.

The N counter value is defined by the following:

$$N = INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1}$$

where:
INT is the 16-bit integer value. When using the 4/5 prescaler, INT = 23 to 32,767, and when using the 8/9 prescaler, INT = 75 to 65,535.
FRAC1 is the numerator of the primary modulus (0 to 33,554,431).
FRAC2 is the numerator of the 14-bit auxiliary modulus (0 to 16,383).
MOD2 is a programmable, 14-bit auxiliary fractional modulus (2 to 16,383).
MOD1 is a 25-bit primary modulus with a fixed value of 2^{25} = 33,554,432.

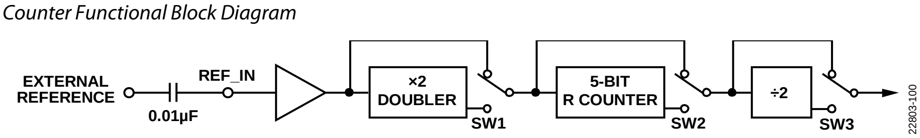


Figure 91. Reference Input Path Block Diagram

These calculations result in a low frequency resolution with no residual frequency error. To apply the previous equation, perform the following steps:

1. Calculate N by dividing f_{VCO}/f_{PFD}. The integer value of this number forms INT.
2. Subtract INT from the full N value.
3. Multiply the remainder by 2^{25}. The integer value of this number forms FRAC1.
4. Calculate MOD2 based on the channel spacing (f_{CHSP}) by using the following equation:

   $$MOD2 = (f_{PFD}/(\text{GCD}(f_{PFD}, f_{CHSP})))$$

   where:
   f_{CHSP} is the desired channel spacing frequency.
   GCD(f_{PFD}, f_{CHSP}) is the greatest common divisor of the PFD frequency and the channel spacing frequency.
5. Calculate FRAC2 by using the following equation:

   $$FRAC2 = ((N - INT) \times 2^{25} - \text{FRAC1}) \times MOD2$$

   The FRAC2 and MOD2 fraction result in outputs with zero frequency error for channel spacing when the following is true:

   $$(f_{PFD}/(\text{GCD}(f_{PFD}, f_{CHSP})) = MOD2 < 16{,}383$$

   If zero frequency error is not required, the MOD1 and MOD2 denominators operate together to create a 39-bit resolution modulus.

INT N MODE

When FRAC1 and FRAC2 are equal to 0, the synthesizer operates in Integer N mode. It is recommended to set the SD_PD bit (Register 0x02B, Bit 0) to 1 to disable the Σ-Δ modulators (SDMs), which improves the in band phase noise and reduces any additional Σ-Δ noise.

PHASE FREQUENCY DETECTOR AND CHARGE PUMP

The phase frequency detector takes inputs from the R counter and N counter to produce an output that is proportional to the phase and frequency differences between these counters. This proportional information is then output to a charge pump circuit that generates current to drive an external loop filter that is then used to appropriately increase or decrease the VTUNE tuning voltage.

Figure 92 shows a simplified schematic of the phase frequency detector and charge pump. Note that the phase frequency detector includes a fixed delay element that is used to ensure that there is no dead zone in the phase frequency detector transfer function for consistent reference spur levels.

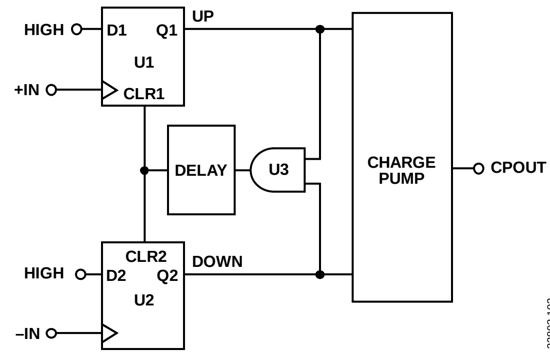


Figure 92. Phase Frequency Detector and Charge Pump Simplified Schematic

LOOP FILTER

Defining a loop filter for a PLL is dependent on several dynamics, such as the f_{PFD}, the N counter value, the K_{VCO}, and the selected charge pump current (I_{CP}). A higher f_{PFD} has the advantage of lowering in band phase noise performance at the expense of integer boundary spur levels when operating in fractional-N mode. Consequently, a lower f_{PFD} can allow the PLL to operate in integer N mode, which can eliminate integer boundary spurs at the expense of higher in band phase noise performance. Given the trade-offs, care must be taken with frequency planning and f_{PFD} selection to ensure the appropriate in band phase noise performance is met with acceptable spur levels for the end application.

The loop filter, as implemented using one of the ADMV4530 evaluation boards (see the Ordering Guide section), is a third-order passive filter, as shown in Figure 93. The filter is designed with the following simulation input parameters: f_{PFD} = 100 MHz, K_{VCO} = 155 MHz/V, f_{VCO} = 15 GHz, and I_{CP} = 4.2 mA. The resulting loop filter bandwidth and phase margin are 540 kHz and 55°, respectively, for the following component values: C1 = 150 pF, C2 = 15 nF, C3 = 20 pF, C4 = do not install (DNI), R1 = 910 Ω, R2 = 910 Ω, and R3 = 0 Ω. For additional guidance with loop filter simulations on the ADMV4530, contact Analog Devices for Technical Support.

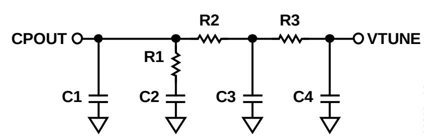


Figure 93. Recommended Loop Filter

CHARGE PUMP CURRENT SETUP

For a specifically designed loop filter, set the I_{CP} by adjusting the CP_CURRENT value in Bits[7:4], Register 0x01E. Calculate I_{CP} by using the following the equation:

$$I_{CP} = (CP\_CURRENT + 1) \times 350\ \mu A$$

where *CP_CURRENT* is an integer value (0 to 15).

The default value for a 100 MHz f_{PFD} for CP_CURRENT = 11, which yields a current of 4.2 mA. The applicable range is 0.35 mA to 5.6 mA, with 0.35 mA steps.

To change the f_{PFD}, if no change has been made to the existing loop filter components, it is recommended to scale I_{CP} by using the following equation:

$$I_{CP\,(NEW)} = \frac{I_{CP\,(DEFAULT)} \times f_{PFD\,(DEFAULT)}}{f_{PFD\,(NEW)}}$$

where:

$I_{CP\,(NEW)}$ is the new desired I_{CP}.
$I_{CP\,(DEFAULT)}$ is the default I_{CP}.
$f_{PFD\,(DEFAULT)}$ is the default f_{PFD}.
$f_{PFD\,(NEW)}$ is the new desired f_{PFD}.

When $I_{CP\,(NEW)}$ is obtained, the CP_CURRENT value in Bits[7:4], Register 0x01E, can be updated by using the following rounding function:

$$CP\_CURRENT = \text{ROUND}\left(\frac{I_{CP\,(NEW)}}{350\ \mu A}\right) - 1$$

where *ROUND* is the mathematical round function.

BLEED CURRENT (CP_BLEED) SETUP

The charge pump includes a binary scaled bleed current (I_{BLEED}) that is set by using the CP_BLEED value in Register 0x026. The bleed current introduces a slight phase offset in the phase frequency detector to improve integer boundary spurs and phase noise when operating in fractional-N mode. To enable the bleed current for fractional-N mode, set CP_BLEED_EN = 1 (Register 0x027, Bit 3). For integer mode, CP_BLEED_EN must be set to 0.

Generally, the optimum bleed current value is 115 (431.25 µA), and this value provides optimal performance for most applications. However, there can be additional performance improvements by empirically determining the appropriate bleed current value from the actual measurements for the intended application. The applicable range is 0 µA to 956.25 µA with 3.75 µA steps.

$$I_{BLEED} = CP\_BLEED \times 3.75\ \mu A$$

where *CP_BLEED* is an integer value (0 to 255).

Figure 94 shows an example of 100 kHz offset phase noise vs. CP_BLEED.

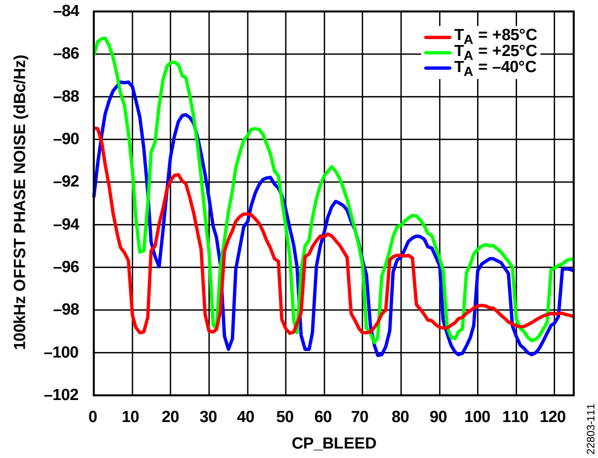


Figure 94. 100 kHz Offset Phase Noise vs. CP_BLEED, LO Frequency = 29.995 GHz, CP_CURRENT = 4.2 mA

Figure 95 is an example of 100 kHz offset phase noise vs. LO frequency with a CP_BLEED value of 115 (431.25 µA). The CP_CURRENT was 4.2 mA and the LO frequency step size was 10 MHz. At each integer boundary, the CP_BLEED was disabled, resulting in approximately −1 dBc/Hz improvement.

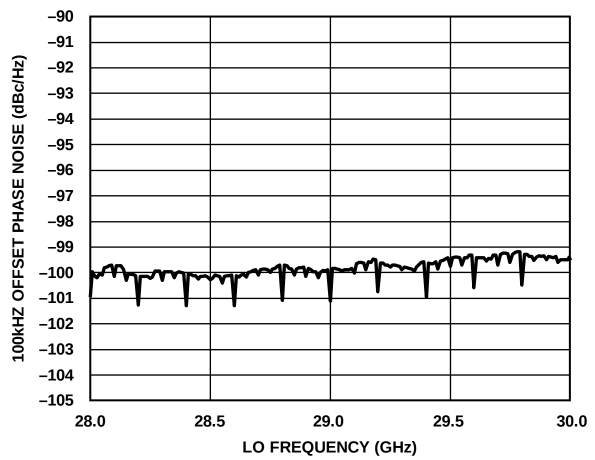


Figure 95. 100 kHz Offset Phase Noise vs. LO Frequency, CP_BLEED = 115, CP_CURRENT = 4.2 mA

MUXOUT

The output multiplexer on the ADMV4530 allows the user to access various internal signals on the chip. The MUXOUT bit field (Register 0x020, Bits[7:4]) shown in Table 30 lists the available signals. When MUXOUT_SEL (Register 0x20, Bit 3) is set to 1, the MUXOUT signal is present on the SDO output pin. Otherwise, the SDO pin is configured for SPI data output.

DIGITAL LOCK DETECT

A digital lock detect function is available on the SDO pin when both the MUXOUT and MUXOUT_SEL bits are set to 1. The digital lock detect function is also available by reading the LD_READBACK bit (Register 0x07C, Bit 0). A logic high indicates that the digital lock detect has declared the PLL is locked.

The digital lock detect function has some adjustable settings in Register 0x027 and Register 0x028. The LD_BIAS and LDP bits adjust an internal precision window and the LD_COUNT bits adjust the consecutive cycle count to declare PLL lock. It is recommended to keep the settings listed in the register map. For special applications, contact Analog Devices Technical Support for guidance on adjusting these settings.

VCO AUTOCALIBRATION

The internal VCO uses an internal autocalibration routine that optimizes the VCO settings for a particular frequency and allows the PLL to lock in approximately 100 μs after the lower portion of the N counter integer value (Register 0x010) is programmed. For nominal applications, maintain the autocalibration default values in the register map (Register 0x030 to Register 0x034).

For applications where it is desirable to bypass the autocalibration routine, there are two necessary procedures. First, generate a lookup table of the resultant VCO calibration data (core and band parameters) for each desired VCO frequency. Second, bypass the autocalibration routine and manually write the lookup table values. Generate a new table for every chip because each chip is unique.

VCO CALIBRATION DATA READ BACK

To read back the VCO calibration data, load the required registers, let the device lock using autocalibration, and read the VCO parameters for each frequency. It is important to ensure that autocalibration has completed before readback. Reading back values before autocalibration has completed results in incorrect values being read.

The bits used for read back include the following:

- Register 0x033, Bits[7:5], VCO_FSM_READBACK
- Register 0x06E, Bits[4:0], VCO_DATA_READBACK
- Register 0x06F, Bit 0, VCO_DATA_READBACK

The VCO_FSM_READBACK bits set what data is sent to the VCO_DATA_READBACK bits.

To read the VCO parameters, take the following steps:

1. Program the device to lock at the desired frequency by using the autocalibration feature. Users must wait for the device to lock.
2. Set VCO_FSM_READBACK = 1 to allow readback of the VCO band and the core.
3. Read Register 0x06F, Bit 0 to read back the current VCO core. The ADMV4530 has only one VCO core. Therefore, this value must always be 1.
4. Read Register 0x06E, Bits[4:0] to read back the VCO band.

Repeat Step 1 through Step 4 for each required frequency to build a lookup table of values.

VCO CALIBRATION DATA MANUAL WRITING

The VCO parameters for each required frequency force the device to the target frequency core and band without the use of autocalibration.

The bits used for writing to the VCO parameters include the following:

- Register 0x034, Bits[7:5], VCO_FSM_TEST_MODES
- Register 0x037, Bits[7:0], SI_BAND_SEL
- Register 0x038, Bits[7:4], SI_VCO_SEL

To write the VCO parameters, take the following steps:

1. At power-up, set up the serial port interface and initialize the device as necessary for normal operation.
2. Set AUTOCAL_EN = 0 (Register 0x012, Bit 6) to disable autocalibration.
3. Set VCO_FSM_TEST_MODES = 010 to overwrite the VCO core and band.
4. Program the registers, except Register 0x010, as required for the target frequency. This step is frequency dependent.
5. Set SI_VCO_SEL = 1. Even though the ADMV4530 has only one VCO core, it is still necessary to program this bit because this bit tells the internal finite state machine to enable the VCO.
6. Set SI_BAND_SEL to the desired band from the previously generated lookup table.
7. Write to Register 0x010. When this register is written to, the device locks to the new frequency.

Repeat Step 4 through Step 7 as required for setting the appropriate VCO frequency.

AUTOCALIBRATION LOCK TIME

The PLL lock time divides into a number of settings. The total lock time for changing frequencies is the sum of three separate times: synthesizer lock, VCO band selection, and PLL settling.

SYNTHESIZER LOCK TIMEOUT

The synthesizer lock timeout ensures that the VCO calibration digital-to-analog converter (DAC), which forces the VCO tune voltage (V_{VTUNE}), has settled to a steady value for the band select circuitry. The SYNTH_LOCK_TIMEOUT and the TIMEOUT bits select the length of time the DAC is allowed to settle to the final voltage before the VCO calibration process continues to the next phase (VCO band selection). The PFD frequency is the clock for this logic, and the duration is set by using the following equation:

$$(SYNTH\_LOCK\_TIMEOUT \times 1024 + TIMEOUT)/f_{PFD}$$

where:
SYNTH_LOCK_TIMEOUT is programmed in Bits[4:0], Register 0x033.
TIMEOUT is programmed in Bits[7:0], Register 0x031 and Bits[1:0], Register 0x032.

The calculated time must be greater than or equal to 20 µs.

For the SYNTH_LOCK_TIMEOUT bits, the minimum value is 2, and the maximum value is 31.

For TIMEOUT, the minimum value is 2, and the maximum value is 1023.

VCO BAND SELECTION TIME

Use the VCO_BAND_DIV bits (Bits[7:0], Register 0x030) and the f_{PFD} to generate the VCO band selection clock (f_{BSC}) as follows:

$$f_{BSC} = (f_{PFD}/VCO\_BAND\_DIV)$$

The calculated frequency must be less than 4 MHz.

Note that 16 clock cycles are required for one VCO core and band calibration step and the total band selection process takes 11 steps, resulting in the following equation:

$$11 \times (16 \times VCO\_BAND\_DIV/f_{PFD})$$

The minimum value for VCO_BAND_DIV is 1, and the maximum value is 255.

PLL SETTLING TIME

The time taken for the loop to settle is inversely proportional to the low-pass filter bandwidth.

CHIP TEMPERATURE READ BACK

Chip temperature readback can provide information regarding system temperature, which is useful for system compensation.

The ADMV4530 includes an analog-to-digital converter (ADC) that enables reading the chip temperature. The ADC clock (ADC_CLK) is generated from the phase frequency detector clock (f_{PFD}) with the following equations:

$$ADC\_CLK = \frac{f_{PFD}}{((ADC\_CLK\_DIV \times 4) + 2)}$$

where *ADC_CLK_DIV* is stored in Register 0x035.

A valid reference signal is required to complete a conversion. Target 100 kHz for ADC_CLK and calculate ADC_CLK_DIV with the following equation:

$$ADC\_CLK\_DIV = ceiling\left(\frac{\left(\left(\frac{f_{PFD}}{100{,}000}\right) - 2\right)}{4}\right)$$

If ADC_CLK_DIV is greater than 255, set these bits to 255.

The bits used for temperature readback are the following:

- Register 0x032, Bit 2, ADC_ENABLE
- Register 0x032, Bit 3, ADC_CONVERSION
- Register 0x033, Bits[7:5], VCO_FSM_READBACK
- Register 0x06E, Bits[7:0], VCO_DATA_READBACK[7:0]
- Register 0x073, Bit 2, ADC_CLK_DISABLE

To read back the temperature, take the following steps:

1. Set ADC_ENABLE = 1 to enable the ADC.
2. Set ADC_CONVERSION = 1 to perform an ADC conversion.
3. Wait 16 ADC_CLK cycles.
4. Set VCO_FSM_READBACK = 101 (skip this step if it is already set).
5. Read the VCO_DATA_READBACK bits in Register 0x06E to read back the raw ADC output that corresponds to the chip temperature (RAW_TEMP).
6. Set ADC_CONVERSION = 0 to disable the conversion.
7. Set ADC_ENABLE = 0 to disable the ADC, which prevents any spurs generated by the ADC clock. Similarly, the ADC_CLK_DISABLE bit can disable the ADC clock.

Perform Step 1 and Step 2 separately. However, Step 6 and Step 7 can be completed together.

To calculate the approximate chip temperature in Celsius (°C), use the following equation:

$$Chip\ Temperature = -100°C + RAW\_TEMP$$

RF OUTPUT DRIVER

As shown in the functional block diagram (see Figure 1), the ADMV4530 incorporates two driver stages along with a voltage variable attenuator (VVA) in the RF output section of the chip. The VCTR_RF pin (Pin 4) is connected to the VVA, which adjusts the RF output gain. The voltage range for the VCTR_RF pin is 0 V to 1.8 V, with a positively sloping linear region between 0.6 V to 1.5 V, as shown in Figure 7. The typical slope within linear region is 32 dB/V.

I/Q MODE MIXER SETUP

In baseband quadrature modulation mode, the input impedance of the baseband pins (IN, IP, QN, and QP) are 100 Ω differential. These inputs can be driven with a dc-coupled 100 Ω differential source. IN and IP are the differential baseband I inputs, and QN and QP are the differential baseband Q inputs. These inputs can operate from a common-mode voltage range of 0 V to 2.5 V. When operating in I/Q mode, program the following registers:

- Register 0x100 = 0x3A
- Register 0x101 = 0x78
- Register 0x102 = 0x11
- Register 0x103 = 0x5D (for 0.5 V V_{CM})
- Register 0x106 to 0x109 = 0x7F
- Register 0x115 = 0x88

When V_{CM} changes, program Register 0x103 by using the following formulas for each mode.

In I/Q mode, for V_{CM} = 0.0 V to 1.5 V, set

$$MIXER\_VCM = \mathrm{ROUND}(23.8 \times V_{CM} + 80.7).$$

In I/Q mode, for V_{CM} = 1.5 V to 2.5 V, set

$$MIXER\_VCM = \mathrm{ROUND}(23.8 \times V_{CM} + 1.3).$$

The I/Q mode default for V_{CM} = 0.5 V is MIXER_VCM = 93 = 0x5D.

I/Q MODE LO NULLING

To perform LO nulling in I/Q mode, apply a differential dc offset on the I and Q inputs. Note that LO nulling is a two-step process. When LO nulling is done on the I side, keep the Q side at V_{CM}, and when LO nulling is done on the Q side, the I side must be kept at V_{CM} or at the determined value in the first step. The optimal LO null is when settings from the I side and the Q side are combined. It is important to keep V_{CM} constant. Therefore, when a dc offset is applied on the negative input (V_{CMN}), the same offset must be applied on the positive input (V_{CMP}) in the opposite direction (V_{CMP} ± dc offset and V_{CMN} ∓ dc offset) to allow the average V_{CM} to hold constant to coincide with the value programmed in Register 0x103. LO nulling at a single point is optimal at that particular frequency and temperature, and the absolute level (dBm) of the LO to RF feedthrough remains the same across gain settings using the VCTR_RF input.

For example, it is possible to null LO down to −50 dBm with VCTR_RF = 1.8 V, depending on the resolution of the dc offset applied and the temperature (as shown in Figure 27 and Figure 28), where LO nulling = 29 GHz. When LO nulling = 29 GHz, the LO to RF feedthrough is <−20 dBm over temperature, and the frequency range is from 28 GHz to 30 GHz.

I/Q MODE SIDEBAND REJECTION NULLING

In I/Q mode, use Register 0x104 or Register 0x105 to perform sideband rejection nulling. Each register has 128 settings, Bits[6:0]. Single frequency nulling allows sideband rejection to null down to −45 dBc for a particular frequency. The sideband rejection degrades to −35 dBc if the frequency or temperature changes (shown in Figure 26 and Figure 29).

IF GAIN CONTROL

As shown in the functional block diagram (see Figure 1), the ADMV4530 incorporates an IF amplifier with analog gain control. The analog voltage for this IF amplifier can either be provided by the internal AGC loop or by applying an external VCTR_IF voltage to the EXT_CAP_N (Pin 10). The voltage range for the IF amplifier gain control is 0 V to 3.3 V, with a negatively sloping linear region between 0.9 V and 2.2 V, as shown in Figure 37. The typical slope within linear region is −32 dB/V.

IF MODE MIXER SETUP

The ADMV4530 features the ability to upconvert a real IF input anywhere from 2 GHz to 3 GHz. When operating in IF mode program the following registers:

- Register 0x100 = 0x03
- Register 0x101 = 0x7D
- Register 0x102 = 0x3F
- Register 0x103 = 0x5B (this register sets V_{CM} in IF mode)
- Register 0x104 to 0x109 = 0x5F
- Register 0x115 = 0x08

When V_{CM} changes, program Register 0x103 by using the following formula:

$$MIXER\_VCM = \mathrm{ROUND}(0.3 \times (128 - TARGET\_MIXER\_DC\_OFFSET) + 80.7)$$

where *TARGET_MIXER_DC_OFFSET* is the value programmed into Register 0x106 to Register 0x109.

IF MODE LO NULLING

LO nulling is performed in IF mode in a similar fashion as in I/Q mode. However, dc offset is applied through Register 0x106 to Register 0x109. Use Register 0x106 and Register 0x107 to force a dc offset on the I side, and use Register 0x108 and Register 0x109 to force a dc offset on the Q side. It is important to sweep the I and Q registers simultaneously in opposite direction so that the following are true:

(*MIXER_DC_OFFSET_IP* + *MIXER_DC_OFFSET_IN*)/2 = *TARGET_MIXER_DC_OFFSET*

(*MIXER_DC_OFFSET_QP* + *MIXER_DC_OFFSET_QN*)/2 = *TARGET_MIXER_DC_OFFSET*

As in I/Q mode, LO nulling is two-step process. When LO nulling on the I side, keep the Q side at the TARGET_MIXER_DC_OFFSET. When LO nulling on the Q side, keep the I side at the TARGET_MIXER_DC_OFFSET, or at the determined value from the first step. The optimal null is achieved when both settings are combined. The recommended TARGET_MIXER_DC_OFFSET value is 95 decimal (0x5F). It is recommended to keep the TARGET_MIXER_DC_OFFSET above 63. The MIXER_DC_OFFSET range for Register 0x106 to Register 0x109 is from 63 decimal to 127 decimal. The LO to RF feedthrough improves to approximately −30 dB following this procedure. When the LO is nulled at a single frequency and temperature, the LO to RF feedthrough is less than −40 dBc, and the LO to RF feedthrough is less than −25 dBc across frequency and temperature, as shown in Figure 56.

IF MODE SIDEBAND REJECTION NULLING

In IF mode, use Register 0x104 or Register 0x105 to perform sideband rejection nulling. Each register has 128 settings, Bits[6:0]. Single frequency nulling allows sideband rejection to null down to −50 dBc for a particular frequency. If the operating frequency or temperature changes, sideband rejection nulling degrades. When sideband rejection is nulled at 29 GHz, it is less than −30 dBc over temperature and the frequency range is from 28 GHz to 30 GHz (as shown in Figure 55).

APPLICATIONS INFORMATION

IF AGC CONFIGURATION

The ADMV4530 includes an AGC circuit on the IF input port. The four bit fields that control the functionality of this AGC follow:

1. AGC_EN (Register 0x101)
2. AGC_EN_OVERRIDE (Register 0x102)
3. DET_RANGE (Register 0x10C)
4. AGC_VREF_GEN (Register 0x10D)

The AGC_EN bit enables or disables the AGC that is only truly enabled when in power-down mode. The AGC_EN_OVERRIDE bit enables the AGC regardless of the power-down mode.

The DET_RANGE bit field selects the appropriate range for the internal power detector, and the AGC_VREF_GEN bit field determines the voltage reference set point for the AGC.

Figure 96 shows an example of the output power vs. the input power level for various settings of DET_RANGE and AGC_VREF_GEN. The first number in the Figure 96 legend is the DET_RANGE setting (decimal value), and the second number in the Figure 96 legend is the AGC_VREF_GEN setting (decimal value).

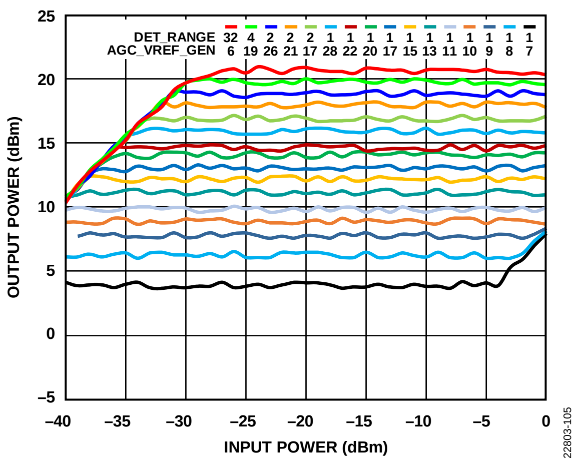


Figure 96. Power Sweep for Various AGC Settings

Figure 97 shows the output power given a −20 dBm input IF signal and sweeping the AGC voltage reference set point for various DET_RANGE settings.

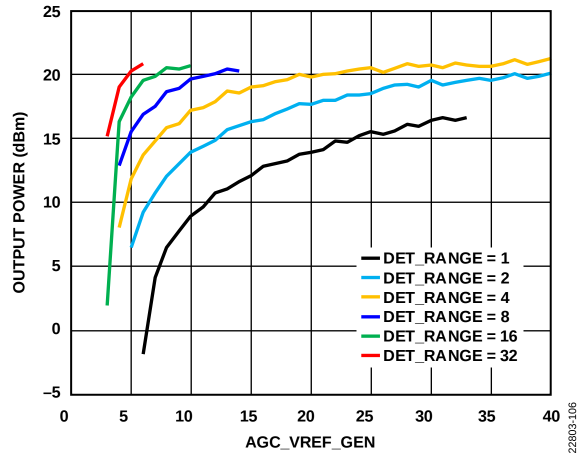


Figure 97. AGC Voltage Reference Sweep

When AGC is enabled, the AGC voltage needed for the IF gain control is accessible on the EXT_CAP_N pin (Pin 10). When the AGC is disabled, this pin functions as an input for the IF amplifier gain control.

ERROR VECTOR MAGNITUDE PERFORMANCE

The error vector magnitude performance of the ADMV4530 is measured at an RF frequency of 29.98 GHz (fractional mode, phase noise adjusted as shown in Figure 94) and an RF frequency of 30 GHz (integer mode) with a single 12 MHz, 8 quadrature phase shifting keying (QPSK) carrier in I/Q mode, 0 Hz offset, 0.2 roll-off factor, and LO and sideband rejection nulled. The measurement was performed at T_A = 25°C.

Figure 98 shows the transmitter error vector magnitude vs. the output power. The transmitter has an approximately 3% error vector magnitude with an output power of 12 dBm.

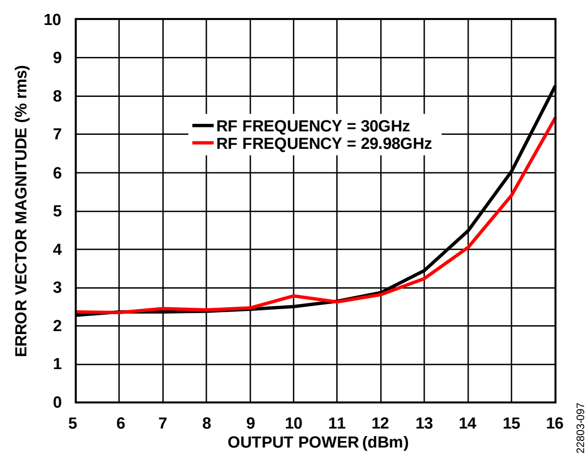


Figure 98. Error Vector Magnitude vs. Output Power, 8 QPSK Modulation, 12 MHz Bandwidth

PLL LOCK TIME IN IF AND I/Q MODE

Using the recommended autocalibration setup described in the VCO Autocalibration section, the typical autocalibration lock time is shown in Figure 99. These results reflect a VCO band selection clock (f_{BSC}) = 4 MHz.

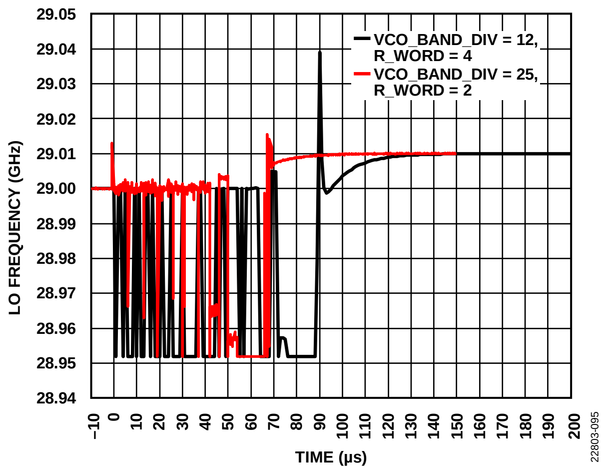


Figure 99. LO Frequency vs. Time, REF_IN Frequency = 200 MHz, f_{BSC} = 4 MHz

POWER UP AND DOWN

The ADMV4530 includes a power-down (PD) pin that when enabled turns off the mixer and output driver section of the chip but keeps the PLL and VCO active. For applications where a fast power-up time is required, this standby mode is useful for muting the RF output signal while keeping the PLL locked. Figure 100 shows the typical response time of the PD pin.

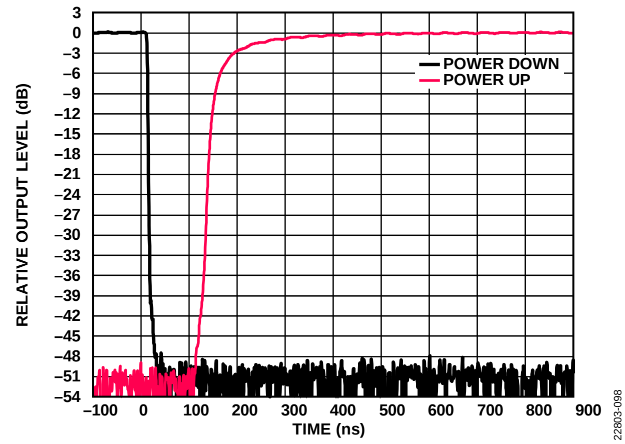


Figure 100. Relative Output Level vs. Time, Power-Up and Power-Down

The chip can be set to its lowest power state by disabling the bias for the PLL, VCO, and RF sections. To accomplish setting the chip to its lowest power state, enable the following bits:

- PLL_PD, Register 0x01E, Bit 2
- VCO_PD, Register 0x027, Bit 2
- RF_BIAS_PD, Register 0x100, Bit 7

When exiting the lowest power state and bringing the device back to nominal operating conditions, the PLL must be relocked by updating Register 0x010. Table 7 details the typical power consumption for nominal, standby, and low power conditions.

Table 7. Typical Power Consumption at T_A = 25°C

State	Power (W)	Test Conditions/Comments
Nominal		Maximum gain
I/Q Mode	1.8	
IF Mode	2.5	
Standby		PD pin high
I/Q Mode	0.7	
IF Mode	1.4	
Low Power	0.2	PD pin high, PLL, VCO, and RF disabled

REGISTER SUMMARY

N/A means not applicable, R means read, and R/W means read/write.

Table 8. Register Summary

Reg (Hex)	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Recommended	R/W
000	REG0000	[7:0]	SOFT_RESET_R	LSB_FIRST_R	ADDR_ ASCN_R	SDO_ ACTIVE_R	SDO_ACTIVE	ADDR_ASCN	LSB_FIRST	SOFT_RESET	0x00	0x18	R/W
001	REG0001	[7:0]	SINGLE_ INSTRUCTION	CSB_STALL	MASTER_ SLAVE_RB	RESERVED					0x00	0x00	R/W
003	REG0003	[7:0]	RESERVED				CHIP_TYPE				0x01	N/A	R
004	REG0004	[7:0]	PRODUCT_ID[7:0]								0x21	N/A	R
005	REG0005	[7:0]	PRODUCT_ID[15:8]								0x00	N/A	R
00A	REG000A	[7:0]	SCRATCH_PAD								0x00	User defined	R/W
00B	REG000B	[7:0]	SPI_REV								0x01	N/A	R
00C	REG000C	[7:0]	VENDOR_ID[7:0]								0x56	N/A	R
00D	REG000D	[7:0]	VENDOR_ID[15:8]								0x04	N/A	R
010	REG0010	[7:0]	BIT_INTEGER_WORD[7:0]								0x80	User defined	R/W
011	REG0011	[7:0]	BIT_INTEGER_WORD[15:8]								0x00	User defined	R/W
012	REG0012	[7:0]	RESERVED	AUTOCAL_EN	PRE_SEL	RESERVED					0x00	8/9: 0x60	R/W
014	REG0014	[7:0]	FRAC1WORD[7:0]								0x00	User defined	R/W
015	REG0015	[7:0]	FRAC1WORD[15:8]								0x00	User defined	R/W
016	REG0016	[7:0]	FRAC1WORD[23:16]								0x00	User defined	R/W
017	REG0017	[7:0]	FRAC2WORD[6:0]							FRAC1WORD[24]	0x00	User defined	R/W
018	REG0018	[7:0]	RESERVED	FRAC2WORD[13:7]							0x00	User defined	R/W
019	REG0019	[7:0]	MOD2WORD[7:0]								0x00	User defined	R/W
01A	REG001A	[7:0]	RESERVED		MOD2WORD[13:8]						0x00	User defined	R/W
01E	REG001E	[7:0]	CP_CURRENT				PD_POL	PLL_PD	RESERVED	CNTR_RESET	0x00	2.1 mA: 0x58, 4.2 mA: 0xB8	R/W
01F	REG001F	[7:0]	RESERVED			R_WORD					0x00	≥0x01	R/W
020	REG0020	[7:0]	MUXOUT				MUXOUT_SEL	MUXOUT_ LEV_SEL	RESERVED		0x00	Data: 0x14, mux: 0x1C	R/W
022	REG0022	[7:0]	RESERVED		REF_X2_EN	RDIV2	RESERVED				0x00	User defined	R/W
025	REG0025	[7:0]	RESERVED						VCO_POUT_SEL		0x00	0x03	R/W
026	REG0026	[7:0]	CP_BLEED								0x00	0x73	R/W
027	REG0027	[7:0]	LD_BIAS		LDP	CP_BLEED_ GATE	CP_BLEED_EN	VCO_PD	RESERVED		0x00	FRAC: 0xC9, INT: 0xE1	R/W
028	REG0028	[7:0]	RESERVED					LD_COUNT		LOL_EN	0x00	0x03	R/W
02A	REG002A	[7:0]	RESERVED		CP_BLEED_ POL	RESERVED	CSB_SYNC	RESERVED			0x00	0x00	R/W
02B	REG002B	[7:0]	RESERVED		LSB_P1	VAR_MOD_EN	RESERVED	SD_MASK_ RESET_EN	RESERVED	SD_PD	0x00	FRAC: 0x10, INT: 0x01	R/W
02C	REG002C	[7:0]	RESERVED							DISABLE_ALC	0x00	0x01	R/W
030	REG0030	[7:0]	VCO_BAND_DIV								0x00	User defined	R/W
031	REG0031	[7:0]	TIMEOUT[7:0]								0x00	User defined	R/W
032	REG0032	[7:0]	ADC_MUX_SEL	RESERVED	ADC_ FAST_CONV	ADC_ CTS_CONV	ADC_ CONVERSION	ADC_ENABLE	TIMEOUT[9:8]		0x00	User defined	R/W
033	REG0033	[7:0]	VCO_FSM_READBACK			SYNTH_LOCK_TIMEOUT					0x00	User defined	R/W
034	REG0034	[7:0]	VCO_FSM_TEST_MODES			VCO_ALC_TIMEOUT					0x00	0x80	R/W
035	REG0035	[7:0]	ADC_CLK_DIVIDER								0x00	0xFF	R/W
036	REG0036	[7:0]	ICP_ADJUST_OFFSET								0x00	0x30	R/W
037	REG0037	[7:0]	SI_BAND_SEL								0x00	0x00	R/W
038	REG0038	[7:0]	SI_VCO_SEL				RESERVED				0x00	0x00	R/W
039	REG0039	[7:0]	RESERVED	VCO_FSM_TEST_MUX_SEL			SI_VTUNE_CAL_SET				0x00	0x07	R/W
03A	REG003A	[7:0]	ADC_OFFSET								0x00	0x55	R/W
03E	REG003E	[7:0]	RESERVED				CP_TMODE		RESERVED		0x00	0x0C	R/W
06E	REG006E	[7:0]	VCO_DATA_READBACK[7:0]								0x00	N/A	R
06F	REG006F	[7:0]	VCO_DATA_READBACK[15:8]								0x00	N/A	R
073	REG0073	[7:0]	RESERVED					ADC_CLK_ DISABLE	NDIV_PD	LD_COUNT_SEL	0x00	0x00	R/W
07C	REG007C	[7:0]	RESERVED							LD_READBACK	0x00	N/A	R

Reg (Hex)	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Recommended	R/W
100	REG0100	[7:0]	RF_BIAS_PD	RESERVED	IFAMP_PD			RESERVED_0	MIXER_ SW_CFG	IF_SW_EN	0x03	I/Q mode: 0x3A, IF mode: 0x03	R/W
101	REG0101	[7:0]	RESERVED				MIXER_EN	IF_DET_EN	RESERVED	AGC_EN	0x7F	I/Q mode: 0x78, IF mode: 0x7D	R/W
102	REG0102	[7:0]	IF_DET_EN_ OVERRIDE	AGC_EN_ OVERRIDE	IF_VVA_CFG	RESERVED	IFAMP_EN			RESERVED	0x3F	I/Q mode: 0x11, IF mode: 0x3F	R/W
103	REG0103	[7:0]	RESERVED	MIXER_VCM							0x51	I/Q mode: 0x5D, IF mode: 0x5B	R/W
104	REG0104	[7:0]	RESERVED	PHASE_ADJ_I							0x5F	0x5F	R/W
105	REG0105	[7:0]	RESERVED	PHASE_ADJ_Q							0x5F	0x5F	R/W
106	REG0106	[7:0]	RESERVED	MIXER_DC_OFFSET_IP							0x7F	I/Q mode: 0x7F, IF mode: 0x5F	R/W
107	REG0107	[7:0]	RESERVED	MIXER_DC_OFFSET_IN							0x7F	I/Q mode: 0x7F, IF mode: 0x5F	R/W
108	REG0108	[7:0]	RESERVED	MIXER_DC_OFFSET_QP							0x7F	I/Q mode: 0x7F, IF mode: 0x5F	R/W
109	REG0109	[7:0]	RESERVED	MIXER_DC_OFFSET_QN							0x7F	I/Q mode: 0x7F, IF mode: 0x5F	R/W
10C	REG010C	[7:0]	RESERVED	DET_RANGE							0x08	User defined	R/W
10D	REG010D	[7:0]	RESERVED	AGC_VREF_GEN							0x69	User defined	R/W
115	REG0115	[7:0]	IF_TERM	RESERVED							0x08	I/Q mode: 0x88, IF mode: 0x08	R/W
116	REG0116	[7:0]	RESERVED				IF_FILTER				0x00	0x00	R/W
117	REG0117	[7:0]	REG_PAGE_SEL		RESERVED						0x4C	PLL: 0x0C, mixer: 0x4C	R/W
119	REG0119	[7:0]	RESERVED		START_ POLY_CAL	CAL_ POLY_EN	RESERVED				0x08	0x08	R/W

REGISTER DETAILS

Address: 0x000, Reset: 0x00, Name: REG0000

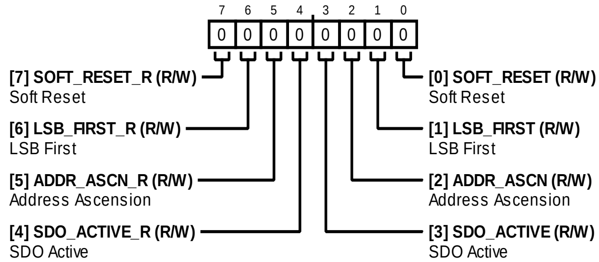


Table 9. Bit Descriptions for REG0000

Bits	Bit Name	Description	Reset	Recommended	Access
7	SOFT_RESET_R	Soft Reset 0: reset not asserted 1: reset asserted	0x0	0x0	R/W
6	LSB_FIRST_R	LSB First 0: MSB first 1: LSB first	0x0	0x0	R/W
5	ADDR_ASCN_R	Address Ascension 0: disable 1: enable	0x0	0x0	R/W
4	SDO_ACTIVE_R	SDO Active 0: disable (3-wire SPI) 1: enable (4-wire SPI)	0x0	0x1	R/W
3	SDO_ACTIVE	SDO Active 0: disable (3-wire SPI) 1: enable (4-wire SPI)	0x0	0x1	R/W
2	ADDR_ASCN	Address Ascension 0: disable 1: enable	0x0	0x0	R/W
1	LSB_FIRST	LSB First 0: MSB first 1: LSB first	0x0	0x0	R/W
0	SOFT_RESET	Soft Reset 0: reset not asserted 1: reset asserted	0x0	0x0	R/W

Address: 0x001, Reset: 0x00, Name: REG0001

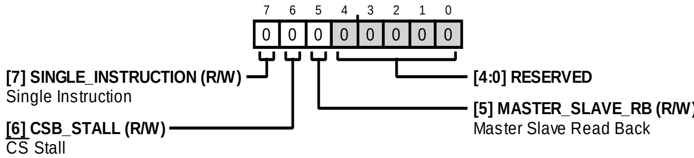


Table 10. Bit Descriptions for REG0001

Bits	Bit Name	Description	Reset	Recommended	Access
7	SINGLE_INSTRUCTION	Single Instruction 0: enable streaming 1: disable streaming (regardless of CS)	0x0	0x0	R/W
6	CSB_STALL	CS Stall	0x0	0x0	R/W
5	MASTER_SLAVE_RB	Master Slave Read Back	0x0	0x0	R/W
[4:0]	RESERVED	Reserved	0x0	0x0	R/W

Address: 0x003, Reset: 0x01, Name: REG0003

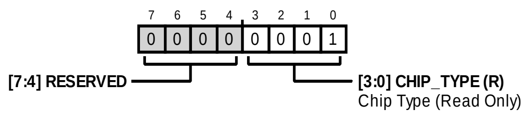


Table 11. Bit Descriptions for REG0003

Bits	Bit Name	Description	Reset	Recommended	Access
[7:4]	RESERVED	Reserved	0x0	N/A	R
[3:0]	CHIP_TYPE	Chip Type (Read Only)	0x1	N/A	R

Address: 0x004, Reset: 0x21, Name: REG0004

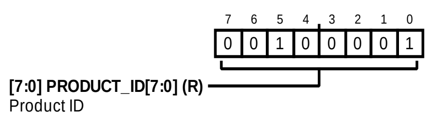


Table 12. Bit Descriptions for REG0004

Bits	Bit Name	Description	Reset	Recommended	Access
[7:0]	PRODUCT_ID[7:0]	Product ID	0x21	N/A	R

Address: 0x005, Reset: 0x00, Name: REG0005

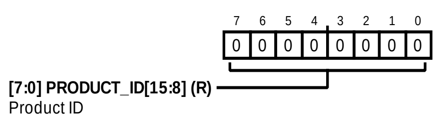


Table 13. Bit Descriptions for REG0005

Bits	Bit Name	Description	Reset	Recommended	Access
[7:0]	PRODUCT_ID[15:8]	Product ID	0x0	N/A	R

Address: 0x00A, Reset: 0x00, Name: REG000A

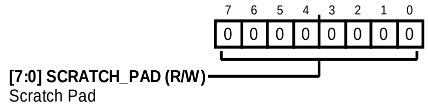


Table 14. Bit Descriptions for REG000A

Bits	Bit Name	Description	Reset	Recommended	Access
[7:0]	SCRATCH_PAD	Scratch Pad	0x0	User defined	R/W

Address: 0x00B, Reset: 0x01, Name: REG000B

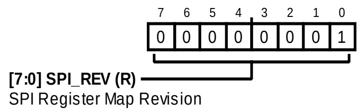


Table 15. Bit Descriptions for REG000B

Bits	Bit Name	Description	Reset	Recommended	Access
[7:0]	SPI_REV	SPI Register Map Revision	0x1	N/A	R

Address: 0x00C, Reset: 0x56, Name: REG000C

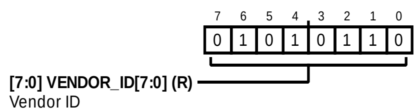


Table 16. Bit Descriptions for REG000C

Bits	Bit Name	Description	Reset	Recommended	Access
[7:0]	VENDOR_ID[7:0]	Vendor ID	0x56	N/A	R

Address: 0x00D, Reset: 0x04, Name: REG000D

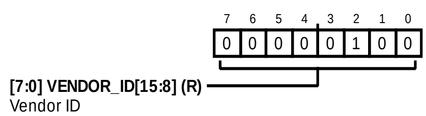


Table 17. Bit Descriptions for REG000D

Bits	Bit Name	Description	Reset	Recommended	Access
[7:0]	VENDOR_ID[15:8]	Vendor ID	0x4	N/A	R

Address: 0x010, Reset: 0x80, Name: REG0010

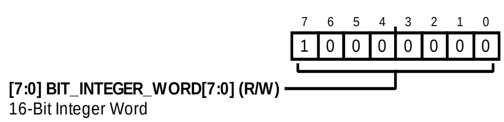


Table 18. Bit Descriptions for REG0010

Bits	Bit Name	Description	Reset	Recommended	Access
[7:0]	BIT_INTEGER_WORD[7:0]	16-Bit Integer Word. Sets the integer value of N. Updates to the PLL N counter, including FRAC1, FRAC2, and MOD2, are double buffered by this bit field.	0x80	User defined	R/W

Address: 0x011, Reset: 0x00, Name: REG0011

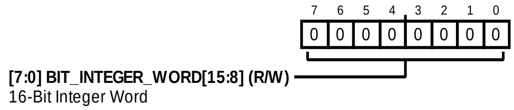


Table 19. Bit Descriptions for REG0011

Bits	Bit Name	Description	Reset	Recommended	Access
[7:0]	BIT_INTEGER_WORD[15:8]	16-Bit Integer Word. Sets the integer value of N. Updates to the PLL N counter, including FRAC1, FRAC2, and MOD2, are double buffered by this bit field.	0x0	User defined	R/W

Address: 0x012, Reset: 0x00, Name: REG0012

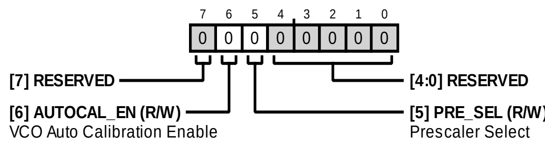


Table 20. Bit Descriptions for REG0012

Bits	Bit Name	Description	Reset	Recommended	Access
7	RESERVED	Reserved.	0x0	0x0	R/W
6	AUTOCAL_EN	VCO Auto Calibration Enable. 0: disable. 1: enable.	0x0	0x1	R/W
5	PRE_SEL	Prescaler Select. The dual modulus prescaler is set by this bit. It divides down the VCO signal such that the frequency going into the N divider is within the appropriate range. This setting affects the RF frequency and the minimum and maximum N values. 0: 4/5. 1: 8/9.	0x0	4/5: 0x0, 8/9: 0x1	R/W
[4:0]	RESERVED[4:0]	Reserved.	0x0	0x0	R/W

Address: 0x014, Reset: 0x00, Name: REG0014

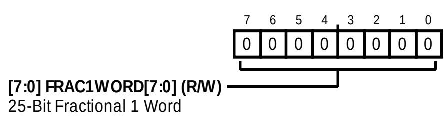


Table 21. Bit Descriptions for REG0014

Bits	Bit Name	Description	Reset	Recommended	Access
[7:0]	FRAC1WORD[7:0]	25-Bit Fractional 1 Word. Sets the FRAC1 value of N.	0x0	User defined	R/W

Address: 0x015, Reset: 0x00, Name: REG0015

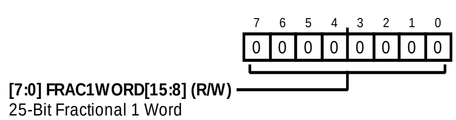


Table 22. Bit Descriptions for REG0015

Bits	Bit Name	Description	Reset	Recommended	Access
[7:0]	FRAC1WORD[15:8]	25-Bit Fractional 1 Word. Sets the FRAC1 value of N.	0x0	User defined	R/W

Address: 0x016, Reset: 0x00, Name: REG0016

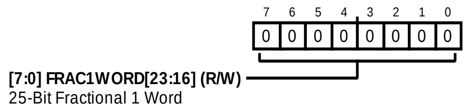


Table 23. Bit Descriptions for REG0016

Bits	Bit Name	Description	Reset	Recommended	Access
[7:0]	FRAC1WORD[23:16]	25-Bit Fractional 1 Word. Sets the FRAC1 value of N.	0x0	User defined	R/W

Address: 0x017, Reset: 0x00, Name: REG0017

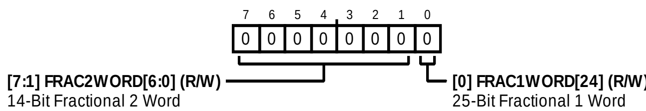


Table 24. Bit Descriptions for REG0017

Bits	Bit Name	Description	Reset	Recommended	Access
[7:1]	FRAC2WORD[6:0]	14-Bit Fractional 2 Word. Sets the FRAC2 value of N.	0x0	User defined	R/W
0	FRAC1WORD[24]	25-Bit Fractional 1 Word. Sets the FRAC1 value of N.	0x0		R/W

Address: 0x018, Reset: 0x00, Name: REG0018

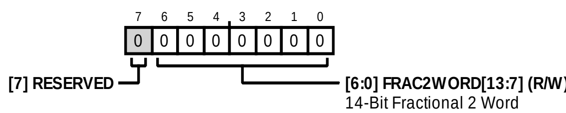


Table 25. Bit Descriptions for REG0018

Bits	Bit Name	Description	Reset	Recommended	Access
7	RESERVED	Reserved.	0x0	0x0	R/W
[6:0]	FRAC2WORD[13:7]	14-Bit Fractional 2 Word. Sets the FRAC2 value of N.	0x0	User defined	R/W

Address: 0x019, Reset: 0x00, Name: REG0019

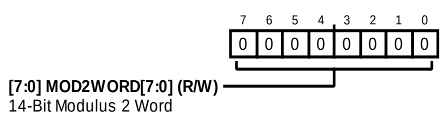


Table 26. Bit Descriptions for REG0019

Bits	Bit Name	Description	Reset	Recommended	Access
[7:0]	MOD2WORD[7:0]	14-Bit Modulus 2 Word. Sets the MOD2 value of N.	0x0	User defined	R/W

Address: 0x01A, Reset: 0x00, Name: REG001A

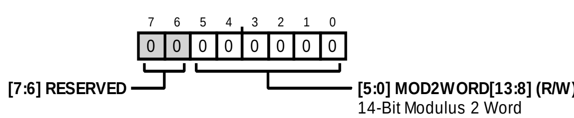


Table 27. Bit Descriptions for REG001A

Bits	Bit Name	Description	Reset	Recommended	Access
[7:6]	RESERVED	Reserved.	0x0	0x0	R/W
[5:0]	MOD2WORD[13:8]	14-Bit Modulus 2 Word. Sets the MOD2 value of N.	0x0	User defined	R/W

Address: 0x01E, Reset: 0x00, Name: REG001E

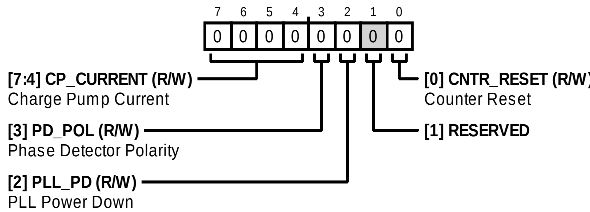


Table 28. Bit Descriptions for REG001E

Bits	Bit Name	Description	Reset	Recommended	Access
[7:4]	CP_CURRENT	Charge Pump Current. 0000: 0.35 mA. 0001: 0.70 mA. 0010: 1.05 mA. 0011: 1.40 mA. 0100: 1.75 mA. 0101: 2.10 mA. 0110: 2.45 mA. 0111: 2.80 mA. 1000: 3.15 mA. 1001: 3.50 mA. 1010: 3.85 mA. 1011: 4.20 mA. 1100: 4.55 mA. 1101: 4.90 mA. 1110: 5.25 mA. 1111: 5.60 mA.	0x0	2.1 mA: 0x5 4.2 mA: 0xB	R/W
3	PD_POL	Phase Detector Polarity. 0: negative (simulate unlock condition). 1: positive (nominal).	0x0	0x1	R/W
2	PLL_PD	PLL Power Down. Setting this bit to 1 powers down all internal PLL blocks. The VCO, doubler, RF, and IF chains remain powered up. The registers do not lose their values. After bringing the PLL out of power-down (setting to 0), a write to REG0010 is required to relock the loop. 0: power up. 1: power down.	0x0	0x0	R/W
1	RESERVED	Reserved.	0x0	0x0	R/W
0	CNTR_RESET	Counter Reset. Setting this bit to 1 holds the N counter and R counter in reset. No signals enter the phase frequency detector. 0: normal operation. 1: counter reset.	0x0	0x0	R/W

Address: 0x01F, Reset: 0x00, Name: REG001F

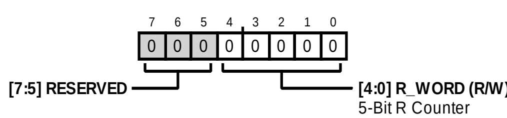


Table 29. Bit Descriptions for REG001F

Bits	Bit Name	Description	Reset	Recommended	Access
[7:5]	RESERVED	Reserved.	0x0	0x0	R
[4:0]	R_WORD	5-Bit R Counter. Programming to 0x0, results in divide by 32.	0x0	≥0x1	R/W

Address: 0x020, Reset: 0x00, Name: REG0020

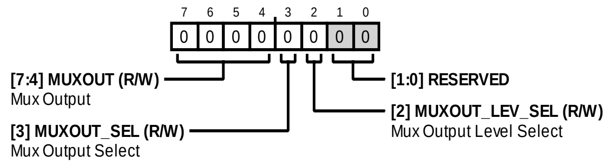


Table 30. Bit Descriptions for REG0020

Bits	Bit Name	Description	Reset	Recommended	Access
[7:4]	MUXOUT	Mux Output 0000: tristate (high impedance, only when MUXOUT_SEL = 0) 0001: digital lock detect 0010: charge pump up 0011: charge pump down 0100: RDIV/2 0101: NDIV/2 0110: VCO test modes 1000: logic high	0x0	0x1	R/W
3	MUXOUT_SEL	Mux Output Select 0: SDO pin used for register read back 1: SDO pin used for MUXOUT signal	0x0	Data: 0x0, mux: 0x1	R/W
2	MUXOUT_LEV_SEL	Mux Output Level Select 0: 1.8 V logic 1: 3.3 V logic	0x0	0x1	R/W
[1:0]	RESERVED	Reserved	0x0	0x0	R

Address: 0x022, Reset: 0x00, Name: REG0022

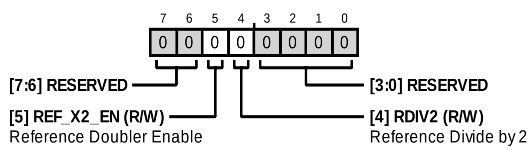


Table 31. Bit Descriptions for REG0022

Bits	Bit Name	Description	Reset	Recommended	Access
[7:6]	RESERVED	Reserved	0x0	0x0	R/W
5	REF_X2_EN	Reference Doubler Enable 0: disable 1: enable	0x0	User defined	R/W
4	RDIV2	Reference Divide by 2 0: disable 1: enable	0x0	User defined	R/W
[3:0]	RESERVED	Reserved	0x0	0x0	R/W

Address: 0x025, Reset: 0x00, Name: REG0025

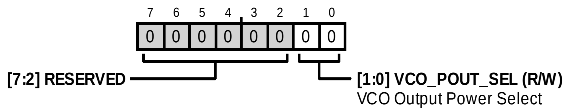


Table 32. Bit Descriptions for REG0025

Bits	Bit Name	Description	Reset	Recommended	Access
[7:2]	RESERVED	Reserved	0x0	0x0	R/W
[1:0]	VCO_POUT_SEL	VCO Output Power Select 00: minimum 11: maximum	0x0	0x3	R/W

Address: 0x026, Reset: 0x00, Name: REG0026

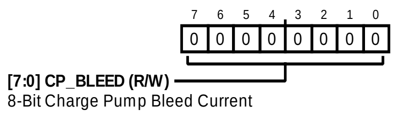


Table 33. Bit Descriptions for REG0026

Bits	Bit Name	Description	Reset	Recommended	Access
[7:0]	CP_BLEED	8-Bit Charge Pump Bleed Current.	0x0	0x73	R/W

Address: 0x027, Reset: 0x00, Name: REG0027

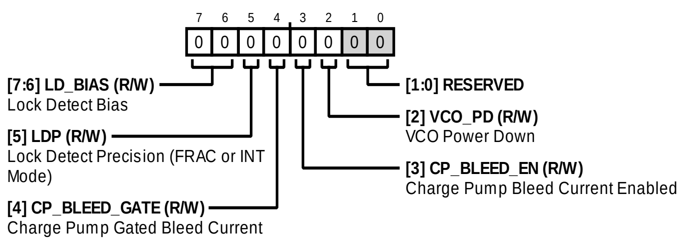


Table 34. Bit Descriptions for REG0027

Bits	Bit Name	Description	Reset	Recommended	Access
[7:6]	LD_BIAS	Lock Detect Bias. Sets lock detect window. 00: 5 ns (if LDP = 0). 01: 6 ns. 10: 8 ns. 11: 12 ns (for large values of bleed current).	0x0	0x3	R/W
5	LDP	Lock Detect Precision (FRAC or INT Mode). Controls the sensitivity of the digital lock detect. 0: FRAC mode (5 ns). 1: INT mode (2.4 ns).	0x0	FRAC: 0x0, INT: 0x1	R/W
4	CP_BLEED_GATE	Charge Pump Gated Bleed Current. 0: disable. 1: enable (digital lock detect must also be enabled).	0x0	0x0	R/W
3	CP_BLEED_EN	Charge Pump Bleed Current Enabled. Bleed current applies a slight offset within the charge pump to improve linearity. The result is lower phase noise and improved spurious performance. Set to 1 to enable negative bleed current. 0: disable. 1: enable.	0x0	FRAC: 0x1, INT: 0x0	R/W

Bits	Bit Name	Description	Reset	Recommended	Access
2	VCO_PD	VCO Power Down. 0: power up. 1: power down.	0x0	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	0x1	R/W

Address: 0x028, Reset: 0x00, Name: REG0028

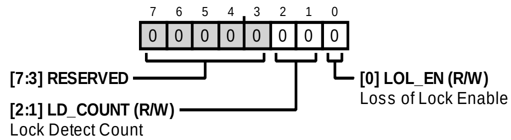


Table 35. Bit Descriptions for REG0028

Bits	Bit Name	Description	Reset	Recommended	Access
[7:3]	RESERVED	Reserved.	0x0	0x0	R/W
[2:1]	LD_COUNT	Lock Detect Count. Sets the number of PFD cycles within the lock detect window before lock detect goes high. 00: 1024 cycles. 01: 2048 cycles. 10: 4096 cycles. 11: 8192 cycles.	0x0	0x1	R/W
0	LOL_EN	Loss of Lock Enable. When loss of lock is enabled, if the digital lock detect is asserted, and the reference signal is removed, then the digital lock detect goes low. It is recommended to set this bit to 1. 0: disable. 1: enable.	0x0	0x1	R/W

Address: 0x02A, Reset: 0x00, Name: REG002A

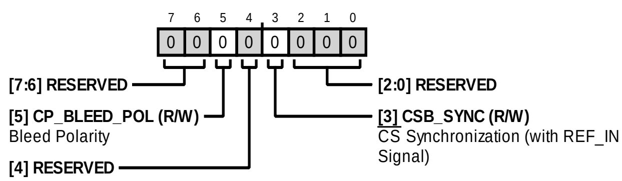


Table 36. Bit Descriptions for REG002A

Bits	Bit Name	Description	Reset	Recommended	Access
[7:6]	RESERVED[1:0]	Reserved	0x0	0x0	R/W
5	CP_BLEED_POL	Bleed Polarity 0: negative (nominal) 1: positive (not recommended)	0x0	0x0	R/W
4	RESERVED	Reserved.	0x0	0x0	R/W
3	CSB_SYNC	CS Synchronization (with REF_IN Signal) 0: disable 1: enable	0x0	0x0	R/W
[2:0]	RESERVED	Reserved	0x0	0x0	R/W

Address: 0x02B, Reset: 0x00, Name: REG002B

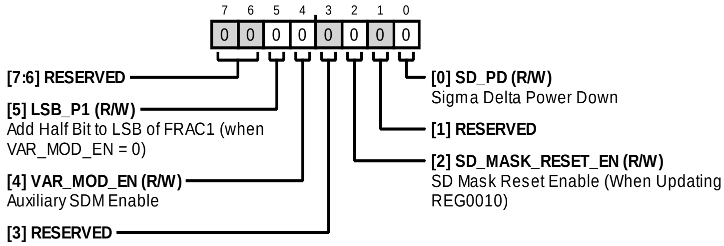


Table 37. Bit Descriptions for REG002B

Bits	Bit Name	Description	Reset	Recommended	Access
[7:6]	RESERVED	Reserved.	0x0	0x0	R/W
5	LSB_P1	Add Half Bit to LSB of FRAC1 (when VAR_MOD_EN = 0). 0: disable. 1: enable.	0x0	0x0	R/W
4	VAR_MOD_EN	Auxiliary SDM Enable. 0: disable (FRAC2 = 0). 1: enable (FRAC2 ≠ 0).	0x0	FRAC: 0x1, INT: 0x0	R/W
3	RESERVED	Reserved.	0x0	0x0	R/W
2	SD_MASK_RESET_EN	SD Mask Reset Enable (When Updating REG0010). 0: disable. 1: enable.	0x0	0x0	R/W
1	RESERVED	Reserved.	0x0	0x0	R/W
0	SD_PD	Sigma Delta Power Down. Set this bit if FRAC1 = FRAC2 = 0. 0: power up (FRAC mode). 1: power down (INT mode).	0x0	FRAC: 0x0, INT: 0x1	R/W

Address: 0x02C, Reset: 0x00, Name: REG002C

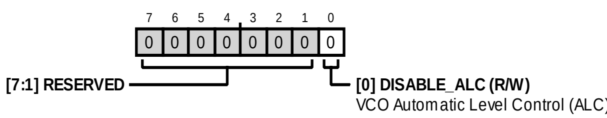


Table 38. Bit Descriptions for REG002C

Bits	Bit Name	Description	Reset	Recommended	Access
[7:1]	RESERVED	Reserved.	0x0	0x0	R/W
0	DISABLE_ALC	VCO Automatic Level Control (ALC). Keep this bit set to 1. 0: enable. 1: disable.	0x0	0x1	R/W

Address: 0x030, Reset: 0x00, Name: REG0030

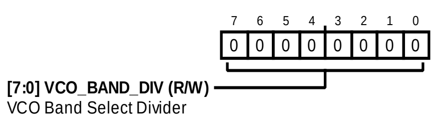


Table 39. Bit Descriptions for REG0030

Bits	Bit Name	Description	Reset	Recommended	Access
[7:0]	VCO_BAND_DIV	VCO Band Select Divider. $f_{BSC} = f_{PFD}$/VCO_BAND_DIV ≤ 2.4 MHz.	0x0	User defined	R/W

Address: 0x031, Reset: 0x00, Name: REG0031

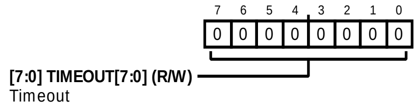


Table 40. Bit Descriptions for REG0031

Bits	Bit Name	Description	Reset	Recommended	Access
[7:0]	TIMEOUT[7:0]	Timeout. See the Autocalibration Lock Time section for details.	0x0	User defined	R/W

Address: 0x032, Reset: 0x00, Name: REG0032

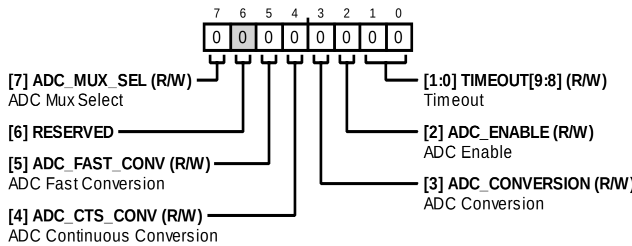


Table 41. Bit Descriptions for REG0032

Bits	Bit Name	Description	Reset	Recommended	Access
7	ADC_MUX_SEL	ADC Mux Select. 0: ADC input connected to proportional to absolute temperature (PTAT) voltage. 1: ADC input connected to scaled VTUNE voltage.	0x0	0x0	R/W
6	RESERVED	Reserved.	0x0	0x0	R/W
5	ADC_FAST_CONV	ADC Fast Conversion. 0: disable. 1: enable.	0x0	0x0	R/W
4	ADC_CTS_CONV	ADC Continuous Conversion. 0: disable. 1: enable.	0x0	0x0	R/W
3	ADC_CONVERSION	ADC Conversion. 0: no ADC conversion. 1: perform ADC conversion.	0x0	0x0	R/W
2	ADC_ENABLE	ADC Enable 0: disable. 1: enable.	0x0	0x0	R/W
[1:0]	TIMEOUT[9:8]	Timeout. See the Autocalibration Lock Time section for details.	0x0	User defined	R/W

Address: 0x033, Reset: 0x00, Name: REG0033

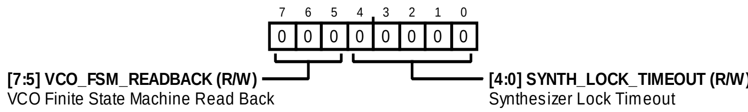


Table 42. Bit Descriptions for REG0033

Bits	Bit Name	Description	Reset	Recommended	Access
[7:5]	VCO_FSM_READBACK	VCO Finite State Machine Read Back. 000: checkerboard. 001: read back core and band. 101: ADC reading (temperature sensor).	0x0	0x0	R/W
[4:0]	SYNTH_LOCK_TIMEOUT	Synthesizer Lock Timeout. See the Autocalibration Lock Time section for details.	0x0	User defined	R/W

Address: 0x034, Reset: 0x00, Name: REG0034

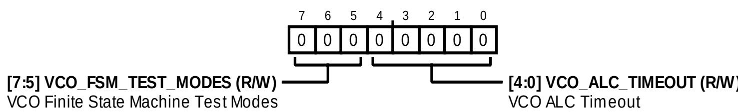


Table 43. Bit Descriptions for REG0034

Bits	Bit Name	Description	Reset	Recommended	Access
[7:5]	VCO_FSM_TEST_MODES	VCO Finite State Machine Test Modes. 000: normal operation. 010: manual overwrite VCO core and band. 100: manual overwrite of VCO calibration voltage.	0x0	0x4	R/W
[4:0]	VCO_ALC_TIMEOUT	VCO ALC Timeout. Keep this bit set to 0.	0x0	0x0	R/W

Address: 0x035, Reset: 0x00, Name: REG0035

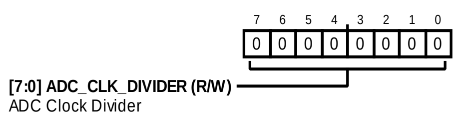


Table 44. Bit Descriptions for REG0035

Bits	Bit Name	Description	Reset	Recommended	Access
[7:0]	ADC_CLK_DIVIDER	ADC Clock Divider. ADC Clock = f_{PFD}/((ADC_CLK_DIVIDER × 4) + 2).	0x0	0xFF	R/W

Address: 0x036, Reset: 0x00, Name: REG0036

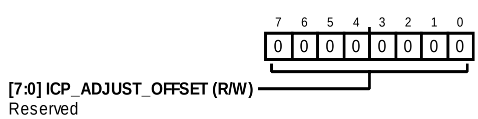


Table 45. Bit Descriptions for REG0036

Bits	Bit Name	Description	Reset	Recommended	Access
[7:0]	ICP_ADJUST_OFFSET	Reserved	0x0	0x30	R/W

Address: 0x037, Reset: 0x00, Name: REG0037

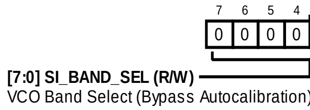


Table 46. Bit Descriptions for REG0037

Bits	Bit Name	Description	Reset	Recommended	Access
[7:0]	SI_BAND_SEL	VCO Band Select (Bypass Autocalibration)	0x0	0x0	R/W

Address: 0x038, Reset: 0x00, Name: REG0038

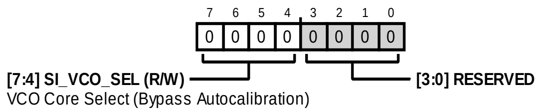


Table 47. Bit Descriptions for REG0038

Bits	Bit Name	Description	Reset	Recommended	Access
[7:4]	SI_VCO_SEL	VCO Core Select (Bypass Autocalibration)	0x0	0x0	R/W
[3:0]	RESERVED	Reserved	0x0	0x0	R/W

Address: 0x039, Reset: 0x00, Name: REG0039

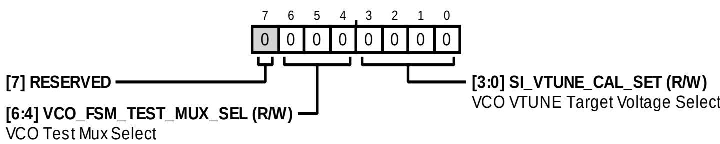


Table 48. Bit Descriptions for REG0039

Bits	Bit Name	Description	Reset	Recommended	Access
7	RESERVED	Reserved	0x0	0x0	R
[6:4]	VCO_FSM_TEST_MUX_SEL	VCO Test Mux Select 000: busy 001: N band 010: R band 011: Reserved 100: timeout clock 101: bias minimum 110: ADC busy 111: logic low	0x0	0x0	R/W

Bits	Bit Name	Description	Reset	Recommended	Access
[3:0]	SI_VTUNE_CAL_SET	VCO VTUNE Target Voltage Select 0: 0.58 V 1: 0.73 V 10: 0.88 V 11: 1.03 V 100: 1.18 V 101: 1.33 V 110: 1.48 V 111: 1.63 V 1000: 1.78 V 1001: 1.93 V 1010: 2.08 V 1011: 2.23 V 1100: 2.38 V 1101: 2.53 V 1110: 2.68 V 1111: 2.83 V	0x0	0x7	R/W

Address: 0x03A, Reset: 0x00, Name: REG003A

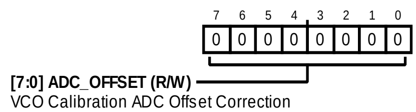


Table 49. Bit Descriptions for REG003A

Bits	Bit Name	Description	Reset	Recommended	Access
[7:0]	ADC_OFFSET	VCO Calibration ADC Offset Correction	0x0		R/W

Address: 0x03E, Reset: 0x00, Name: REG003E

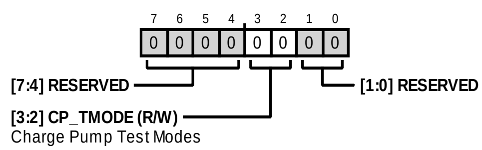


Table 50. Bit Descriptions for REG003E

Bits	Bit Name	Description	Reset	Recommended	Access
[7:4]	RESERVED	Reserved	0x0	0x0	R/W
[3:2]	CP_TMODE	Charge Pump Test Modes 00: tristate 11: normal	0x0	0x3	R/W
[1:0]	RESERVED	Reserved	0x0	0x	R/W

Address: 0x06E, Reset: 0x00, Name: REG006E

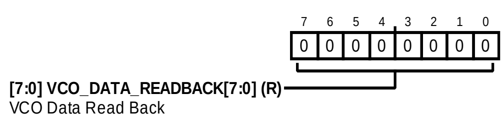


Table 51. Bit Descriptions for REG006E

Bits	Bit Name	Description	Reset	Recommended	Access
[7:0]	VCO_DATA_READBACK[7:0]	VCO Data Read Back	0x0	N/A	R

Address: 0x06F, Reset: 0x00, Name: REG006F

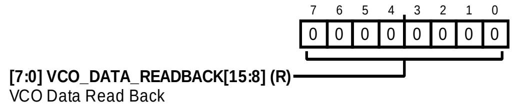


Table 52. Bit Descriptions for REG006F

Bits	Bit Name	Description	Reset	Recommended	Access
[7:0]	VCO_DATA_READBACK[15:8]	VCO Data Read Back	0x0	N/A	R

Address: 0x073, Reset: 0x00, Name: REG0073

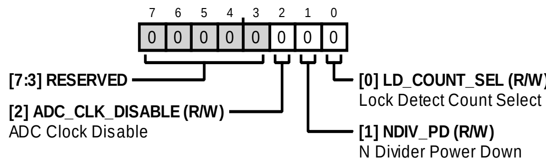


Table 53. Bit Descriptions for REG0073

Bits	Bit Name	Description	Reset	Recommended	Access
[7:3]	RESERVED	Reserved.	0x0	0x0	R/W
2	ADC_CLK_DISABLE	ADC Clock Disable. ADC_ENABLE overwrites this bit. 0: enable. 1: disable.	0x0	0x0	R/W
1	NDIV_PD	N Divider Power Down. 0: power up. 1: power down.	0x0	0x0	R/W
0	LD_COUNT_SEL	Lock Detect Count Select. Declares lock in 32, 64, 128, or 256 phase frequency detector cycles vs. the default 1024, 2048, 4096, or 8192 phase frequency detector cycles. 0: nominal (LD_COUNT). 1: divided (LD_COUNT/32).	0x0	0x0	R/W

Address: 0x07C, Reset: 0x00, Name: REG007C

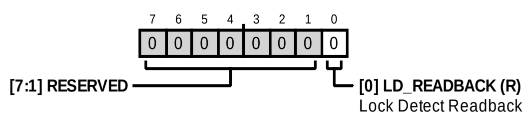


Table 54. Bit Descriptions for REG007C

Bits	Bit Name	Description	Reset	Recommended	Access
[7:1]	RESERVED	Reserved.	0x0	N/A	R
0	LD_READBACK	Lock Detect Readback	0x0	N/A	R

Address: 0x100, Reset: 0x03, Name: REG0100

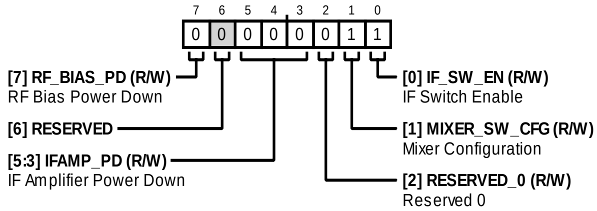


Table 55. Bit Descriptions for REG0100

Bits	Bit Name	Description	Reset	Recommended	Access
7	RF_BIAS_PD	RF Bias Power Down 0: power up 1: power down	0x0	0x0	R/W
6	RESERVED	Reserved	0x0	0x0	R/W
[5:3]	IFAMP_PD	IF Amplifier Power Down 000: power up (IF mode). 111: power down (I/Q mode)	0x0	I/Q mode: 0x7, IF mode: 0x0	R/W
2	RESERVED_0	Reserved 0	0x0	0x0	R/W
1	MIXER_SW_CFG	Mixer Configuration 0: mixer bypassed 1: enable mixer	0x1	0x1	R/W
0	IF_SW_EN	IF Switch Enable 0: disable (I/Q mode) 1: enable (IF mode)	0x1	I/Q mode: 0x0, IF mode: 0x1	R/W

Address: 0x101, Reset: 0x7F, Name: REG0101

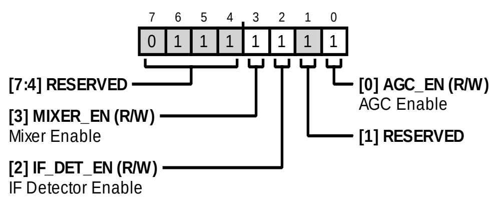


Table 56. Bit Descriptions for REG0101

Bits	Bit Name	Description	Reset	Recommended	Access
[7:4]	RESERVED	Reserved.	0x7	0x7	R/W
3	MIXER_EN	Mixer Enable 0: disabled. 1: enabled (I/Q and IF modes)	0x1	0x1	R/W
2	IF_DET_EN	IF Detector Enable 0: disable (I/Q mode) 1: enable (IF mode)	0x1	I/Q mode: 0x0, IF mode: 0x1	R/W
1	RESERVED	Reserved	0x1	0x0	R/W
0	AGC_EN	AGC Enable 0: disable (I/Q mode) 1: enable (IF mode)	0x1	I/Q mode: 0x0, IF mode: 0x1	R/W

Address: 0x102, Reset: 0x3F, Name: REG0102

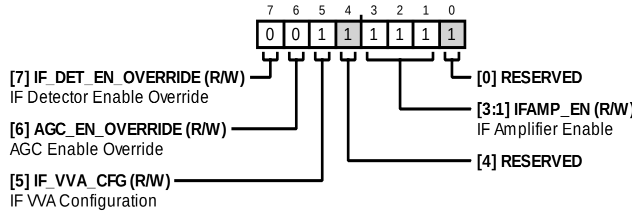


Table 57. Bit Descriptions for REG0102

Bits	Bit Name	Description	Reset	Recommended	Access
7	IF_DET_EN_OVERRIDE	IF Detector Enable Override 0: disable (IF detector only active in power-down mode) 1: enable (IF detector always on)	0x0	0x0	R/W
6	AGC_EN_OVERRIDE	AGC Enable Override 0: disable (IF AGC only active in power-down mode) 1: enable (IF AGC always on)	0x0	0x0	R/W
5	IF_VVA_CFG	IF VVA Configuration 0: disable (I/Q mode) 1: enable (IF mode)	0x1	I/Q mode: 0x0, IF mode: 0x1	R/W
4	RESERVED	Reserved	0x1	0x1	R/W
[3:1]	IFAMP_EN	IF Amplifier Enable 000: disable (I/Q mode) 111: enable (IF mode)	0x7	I/Q mode: 0x0, IF mode: 0x7	R/W
0	RESERVED	Reserved	0x1	0x1	R/W

Address: 0x103, Reset: 0x51, Name: REG0103

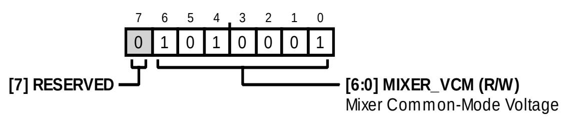


Table 58. Bit Descriptions for REG0103

Bits	Bit Name	Description	Reset	Recommended	Access
7	RESERVED	Reserved.	0x0	0x0	R/W
[6:0]	MIXER_VCM	Mixer Common-Mode Voltage. In I/Q mode, for V_{CM} = 0.0 V to 1.5 V, set MIXER_VCM = ROUND(23.8 × V_{CM} + 80.7). In I/Q mode, V_{CM} for = 1.5 V to 2.5 V, set MIXER_VCM = ROUND(23.8 × V_{CM} + 1.3). The default in I/Q mode for V_{CM} = 0 V, is MIXER_VCM = 81 = 0x51. In IF mode, set MIXER_VCM = ROUND(0.3 × (128 − TARGET_MIXER_DC_OFFSET) + 80.7)	0x51	I/Q mode: 0x5D, IF mode: 0x5B	R/W

Address: 0x104, Reset: 0x5F, Name: REG0104

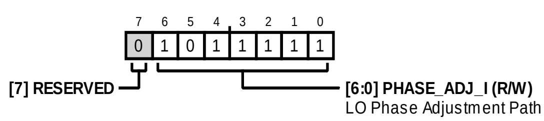


Table 59. Bit Descriptions for REG0104

Bits	Bit Name	Description	Reset	Recommended	Access
7	RESERVED	Reserved.	0x0	0x0	R/W
[6:0]	PHASE_ADJ_I	LO Phase Adjustment Path I	0x5F	0x5F	R/W

Address: 0x105, Reset: 0x5F, Name: REG0105

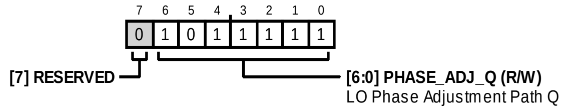


Table 60. Bit Descriptions for REG0105

Bits	Bit Name	Description	Reset	Recommended	Access
7	RESERVED	Reserved.	0x0	0x0	R/W
[6:0]	PHASE_ADJ_Q	LO Phase Adjustment Path Q	0x5F	0x5F	R/W

Address: 0x106, Reset: 0x7F, Name: REG0106

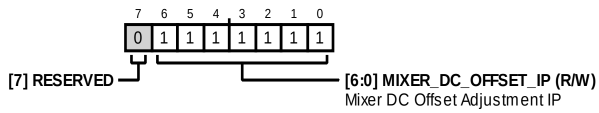


Table 61. Bit Descriptions for REG0106

Bits	Bit Name	Description	Reset	Recommended	Access
7	RESERVED	Reserved.	0x0	0x0	R/W
[6:0]	MIXER_DC_OFFSET_IP	Mixer DC Offset Adjustment IP. For I/Q mode, the default = 127 = 0x7F. For IF mode, the default = 95 = 0x5F.	0x7F	I/Q mode: 0x7F, IF mode: 0x5F	R/W

Address: 0x107, Reset: 0x7F, Name: REG0107

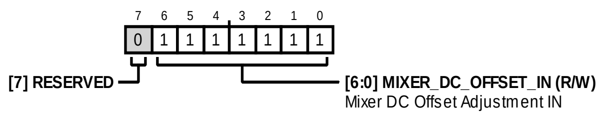


Table 62. Bit Descriptions for REG0107

Bits	Bit Name	Description	Reset	Recommended	Access
7	RESERVED	Reserved.	0x0	0x0	R/W
[6:0]	MIXER_DC_OFFSET_IN	Mixer DC Offset Adjustment IN. In I/Q mode, the default = 127 = 0x7F. For IF mode, the default = 95 = 0x5F.	0x7F	I/Q mode: 0x7F, IF mode: 0x5F	R/W

Address: 0x108, Reset: 0x7F, Name: REG0108

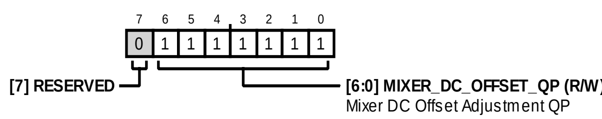


Table 63. Bit Descriptions for REG0108

Bits	Bit Name	Description	Reset	Recommended	Access
7	RESERVED	Reserved.	0x0	0x0	R/W
[6:0]	MIXER_DC_OFFSET_QP	Mixer DC Offset Adjustment QP. For I/Q mode, the default = 127 = 0x7F. For IF mode, the default = 95 = 0x5F.	0x7F	I/Q mode: 0x7F, IF mode: 0x5F	R/W

Address: 0x109, Reset: 0x7F, Name: REG0109

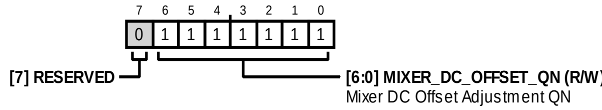


Table 64. Bit Descriptions for REG0109

Bits	Bit Name	Description	Reset	Recommended	Access
7	RESERVED	Reserved.	0x0	0x0	R/W
[6:0]	MIXER_DC_OFFSET_QN	Mixer DC Offset Adjustment QN. For I/Q mode, the default = 127 = 0x7F. For IF mode, the default = 95 = 0x5F.	0x7F	I/Q mode: 0x7F, IF mode: 0x5F	R/W

Address: 0x10C, Reset: 0x08, Name: REG010C

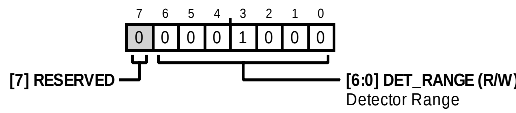


Table 65. Bit Descriptions for REG010C

Bits	Bit Name	Description	Reset	Recommended	Access
7	RESERVED	Reserved	0x0	0x0	R/W
[6:0]	DET_RANGE	Detector Range. Refer to the IF AGC Configuration section for details.	0x8	User defined	R/W

Address: 0x10D, Reset: 0x69, Name: REG010D

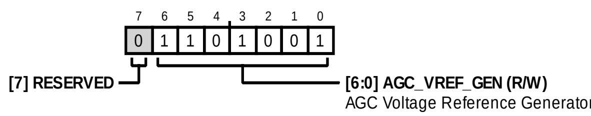


Table 66. Bit Descriptions for REG010D

Bits	Bit Name	Description	Reset	Recommended	Access
7	RESERVED	Reserved.	0x0	0x0	R/W
[6:0]	AGC_VREF_GEN	AGC Voltage Reference Generator. Refer to the IF AGC Configuration section for details.	0x69	User defined	R/W

Address: 0x115, Reset: 0x08, Name: REG0115

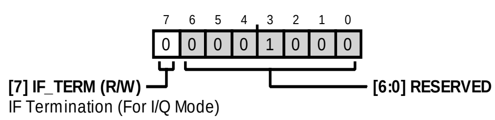


Table 67. Bit Descriptions for REG0115

Bits	Bit Name	Description	Reset	Recommended	Access
7	IF_TERM	IF Termination (For I/Q Mode) 0: unterminated (IF mode) 1: terminated (I/Q mode)	0x0	I/Q mode: 0x1 IF mode: 0x0	R/W
[6:0]	RESERVED	Reserved	0x8	0x8	R/W

Address: 0x116, Reset: 0x00, Name: REG0116

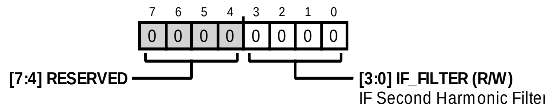


Table 68. Bit Descriptions for REG0116

Bits	Bit Name	Description	Reset	Recommended	Access
[7:4]	RESERVED	Reserved.	0x0	0x0	R/W
[3:0]	IF_FILTER	IF Second Harmonic Filter 0000: ~6.75 GHz 0001: ~6.50 GHz 0010: ~6.25 GHz 0011: ~6.00 GHz 0100: ~5.75 GHz 0101: ~5.50 GHz 0110: ~5.25 GHz 0111: ~5.00 GHz 1000: ~4.75 GHz 1001: ~4.50 GHz	0x0	0x0	R/W

Address: 0x117, Reset: 0x4C, Name: REG0117

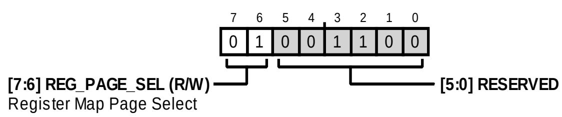


Table 69. Bit Descriptions for REG0117

Bits	Bit Name	Description	Reset	Recommended	Access
[7:6]	REG_PAGE_SEL	Register Map Page Select 0: read from Register 0x010 to Register 0x07C (the PLL section) 1: read from Register 0x000 to Register 0x00D or Register 0x100 to Register 0x119 (the mixer section)	0x1	PLL: 0x0, mixer: 0x1	R/W
[5:0]	RESERVED	Reserved	0xC	0xC	R/W

Address: 0x119, Reset: 0x08, Name: REG0119

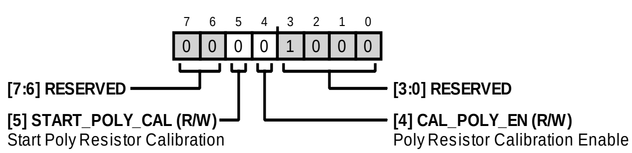


Table 70. Bit Descriptions for REG0119

Bits	Bit Name	Description	Reset	Recommended	Access
[7:6]	RESERVED	Reserved.	0x0	0x0	R/W
5	START_POLY_CAL	Start Poly Resistor Calibration 0: disable 1: enable	0x0	0x0	R/W
4	CAL_POLY_EN	Poly Resistor Calibration Enable 0: disable 1: enable	0x0	0x0	R/W
[3:0]	RESERVED	Reserved	0x8	0x8	R/W

OUTLINE DIMENSIONS

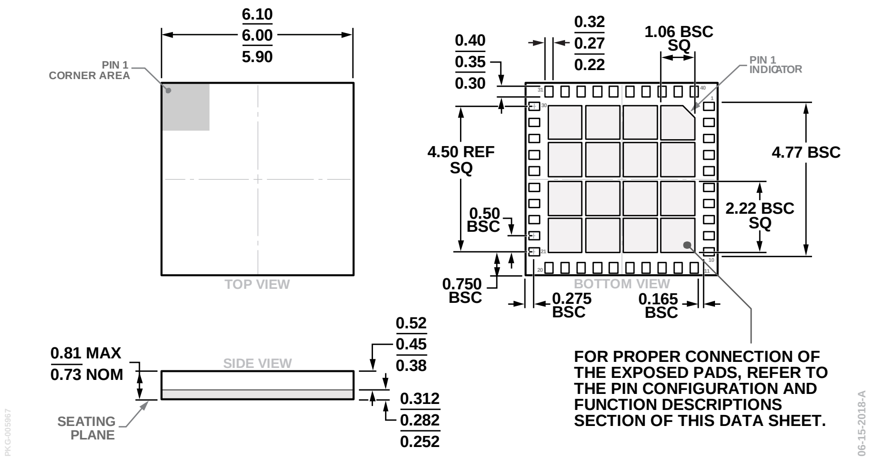


Figure 101. 40-Terminal Land Grid Array [LGA]
(CC-40-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADMV4530ACCZ	−40°C to +85°C	40-Terminal Land Grid Array [LGA]	CC-40-8
ADMV4530ACCZ-RL7	−40°C to +85°C	40-Terminal Land Grid Array [LGA]	CC-40-8
ADMV4530IF-EVALZ		IF Mode Evaluation Board	
ADMV4530IQ-EVALZ		I/Q Mode Evaluation Board	

[1] Z = RoHS Compliant Part.