Precision, Low Noise, CMOS, Rail-to-Rail, Input/Output Operational Amplifier

Known Good Die

AD8608-KGD

FEATURES

Low offset voltage: 65 µV maximum
Low input bias currents: 1 pA maximum
Low noise: 8 nV/√Hz
Wide bandwidth: 10 MHz
High open-loop gain: 1000 V/mV
Unity gain stable
Single-supply operation: 2.7 V to 5.5 V
Known good die (KGD): these die are fully guaranteed to data sheet specifications

APPLICATIONS

Photodiode amplification
Battery-powered instrumentation
Multipole filters
Sensors
Barcode scanners
Audio

GENERAL DESCRIPTION

The AD8608-KGD[1] is a single, rail-to-rail input and output, single-supply amplifier that features very low offset voltage, low input voltage and current noise, and wide signal bandwidth. The AD8608-KGD uses the Analog Devices, Inc. patented DigiTrim® trimming technique, which achieves superior precision without laser trimming.

The combination of low offsets, low noise, very low input bias currents, and high speed makes this amplifier useful in a wide variety of applications. Filters, integrators, photodiode amplifiers, and high impedance sensors all benefit from the combination of performance features. Audio and other ac applications benefit from the wide bandwidth and low distortion. Applications for this amplifier include optical control loops, portable and loop-powered instrumentation, and audio amplification for portable devices.

The AD8608-KGD is specified over the extended industrial temperature range (−40°C to +125°C).

Additional application and technical information can be found in the AD8605/AD8606/AD8608 data sheet.

[1] Protected by U.S. Patent No. 5,969,657.

Rev. 0 **Document Feedback**

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REVISION HISTORY

4/15—Revision 0: Initial Version

SPECIFICATIONS

5 V ELECTRICAL SPECIFICATIONS

V_S = 5 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_S = 3.5 V, V_{CM} = 2.7 V		20	75	µV
		V_S = 5 V, V_{CM} = 0 V to 5 V		80	300	µV
		−40°C < T_A < +125°C			750	µV
Input Bias Current	I_B			0.2	1	pA
		−40°C < T_A < +125°C			300	pA
Input Offset Current	I_{OS}			0.1	0.5	pA
		−40°C < T_A < +125°C			75	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	85	100		dB
		−40°C < T_A < +125°C	75	90		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 4.5 V	300	1000		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		1.5	6.0	µV/°C
INPUT CAPACITANCE						
Common-Mode Input Capacitance	C_{COM}			8.8		pF
Differential Input Capacitance	C_{DIFF}			2.6		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	4.96	4.98		V
		I_L = 10 mA	4.7	4.79		V
		−40°C < T_A < +125°C	4.6			V
Output Voltage Low	V_{OL}	I_L = 1 mA		20	40	mV
		I_L= 10 mA		170	210	mV
		−40°C < T_A < +125°C			290	mV
Output Current	I_{OUT}			±80		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 5.5 V	77	92		dB
		−40°C < T_A < +125°C	70	90		dB
Supply Current/Amplifier	I_{SY}	I_{OUT} = 0 mA		1	1.2	mA
		−40°C < T_A < +125°C			1.4	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ, C_L = 16 pF		5		V/µs
Settling Time	t_S	To 0.01%, 0 V to 2 V step, A_V = 1		<1		µs
Unity Gain Bandwidth Product	GBP			10		MHz
Phase Margin	Φ_M			65		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		2.3	3.5	µV p-p
Voltage Noise Density	e_n	f = 1 kHz		8	12	nV/√Hz
	e_n	f = 10 kHz		6.5		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.01		pA/√Hz

2.7 V ELECTRICAL SPECIFICATIONS

V_S = 2.7 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_S = 3.5 V, V_{CM} = 2.7 V		20	75	
		V_S = 2.7 V, V_{CM} = 0 V to 2.7 V		80	300	μV
		−40°C < T_A < +125°C			750	μV
Input Bias Current	I_B			0.2	1	pA
		−40°C < T_A < +125°C			300	pA
Input Offset Current	I_{OS}			0.1	0.5	pA
		−40°C < T_A < +125°C			75	pA
Input Voltage Range			0		2.7	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.7 V	80	95		dB
		−40°C < T_A < +125°C	70	85		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 2.2 V	110	350		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		1.5	6.0	μV/°C
INPUT CAPACITANCE						
Common-Mode Input Capacitance	C_{COM}			8.8		pF
Differential Input Capacitance	C_{DIFF}			2.6		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	2.6	2.66		V
		−40°C < T_A < +125°C	2.6			V
Output Voltage Low	V_{OL}	I_L = 1 mA		25	40	mV
		−40°C < T_A < +125°C			50	mV
Output Current	I_{OUT}			±30		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		1.2		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 5.5 V	77	92		dB
		−40°C < T_A < +125°C	70	90		dB
Supply Current/Amplifier	I_{SY}	I_{OUT} = 0 mA		1.15	1.4	mA
		−40°C < T_A < +125°C			1.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ, C_L = 16 pF		5		V/μs
Settling Time	t_S	To 0.01%, 0 V to 1 V step, A_V = 1		<0.5		μs
Unity Gain Bandwidth Product	GBP			9		MHz
Phase Margin	Φ_M			50		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		2.3	3.5	μV p-p
Voltage Noise Density	e_n	f = 1 kHz		8	12	nV/√Hz
	e_n	f = 10 kHz		6.5		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.01		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to V_S
Differential Input Voltage	6 V
Output Short-Circuit Duration to GND	Observe Derating Curves
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

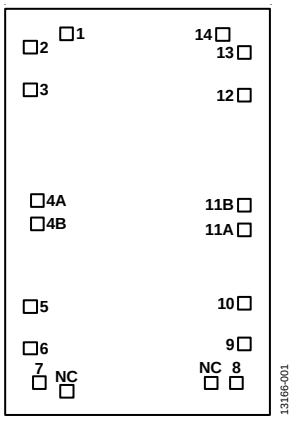

Figure 1. Pad Configuration

Table 4. Pad Function Descriptions

Pad	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Pad Type	Description
1	−490	+1239	OUT A	Single	Output Channel A
2	−749	+1153	− IN A	Single	Inverting Input Channel A
3	−749	+853	+ IN A	Single	Noninverting Input Channel A
4A	−703	+85	V+ Supply	Double	Positive Supply Voltage
4B	−703	−84	V+ Supply	Double	Positive Supply Voltage, Double Bond Pad
5	−749	−659	+ IN B	Single	Noninverting Input Channel B
6	−749	−944	− IN B	Single	Inverting Input Channel B
7	−683	−1189	OUTB	Single	Output Channel B
8	+688	−1189	OUTC	Single	Output Channel C
9	+749	−916	− IN C	Single	Inverting Input Channel C
10	+749	−631	+ IN C	Single	Noninverting Input Channel C
11A	+749	−122	V− Supply	Double	Negative Supply Voltage
11B	+749	+47	V− Supply	Double	Negative Supply Voltage, Double Bond Pad
12	+749	+813	+ IN D	Single	Noninverting Input Channel D
13	+749	+1113	− IN D	Single	Inverting Input Channel D
14	+597	+1239	OUT D	Single	Output Channel D

OUTLINE DIMENSIONS

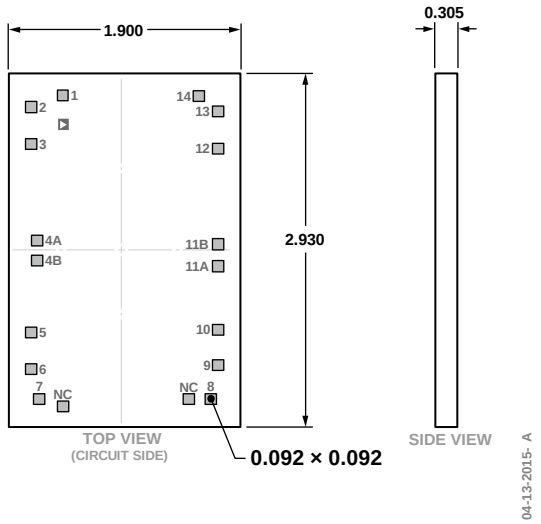

Figure 2. 14-Pad Bare Die [CHIP]
(C-14-3)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 5. Die Specifications

Parameter	Value	Unit
Die Size (Maximum)	1900 × 2930	µm
Bond Pad Composition	AlCu (0.5%)	%
Bond Pad (Minimum)	92 × 92	µm
Passivation Type	OxyNitride	Not applicable
Thickness	305	µm
Backside Bias	GND	Not applicable
Scribe Line (Street) Width	100 × 150	µm
ESD	HBM 4000	V

Table 6. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Ablestik 84-1LMIS R4
Bonding Method	1 mil gold

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8608-KGD-CHIP	−40°C to +125°C	14-Pad Bare Die [CHIP]	C-14-3