REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. - ro	17-04-11	C. SAFFLE

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJSEH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
15-10-01

REVISION LEVEL
A

MICROCIRCUIT, LINEAR, LOW NOISE INSTRUMENTATION AMPLIFIER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-14205**

SHEET 1 OF 14

DSCC FORM 2233
APR 97

5962-E276-17

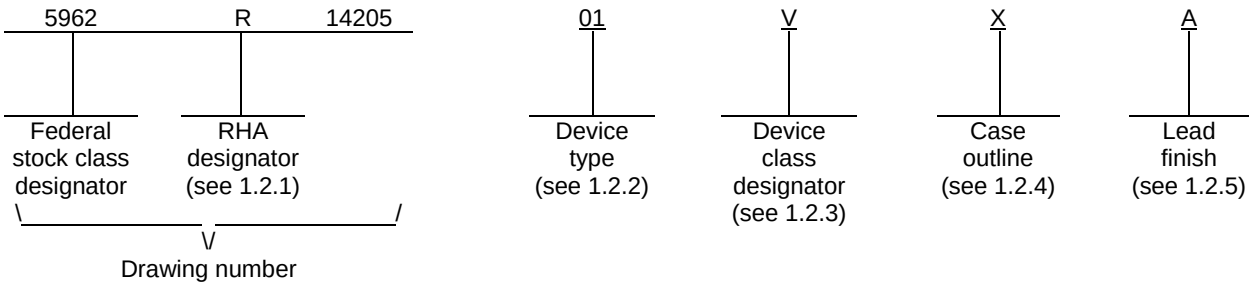
DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

Downloaded from Arrow.com.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD8229S	Low noise instrumentation amplifier
02	AD8229S	Low noise instrumentation amplifier

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDFP3-F14	14	Bottom brazed flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

Downloaded from Arrow.com.

1.3 Absolute maximum ratings. 1/

Supply voltage (+V_S to –V_S)	36 V
Output short circuit current duration	Indefinite
Maximum voltage at –IN, +IN	±V_S 2/
Differential input voltage –IN to +IN, gain ≤ 4	±V_S 2/
Differential input voltage –IN to +IN, 4 > gain > 50	±50 V / Gain 2/
Differential input voltage –IN to +IN, gain ≥ 50	±1 V 2/
Maximum voltage at REF	±V_S 2/
Storage temperature range	-65°C to +150°C
Power dissipation (P_D)	400 mW 3/
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+150°C
Thermal resistance, junction-to-case (θ_{JC})	27°C/W 4/
Thermal resistance, junction-to-ambient (θ_{JA})	50°C/W 4/

1.4 Recommended operating conditions.

Supply voltage (±V_S)	±5 V to ±15 V
Ambient operating temperature range (T_A)	-55°C to +125°C

Gain set by R_G resistor across the two R_G pins per G = 1 + (6 kΩ / R_G)

Acceptable value range; for R_G = ∞ Ω (open) for G = 1 to R_G = 6.006 Ω for G = 1000.

1.5 Operating performance characteristics. 5/

Input / output characteristics:

Gain nonlinearity R_L = 10 kΩ, V_{OUT} = ±10 V, G = 1 to 1000	2 ppm
Gain temperature drift: G = 1	2 ppm/°C
Gain temperature drift: G > 1	-100 ppm/°C
CMRR dc to 60 Hz with 1 kΩ imbalance, V_{CM} = ±10 V, G = 1	90 dB
CMRR dc to 60 Hz with 1 kΩ imbalance, V_{CM} = ±10 V, G = 10	110 dB
CMRR dc to 60 Hz with 1 kΩ imbalance, V_{CM} = ±10 V, G = 100	130 dB
CMRR dc to 60 Hz with 1 kΩ imbalance, V_{CM} = ±10 V, G = 1000	140 dB
CMRR at 5 kHz, V_{CM} = ±10 V, G = 1	80 dB
CMRR at 5 kHz, V_{CM} = ±10 V, G = 10 to 1000	90 dB
Offset referred to input (RTI) versus supply (PSRR), V_S = ±5 V to ±15 V, G = 10	120 dB
Offset referred to input (RTI) versus supply (PSRR), V_S = ±5 V to ±15 V, G = 100\1000	130 dB

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ For voltages beyond these limits, use input protection resistors. See manufacturer's datasheet for more application information regarding these specifications.

3/ Include supply and output drive current for total power dissipation in actual application. Absolute maximum power limited by application actual maximum operating temperature and actual θ_{JA} to prevent exceeding absolute maximum T_J limit.

4/ Measurement taken under absolute worst case condition and represent data taken with thermal camera for highest power density location. See MIL-STD-1835 for average package θ_{JA} number.

5/ Unless otherwise specified, ±V_S = ±15 V, V_{REF} = 0 V, T_A = 25°C, G = 1, and R_L = 10 kΩ.

Downloaded from Arrow.com.

1.5 Operating performance characteristics - continued. 5/

Input / output characteristics - continued:

Output swing, R_L = 2 kΩ	-V_S + 1.8 V to +V_S - 1.2 V
Output swing, R_L = 2 kΩ, T_A = -55°C to +125°C	-V_S + 1.9 V to +V_S - 1.3 V
Output short circuit current	35 mA
Input impedance (±IN to ground)	1.5 GΩ || 3 pF 6/

Reference characteristics:

Reference input resistance	10 kΩ
Reference input current, ±IN = 0 V	70 µA
Reference input voltage range	±V_S

Noise characteristics:

Voltage noise RTI, peak to peak, 0.1 Hz to 10 Hz, ±IN = 0 V, G = 1000	100 nV_{PP}
Current noise spectral density: 1 kHz	1.5 pA / $\sqrt{Hz}$
Peak to peak current noise, 0.1 Hz to 10 Hz, G = 1000	100 pA_{PP}

Dynamic signal response:

Small signal bandwidth -3 dB, G = 10	4 MHz
Small signal bandwidth -3 dB, G = 100	1.2 MHz
Small signal bandwidth -3 dB, G = 1000	0.15 MHz
Settling time 0.01%, 10 V step, G = 1	0.75 µs
Settling time 0.01%, 10 V step, G = 10	0.65 µs
Settling time 0.01%, 10 V step, G = 100	0.85 µs
Settling time 0.01%, 10 V step, G = 1000	5 µs
Settling time 0.001%, 10 V step, G = 1	0.9 µs
Settling time 0.001%, 10 V step, G = 10	0.9 µs
Settling time 0.001%, 10 V step, G = 100	1.2 µs
Settling time 0.001%, 10 V step, G = 1000	7 µs
Total harmonic distortion, first five harmonics, f = 1 kHz, R_L = 2 kΩ, V_{OUT} = 10 V_{PP}, G = 1	-130 dBc
Total harmonic distortion, first five harmonics, f = 1 kHz, R_L = 2 kΩ, V_{OUT} = 10 V_{PP}, G = 10	-116 dBc
Total harmonic distortion, first five harmonics, f = 1 kHz, R_L = 2 kΩ, V_{OUT} = 10 V_{PP}, G = 100	-113 dBc
Total harmonic distortion, first five harmonics, f = 1 kHz, R_L = 2 kΩ, V_{OUT} = 10 V_{PP}, G = 1000	-111 dBc
Total harmonic distortion + N, f = 1 kHz, R_L = 2 kΩ, V_{OUT} = 10 V_{PP}, G = 100	0.0005%

1.6 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s) :

Device type 01	100 krad(Si) 7/

Maximum total dose available (dose rate ≤ 10 mrads(Si)/s) :

Device type 02	50 krad(Si) 8/

6/ Differential and common mode input impedance can be calculated from the pin impedance: Z_{DIFF} = 2(ZPIN), Z_{CM} = ZPIN/2.

7/ Device type 01 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.

8/ For device type 02, radiation end point limits for the noted parameters are guaranteed for the conditions specified in MIL-STD-883, method 1019, condition D.

Downloaded from Arrow.com.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

Downloaded from Arrow.com.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ $\pm V_S = \pm5$ V and ±15 V unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input/output characteristics.								
Input offset voltage 4/	V_{OSI}			1	01, 02	-100	100	µV
				2,3		-125	125	
			P,L,R	1	01	-100	100	
			D,P,L		02	-100	100	
Input offset voltage drift 4/ 5/	$\Delta V_{OSI} / \Delta T$			2,3	01, 02	-1	1	µV/°C
Output offset voltage 4/	V_{OSO}			1	01, 02	-1000	1000	µV
				2,3		-1250	1250	
			P,L,R	1	01	-1000	1000	
			D,P,L		02	-1000	1000	
Output offset voltage drift 4/ 5/	$\Delta V_{OSO} / \Delta T$			2,3	01, 02	-10	10	µV/°C
Gain range (G = 1 + 6 kΩ/Rgain)	G			1,2,3	01, 02	1	1000	V/V
			P,L,R	1	01	1	1000	
			D,P,L		02	1	1000	
Gain error Gain = 1	GERR1	$V_S = \pm5$ V, $V_{OUT} = \pm2$ V,		1	01, 02	-0.03	0.03	%
		$V_S = \pm15$ V, $V_{OUT} = \pm10$ V,		2,3		-0.04	0.04	
		G = 1	P,L,R	1	01	-0.03	0.03	
			D,P,L		02	-0.03	0.03	
Gain error 6/ Gain > 1	GERR > 1	G = 1000		1	01, 02	-0.6	0.6	%
				2,3		-1.2	1.2	
			P,L,R	1	01	-0.6	0.6	
			D,P,L		02	-0.6	0.6	

See footnotes at end of table.

Downloaded from Arrow.com.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ $\pm V_S = \pm 5$ V and ± 15 V unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input/output characteristics - continued.								
Input bias current	IIB	$V_S = \pm 15$ V		1,2,3	01, 02	-175	175	nA
			P,L,R	1	01	-250	250	
			D,P,L		02	-250	250	
		$V_S = \pm 5$ V		1,2	01, 02	-175	175	
				3		-275	275	
			P,L,R	1	01	-175	175	
			D,P,L		02	-175	175	
Input offset current	IOS			1,2,3	01, 02	-30	30	nA
			P,L,R	1	01	-30	30	
			D,P,L		02	-30	30	
Input voltage range 7/	IVR	$V_S = \pm 5$ V, V_{CM} = -2.2 V/+2.5 V, CMRR 1000 min 126 dB		1	01, 02	$-V_S + 2.8$	$+V_S - 2.5$	V
		$V_S = \pm 5$ V, V_{CM} = -2.2 V/+2.5 V, CMRR 1000 min 125 dB		2,3		$-V_S + 2.8$	$+V_S - 2.5$	
			P,L,R	1	01	$-V_S + 2.8$	$+V_S - 2.5$	
			D,P,L		02	$-V_S + 2.8$	$+V_S - 2.5$	
Common mode rejection ratio Gain = 1 7/	CMRR1	$V_S = \pm 5$ V, V_{CM} = -2.2 V/+2.5 V,		1	01, 02	86		dB
		$V_S = \pm 15$ V, V_{CM} = -12.2 V/+12.5 V,		2,3		85		
		G = 1	P,L,R	1	01	86		
			D,P,L		02	86		
Common mode rejection ratio Gain = 1000 7/	CMRR 1000	$V_S = \pm 15$ V, $V_{CM} = \pm 10$ V, G = 1000		1	01, 02	134		dB
				2,3		133		
			P,L,R	1	01	134		
			D,P,L		02	134		

See footnotes at end of table.

Downloaded from Arrow.com.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ $\pm V_S = \pm5$ V and ±15 V unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input/output characteristics - continued.								
Output swing	V_{SWING}	$R_L = 10\ k\Omega$		1	01, 02	$-V_S + 1.7$	$+V_S - 1.1$	V
				2		$-V_S + 1.8$	$+V_S - 1.2$	
				3		$-V_S + 2.0$	$+V_S - 1.2$	
			P,L,R	1	01	$-V_S + 1.7$	$+V_S - 1.1$	
			D,P,L		02	$-V_S + 1.7$	$+V_S - 1.1$	
Reference/power supply								
Reference gain error	REFerr	$V_S = \pm5$ V, REF = ±2.5 V, $V_S = \pm15$ V, REF = ±10 V		1,2,3	01, 02	-0.05	0.05	%
			P,L,R	1	01	-0.05	0.05	
			D,P,L		02	-0.05	0.05	
Power supply rejection ratio	PSRR	$V_S = \pm5$ V to ±15 V		1	01, 02	87		dB
				2,3		89		
			P,L,R	1	01	87		
			D,P,L		02	87		
Supply current	I_S	$V_S = \pm5$ V, ±15 V, $V_{CM} = 0$ V		1,2,3	01, 02		9	mA
			P,L,R	1	01		9	
			D,P,L		02		9	
Dynamic performance.								
Peak to peak voltage noise 5/ 8/	Enp-p	$V_S = \pm15$ V, 0.1 Hz to 10 Hz, $\pm IN = 0$ V		4,5,6	01, 02		5	μV_{P-P}
Input spectral density voltage noise 5/ 8/	Eni	$V_S = \pm15$ V, 10 kHz, $\pm IN = 0$ V		4	01, 02		1.1	nV / $\sqrt{Hz}$
				5			1.3	
				6			1.0	

See footnotes at end of table.

Downloaded from Arrow.com.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ $\pm V_S = \pm 5$ V and ± 15 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Reference/power supply – continued.							
Output spectral density 5/ 8/ voltage noise	Eno	$V_S = \pm 15$ V, 10 kHz, $\pm IN = 0$ V	4	01, 02		50	nV / $\sqrt{Hz}$
			5			57	
			6			42	
Small signal bandwidth 5/	BWSS	$V_S = \pm 15$ V, V_{IN} = 100 mV_{P-P} single ended	4,5	01, 02	15		MHz
			6		13		
Slew rate 5/	SR	$V_S = \pm 15$ V, G = 1, 100, 10% to 90% of 10 V output	4	01, 02	22		V/µs
			5		24		
			6		12		

1/ Device type 01 supplied to this drawing has been characterized through all levels P, L, and R of irradiation. Device type 02 supplied to this drawing has been characterized through all levels D, P, and L of irradiation. However, device type 01 is only tested at the "R" level and device type 02 is only tested at the "L" level. Pre and post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, $T_A = +25°C$.

2/ Device type 01 may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A for device type 01 and condition D for device type 02.

3/ Unless otherwise specified, $\pm V_S = \pm 5$ V and ± 15 V, $V_{REF} = 0$ V, G = 1, and $R_L = 10$ kΩ. Gain set by R_G resistor across the two R_G pins per $G = 1 + (6\ k\Omega / R_G)$. Acceptable value range for $R_G = \infty\ \Omega$ (open) for G = 1 to $R_G = 6.006\ \Omega$ for G = 1000.

4/ Total reference to input (RTI) $V_{OS} = V_{OSI} + (V_{OSO}/G)$.

5/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots. The test parameter Enp-p is also 100% production tested at T_A = ambient temperature.

6/ This specification is based on internal device gain settling resistors accuracies only and does not include the tolerance of the external gain settling resistor (R_G). For G > 1, external R_G errors should be added to the GERR > 1 specification.

7/ Input voltage range of the device input stage only. CMRR only specified under V_{CM} input range conditioned specified. The input range can depend on the common mode voltage, differential voltage, gain, and reference voltage. See manufacturer's datasheet for more application information regarding these specifications.

8/ $R_L = 50\ \Omega$ for Eno/Eni tests. No R_L used Enp-p. Total voltage noise = $\sqrt{(eni^2 + (eno/G)^2 + eRG^2)}$.

Downloaded from Arrow.com.

Device types	01 and 02		
Case outline	X		
Terminal number	Terminal symbol	Terminal type	Description
1	NC / GND	---	No connection or ground for this terminal. See note 1.
2	-IN	Analog input	Negative input terminal.
3	R_G	Analog input	Gain settling terminal. Place resistor across the two R_G pins to set the gain. G = 1 + (6 kΩ / R_G). Acceptable value range for R_G = ∞ Ω (open) for G = 1 to R_G = 6.006 Ω for G = 1000. See note 2.
4	R_G	Analog input	Gain settling terminal. Place resistor across the two R_G pins to set the gain. G = 1 + (6 kΩ / R_G). Acceptable value range for R_G = ∞ Ω (open) for G = 1 to R_G = 6.006 Ω for G = 1000. See note 2.
5	+IN	Analog input	Positive input terminals.
6	NC / GND	---	No connection or ground for this terminal. See note 1.
7	NC / GND	---	No connection or ground for this terminal. See note 1.
8	NC / GND	---	No connection or ground for this terminal. See note 1.
9	NC / GND	---	No connection or ground for this terminal. See note 1.
10	$-V_S$	Supply	Negative power supply terminal.
11	REF	Analog input	Reference voltage terminal. Drive this terminal with low impedance voltage source to level shift the output.
12	V_{OUT}	Analog output	Output terminal.
13	$+V_S$	Supply	Positive power supply terminal.
14	NC / GND	---	No connection or ground for this terminal. See note 1.

NOTES:

1. No internal circuitry connected to NC/GND pins so user may ground pin if desired.
2. This specification is based on internal device gain settling resistors accuracies only and does not include the tolerance of the external gain settling resistor (R_G). For G > 1, external R_G errors should be added to the GERR > 1 specification.

FIGURE 1. Terminal connections.

Downloaded from Arrow.com.

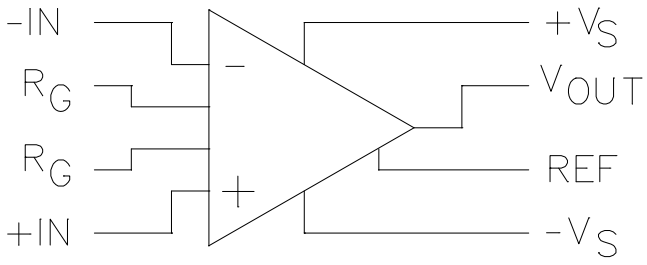


FIGURE 2. Block diagram.

Downloaded from Arrow.com.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

Downloaded from Arrow.com.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Final electrical parameters (see 4.2)	1,2,3, 1/ 3/ 4,5,6	1,2,3, 1/ 2/ 3/ 4,5,6
Group A test requirements (see 4.4)	1,2,3, 3/ 4,5,6	1,2,3, 3/ 4,5,6
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3, 2/ 3/ 4,5,6
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	1	1

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the previous electrical parameters.
3/ Subgroups 4, 5, and 6 parameters specified in Table I are part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C.

Parameters	Symbol	Conditions	Delta limits	Limit
Supply current	I_S	V_S = ±15 V	±0.2	mA
Input offset voltage	V_{OSI}	V_S = ±5 V	±10	µV
Output offset voltage	V_{OSO}	V_S = ±15 V	±380	µV
Input bias current	I_B	V_S = ±15 V	±16	nA

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A for device type 01 and condition D for device type 02 and as specified herein.

Downloaded from Arrow.com.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Application notes.

6.7.1 Architecture. The device is based on the classic 3 operational amplifier topology. This topology has two stages: a preamplifier to provide differential amplification followed by a difference amplifier that removes the common mode voltage and provides additional amplification. See manufacturer's datasheet for more application information regarding the device.

Downloaded from Arrow.com.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 17-04-11

Approved sources of supply for SMD 5962-14205 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1420501VXA	24355	AD8229AF/QMLR
5962L1420502VXA	24355	AD8229AF/QMLL

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 7910 Triad Center Greensboro, NC 27409-9605

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

Downloaded from Arrow.com.