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S29GL064N, S29GL032N

64 Mbit, 32 Mbit 3 V Page Mode MirrorBit Flash

Distinctive Characteristics

Architectural Advantages

- Single power supply operation
- Manufactured on 110 nm MirrorBit process technology
- Secured Silicon Sector region
  - 128-word/256-byte sector for permanent, secure identification through an 8-word/16-byte random Electronic Serial Number, accessible through a command sequence
  - Programmed and locked at the factory or by the customer
- Flexible sector architecture
  - 64Mb (uniform sector models): One hundred twenty-eight 32 Kword (64 KB) sectors
  - 64 Mb (boot sector models): One hundred twenty-seven 32 Kword (64 KB) sectors + eight 4Kword (8KB) boot sectors
  - 32 Mb (uniform sector models): Sixty-four 32Kword (64 KB) sectors
  - 32 Mb (boot sector models): Sixty-three 32Kword (64 KB) sectors + eight 4Kword (8KB) boot sectors
- Enhanced VersatileI/O™ Control
  - All input levels (address, control, and DQ input levels) and outputs are determined by voltage on V_{IO} input. V_{IO} range is 1.65 to V_{CC}
- Compatibility with JEDEC standards
  - Provides pin out and software compatibility for single-power supply flash, and superior inadvertent write protection
- 100,000 erase cycles typical per sector
- 20-year data retention typical

Performance Characteristics

- High performance
  - 90 ns access time
  - 8-word/16-byte page read buffer
  - 25 ns page read time
  - 16-word/32-byte write buffer which reduces overall programming time for multiple-word updates
- Low power consumption
  - 25 mA typical initial read current, 1 mA typical page read current
  - 50 mA typical erase/program current
  - 1 µA typical standby mode current
- Package options
  - 48-pin TSOP
  - 56-pin TSOP
  - 64-ball Fortified BGA
  - 48-ball fine-pitch BGA

Software and Hardware Features

- Software features
  - Advanced Sector Protection: offers Persistent Sector Protection and Password Sector Protection
  - Program Suspend & Resume: read other sectors before programming operation is completed
  - Erase Suspend & Resume: read/program other sectors before an erase operation is completed
  - Data# polling & toggle bits provide status
  - CFI (Common Flash Interface) compliant: allows host system to identify and accommodate multiple flash devices
  - Unlock Bypass Program command reduces overall multiple-word programming time
- Hardware features
  - WP#/ACC input accelerates programming time (when high voltage is applied) for greater throughput during system production. Protects first or last sector regardless of sector protection settings on uniform sector models
  - Hardware reset input (RESET#) resets device
  - Ready/Busy# output (RY/BY#) detects program or erase cycle completion

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General Description

The S29GL-N family of devices are 3.0-Volt single-power Flash memory manufactured using 110 nm MirrorBit technology. The S29GL064N is a 64-Mb device organized as 4,194,304 words or 8,388,608 bytes. The S29GL032N is a 32-Mb device organized as 2,097,152 words or 4,194,304 bytes. Depending on the model number, the devices have 16-bit wide data bus only, or a 16-bit wide data bus that can also function as an 8-bit wide data bus by using the BYTE# input. The devices can be programmed either in the host system or in standard EPROM programmers.

Access times as fast as 90 ns are available. Note that each access time has a specific operating voltage range (V_{CC}) as specified in the Product Selector Guide and the Ordering Information–S29GL032N, and Ordering Information–S29GL064N. Package offerings include 48-pin TSOP, 56-pin TSOP, 48-ball fine-pitch BGA and 64-ball Fortified BGA, depending on model number. Each device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Each device requires only a **single 3.0-Volt power supply** for both read and write functions. In addition to a V_{CC} input, a high-voltage **accelerated program (ACC)** feature provides shorter programming times through increased voltage on the WP#/ACC or ACC input. This feature is intended to facilitate factory throughput during system production, but may also be used in the field if desired.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the device using standard microprocessor write timing. Write cycles also internally latch addresses and data needed for the programming and erase operations.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

The **Advanced Sector Protection** features several levels of sector protection, which can disable both the program and erase operations in certain sectors. Persistent Sector Protection is a method that replaces the previous 12-volt controlled protection method. Password Sector Protection is a highly sophisticated protection method that requires a password before changes to certain sectors are permitted.

Device programming and erasure are initiated through command sequences. Once a program or erase operation begins, the host system need only poll the DQ7 (Data# Polling) or DQ6 (toggle) **status bits** or monitor the **Ready/Busy# (RY/BY#)** output to determine whether the operation is complete. To facilitate programming, an **Unlock Bypass** mode reduces command sequence overhead by requiring only two write cycles to program data instead of four.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature allows the host system to pause an erase operation in a given sector to read or program any other sector and then complete the erase operation. The **Program Suspend/Program Resume** feature enables the host system to pause a program operation in a given sector to read any other sector and then complete the program operation.

The **hardware RESET# pin** terminates any operation in progress and resets the device, after which it is then ready for a new operation. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the host system to read boot-up firmware from the Flash memory device.

The device reduces power consumption in the **standby mode** when it detects specific voltage levels on CE# and RESET#, or when addresses are stable for a specified period of time.

The **Write Protect (WP#)** feature protects the first or last sector by asserting a logic low on the WP#/ACC pin or WP# pin, depending on model number. The protected sector is still protected even during accelerated programming.

The **Secured Silicon Sector** provides a 128-word/256-byte area for code or data that can be permanently protected. Once this sector is protected, no further changes within the sector can occur.

Cypress MirrorBit flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via hot-hole assisted erase. The data is programmed using hot electron injection.

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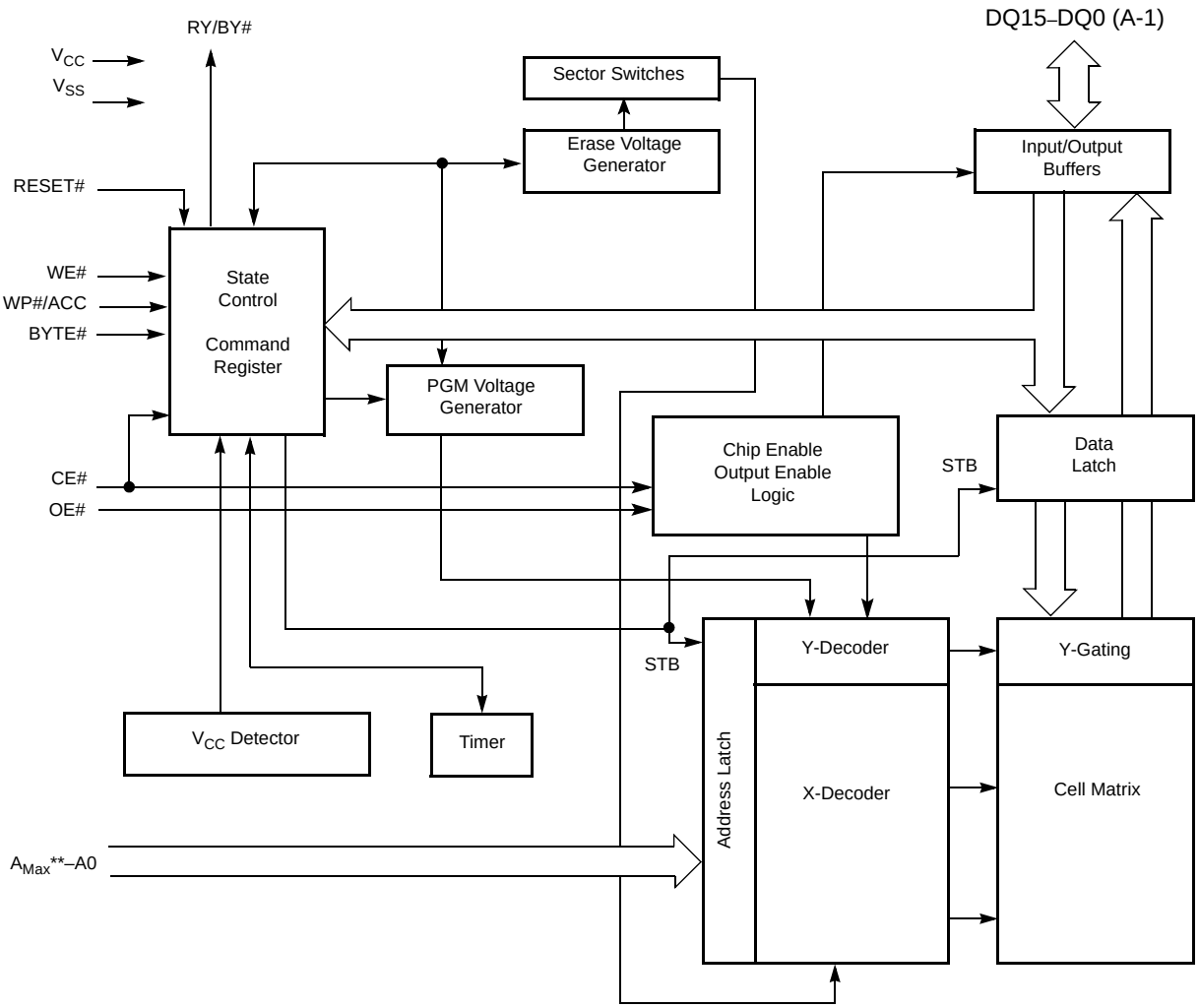
1. Product Selector Guide

Part Number			S29GL064N		S29GL032N	
Speed Option	V_{CC} = 2.7–3.6 V	V_{IO} = 2.7–3.6 V	**90**		**90**	
		V_{IO} = 1.65–3.6 V		**110**		**110**
Max. Access Time (ns)			90	110	90	110
Max. CE# Access Time (ns)			90	110	90	110
Max. Page Access Time (ns)			25	30	25	30
Max. OE# Access Time (ns)			25	30	25	30

2. Block Diagram



Note
***A_{MAX} GL064N = A21, GL032N = A20.*

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3. Connection Diagrams

Special Package Handling Instructions

Special handling is required for Flash Memory products in molded packages (TSOP and BGA). The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

Figure 1. 48-Pin Standard TSOP

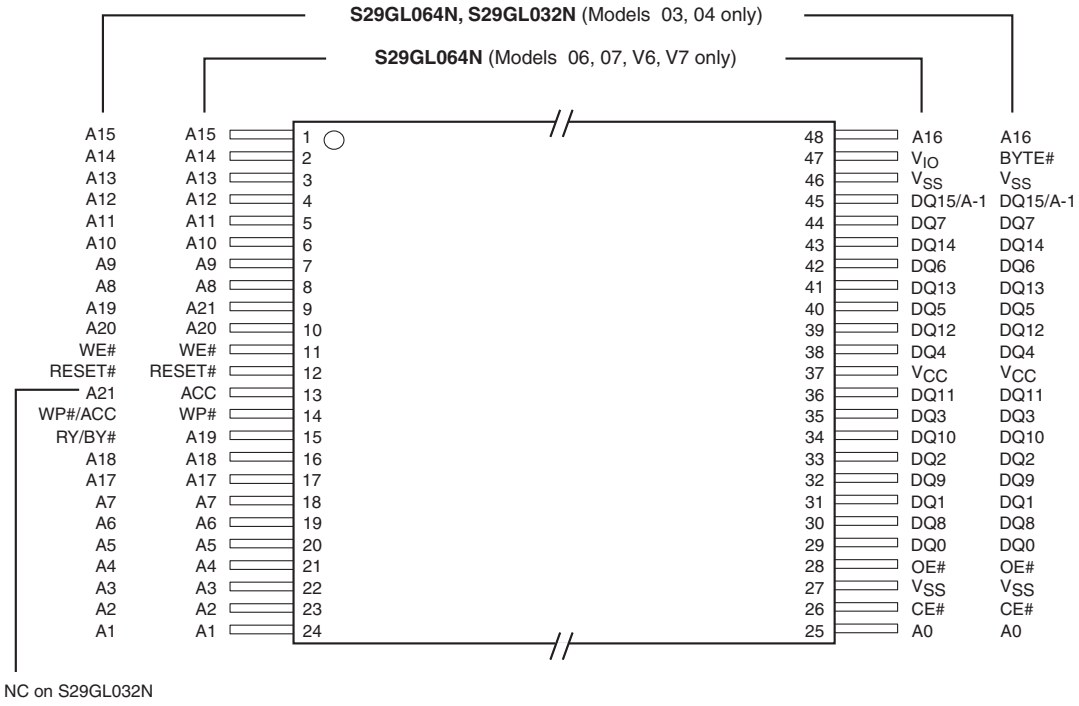

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Figure 2. 56-Pin Standard TSOP

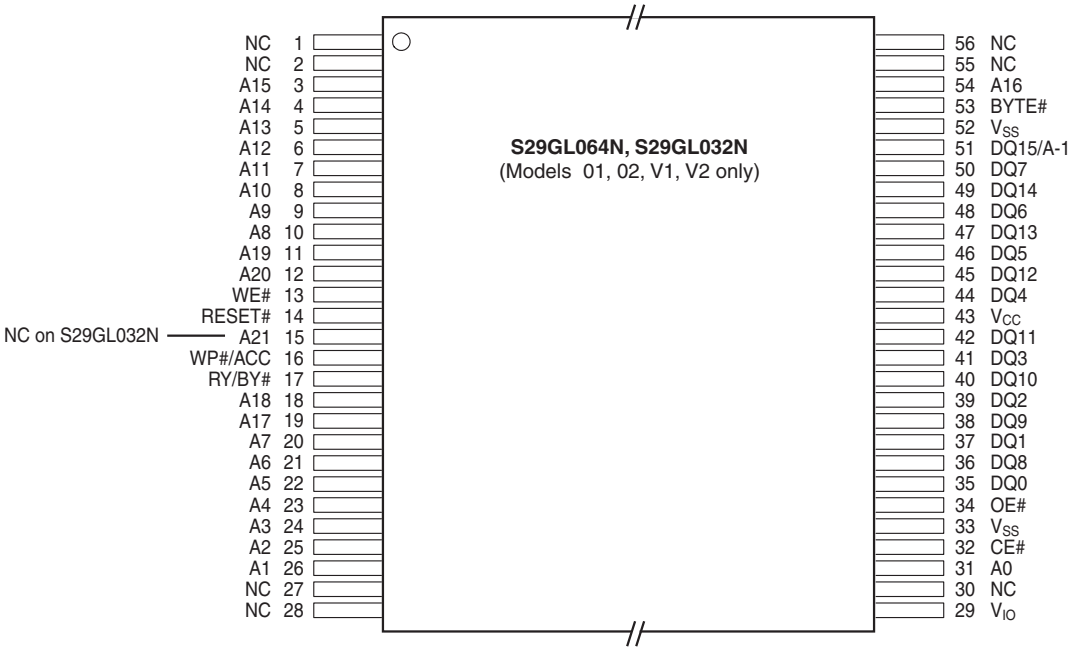

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Figure 3. 64-ball Fortified BGA

S29GL064N, S29GL032N (Models 01, 02, 03, 04, V1, V2 only)
Top View, Balls Facing Down

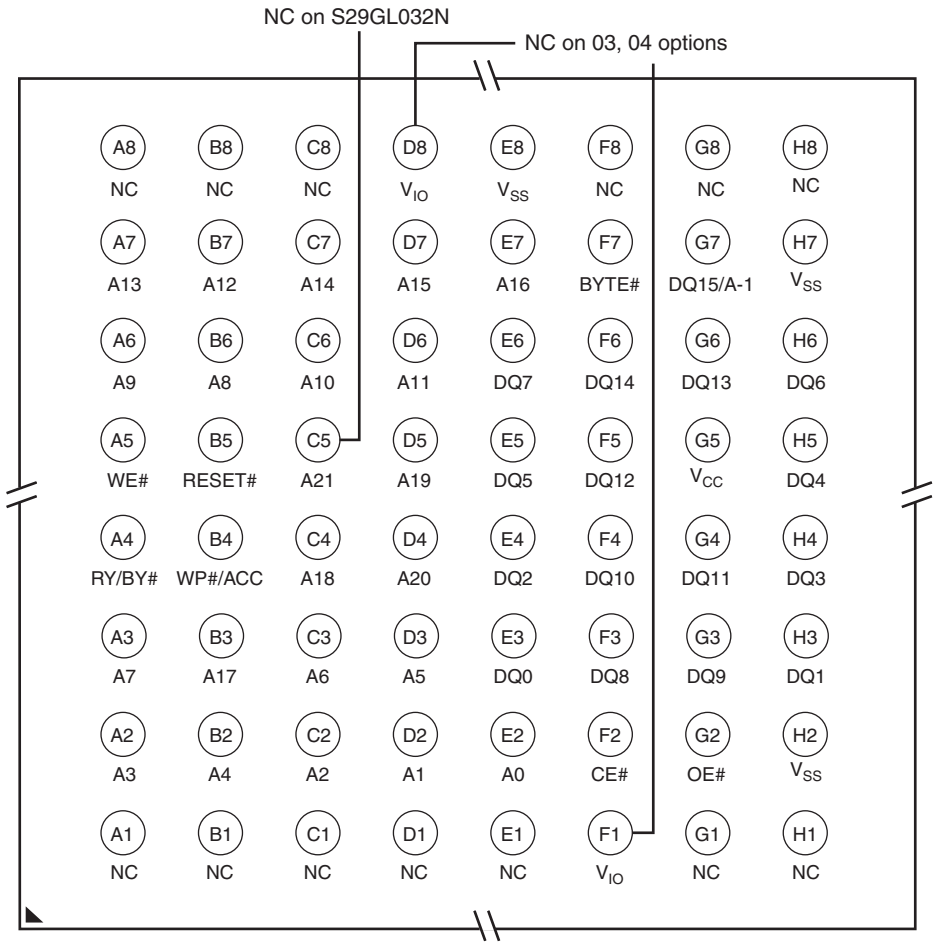

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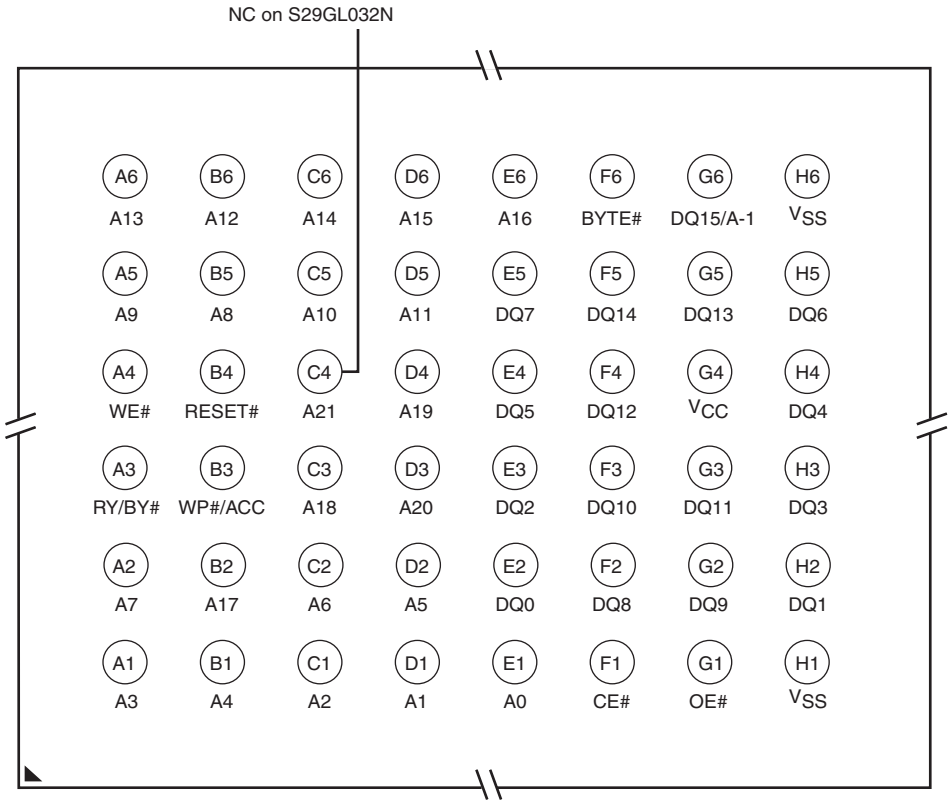
Figure 4. 48-ball Fine-pitch BGA (VBK 048)

S29GL064N, S29GL032N (Models 03, 04 only)
Top View, Balls Facing Down



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4. Pin Description

Pin	Description
A21–A0	22 Address inputs (S29GL064N)
A20–A0	21 Address inputs (S29GL032N)
DQ7–DQ0	8 Data inputs/outputs
DQ14–DQ0	15 Data inputs/outputs
DQ15/A-1	DQ15 (Data input/output, word mode), A-1 (LSB Address input, byte mode)
CE#	Chip Enable input
OE#	Output Enable input
WE#	Write Enable input
WP#/ACC	Hardware Write Protect input/Programming Acceleration input
ACC	Acceleration input
WP#	Hardware Write Protect input
RESET#	Hardware Reset Pin input
RY/BY#	Ready/Busy output
BYTE#	Selects 8-bit or 16-bit mode
V_{CC}	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{IO}	Output Buffer Power
V_{SS}	Device Ground
NC	Pin Not Connected Internally

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5. Logic Symbols

Figure 5. S29GL064N Logic Symbol (Models 01, 02, V1, V2)

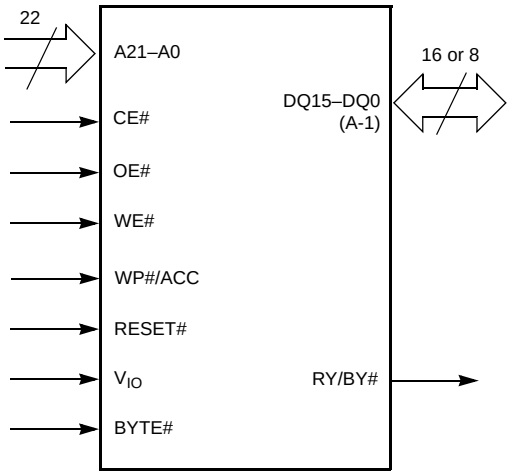

Figure 6. S29GL064N Logic Symbol (Models 03, 04)

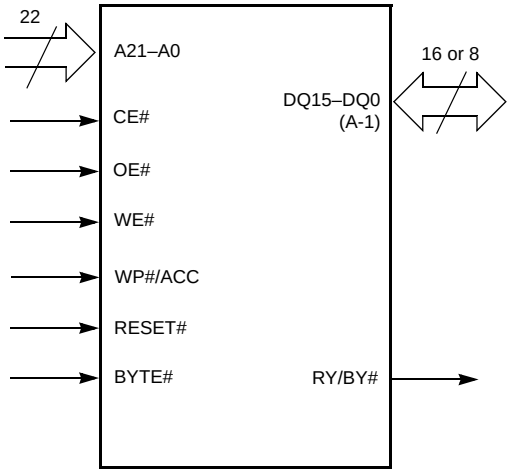

Figure 7. S29GL064N Logic Symbol (Models 06, 07, V6, V7)

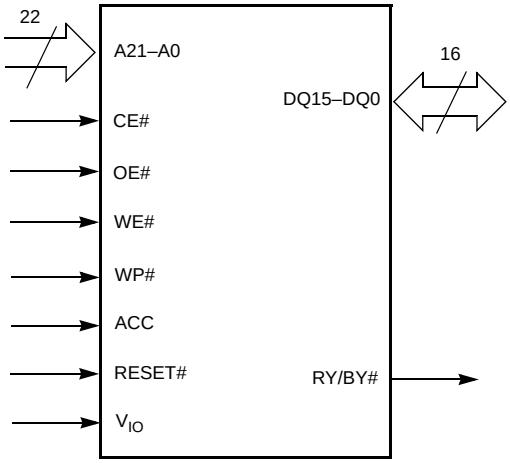

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Figure 8. S29GL032N Logic Symbol (Models 01, 02, V1, V2)

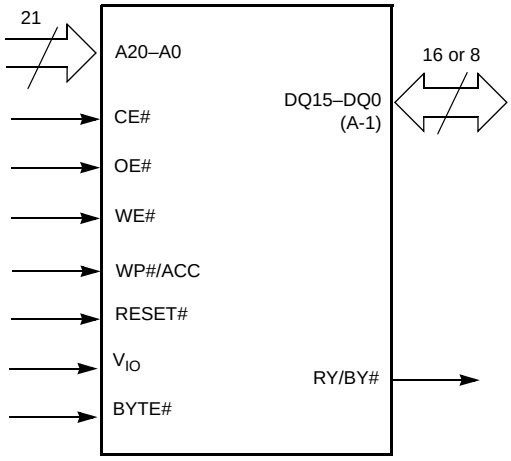
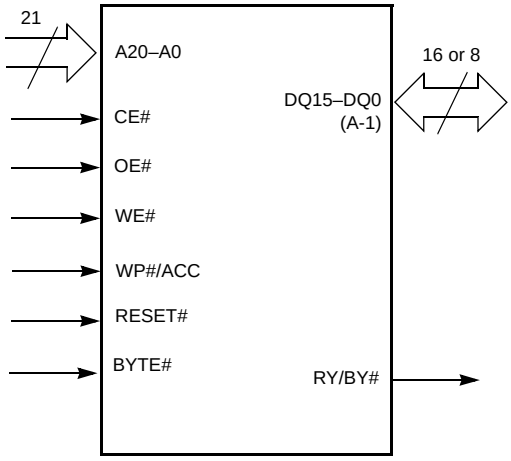


Figure 9. S29GL032N Logic Symbol (Models 03, 04)



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8.8 Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} on address pin A9. Address pins A6, A3, A2, A1, and A0 must be as shown in Table 10 on page 29. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 3 - Table 9). Table 10 shows the remaining address bits that are don't care. When all necessary bits are set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 17 on page 47 and Table 19 on page 50. This method does not require V_{ID}. Refer to the Autoselect Command Sequence section for more information.

Table 10. Autoselect Codes, (High Voltage Method)

Description		CE#	OE#	WE#	A_{max} to A15	A14 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	DQ8 to DQ15		DQ7 to DQ0		
															Model Number		
														BYTE# = V_{IH}	BYTE# = V_{IL}	01, 02 V1, V2	03, 04	06, 07, V6, V7
Manufacturer ID: Cypress Products		L	L	H	X	X	V_{ID}	X	L	X	L	L	L	00	X	01h	01h	01h
S29GL064N	Cycle 1	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22	X	7Eh	7Eh	7Eh
	Cycle 2										H	H	L	22	X	0Ch	10h	13h
	Cycle 3										H	H	H	22	X	01h	00h (04, bottom boot) 01h (03, top boot)	01h
S29GL032N	Cycle 1	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22	X	7Eh	7Eh	
	Cycle 2										H	H	L	22	X	1Dh	1Ah	
	Cycle 3										H	H	H	22	X	00h	00h (04, bottom boot) 01h (03, top boot)	
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	L	H	L	X	X	01h (protected), 00h (unprotected)		
Secured Silicon Sector Indicator Bit (DQ7), WP# protects highest address sector		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	X	For S29GL064N and S29GL032N: 9A (factory locked), 1A (not factory locked)		
Secured Silicon Sector Indicator Bit (DQ7), WP# protects lowest address sector		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	X	For S29GL064N and S29GL032N: 8A (factory locked), 0A (not factory locked)		

Legend
L = Logic Low = V_{IL}
H = Logic High = V_{IH}
SA = Sector Address
X = Don't care

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8.9 Advanced Sector Protection

The device features several levels of sector protection, which can disable both the program and erase operations in certain sectors:

8.9.1 Persistent Sector Protection

A command sector protection method that replaces the old 12 V controlled protection method.

8.9.2 Password Sector Protection

A highly sophisticated protection method that requires a password before changes to certain sectors are permitted

8.9.3 WP# Hardware Protection

A write protect pin that can prevent program or erase operations in the outermost sectors.

The WP# Hardware Protection feature is always available, independent of the software managed protection method chosen.

8.9.4 Selecting a Sector Protection Mode

All parts default to operate in the Persistent Sector Protection mode. The user must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which sector protection method is used. If the user decides to continue using the Persistent Sector Protection method, they must set the **Persistent Sector Protection Mode Locking Bit**. This permanently sets the part to operate only using Persistent Sector Protection. If the user decides to use the password method, they must set the **Password Mode Locking Bit**. This permanently sets the part to operate only using password sector protection.

It is important to remember that setting either the **Persistent Sector Protection Mode Locking Bit** or the **Password Mode Locking Bit** permanently selects the protection mode. It is not possible to switch between the two methods once a locking bit is set. **It is important that one mode is explicitly selected when the device is first programmed, rather than relying on the default mode alone.** This is so that it is not possible for a system program or virus to later set the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Protection Mode.

The device is shipped with all sectors unprotected. Cypress offers the option of programming and protecting sectors at the factory prior to shipping the device through the ExpressFlash™ Service. Contact your sales representative for details.

It is possible to determine whether a sector is protected or unprotected. See Autoselect Command Sequence on page 39 for details.

8.10 Lock Register

The Lock Register consists of 3 bits (DQ2, DQ1, and DQ0). These DQ2, DQ1, DQ0 bits of the Lock Register are programmable by the user. Users are not allowed to program both DQ2 and DQ1 bits of the Lock Register to the 00 state. If the user tries to program DQ2 and DQ1 bits of the Lock Register to the 00 state, the device aborts the Lock Register back to the default 11 state. The programming time of the Lock Register is same as the typical word programming time (t_{WHWH1}) without utilizing the Write Buffer of the device. During a Lock Register programming sequence execution, the DQ6 Toggle Bit I toggles until the programming of the Lock Register has completed to indicate programming status. All Lock Register bits are readable to allow users to verify Lock Register statuses.

The Customer Secured Silicon Sector Protection Bit is DQ0, Persistent Protection Mode Lock Bit is DQ1, and Password Protection Mode Lock Bit is DQ2 are accessible by all users. Each of these bits are non-volatile. DQ15-DQ3 are reserved and must be 1's when the user tries to program the DQ2, DQ1, and DQ0 bits of the Lock Register. The user is not required to program DQ2, DQ1 and DQ0 bits of the Lock Register at the same time. This allows users to lock the Secured Silicon Sector and then set the device either permanently into Password Protection Mode or Persistent Protection Mode and then lock the Secured Silicon Sector at separate instances and time frames.

- Secured Silicon Sector Protection allows the user to lock the Secured Silicon Sector area
- Persistent Protection Mode Lock Bit allows the user to set the device permanently to operate in the Persistent Protection Mode
- Password Protection Mode Lock Bit allows the user to set the device permanently to operate in the Password Protection Mode

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Table 11. Lock Register

DQ15-3	DQ2	DQ1	DQ0
Don't Care	Password Protection Mode Lock Bit	Persistent Protection Mode Lock Bit	Secured Silicon Sector Protection Bit

8.11 Persistent Sector Protection

The Persistent Sector Protection method replaces the old 12 V controlled protection method while at the same time enhancing flexibility by providing three different sector protection states.

Dynamically Locked	The sector is protected and can be changed by a simple command
Persistently Locked	A sector is protected and cannot be changed
Unlocked	The sector is unprotected and can be changed by a simple command

To achieve these states, three types of "bits" are used:

8.11.1 Dynamic Protection Bit (DYB)

A volatile protection bit is assigned for each sector. After power-up or hardware reset, the contents of all DYB bits are in the "unprotected state". Each DYB is individually modifiable through the DYB Set Command and DYB Clear Command. The DYB bits and *Persistent Protect Bits* (PPB) Lock bit are defaulted to power up in the cleared state or unprotected state - meaning the all PPB bits are changeable.

The Protection State for each sector is determined by the logical OR of the PPB and the DYB related to that sector. For the sectors that have the PPB bits cleared, the DYB bits control whether or not the sector is protected or unprotected. By issuing the DYB Set and DYB Clear command sequences, the DYB bits is protected or unprotected, thus placing each sector in the protected or unprotected state. These are the so-called Dynamic Locked or Unlocked states. They are called dynamic states because it is very easy to switch back and forth between the protected and un-protected conditions. This allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed.

The DYB bits maybe set or cleared as often as needed. The PPB bits allow for a more static, and difficult to change, level of protection. The PPB bits retain their state across power cycles because they are Non-Volatile. Individual PPB bits are set with a program command but must all be cleared as a group through an erase command.

The PPB Lock Bit adds an additional level of protection. Once all PPB bits are programmed to the desired settings, the PPB Lock Bit may be set to the "freeze state". Setting the PPB Lock Bit to the "freeze state" disables all program and erase commands to the Non-Volatile PPB bits. In effect, the PPB Lock Bit locks the PPB bits into their current state. The only way to clear the PPB Lock Bit to the "unfreeze state" is to go through a power cycle, or hardware reset. The Software Reset command does not clear the PPB Lock Bit to the "unfreeze state". System boot code can determine if any changes to the PPB bits are needed e.g. to allow new system code to be downloaded. If no changes are needed then the boot code can set the PPB Lock Bit to disable any further changes to the PPB bits during system operation.

The WP# write protect pin adds a final level of hardware protection. When this pin is low it is not possible to change the contents of the WP# protected sectors. These sectors generally hold system boot code. So, the WP# pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DYB Set command sequence is all that is necessary. The DYB Set and DYB Clear commands for the dynamic sectors switch the DYB bits to signify protected and unprotected, respectively. If there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock Bit must be disabled to the "unfreeze state" by either putting the device through a power-cycle, or hardware reset. The PPB bits can then be changed to reflect the desired settings. Setting the PPB Lock Bit once again to the "freeze state" locks the PPB bits, and the device operates normally again.

To achieve the best protection, execute the PPB Lock Bit Set command early in the boot code, and protect the boot code by holding WP# = V_{IL}.

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8.11.2 Persistent Protection Bit (PPB)

A single Persistent (non-volatile) Protection Bit is assigned to each sector. If a PPB is programmed to the protected state through the “PPB Program” command, that sector is protected from program or erase operations and is therefor read-only. If a PPB requires erasure, all of the sector PPB bits must first be erased in parallel through the “All PPB Erase” command. The “All PPB Erase” command preprograms all PPB bits prior to PPB erasing. All PPB bits erase in parallel, unlike programming where individual PPB bits are programmable. The PPB bits are limited to the same number of cycles as a flash memory sector.

Programming the PPB bit requires the typical word programming time without utilizing the Write Buffer. During a PPB bit programming and all PPB bit erasing sequence executions, the DQ6 Toggle Bit I toggles until the programming of the PPB bit or erasing of all PPB bits has completed to indicate programming and erasing status. Erasing all of the PPB bits at once requires typical sector erase time. During the erasing of all PPB bits, the DQ3 Sector Erase Timer bit outputs a 1 to indicate the erasure of all PPB bits are in progress. When the erasure of all PPB bits has completed, the DQ3 Sector Erase Timer bit outputs a 0 to indicate that all PPB bits have been erased. Reading the PPB Status bit requires the initial access time of the device.

8.11.3 Persistent Protection Bit Lock (PPB Lock Bit)

A global volatile bit. When set to the “freeze state”, the PPB bits cannot be changed. When cleared to the “unfreeze state”, the PPB bits are changeable. There is only one PPB Lock Bit per device. The PPB Lock Bit is cleared to the “unfreeze state” at power-up or hardware reset. There is no command sequence to unlock or “unfreeze” the PPB Lock Bit.

Configuring the PPB Lock Bit to the freeze state requires approximately 100ns. Reading the PPB Lock Status bit requires the initial access time (t_{ACC}) of the device.

Table 12. Sector Protection Schemes

Protection States			Sector State
DYB Bit	PPB Bit	PPB Lock Bit	
Unprotect	Unprotect	Unfreeze	Unprotected – PPB and DYB are changeable
Unprotect	Unprotect	Freeze	Unprotected – PPB not changeable, DYB is changeable
Unprotect	Protect	Unfreeze	Protected – PPB and DYB are changeable
Unprotect	Protect	Freeze	Protected – PPB not changeable, DYB is changeable
Protect	Unprotect	Unfreeze	Protected – PPB and DYB are changeable
Protect	Unprotect	Freeze	Protected – PPB not changeable, DYB is changeable
Protect	Protect	Unfreeze	Protected – PPB and DYB are changeable
Protect	Protect	Freeze	Protected – PPB not changeable, DYB is changeable

Table 12 contains all possible combinations of the DYB bit, PPB bit, and PPB Lock Bit relating to the status of the sector. In summary, if the PPB bit is set, and the PPB Lock Bit is set, the sector is protected and the protection cannot be removed until the next power cycle or hardware reset clears the PPB Lock Bit to “unfreeze state”. If the PPB bit is cleared, the sector can be dynamically locked or unlocked. The DYB bit then controls whether or not the sector is protected or unprotected. If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program command to a protected sector enables status polling for approximately 1 µs before the device returns to read mode without having modified the contents of the protected sector. An erase command to a protected sector enables status polling for approximately 50 µs after which the device returns to read mode without having erased the protected sector. The programming of the DYB bit, PPB bit, and PPB Lock Bit for a given sector can be verified by writing a DYB Status Read, PPB Status Read, and PPB Lock Status Read commands to the device.

The Autoselect Sector Protection Verification outputs the OR function of the DYB bit and PPB bit per sector basis. When the OR function of the DYB bit and PPB bit is a 1, the sector is either protected by DYB or PPB or both. When the OR function of the DYB bit and PPB bit is a 0, the sector is unprotected through both the DYB and PPB.

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8.12 Password Sector Protection

The Password Sector Protection method allows an even higher level of security than the Persistent Sector Protection method. There are two main differences between the Persistent Sector Protection and the Password Sector Protection methods:

- When the device is first powered on, or comes out of a reset cycle, the PPB Lock Bit is set to the locked state, or the freeze state, rather than cleared to the unlocked state, or the unfreeze state.
- The only means to clear and unfreeze the PPB Lock Bit is by writing a unique 64-bit Password to the device.

The Password Sector Protection method is otherwise identical to the Persistent Sector Protection method.

A 64-bit password is the only additional tool utilized in this method.

The password is stored in a one-time programmable (OTP) region outside of the flash memory. Once the Password Protection Mode Lock Bit is set, the password is permanently set with no means to read, program, or erase it. The password is used to clear and unfreeze the PPB Lock Bit. The Password Unlock command must be written to the flash, along with a password. The flash device internally compares the given password with the pre-programmed password. If they match, the PPB Lock Bit is cleared to the *unfreezed state*, and the PPB bits can be altered. If they do not match, the flash device does nothing. There is a built-in 2 µs delay for each *password check* after the valid 64-bit password is entered for the PPB Lock Bit to be cleared to the “unfreezed state”. This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password.

8.13 Password and Password Protection Mode Lock Bit

In order to select the Password Sector Protection method, the user must first program the password. Cypress recommends that the password be somehow correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Read operations. Once the desired password is programmed in, the customer must then set the Password Protection Mode Lock Bit. This operation achieves two objectives:

1. It permanently sets the device to operate using the Password Protection Mode. It is not possible to reverse this function.
2. It also disables all further commands to the password region. All program, and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Sector Protection method is desired when programming the Password Protection Mode Lock Bit. More importantly, the user must be sure that the password is correct when the Password Protection Mode Lock Bit is programmed. Due to the fact that read operations are disabled, there is no means to read what the password is afterwards. If the password is lost after programming the Password Protection Mode Lock Bit, there is no way to clear and unfreeze the PPB Lock Bit. The Password Protection Mode Lock Bit, once programmed, prevents reading the 64-bit password on the DQ bus and further password programming. The Password Protection Mode Lock Bit is not erasable. Once Password Protection Mode Lock Bit is programmed, the Persistent Protection Mode Lock Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

8.13.1 64-bit Password

The 64-bit Password is located in its own memory space and is accessible through the use of the Password Program and Password Read commands. The password function works in conjunction with the Password Protection Mode Lock Bit, which when programmed, prevents the Password Read command from reading the contents of the password on the pins of the device.

8.14 Persistent Protection Bit Lock (PPB Lock Bit)

A global volatile bit. The PPB Lock Bit is a volatile bit that reflects the state of the Password Protection Mode Lock Bit after power-up reset. If the Password Protection Mode Lock Bit is also programmed after programming the Password, the Password Unlock command must be issued to clear and unfreeze the PPB Lock Bit after a hardware reset (RESET# asserted) or a power-up reset. Successful execution of the Password Unlock command clears and unfreezes the PPB Lock Bit, allowing for sector PPB bits to be modified. Without issuing the Password Unlock command, while asserting RESET#, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit to a the “freeze state”.

If the Password Protection Mode Lock Bit is not programmed, the device defaults to Persistent Protection Mode. In the Persistent Protection Mode, the PPB Lock Bit is cleared to the *unfreeze state* after power-up or hardware reset. The PPB Lock Bit is set to the *freeze state* by issuing the PPB Lock Bit Set command. Once set to the *freeze state* the only means for clearing the PPB Lock Bit to the “unfreeze state” is by issuing a hardware or power-up reset. The Password Unlock command is ignored in Persistent Protection Mode.

Reading the PPB Lock Bit requires a 200 ns access time.

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8.15 Secured Silicon Sector Flash Memory Region

The Secured Silicon Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The Secured Silicon Sector is 256 bytes in length, and uses a Secured Silicon Sector Indicator Bit (DQ7) to indicate whether or not the Secured Silicon Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

The factory offers the device with the Secured Silicon Sector either customer lockable (standard shipping option) or factory locked (contact an AMD sales representative for ordering information). The customer-lockable version is shipped with the Secured Silicon Sector unprotected, allowing customers to program the sector after receiving the device. The customer-lockable version also has the Secured Silicon Sector Indicator Bit permanently set to a *0*. The factory-locked version is always protected when shipped from the factory, and has the Secured Silicon Sector Indicator Bit permanently set to a *1*. Thus, the Secured Silicon Sector Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked.

The Secured Silicon sector address space in this device is allocated as follows:

Secured Silicon Sector Address Range	Customer Lockable	ESN Factory Locked	ExpressFlash Factory Locked
000000h–000007h	Determined by customer	ESN	ESN or determined by customer
000008h–00007Fh		Unavailable	Determined by customer

The system accesses the Secured Silicon Sector through a command sequence (see Write Protect (WP#/ACC) on page 35). After the system has written the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the addresses normally occupied by the first sector (SA0). This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to sector SA0.

8.15.1 Customer Lockable: Secured Silicon Sector NOT Programmed or Protected At the Factory

Unless otherwise specified, the device is shipped such that the customer may program and protect the 256-byte Secured Silicon sector.

The system may program the Secured Silicon Sector using the write-buffer, accelerated and/or unlock bypass methods, in addition to the standard programming command sequence. See Command Definitions on page 39.

Programming and protecting the Secured Silicon Sector must be used with caution since, once protected, there is no procedure available for unprotecting the Secured Silicon Sector area and none of the bits in the Secured Silicon Sector memory space can be modified in any way.

The Secured Silicon Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter Secured Silicon Sector Region command.
- To verify the protect/unprotect status of the Secured Silicon Sector, follow the algorithm.

Once the Secured Silicon Sector is programmed, locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return to reading and writing within the remainder of the array.

8.15.2 Factory Locked: Secured Silicon Sector Programmed and Protected At the Factory

In devices with an ESN, the Secured Silicon Sector is protected when the device is shipped from the factory. The Secured Silicon Sector cannot be modified in any way. An ESN Factory Locked device has an 16-byte random ESN at addresses 000000h–000007h. Please contact your sales representative for details on ordering ESN Factory Locked devices.

Customers may opt to have their code programmed by the factory through the ExpressFlash service (Express Flash Factory Locked). The devices are then shipped from the factory with the Secured Silicon Sector permanently locked. Contact your sales representative for details on using the ExpressFlash service.

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8.16 Write Protect (WP#/ACC)

The Write Protect function provides a hardware method of protecting the first or last sector without using V_{ID}. Write Protect is one of two functions provided by the WP#/ACC input.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the first or last sector independently of whether those sectors were protected or unprotected. Note that if WP#/ACC is at V_{IL} when the device is in the standby mode, the maximum input load current is increased. See the table in DC Characteristics on page 58.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether the first or last sector was previously set to be protected or unprotected using the method described in Advanced Sector Protection on page 30. *Note that WP#/ACC contains an internal pull-up; when unconnected, WP#/ACC is at V_{IH}.*

8.17 Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 17 on page 47 and Table 19 on page 50 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

8.17.1 Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

8.17.2 Write Pulse *Glitch* Protection

Noise pulses of less than 3 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

8.17.3 Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

8.17.4 Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

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9. Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 13 on page 36 – Table 16 on page 38. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Table 13 on page 36 – Table 16 on page 38. The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100. Alternatively, contact your sales representative for copies of these documents.

Table 13. CFI Query Identification String

Addresses (x16)	Addresses (x8)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 14. System Interface String

Addresses (x16)	Addresses (x8)	Data	Description
1Bh	36h	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	38h	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	3Ah	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	3Eh	0007h	Reserved for future use
20h	40h	0007h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	42h	000Ah	Typical timeout per individual block erase 2^N ms
22h	44h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0003h	Max. timeout for byte/word program 2^N times typical.
24h	48h	0005h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0004h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Note

CFI data related to V_{CC} and time-outs may differ from actual V_{CC} and time-outs of the product. Please consult the Ordering Information tables to obtain the V_{CC} range for particular part numbers. Please consult the Erase and Programming Performance table for typical timeout specifications.

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Table 15. Device Geometry Definition

Addresses (x16)	Addresses (x8)	Data	Description
27h	4Eh	00xxh	Device Size = 2^N byte 0017h = 64 Mb, 0016h = 32 Mb
28h 29h	50h 52h	000xh 0000h	Flash Device Interface description (refer to CFI publication 100) 0001h = x16-only bus devices 0002h = x8/x16 bus devices
2Ah 2Bh	54h 56h	0005h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	00xxh	Number of Erase Block Regions within device (01h = uniform device, 02h = boot device)
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	00xxh 000xh 00x0h 000xh	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100) 007Fh, 0000h, 0000h, 0001h = 64 Mb (01, 02, 06, 07, V1, V2, V6, V7) 0007h, 0000h, 0020h, 0000h = 64 Mb (03, 04) 003Fh, 0000h, 0000h, 0001h = 32 Mb (01, 02, V1, V2) 0007h, 0000h, 0020h, 0000h = 32 Mb (03, 04)
31h 32h 33h 34h	60h 64h 66h 68h	00xxh 0000h 0000h 000xh	Erase Block Region 2 Information (refer to CFI publication 100) 0000h, 0000h, 0000h, 0000h = 64 Mb (01, 02, 06, 07, V1, V2, V6, V7) 007Eh, 0000h, 0000h, 0001h = 64 Mb (03, 04) 0000h, 0000h, 0000h, 0000h = 32 Mb (01, 02, V1, V2) 003Eh, 0000h, 0000h, 0001h = 32 Mb (03, 04)
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information (refer to CFI publication 100)
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to CFI publication 100)

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Table 16. Primary Vendor-Specific Extended Query

Addresses (x16)	Addresses (x8)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII
44h	88h	0033h	Minor version number, ASCII
45h	8Ah	00xxh	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Process Technology (Bits 7-2) 0100b = 110 nm MirrorBit 0011h = x8-only bus devices 0010h = all other devices
46h	8Ch	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	8Eh	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in smallest sector
48h	90h	0000h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	92h	0008h	Sector Protect/Unprotect scheme 0008h = Advanced sector Protection
4Ah	94h	0000h	Simultaneous Operation 00 = Not Supported, X = Number of Sectors in Bank
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	98h	0002h	Page Mode Type 02 = 8 Word Page
4Dh	9Ah	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	9Ch	00C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	9Eh	00xxh	Top/Bottom Boot Sector Flag 02h = Bottom Boot Device, 03h = Top Boot Device, 04h = Uniform sectors bottom WP# protect, 05h = Uniform sectors top WP# protect
50h	A0h	0001h	Program Suspend 00h = Not Supported, 01h = Supported

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10. Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table 17 on page 47 and Table 19 on page 50 define the valid register command sequences. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state.* A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the AC Characteristics section for timing diagrams.

10.1 Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See Erase Suspend/Erase Resume Commands on page 46 for more information.

The system *must* issue the reset command to return the device to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the device is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Reading Array Data in the Device Bus Operations section for more information. The Read-Only Operations–AC Characteristics on page 61 provide the read parameters, and Figure 21 on page 62 shows the timing diagram.

10.2 Reset Command

Writing the reset command resets the device to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to the read mode. If the program command sequence is written while the device is in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If the device entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to the read mode (or erase-suspend-read mode if the device was in Erase Suspend).

Note that if DQ1 goes high during a Write Buffer Programming operation, the system must write the Write-to-Buffer-Abort Reset command sequence to reset the device for the next operation.

10.3 Autoselect Command Sequence

The autoselect command sequence allows the host system to read several identifier codes at specific addresses.

Identifier Code	A7:A0 (x16)	A6:A-1 (x8)
Manufacturer ID	00h	00h
Device ID, Cycle 1	01h	02h
Device ID, Cycle 2	0Eh	1Ch
Device ID, Cycle 3	0Fh	1Eh
Secured Silicon Sector Factory Protect	03h	06h
Sector Protect Verify	(SA)02h	(SA)04h

Note
The device ID is read over three cycles. SA = Sector Address

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The autoselect command sequence is initiated by first writing on unlock cycle (two cycles). This is followed by a third write cycle that contains the autoselect command. The device then enters the autoselect mode. The system may read at any address any number of times without initiating another autoselect command sequence:

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the device was previously in Erase Suspend).

10.4 Enter/Exit Secured Silicon Sector Command Sequence

The Secured Silicon Sector region provides a secured data area containing an 8-word/16-byte random Electronic Serial Number (ESN). The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence. The Exit Secured Silicon Sector command sequence returns the device to normal operation. Table 17 on page 47 and Table 19 on page 50 show the address and data requirements for both command sequences. See also Secured Silicon Sector Flash Memory Region on page 34 for further information. *Note that the ACC function and unlock bypass modes are not available when the Secured Silicon Sector is enabled.*

10.4.1 Word Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 17 on page 47 and Table 19 on page 50 show the address and data requirements for the word program command sequence, respectively.

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. Refer to the Write Operation Status section for information on these status bits. Any commands written to the device during the Embedded Program Algorithm are ignored. *Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when a program operation is in progress.* Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once the device returns to the read mode, to ensure data integrity.

Programming is allowed in any sequence of address locations and across sector boundaries. Programming to the same word address multiple times without intervening erases (incremental bit programming) requires a modified programming method. For such application requirements, please contact your local Cypress representative. Word programming is supported for backward compatibility with existing Flash driver software and for occasional writing of individual words. Use of write buffer programming (see below) is strongly recommended for general programming use when more than a few words are to be programmed. The effective word programming time using write buffer programming is approximately four times shorter than the single word programming time.

Any bit in a word cannot be programmed from *0* back to a *1*. Attempting to do so may cause the device to set DQ5=1, or cause DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read shows that the data is still *0*. Only erase operations can convert a *0* to a *1*.

10.4.2 Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass mode command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 17 on page 47 and Table 19 on page 50 show the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h. The second cycle must contain the data 00h. The device then returns to the read mode.

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10.4.3 Write Buffer Programming

Write Buffer Programming allows the system write to a maximum of 16 words/32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the Sector Address in which programming occurs. The fourth cycle writes the sector address and the number of word locations, minus one, to be programmed. For example, if the system programs six unique address locations, then 05h should be written to the device. This tells the device how many write buffer addresses are loaded with data and therefore when to expect the Program Buffer to Flash command. The number of locations to program cannot exceed the size of the write buffer or the operation aborts.

The fifth cycle writes the first address location and data to be programmed. The write-buffer-page is selected by address bits A_{MAX}–A_4. All subsequent address/data pairs must fall within the selected-write-buffer-page. The system then writes the remaining address/data pairs into the write buffer. Write buffer locations may be loaded in any order.

The write-buffer-page address must be the same for all address/data pairs loaded into the write buffer. (This means Write Buffer Programming cannot be performed across multiple write-buffer pages.) This also means that Write Buffer Programming cannot be performed across multiple sectors. If the system attempts to load programming data outside of the selected write-buffer page, the operation aborts.

Note that if a Write Buffer address location is loaded multiple times, the address/data pair counter is decremented for every data load operation. The host system must therefore account for loading a write-buffer location more than once. The counter decrements for each data load operation, not for each unique write-buffer-address location. Note also that if an address location is loaded more than once into the buffer, the final data loaded for that address is programmed.

Once the specified number of write buffer locations are loaded, the system must then write the Program Buffer to Flash command at the sector address. Any other address and data combination aborts the Write Buffer Programming operation. The device then begins programming. Data polling should be used while monitoring the last address location loaded into the write buffer. DQ7, DQ6, DQ5, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer programming operation can be suspended using the standard program suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device is ready to execute the next command.

The Write Buffer Programming Sequence can be aborted in the following ways:

- Load a value that is greater than the page buffer size during the Number of Locations to Program step.
- Write to an address in a sector different than the one specified during the Write-Buffer-Load command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the Starting Address during the write buffer data loading stage of the operation.
- Write data other than the Confirm Command after the specified number of data load cycles.

The abort condition is indicated by DQ1 = *1*, DQ7 = DATA# (for the last address location loaded), DQ6 = toggle, and DQ5= *0*. A Write-to-Buffer-Abort Reset command sequence must be written to reset the device for the next operation.

Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when a program operation is in progress. This flash device is capable of handling multiple write buffer programming operations on the same write buffer address range without intervening erases. For applications requiring incremental bit programming, a modified programming method is required; please contact your local Cypress representative. **Any bit in a write buffer address range cannot be programmed from *0* back to a *1*.** Attempting to do so may cause the device to set DQ5=1, of cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read shows that the data is still *0*. Only erase operations can convert a *0* to a *1*.

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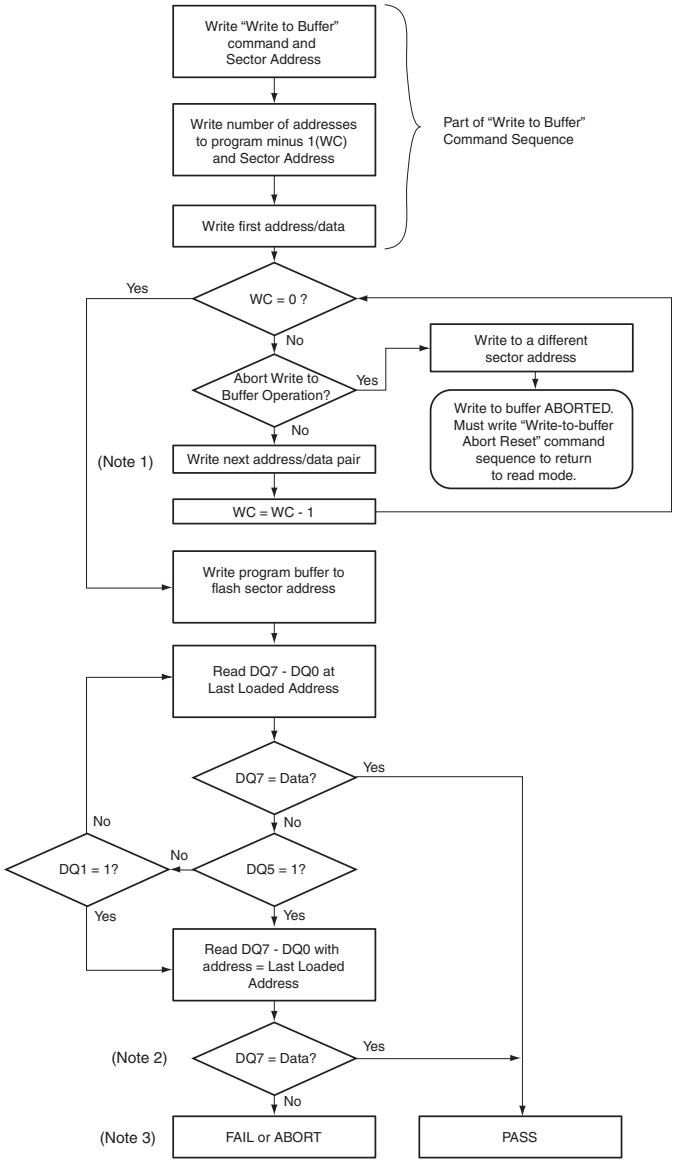
10.4.4 Accelerated Program

The device offers accelerated program operations through the WP#/ACC or ACC pin depending on the particular product. When the system asserts V_{HH} on the WP#/ACC or ACC pin. The device uses the higher voltage on the WP#/ACC or ACC pin to accelerate the operation. *Note that the* WP#/*ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. WP# contains an internal pull-up; when unconnected, WP# is at V_{IH}.*

Figure 10 on page 42 illustrates the algorithm for the program operation. Refer to the Erase and Program Operations–AC Characteristics on page 61 for parameters, and Figure 22 on page 62 for timing diagrams.

Figure 10. Write Buffer Programming Operation



Notes

1. *When Sector Address is specified, any address in the selected sector is acceptable. However, when loading Write-Buffer address locations with data, all addresses must fall within the selected Write-Buffer Page.*
2. *DQ7 may change simultaneously with DQ5. Therefore, DQ7 should be verified.*
3. *If this flowchart location was reached because DQ5= 1, then the device FAILED. If this flowchart location was reached because DQ1= 1, then the Write to Buffer operation was ABORTED. In either case, the proper reset command must be written before the device can begin another operation. If DQ1= 1, write the Write-Buffer-Programming-Abort-Reset command. if DQ5= 1, write the Reset command.*
4. *See Table 17 on page 47 and Table 19 on page 50 for command sequences required for write buffer programming.*

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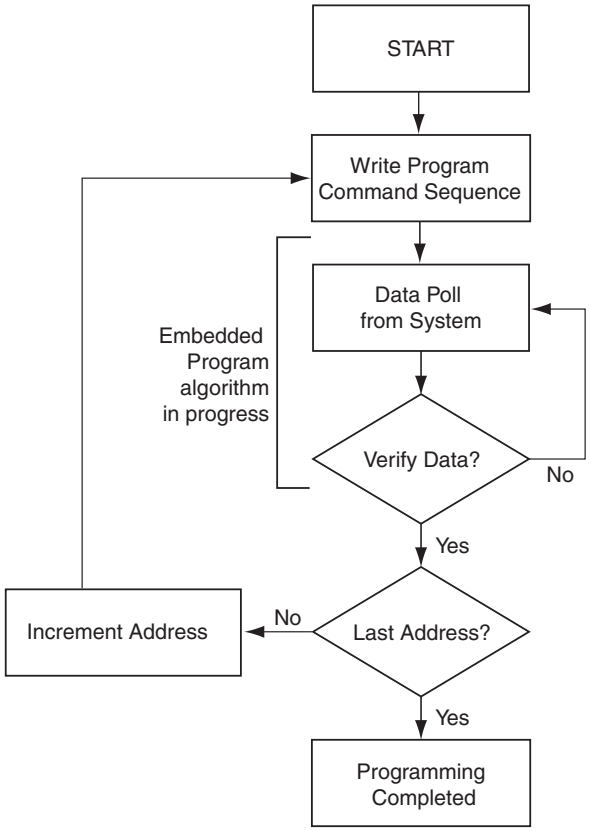
Figure 11. Program Operation



Note
See Table 17 on page 47 and Table 19 on page 50 for program command sequence.

10.5 Program Suspend/Program Resume Command Sequence

The Program Suspend command allows the system to interrupt a programming operation or a Write to Buffer programming operation so that data can be read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the program operation within 20 μs maximum and updates the status bits. Addresses are not required when writing the Program Suspend command.

After the programming operation is suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the Secured Silicon Sector area (One-time Program area), then user must use the proper command sequences to enter and exit this region. Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when a program operation is in progress.

The system may also write the autoselect command sequence when the device is in the Program Suspend mode. The system can read as many autoselect codes as required. When the device exits the autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See Autoselect Command Sequence on page 39 for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See Write Operation Status on page 52 for more information.

The system must write the Program Resume command (address bits are don't care) to exit the Program Suspend mode and continue the programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device resumes programming.

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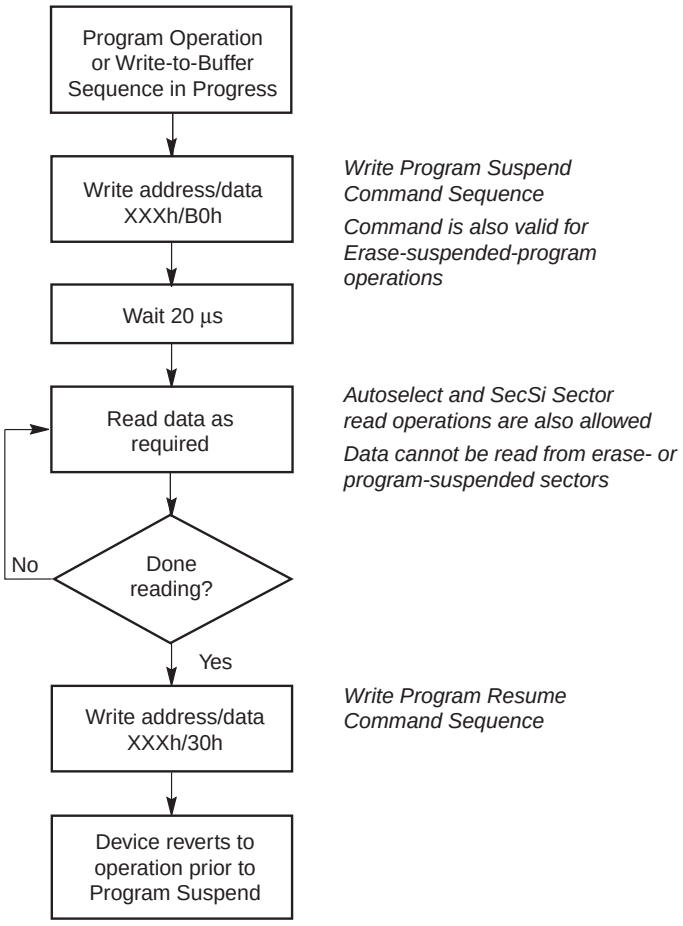
Figure 12. Program Suspend/Program Resume



10.6 Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 17 on page 47 and Table 19 on page 50 show the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, the device returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. Refer to Write Operation Status on page 52 for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If this occurs, the chip erase command sequence should be reinitiated once the device returns to reading array data, to ensure data integrity.

Figure 13 on page 45 illustrates the algorithm for the erase operation. Refer to Table 27 on page 64 for parameters, and Figure 26 on page 66 for timing diagrams.

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10.7 Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 17 on page 47 and Table 19 on page 50 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to the read mode. *Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when an erase operation is in progress.*** The system must rewrite the command sequence and any additional addresses and commands.

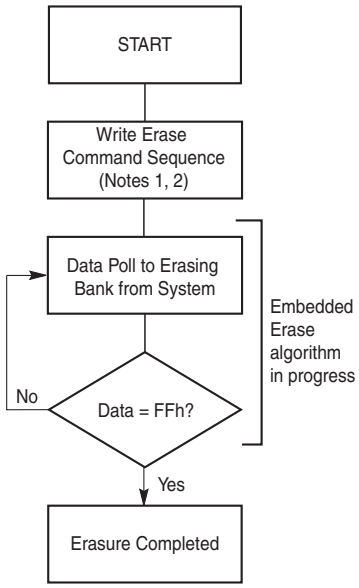
The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by reading DQ7, DQ6, or DQ2 in the erasing sector. Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation begins, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once the device returns to reading array data, to ensure data integrity.

Figure 13 on page 45 illustrates the algorithm for the erase operation. Refer to Table 27 on page 64 for parameters, and Figure 26 on page 66 for timing diagrams.

Figure 13. Erase Operation



Notes

1. *See Table 17 and Table 19 for program command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

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10.8 Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a typical of 5 µs (maximum of 20 µs) to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation is suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device *erase suspends* all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to Write Operation Status on page 52 for information on these status bits.

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard word program operation. Refer to Write Operation Status on page 52 for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the Autoselect Mode on page 29 and Autoselect Command Sequence on page 39 sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip resumes erasing.

During an erase operation, this flash device performs multiple internal operations which are invisible to the system. When an erase operation is suspended, any of the internal operations that were not fully completed must be restarted. As such, if this flash device is continually issued suspend/resume commands in rapid succession, erase progress is impeded as a function of the number of suspends. The result is a longer cumulative erase time than without suspends. Note that the additional suspends do not affect device reliability or future performance. In most systems rapid erase/suspend activity occurs only briefly. In such cases, erase performance is not significantly impacted.

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10.9 Command Definitions

Table 17. Command Definitions (x16 Mode, BYTE# = V_{IH})

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
Read (Note 5)		1	RA	RD										
Reset (Note 6)		1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	0001				
	Device ID (Note 8)	6	555	AA	2AA	55	555	90	X01	227E	X0E	(Note 18)	X0F	(Note 18)
	Device ID	4	555	AA	2AA	55	555	90	X01	(Note 17)				
	Secured Silicon Sector Factory Protect	4	555	AA	2AA	55	555	90	X03	(Note 9)				
	Sector Protect Verify (Note 10)	4	555	AA	2AA	55	555	90	(SA)X02	00/01				
Enter Secured Silicon Sector Region		3	555	AA	2AA	55	555	88						
Exit Secured Silicon Sector Region		4	555	AA	2AA	55	555	90	XXX	00				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Write to Buffer (Note 11)		3	555	AA	2AA	55	SA	25	SA	WC	PA	PD	WBL	PD
Program Buffer to Flash		1	SA	29										
Write to Buffer Abort Reset (Note 12)		3	555	AA	2AA	55	555	F0						
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (Note 13)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 14)		2	XXX	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Program/Erase Suspend (Note 15)		1	XXX	B0										
Program/Erase Resume (Note 16)		1	XXX	30										
CFI Query (Note 17)		1	55	98										

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Legend

X = Don't care

RA = Read Address of memory location to be read.

RD = Read Data read from location RA during read operation.

PA = Program Address. Addresses latch on falling edge of WE# or CE# pulse, whichever happens later.

PD = Program Data for location PA. Data latches on rising edge of WE# or CE# pulse, whichever happens first.

SA = Sector Address of sector to be verified (in autoselect mode) or erased. Address bits A21–A15 uniquely select any sector.

WBL = Write Buffer Location. Address must be within same write buffer page as PA.

WC = Word Count. Number of write buffer locations to load minus 1.

Notes

1. *See Table 2 on page 16 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells indicate read cycles. All others are write cycles.*
4. *During unlock and command cycles, when lower address bits are 555 or 2AA as shown in table, address bits above A11 and data bits above DQ7 are don't care.*
5. *No unlock or command cycles required when device is in read mode.*
6. *Reset command is required to return to read mode (or to erase-suspend-read mode if previously in Erase Suspend) when device is in autoselect mode, or if DQ5 goes high while device is providing status information.*
7. *Fourth cycle of the autoselect command sequence is a read cycle. Data bits DQ15–DQ8 are don't care. Except for RD, PD and WC. See Autoselect Command Sequence on page 39 for more information.*
8. *For S29GL064N and S29GL032N, Device ID must be read in three cycles.*
9. *Refer to Table 10 on page 29 for data indicating Secured Silicon Sector factory protect status.*
10. *Data is 00h for an unprotected sector and 01h for a protected sector.*
11. *Total number of cycles in command sequence is determined by number of words written to write buffer. Maximum number of cycles in command sequence is 21, including* Program Buffer to Flash *command.*
12. *Command sequence resets device for next command after aborted write-to-buffer operation.*
13. *Unlock Bypass command is required prior to Unlock Bypass Program command.*
14. *Unlock Bypass Reset command is required to return to read mode when device is in unlock bypass mode.*
15. *System may read and program in non-erasing sectors, or enter autoselect mode, when in Erase Suspend mode. Erase Suspend command is valid only during a sector erase operation.*
16. *Erase Resume command is valid only during Erase Suspend mode.*
17. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
18. *Refer to Table 10 on page 29, for individual Device IDs per device density and model number.*

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Table 18. Sector Protection Commands (x16)

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 2–4)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Lock Register Bits	Command Set Entry (Note 5)	3	555	AA	2AA	55	555	40								
	Program (Note 6)	2	XX	A0	XXX	Data										
	Read (Note 6)	1	00	Data												
	Command Set Exit (Note 7)	2	XX	90	XX	00										
Password Protection	Command Set Entry (Note 5)	3	555	AA	2AA	55	555	60								
	Program (Note 8)	2	XX	A0	PWAx	PWDx										
	Read (Note 9)	4	XXX	PWD0	01	PWD1	02	PWD2	03	PWD3						
	Unlock (Note 10)	7	00	25	00	03	00	PWD0	01	PWD1	02	PWD2	03	PWD3	00	29
	Command Set Exit (Note 7)	2	XX	90	XX	00										
Non-Volatile Sector Protection (PPB)	Command Set Entry (Note 5)	3	555	AA	2AA	55	555	C0								
	PPB Program (Note 11)	2	XX	A0	SA	00										
	All PPB Erase (Notes 11, 12)	2	XX	80	00	30										
	PPB Status Read	1	SA	RD(0)												
	Command Set Exit (Note 7)	2	XX	90	XX	00										
Global Volatile Sector Protection Freeze (PPB Lock)	Command Set Entry (Note 5)	3	555	AA	2AA	55	555	50								
	PPB Lock Bit Set	2	XX	A0	XX	00										
	PPB Lock Bit Status Read	1	XXX	RD(0)												
	Command Set Exit (Note 7)	2	XX	90	XX	00										
Volatile Sector Protection (DYB)	Command Set Entry (Note 5)	3	555	AA	2AA	55	555	E0								
	DYB Set	2	XX	A0	SA	00										
	DYB Clear	2	XX	A0	SA	01										
	DYB Status Read	1	SA	RD(0)												
	Command Set Exit (Note 7)	2	XX	90	XX	00										

Legend

X = Don't care.

RA = Address of the memory location to be read.

SA = Sector Address. Any address that falls within a specified sector. See Tables 3–9 for sector address ranges.

PWA = Password Address. Address bits A1 and A0 are used to select each 16-bit portion of the 64-bit entity.

PWD = Password Data.

RD(0) = DQ0 protection indicator bit. If protected, DQ0 = 0. If unprotected, DQ0 = 1.

Notes

1. *All values are in hexadecimal.*
2. *Shaded cells indicate read cycles.*
3. *Address and data bits not specified in table, legend, or notes are don't cares (each hex digit implies 4 bits of data).*
4. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.*
5. *Entry commands are required to enter a specific mode to enable instructions only available within that mode.*
6. *No unlock or command cycles required when bank is reading array data.*
7. *Exit command must be issued to reset the device into read mode; device may otherwise be placed in an unknown state.*
8. *Entire two bus-cycle sequence must be entered for each portion of the password.*
9. *Full address range is required for reading password.*
10. *Password may be unlocked or read in any order. Unlocking requires the full password (all seven cycles).*
11. *ACC must be at V_{IH} when setting PPB or DYB.*
12. *"All PPB Erase" command pre-programs all PPBs before erasure to prevent over-erasure.*

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Table 19. Command Definitions (x8 Mode, BYTE# = V_{IL})

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)		1	RA	RD										
Reset (Note 7)		1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	4	AAA	AA	555	55	AAA	90	X00	01				
	Device ID (Note 9)	6	AAA	AA	555	55	AAA	90	X02	7E	X1C	(Note 17)	X1E	(Note 17)
	Device ID	4	AAA	AA	555	55	AAA	90	X02	(Note 10)				
	Secured Silicon Sector Factory Protect	4	AAA	AA	555	55	AAA	90	X06					
	Sector Protect Verify (Note 11)	4	AAA	AA	555	55	AAA	90	(SA)X04	00/01				
Enter Secured Silicon Sector Region		3	AAA	AA	555	55	AAA	88						
Exit Secured Silicon Sector Region		4	AAA	AA	555	55	AAA	90	XXX	00				
Program		4	AAA	AA	555	55	AAA	A0	PA	PD				
Write to Buffer (Note 12)		3	AAA	AA	555	55	SA	25	SA	BC	PA	PD	WBL	PD
Program Buffer to Flash		1	SA	29										
Write to Buffer Abort Reset (Note 13)		3	AAA	AA	555	55	AAA	F0						
Chip Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Sector Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
Unlock Bypass			AAA	AA	555	55	AAA	20						
Unlock Bypass Program			XXX	A0	PA	PD								
Unlock Bypass RESET			XXX	90	XXX	00								
Program/Erase Suspend (Note 14)		1	XXX	B0										
Program/Erase Resume (Note 15)		1	XXX	30										
CFI Query (Note 16)		1	AA	98										

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Legend

X = Don't care

RA = Read Address of memory location to be read.

RD = Read Data read from location RA during read operation.

PA = Program Address. Addresses latch on falling edge of WE# or CE# pulse, whichever happens later.

PD = Program Data for location PA. Data latches on rising edge of WE# or CE# pulse, whichever happens first.

SA = Sector Address of sector to be verified (in autoselect mode) or erased. Address bits A21–A15 uniquely select any sector.

WBL = Write Buffer Location. Address must be within same write buffer page as PA.

BC = Byte Count. Number of write buffer locations to load minus 1.

Notes

1. *See Table 2 on page 16 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells indicate read cycles. All others are write cycles.*
4. *During unlock and command cycles, when lower address bits are 555 or AAA as shown in table, address bits above A11 are don't care.*
5. *Unless otherwise noted, address bits A21–A11 are don't cares.*
6. *No unlock or command cycles required when device is in read mode.*
7. *Reset command is required to return to read mode (or to erase-suspend-read mode if previously in Erase Suspend) when device is in autoselect mode, or if DQ5 goes high while device is providing status information.*
8. *Fourth cycle of autoselect command sequence is a read cycle. Data bits DQ15–DQ8 are don't care. See Autoselect Command Sequence on page 39 for more information.*
9. *For S29GL064N and S29GL032A Device ID must be read in three cycles.*
10. *Refer to Table 10 on page 29, for data indicating Secured Silicon Sector factory protect status.*
11. *Data is 00h for an unprotected sector and 01h for a protected sector.*
12. *Total number of cycles in command sequence is determined by number of bytes written to write buffer. Maximum number of cycles in command sequence is 37, including* Program Buffer to Flash *command.*
13. *Command sequence resets device for next command after aborted write-to-buffer operation.*
14. *System may read and program in non-erasing sectors, or enter autoselect mode, when in Erase Suspend mode. Erase Suspend command is valid only during a sector erase operation.*
15. *Erase Resume command is valid only during Erase Suspend mode.*
16. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
17. *Refer to Table 10 on page 29, for individual Device IDs per device density and model number.*

Table 20. Sector Protection Commands (x8)

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 2–5)													
			1st/8th		2nd/9th		3rd/10th		4th/11th		5th		6th		7th	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Lock Register Bits	Command Set Entry (Note 5)	3	AAA	AA	555	55	AAA	40								
	Program (Note 6)	2	XXX	A0	XXX	Data										
	Read (Note 6)	1	00	Data												
	Command Set Exit (Note 7)	2	XXX	90	XXX	00										
Password Protection	Command Set Entry (Note 5)	3	AAA	AA	555	55	AAA	60								
	Program (Note 8)	2	XXX	A0	PWAx	PWDx										
	Read (Note 9)	8	00	PWD0	01	PWD1	02	PWD2	03	PWD3	04	PWD4	05	PWD5	06	PWD6
			07	PWD7												
	Unlock (Note 10)	11	00	25	00	03	00	PWD0	01	PWD1	02	PWD2	03	PWD3	04	PWD4
			05	PWD5	06	PWD6	07	PWD7	00	29						
	Command Set Exit (Note 7)	2	XX	90	XX	00										

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Table 20. Sector Protection Commands (x8) (Continued)

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 2–5)													
			1st/8th		2nd/9th		3rd/10th		4th/11th		5th		6th		7th	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Non-Volatile Sector Protection (PPB)	Command Set Entry (Note 5)	3	AAA	AA	555	55	AAA	C0								
	PPB Program (Note 11)	2	XXX	A0	SA	00										
	All PPB Erase (Notes 11, 12)	2	XXX	80	00	30										
	PPB Status Read	1	SA	RD(0)												
	Command Set Exit (Note 7)	2	XXX	90	XXX	00										
Global Volatile Sector Protection Freeze (PPB Lock)	Command Set Entry (Note 5)	3	AAA	AA	555	55	AAA	50								
	PPB Lock Bit Set	2	XXX	A0	XXX	00										
	PPB Lock Bit Status Read	1	XXX	RD(0)												
	Command Set Exit (Note 7)	2	XXX	90	XX	00										
Volatile Sector Protection (DYB)	Command Set Entry (Note 5)	3	AAA	AA	555	55	AAA	E0								
	DYB Set	2	XXX	A0	SA	00										
	DYB Clear	2	XXX	A0	SA	01										
	DYB Status Read	1	SA	RD(0)												
	Command Set Exit (Note 7)	2	XXX	90	XXX	00										

Legend

X = Don't care.

RA = Address of the memory location to be read.

SA = Sector Address. Any address that falls within a specified sector. See Tables 3–9 for sector address ranges.

PWA = Password Address. Address bits A1 and A0 are used to select each 16-bit portion of the 64-bit entity.

PWD = Password Data.

RD(0) = DQ0 protection indicator bit. If protected, DQ0 = 0. If unprotected, DQ0 = 1.

Notes

1. *All values are in hexadecimal.*
2. *Shaded cells indicate read cycles.*
3. *Address and data bits not specified in table, legend, or notes are don't cares (each hex digit implies 4 bits of data).*
4. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.*
5. *Entry commands are required to enter a specific mode to enable instructions only available within that mode.*
6. *No unlock or command cycles required when bank is reading array data.*
7. *Exit command must be issued to reset the device into read mode; device may otherwise be placed in an unknown state.*
8. *Entire two bus-cycle sequence must be entered for each portion of the password.*
9. *Full address range is required for reading password.*
10. *Password may be unlocked or read in any order. Unlocking requires the full password (all seven cycles).*
11. *ACC must be at V_{IH} when setting PPB or DYB.*
12. *"All PPB Erase" command pre-programs all PPBs before erasure to prevent over-erasure.*

10.10 Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 22 on page 56 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or is completed.

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10.11 DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to the read mode.

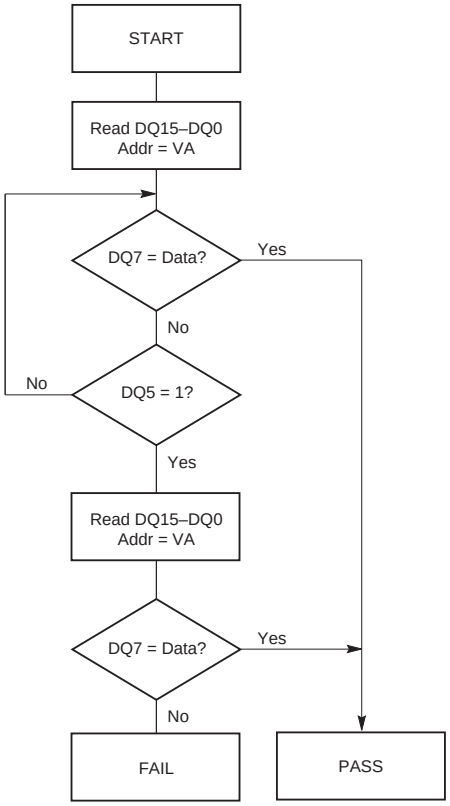
During the Embedded Erase algorithm, Data# Polling produces a *0* on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a *1* on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device completed the program or erase operation and DQ7 has valid data, the data outputs on DQ0–DQ6 may be still invalid. Valid data on DQ0–DQ7 appears on successive read cycles.

Table 22 on page 56 shows the outputs for Data# Polling on DQ7. Figure 14 on page 53 shows the Data# Polling algorithm. Figure 27 on page 66 shows the Data# Polling timing diagram.

Figure 14. Data# Polling Algorithm



Notes

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = 1 because DQ7 may change simultaneously with DQ5.*

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10.12 RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or in the erase-suspend-read mode. Table 22 on page 56 shows the outputs for RY/BY#.

10.13 DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

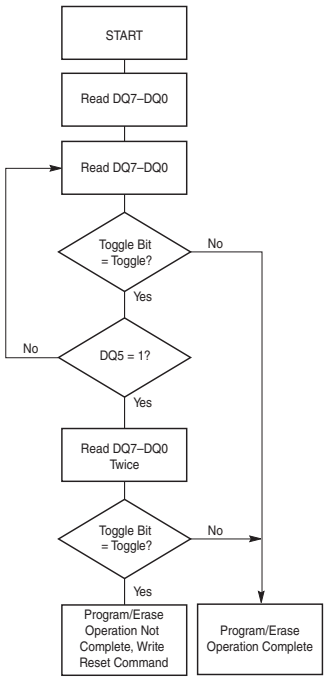
The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see DQ7: Data# Polling on page 53).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 22 on page 56 shows the outputs for Toggle Bit I on DQ6. Figure 15 on page 54 shows the toggle bit algorithm. Figure 28 on page 67 shows the toggle bit timing diagrams. Figure 29 on page 67 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II on page 55.

Figure 15. Toggle Bit Algorithm



Note
The system should recheck the toggle bit even if DQ5 = 1 because the toggle bit may stop toggling as DQ5 changes to 1. See the subsections on DQ6 and DQ2 for more information.

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10.14 DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that were selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 22 on page 56 to compare outputs for DQ2 and DQ6. Figure 15 on page 54 shows the toggle bit algorithm in flowchart form. Figure 28 on page 67 shows the toggle bit timing diagram. Figure 29 on page 67 shows the differences between DQ2 and DQ6 in graphical form.

10.15 Reading Toggle Bits DQ6/DQ2

Refer to Figure 15 on page 54 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 15 on page 54).

10.16 DQ5: Exceeded Timing Limits

DQ5 indicates whether the program, erase, or write-to-buffer time exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a *1*. indicating that the program or erase cycle was not successfully completed.

The device may output a *1* on DQ5 if the system tries to program a *1* to a location that was previously programmed to *0*. **Only an erase operation can change a *0* back to a *1*.** Under this condition, the device halts the operation, and when the timing limit is exceeded, DQ5 produces a *1*.

In all these cases, the system must write the reset command to return the device to the reading the array (or to erase-suspend-read if the device was previously in the erase-suspend-program mode).

10.17 DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure began. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a *0* to a *1*. If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device accepted the command sequence, and then read DQ3. If DQ3 is *1*, the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is *0*, the device accepts additional sector erase commands. To ensure the command is accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 22 on page 56 shows the status of DQ3 relative to the other status bits.

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10.18 DQ1: Write-to-Buffer Abort

DQ1 indicates whether a Write-to-Buffer operation was aborted. Under these conditions DQ1 produces a *1*. The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data. See Write Buffer on page 17 for more details.

Table 21. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	DQ1	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	N/A	0
Program Suspend Mode	Program-Suspend Read	Program-Suspended Sector	Invalid (not allowed)						1
		Non-Program Suspended Sector	Data						1
Erase Suspend Mode	Erase-Suspend Read	Erase-Suspended Sector	1	No toggle	0	N/A	Toggle	N/A	1
		Non-Erase Suspended Sector	Data						1
	Erase-Suspend-Program (Embedded Program)		DQ7#	Toggle	0	N/A	N/A	N/A	0
Write-to-Buffer	Busy (Note 3)		DQ7#	Toggle	0	N/A	N/A	0	0
	Abort (Note 4)		DQ7#	Toggle	0	N/A	N/A	1	0

Table 22. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	DQ1	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	N/A	0
Program Suspend Mode	Program-Suspend Read	Program-Suspended Sector	Invalid (not allowed)						1
		Non-Program Suspended Sector	Data						1
Erase Suspend Mode	Erase-Suspend Read	Erase-Suspended Sector	1	No toggle	0	N/A	Toggle	N/A	1
		Non-Erase Suspended Sector	Data						1
	Erase-Suspend-Program (Embedded Program)		DQ7#	Toggle	0	N/A	N/A	N/A	0
Write-to-Buffer	Busy (Note 3)		DQ7#	Toggle	0	N/A	N/A	0	0
	Abort (Note 4)		DQ7#	Toggle	0	N/A	N/A	1	0

Notes

1. *DQ5 switches to 1 when an Embedded Program, Embedded Erase, or Write-to-Buffer operation exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *The Data# Polling algorithm should be used to monitor the last loaded write-buffer address location.*
4. *DQ1 switches to 1 when the device aborts the write-to-buffer operation.*

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11. Absolute Maximum Ratings

Parameter		Rating
Storage Temperature, Plastic Packages		–65°C to +150°C
Ambient Temperature with Power Applied		–65°C to +125°C
Voltage with Respect to Ground	V_{CC} (Note 1)	–0.5 V to +4.0 V
	A9, ACC and RESET# (Note 2)	–0.5 V to +12.5 V
	All other pins (Note 1)	–0.5 V to V_{CC}+0.5 V
Output Short Circuit Current	(Note 3)	200 mA

Notes

1. *Minimum DC voltage on input or I/Os is –0.5 V. During voltage transitions, inputs or I/Os may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 16. Maximum DC voltage on input or I/Os is V_{CC} + 0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 17.*
2. *Minimum DC input voltage on pins A9, ACC, and RESET# is –0.5 V. During voltage transitions, A9, ACC, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 16. Maximum DC input voltage on pin A9, ACC, and RESET# is +12.5 V which may overshoot to +14.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under* Absolute Maximum Ratings *may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

Figure 16. Maximum Negative Overshoot Waveform

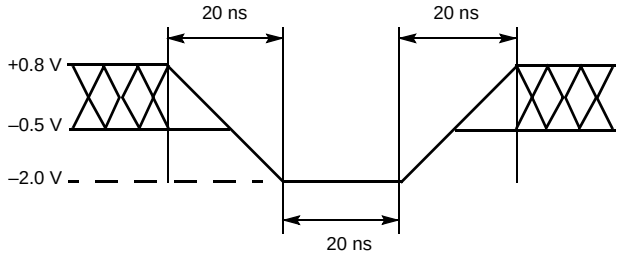
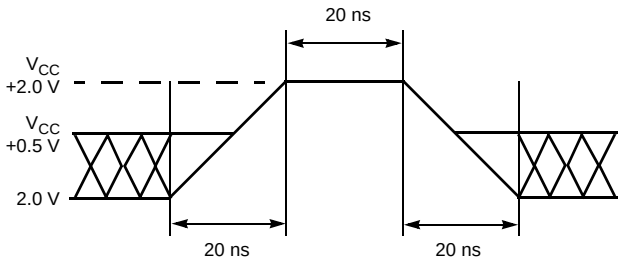


Figure 17. Maximum Positive Overshoot Waveform



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12. Operating Ranges

Parameter		Range
Ambient Temperature (T_A), Industrial (I) Devices		–40°C to +85°C
Supply Voltages	V_{CC} for full voltage range	+2.7 V to +3.6 V
	V_{IO}	+1.65 to +3.6 V

Notes

1. *Operating ranges define those limits between which the functionality of the device is guaranteed.*
2. *V_{IO} input voltage always must be lower than V_{CC} input voltage.*

13. DC Characteristics

Table 23. DC Characteristics, CMOS Compatible

Parameter Symbol	Parameter Description (Notes)	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current (Note 1)	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				WP#/ACC: ±2.0 µA	µA
						Others: ±1.0 µA	
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC\ max}$; A9 = 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Initial Read Current (Note 1)	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC\ max}$, f = 1 MH			6	10	mA
		CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC\ max}$, f = 5 MHz			25	30	
		CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC\ max}$, f = 10 MHz			45	50	
I_{CC2}	V_{CC} Intra-Page Read Current (Note 1)	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC\ max}$ f = 10 MHz			1	10	mA
		CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC\ max}$ f = 33 MH			5	20	
I_{CC3}	V_{CC} Active Erase/Program Current (Notes 2, 3)	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC\ max}$			50	60	mA
I_{CC4}	V_{CC} Standby Current	$V_{CC} = V_{CC\ max}$; $V_{IO} = V_{CC}$; OE# = V_{IH}; $V_{IL} = (V_{SS}+0.3V) / –0.1V$; CE#, RESET# = $V_{CC} \pm 0.3$ V			1	5	µA
I_{CC5}	V_{CC} Reset Current	$V_{CC} = V_{CCmax}$, $V_{IO} = V_{CC}$, $V_{IL} = (V_{SS}+0.3V) / –0.1V$; RESET# = $V_{SS} \pm 0.3$ V			1	5	µA
I_{CC6}	Automatic Sleep Mode (Note 4)	$V_{CC} = V_{CCmax}$, $V_{IO} = V_{CC}$, $V_{IH} = V_{CC} \pm 0.3$ V; $V_{IL} = (V_{SS}+0.3V) / –0.1V$; WP#/ACC = V_{IH}			1	5	µA
I_{ACC}	ACC Accelerated Program Current	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC}$max, WP#/ACC = V_{IH}	WP#/ACC		10	20	mA
			V_{CC}		50	60	mA
V_{IL}	Input Low Voltage 1 (Note 5)			–0.1		0.3 x V_{IO}	V
V_{IH}	Input High Voltage 1 (Note 5)			0.7 V_{IO}		V_{IO} + 0.3	V
V_{HH}	Voltage for ACC Program Acceleration	V_{CC} = 2.7 –3.6 V		11.5		12.5	V
V_{ID}	Voltage for Autoselect	V_{CC} = 2.7 –3.6 V		11.5		12.5	V

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Table 23. DC Characteristics, CMOS Compatible (Continued)

Parameter Symbol	Parameter Description (Notes)	Test Conditions	Min	Typ	Max	Unit
V_{OL}	Output Low Voltage (Note 5)	I_{OL} = 100 µA			0.15 x V_{IO}	V
V_{OH1}	Output High Voltage (Note 5)	I_{OH} = –100 µA	0.85 V_{IO}			V
V_{OH2}						
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 3)		2.3		2.5	V

Notes

1. *I_{CC} current listed is typically less than 5.5 mA/MHz, with OE# at V_{IH}.*
2. *I_{CC} active while Embedded Erase, Embedded Program, or Write Buffer Programming is in progress.*
3. *Not 100% tested.*
4. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns.*
5. *V_{IO} = 1.65–1.95 V or 2.7–3.6 V.*
6. *V_{CC} = 3 V and V_{IO} = 3 V or 1.8 V. When V_{IO} is at 1.8 V, I/Os cannot operate at 3 V.*

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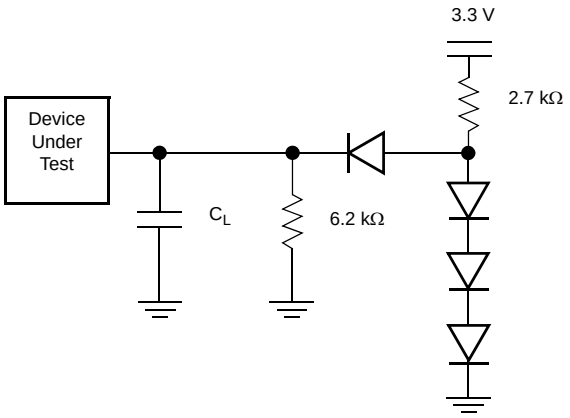
14. Test Conditions

Figure 18. Test Setup



Note
Diodes are IN3064 or equivalent.

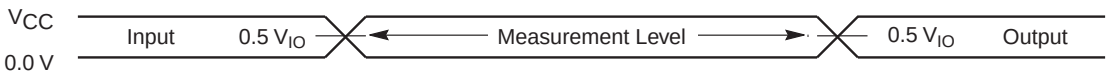
Table 24. Test Specifications

Test Condition	All Speeds	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0 or V_{IO}	V
Input timing measurement reference levels	0.5 V_{IO}	V
Output timing measurement reference levels	0.5 V_{IO}	V

14.1 Key to Switching Waveforms

Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

Figure 19. Input Waveforms and Measurement Levels



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15. AC Characteristics

Table 25. Read-Only Operations

Parameter		Description		Test Setup		Speed Options		Unit
JEDEC	Std.					90	110	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	90	110	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE#, OE# = V_{IL}	Max	90	110	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	90	110	ns
	t_{PACC}	Page Access Time		V_{IO} = V_{CC} = 3 V	Max	25	25	ns
				V_{IO} = 1.8 V, V_{CC} = 3 V		—	30	
t_{GLQV}	t_{OE}	Output Enable to Output Delay		V_{IO} = V_{CC} = 3 V	Max	25	25	ns
				V_{IO} = 1.8 V, V_{CC} = 3 V		—	30	
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	20		ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	20		ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First			Min	0		ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0		ns
			Toggle and Data# Polling		Min	10		ns

Notes

1. *Not 100% tested.*
2. *See Figure 18 on page 60 and Table 24 on page 60 for test specifications.*

Figure 20. V_{CC} Power-up Diagram

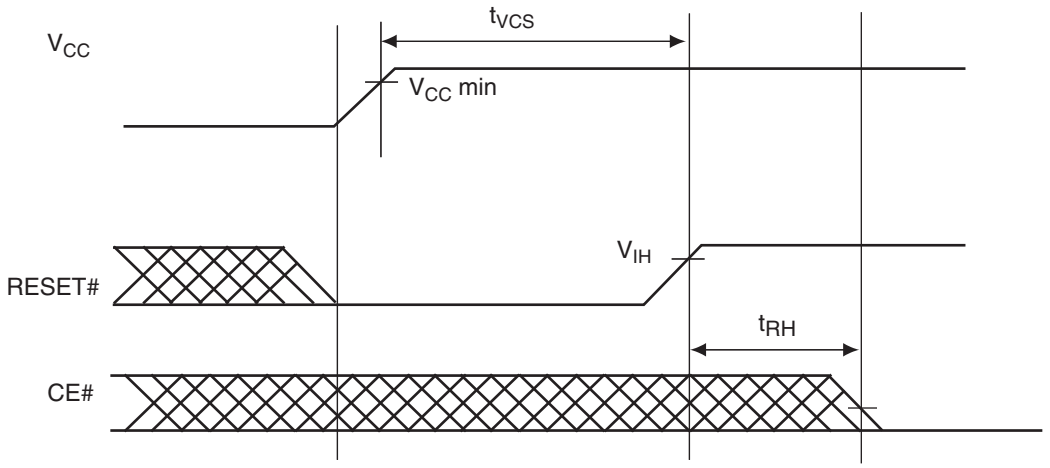

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Figure 21. Read Operation Timings

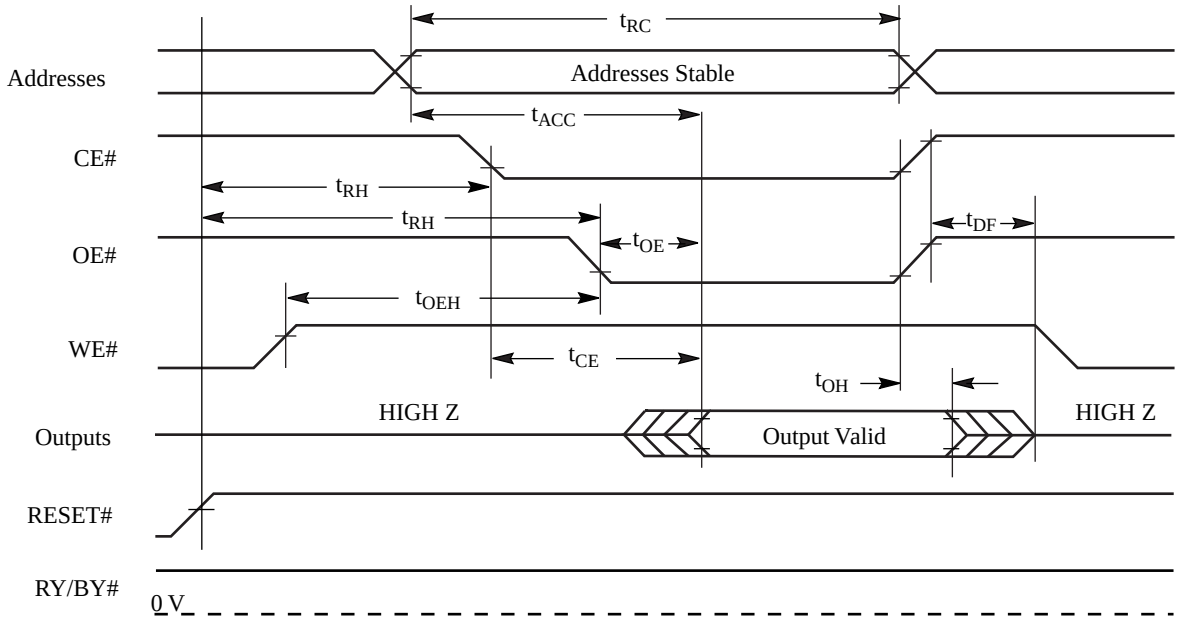
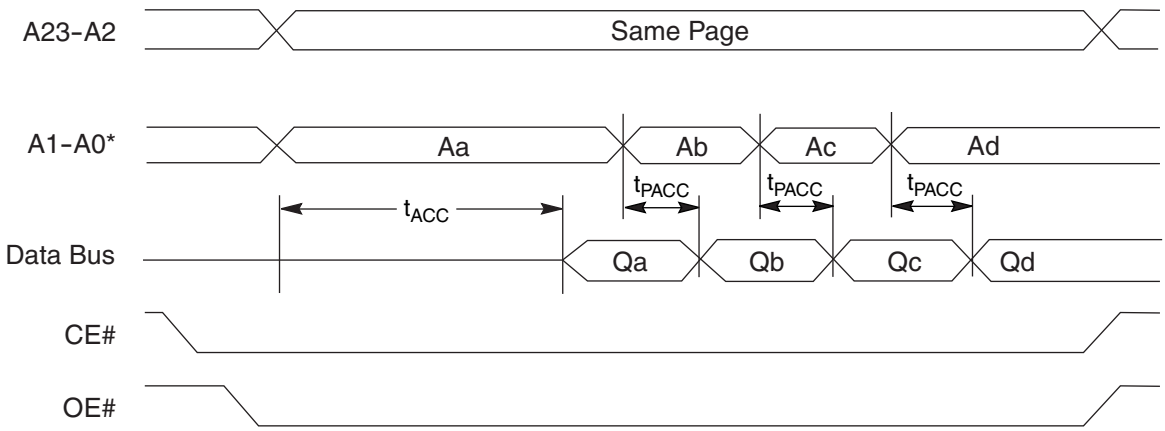


Figure 22. Page Read Timings



Note

** Figure shows device in word mode. Addresses are A1–A-1 for byte mode.*

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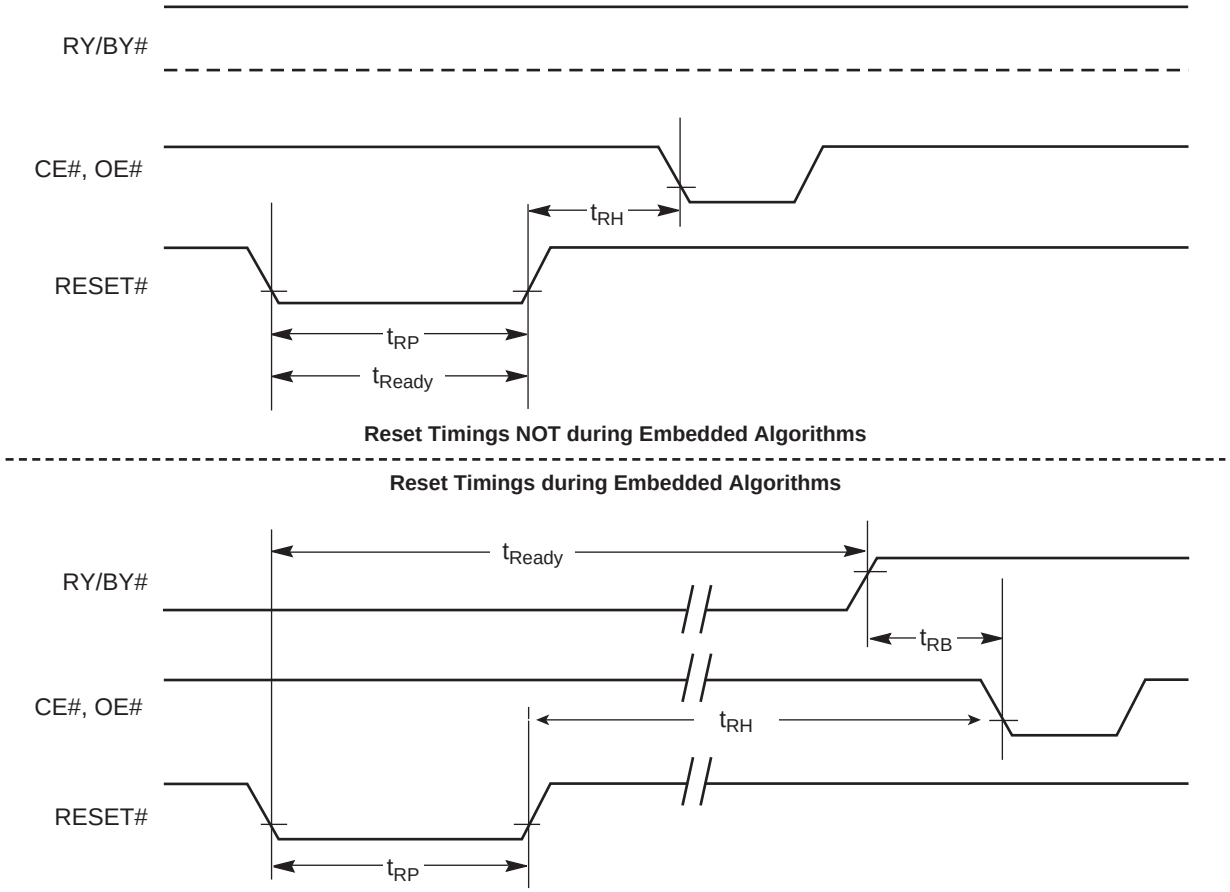
Table 26. Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std.				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Input Low to Standby Mode (See Note)	Min	20	µs
	t_{RB}	RY/BY# Output High to CE#, OE# pin Low	Min	0	ns

Note
Not 100% tested.

Figure 23. Reset Timings



Notes
1. *Not 100% tested.*
2. *See the Erase And Programming Performance on page 70 for more information.*
3. *For 1–16 words/1–32 bytes programmed.*

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Table 27. Erase and Program Operations

Parameter		Description		Speed Options		Unit
JEDEC	Std.			90	110	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	90	110	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0		ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling	Min	15		ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45		ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling	Min	0		ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	35		ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0		ns
	t_{CEPH}	CE# High during toggle bit polling	Min	20		ns
	t_{OEPH}	OE# High during toggle bit polling	Min	20		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0		ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0		ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35		ns
t_{WHDL}	t_{WPH}	Write Pulse Width High	Min	30		ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)	Typ	240		µs
		Single Word Program Operation (Note 2)	Typ	60		
		Accelerated Single Word Program Operation (Note 2)	Typ	54		
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.5		sec
	t_{VHH}	V_{HH} Rise and Fall Time (Note 1)	Min	250		ns
	t_{VCS}	V_{CC} Setup Time (Note 1)	Min	50		µs
	t_{BUSY}	WE# High to RY/BY# Low	Min	90	110	ns

Notes

1. *Not 100% tested.*
2. *See the Erase And Programming Performance on page 70 for more information.*
3. *For 1–16 words/1–32 bytes programmed.*

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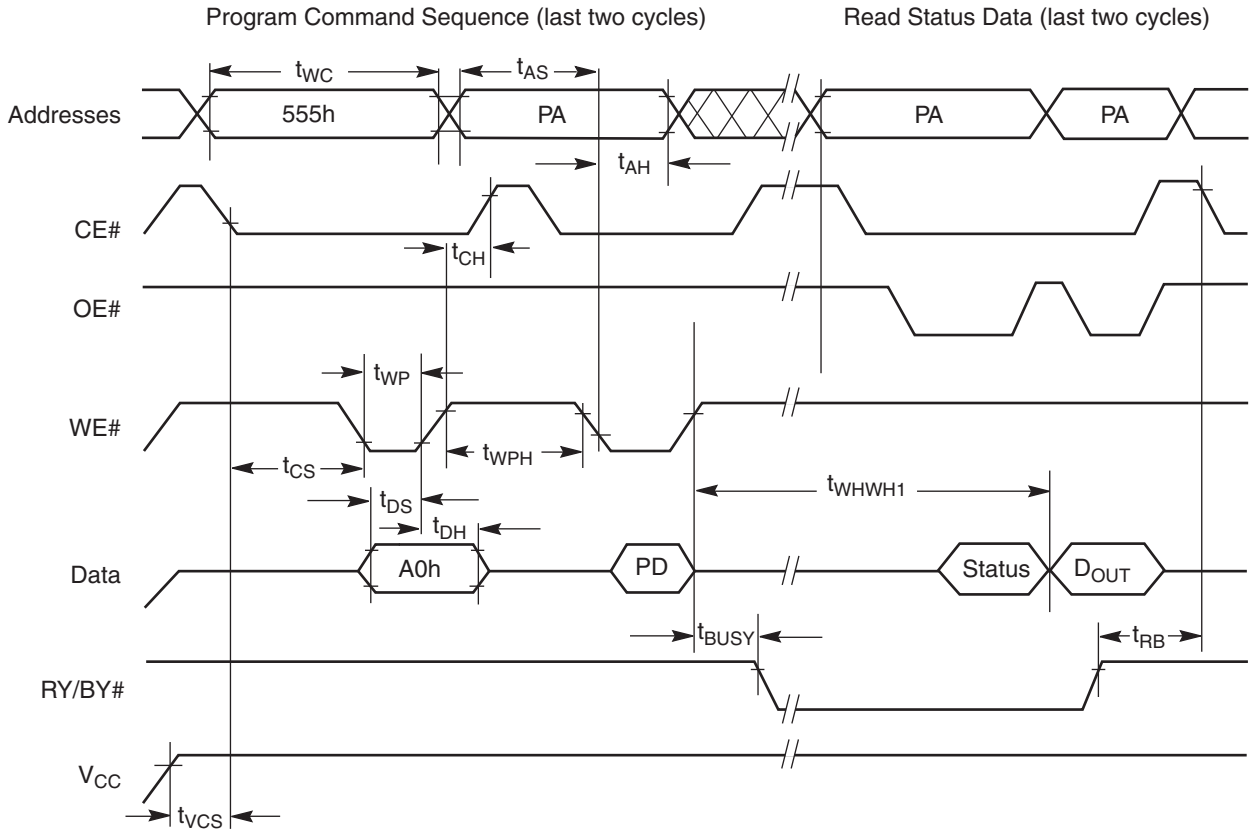
Figure 24. Program Operation Timings



Notes

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode.*

Figure 25. Accelerated Program Timing Diagram

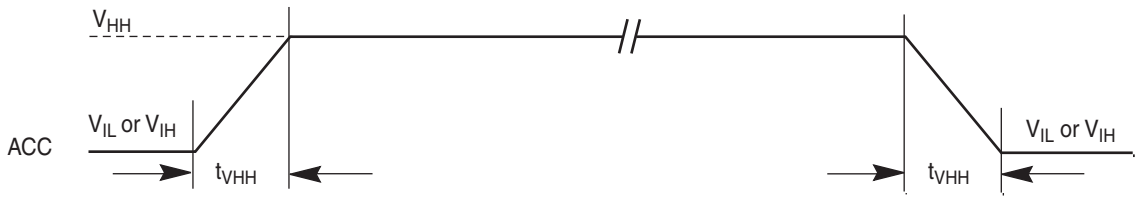


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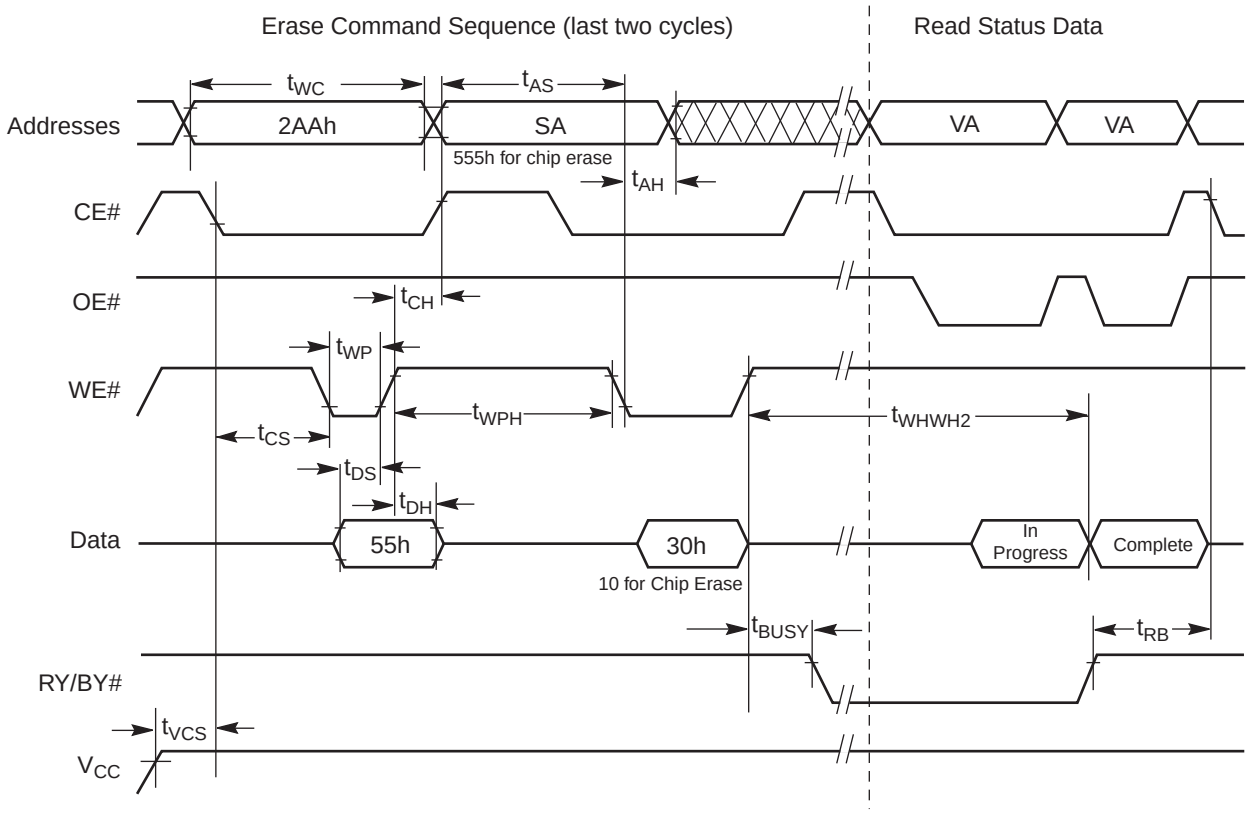
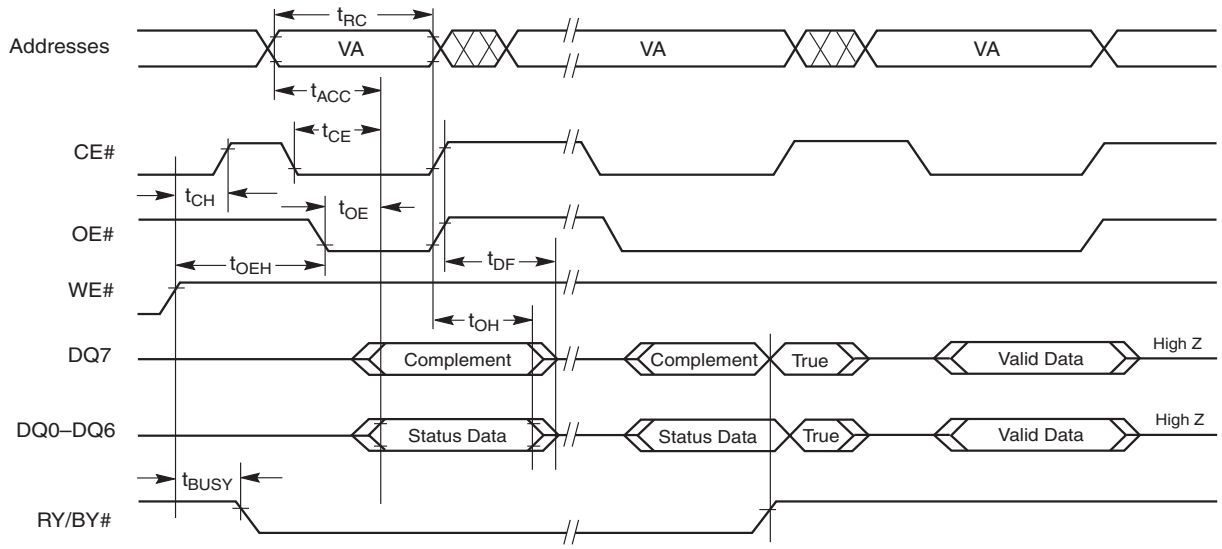
Figure 26. Chip/Sector Erase Operation Timings



Notes

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see Write Operation Status on page 52.)*
2. *Illustration shows device in word mode.*

Figure 27. Data# Polling Timings (During Embedded Algorithms)



Note

VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

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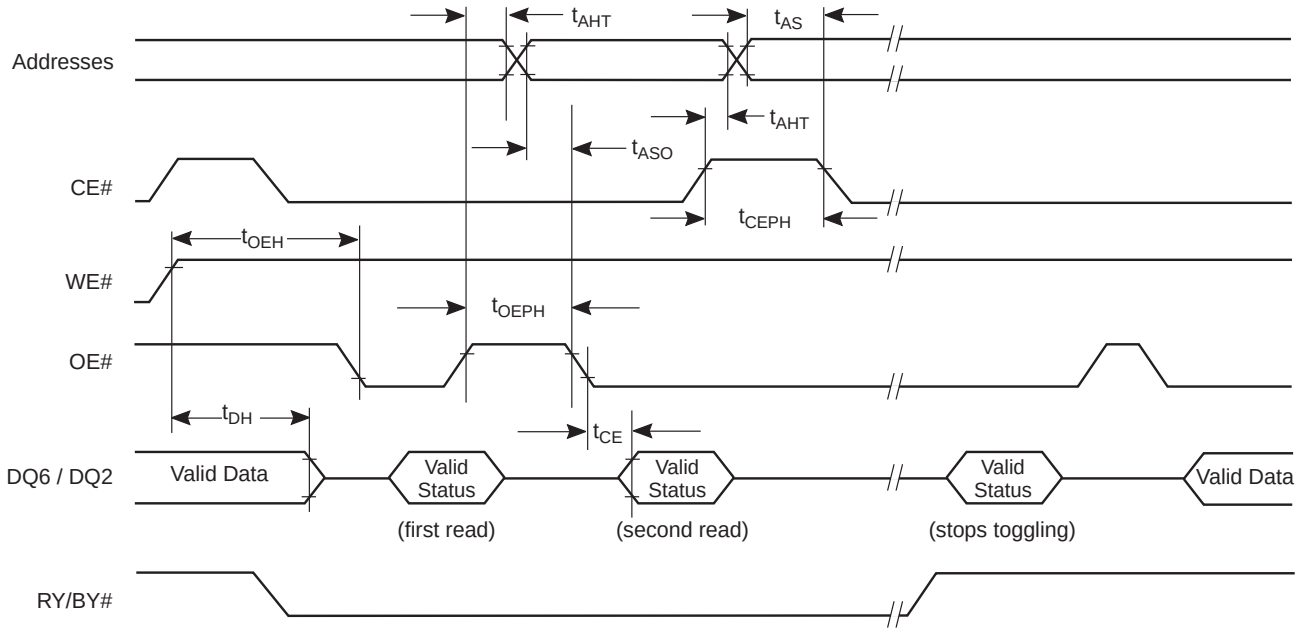
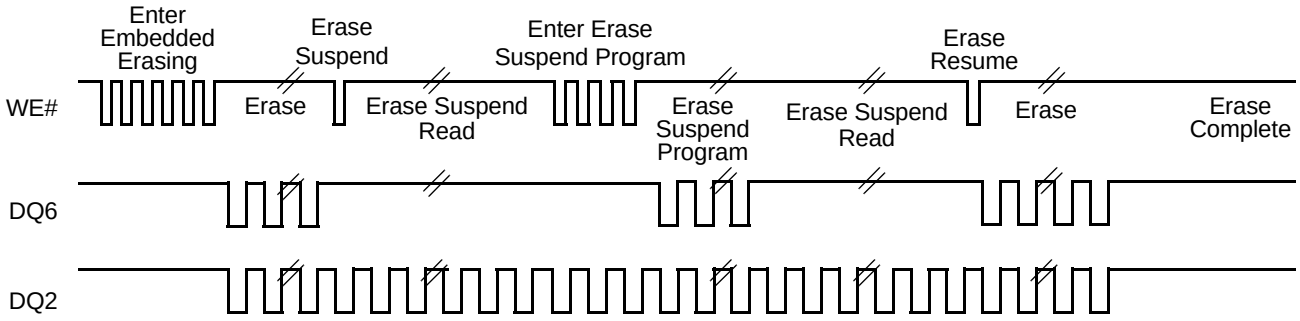
Figure 28. Toggle Bit Timings (During Embedded Algorithms)



Note
VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 29. DQ2 vs. DQ6



Note
DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.

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Table 28. Alternate CE# Controlled Erase and Program Operations

Parameter		Description		Speed Options		Unit
JEDEC	Std.			90	110	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	90	110	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0		ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45		ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	35		ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0		ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to CE# Low)	Min	0		ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0		ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0		ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	35		ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min	25		ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)	Typ	240		µs
		Single Word Program Operation (Note 2)	Typ	60		
		Accelerated Single Word Program Operation (Note 2)	Typ	54		
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.5		sec
	t_{RH}	RESET# High Time Before Write	Min	50		ns

Notes

1. *Not 100% tested.*
2. *See the Erase And Programming Performance on page 70 for more information.*
3. *For 1–16 words/1–32 bytes programmed.*

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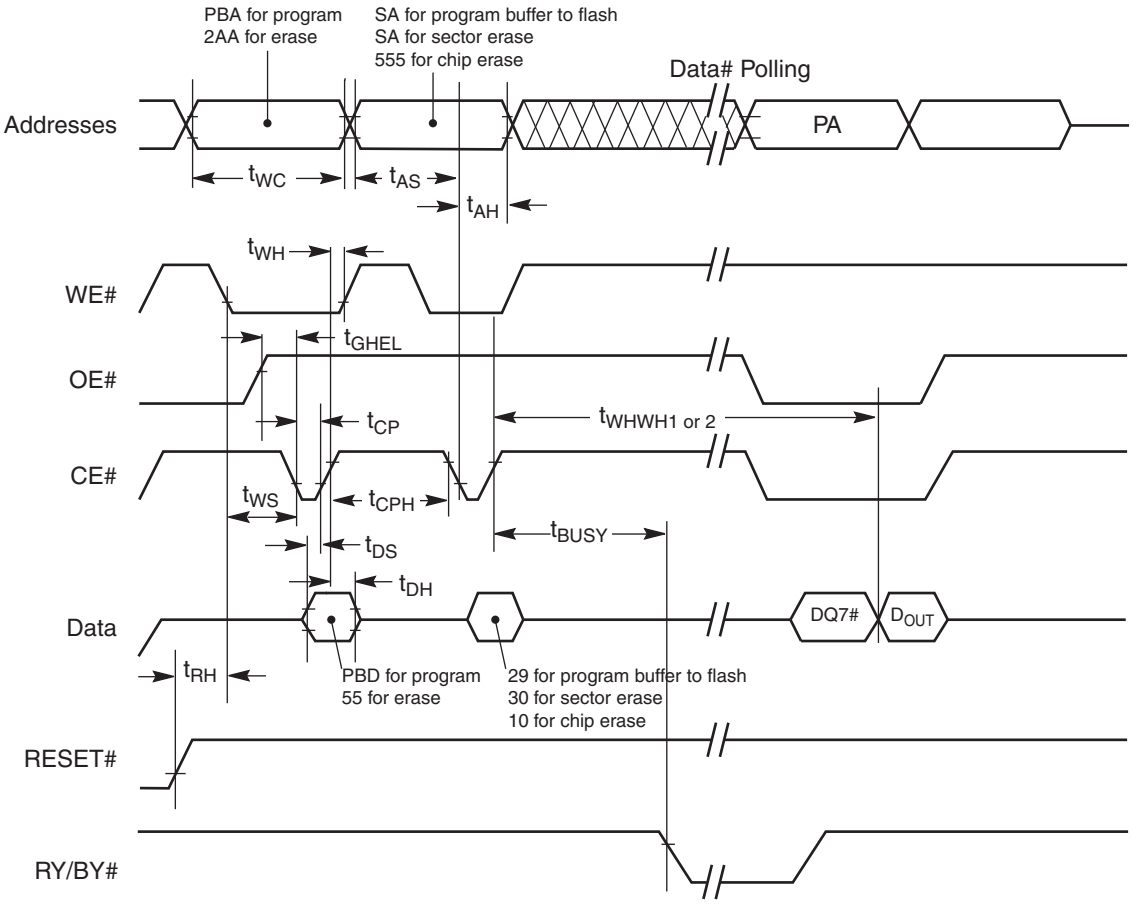
Figure 30. Alternate CE# Controlled Write (Erase/Program) Operation Timings



Notes

1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device.*
4. *Illustration shows device in word mode.*

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16. Erase And Programming Performance

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.5	3.5	sec	Excludes 00h programming prior to erasure (Note 6)
Chip Erase Time	S29GL032N	32	64		
	S29GL064N	64	128		
Total Write Buffer Program Time (Notes 3, 5)		240		µs	Excludes system level overhead (Note 7)
Total Accelerated Effective Write Buffer Program Time (Notes 4, 5)		200			
Chip Program Time	S29GL032N	31.5		sec	
	S29GL064N	63			

Notes

1. *Typical program and erase times assume the following conditions: 25°C, V_{CC} = 3.0V, 10,000 cycles; checkerboard data pattern.*
2. *Under worst case conditions of 90°C; Worst case V_{CC}, 100,000 cycles.*
3. *Programming time (typ) is 15 µs (per word), 7.5 µs (per byte).*
4. *Accelerated programming time (typ) is 12.5 µs (per word), 6.3 µs (per byte).*
5. *Write buffer Programming time is calculated on a per-word/per-byte basis for a 16-word/32-byte write buffer operation.*
6. *In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.*
7. *System-level overhead is the time required to execute the command sequence(s) for the program command. See Table 17 on page 47 and Table 19 on page 50 for further information on command definitions.*

Table 29. TSOP Pin and BGA Package Capacitance

Parameter Symbol	Parameter Description	Test Setup		Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	TSOP	6	10	pF
			BGA	TBD	TBD	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	TSOP	6	12	pF
			BGA	TBD	TBD	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	TSOP	6	10	pF
			BGA	TBD	TBD	pF
C_{IN3}	#RESET, WP#/ACC Pin Capacitance	V_{IN} = 0	TSOP	27	30	pF
			BGA	TBD	TBD	pF

Notes

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

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17. Data Integrity

17.1 Erase Endurance

Table 17.1 Erase Endurance

Parameter	Minimum	Unit
Program/Erase cycles per main Flash array sectors	100K	PE cycle
Program/Erase cycles per PPB array or non-volatile register array (1)	100K	PE cycle

Note:
1. Each write command to a non-volatile register causes a PE cycle on the entire non-volatile register array.

17.2 Data Retention

Table 17.2 Data Retention

Parameter	Test Conditions	Minimum Time	Unit
Data Retention Time	10K Program/Erase Cycles	20	Years
	100K Program/Erase Cycles	2	Years

Contact Cypress Sales and FAE for further information on the data integrity. An application note is available at: www.cypress.com/appnotes.

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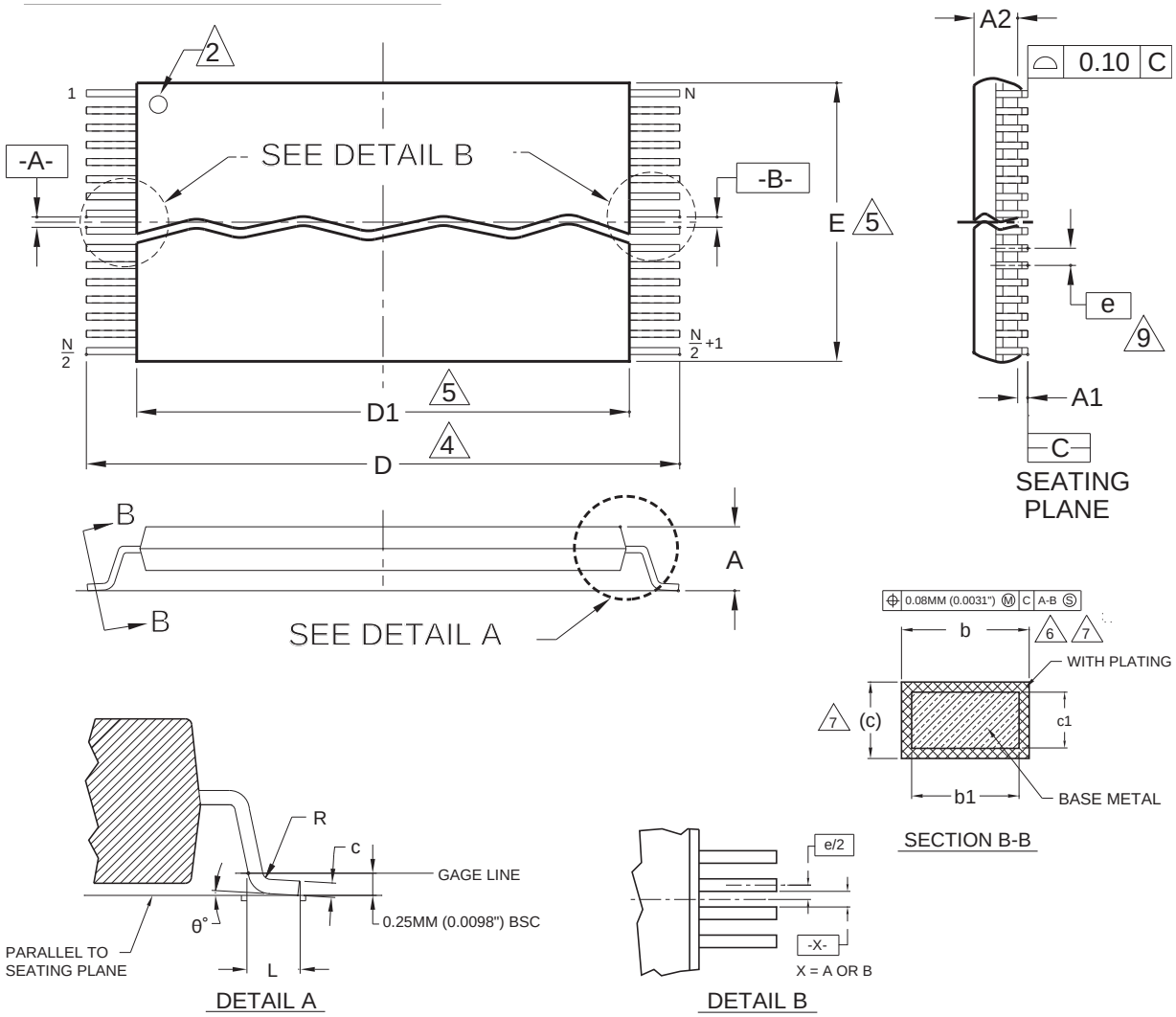
18. Physical Dimensions

18.1 TS048—48-Pin Standard Thin Small Outline Package (TSOP)



Package	TS 048		
Jedec	MO-142 (B) EC		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
0	0°	3°	5°

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (MM). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. NOT APPLICABLE.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15MM (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08 (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07 (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10MM (.0039") AND 0.25MM (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10MM (0.004") AS MEASURED FROM THE SEATING PLANE.

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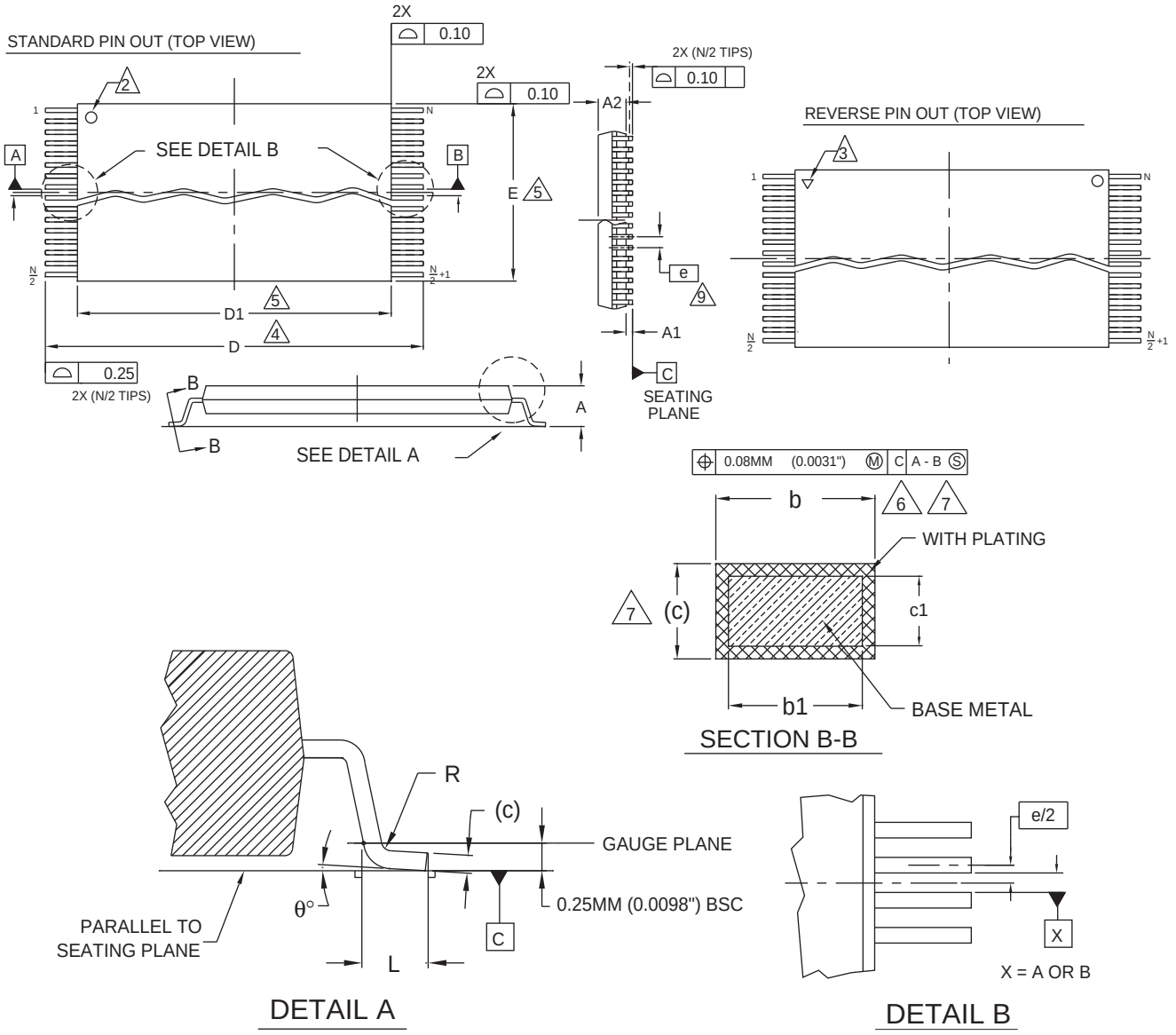
18.2 TS056—56-Pin Standard Thin Small Outline Package (TSOP)



Package	TS 056		
Jedec	MO-142 (D) EC		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	13.90	14.00	14.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8°
R	0.08	—	0.20
N	56		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN), INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08 (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07 (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10MM (.0039") AND 0.25MM (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

3356 \ 16-038.10c

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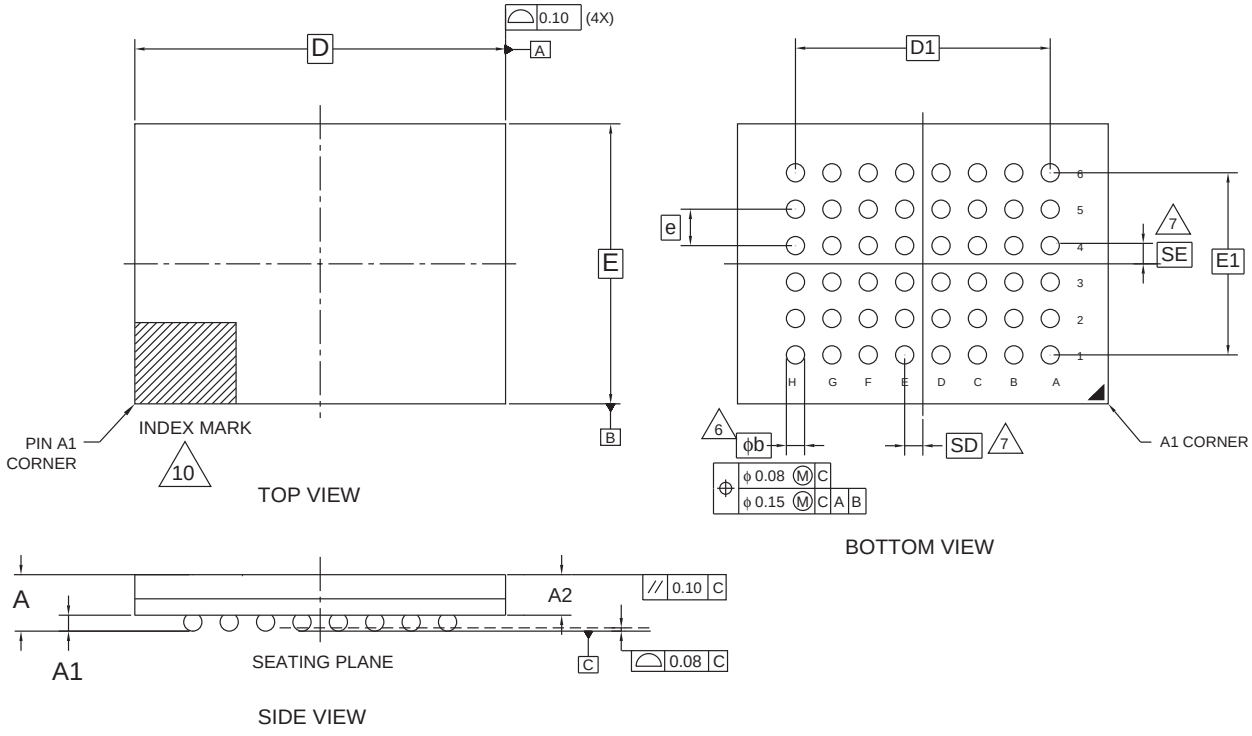
18.3 VBK048—Ball Fine-pitch Ball Grid Array (BGA) 8.15x 6.15 mm Package



PACKAGE	VBK 048			
JEDEC	N/A			
	8.15 mm x 6.15 mm NOM PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.00	OVERALL THICKNESS
A1	0.18	---	---	BALL HEIGHT
A2	0.62	---	0.76	BODY THICKNESS
D	8.15 BSC.			BODY SIZE
E	6.15 BSC.			BODY SIZE
D1	5.60 BSC.			BALL FOOTPRINT
E1	4.00 BSC.			BALL FOOTPRINT
MD	8			ROW MATRIX SIZE D DIRECTION
ME	6			ROW MATRIX SIZE E DIRECTION
N	48			TOTAL BALL COUNT
ϕb	0.35	---	0.43	BALL DIAMETER
e	0.80 BSC.			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	---			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.

   N IS THE TOTAL NUMBER OF SOLDER BALLS.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. NOT USED.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3338 \ 16-038.25 \ 10.05.04

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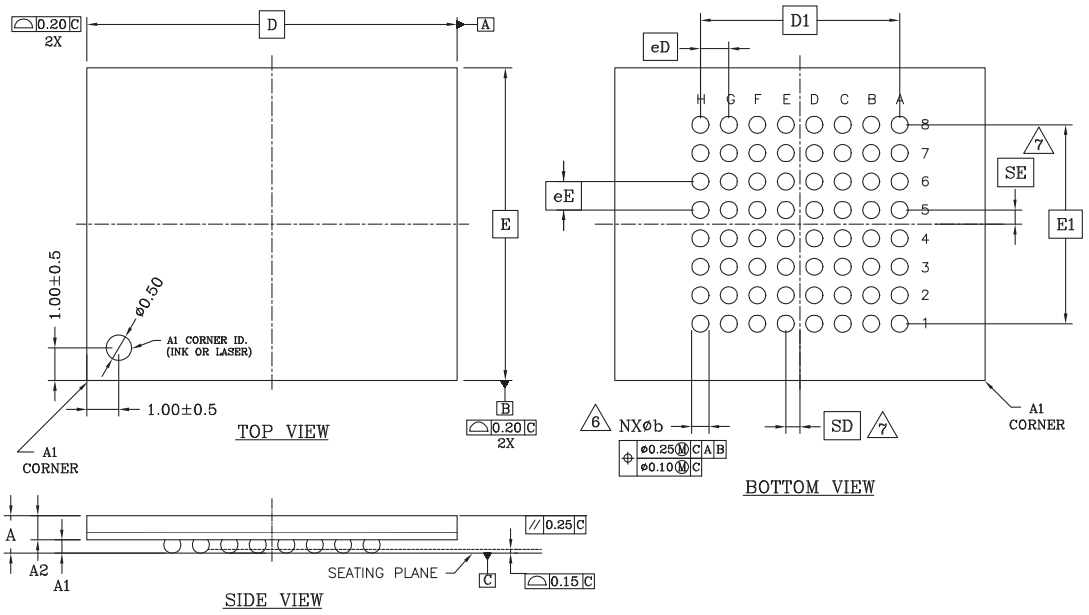
18.4 LAA064—64-Ball Fortified Ball Grid Array (BGA) 13 x 11 mm Package



PACKAGE	LAA 064			
JEDEC	N/A			
	13.00 mm x 11.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.40	PROFILE HEIGHT
A1	0.40	---	---	STANDOFF
A2	0.60	---	---	BODY THICKNESS
D		13.00 BSC.		BODY SIZE
E		11.00 BSC.		BODY SIZE
D1		7.00 BSC.		MATRIX FOOTPRINT
E1		7.00 BSC.		MATRIX FOOTPRINT
MD		8		MATRIX SIZE D DIRECTION
ME		8		MATRIX SIZE E DIRECTION
N		64		BALL COUNT
ϕb	0.50	0.60	0.70	BALL DIAMETER
eD		1.00 BSC.		BALL PITCH - D DIRECTION
eE		1.00 BSC.		BALL PITCH - E DIRECTION
SD / SE		0.50 BSC.		SOLDER BALL PLACEMENT
		NONE		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.

   N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. NOT USED.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

3354 \ 16-038.12d

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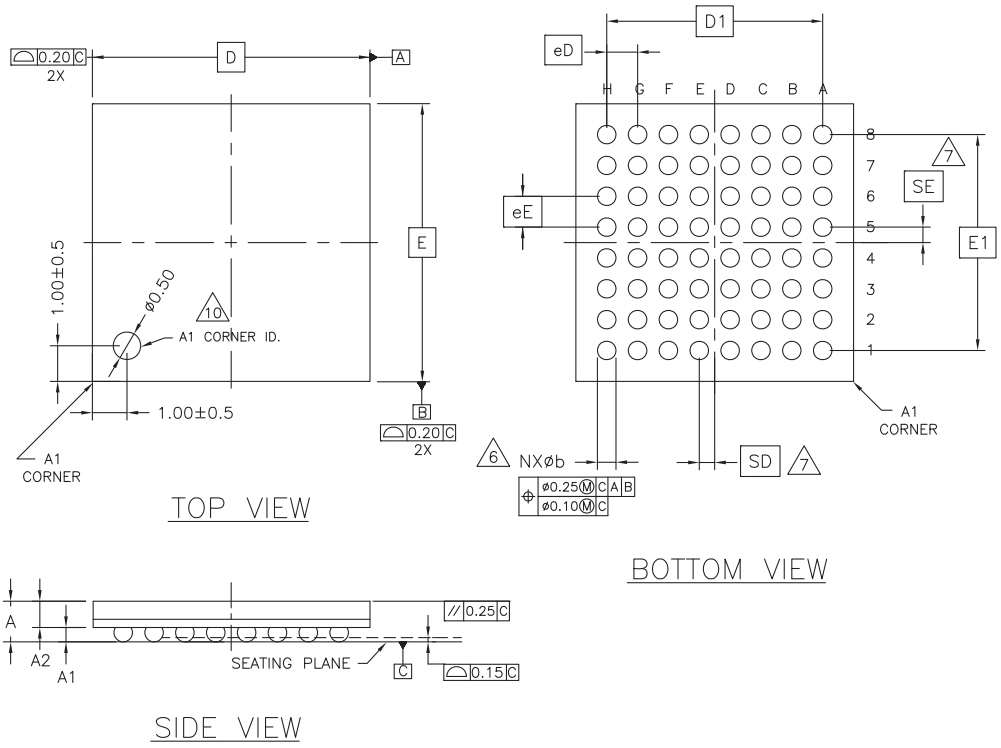
18.5 LAE064-64-Ball Fortified Ball Grid Array (BGA) 9 x 9 mm Package



PACKAGE	LAE 064			
JEDEC	N/A			
	9.00 mm x 9.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.40	PROFILE HEIGHT
A1	0.40	---	---	STANDOFF
A2	0.60	---	---	BODY THICKNESS
D	9.00 BSC.			BODY SIZE
E	9.00 BSC.			BODY SIZE
D1	7.00 BSC.			MATRIX FOOTPRINT
E1	7.00 BSC.			MATRIX FOOTPRINT
MD	8			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
N	64			BALL COUNT
ϕb	0.50	0.60	0.70	BALL DIAMETER
eD	1.00 BSC.			BALL PITCH - D DIRECTION
eE	1.00 BSC.			BALL PITCH - E DIRECTION
SD / SE	0.50 BSC.			SOLDER BALL PLACEMENT
	NONE			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.

   N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. NOT USED.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

3623 \ 16-038.12 \ 1.16.07

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19. Revision History

Document Title: S29GL064N, S29GL032N, 64 Mbit, 32 Mbit 3 V Page Mode MirrorBit Flash Document Number: 001-98525				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	RYSU	02/12/2007 to 10/29/2008	Initial release. Global: Replaced LAE064 package with LAA064. Page Mode Read: Corrected bit ranges in first paragraph. Erase And Programming Performance: Modified maximum sector erase time in table. Connection Diagrams: 64-ball Fortified BGA (LAA 064) figure - Changed inputs for balls F1 and F7. Ordering Information: Removed regulated VCC range and replaced 90 ns with 110 ns for low VIO option Added Note 4 to PACKAGE MATERIAL SET Standard option Sector Addresses table: Corrected a table TSOP Pin and BGA Package Capacitance: Added values for TSOP Ordering Information: Removed leaded parts CFI Table: Altered Erase Block Region 1 & 2 Global: Change document status to Full Production Removed 70ns access speed Command Definitions (x16 mode) Table: Corrected addresses for Program operation Command Definitions (x8 mode) Table: Corrected addresses for Program operation GlobalRemoved VID (12V) Sector protect & unprotect features Primary Vendor-Specific Extended Query Table: Updated the data of CFI address 45hex Primary Vendor-Specific Extended Query Table: Updated the data of CFI address 2D hex thru 34 hex. S29GL064N (Model 04) Bottom Boot Sector Addresses Table: Updated S29GL064N (Model 04) Bottom Boot Sector Addresses Erase and Program Operations TableChanged tDS from 45 ns to 35 ns Absolute Maximum Rating: Removed OE# form table and notes Alternate CE# Controlled Erase and Program Operations: Changed tDS from 45 ns to 35 ns Changed tCPH from 30 ns to 25 ns Requirements for Reading Array DataEntire section is re-written to explain requirements for reading array data Sector ProtectionTitle changed to Advanced Sector Protection Advanced Sector ProtectionSection removed Erase and Program OperationsRemoved note 4 Alternate CE# Controlled Erase and Program OperationsRemoved note 4 GlobalCorrected minor typos AC Characteristics: Updated Data#Polling Timing DC Characteristics: Changed Note 1 in Table DC Characteristics- CMOS Compatible Ordering Information: Added LAE064 package option Connection Diagram: Figure 3.3; Title changed to 64ball Fortified BGA Physical Dimensions: Added LAE064 package option Ordering Information: Updated Valid Combinations Table
*A	4968016	RYSU	10/16/2015	Updated to Cypress template.
*B	5737059	RYSU	05/26/2017	Updated Cypress logo. Added Automotive part numbers. Added Section 17.1 Erase Endurance on page 71 and Section 17.2 Data Retention on page 71.

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