# 10V, High Efficiency, Buck-Boost Controller with Power Good

## FEATURES

- **Single Inductor Architecture Allows $V_{IN}$ Above, Below or Equal to $V_{OUT}$**
- **Power Good Output Indicator**
- **2.7V to 10V Input and Output Range**
- **Up to 96% Efficiency**
- **Up to 10A of Output Current**
- **All N-channel MOSFETs, No $R_{SENSE}$™**
- True Output Disconnect During Shutdown
- Programmable Current Limit and Soft-Start
- Optional Short-Circuit Shutdown Timer
- Output Overvoltage and Undervoltage Protection
- Programmable Frequency: 100kHz to 1MHz
- Selectable Burst Mode® Operation
- Available in 24-Lead (4mm × 4mm) Exposed Pad QFN Package

## APPLICATIONS

- Palmtop Computers
- Handheld Instruments
- Wireless Modems
- Cellular Telephones

## DESCRIPTION

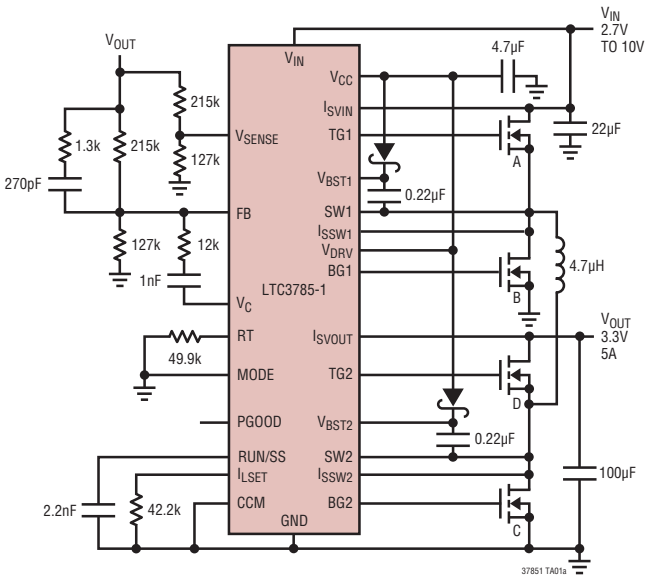
The LTC®3785-1 is a high power synchronous buck-boost controller that drives all N-channel power MOSFETs from input voltages above, below and equal to the output voltage. With an input range of 2.7V to 10V, the LTC3785-1 is well suited for a wide variety of single or dual cell Li-Ion or multicell alkaline/NiMH applications.

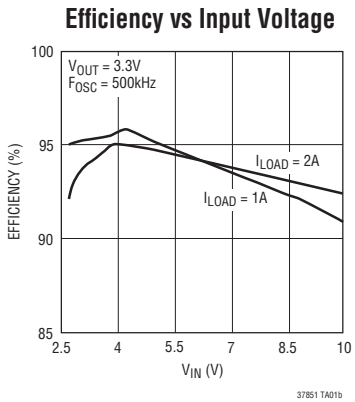
The operating frequency can be programmed from 100kHz to 1MHz. The soft-start time and current limit are also programmable. The soft-start capacitor doubles as the fault timer which can program the IC to latch off or recycle after a determined off time. Burst Mode operation is user controlled and can be enabled by driving the mode pin high. The LTC3785-1 includes a power good output that indicates when the output voltage is within 7.5% of its designed setpoint.

Protection features include foldback current limit, short-circuit and overvoltage protection.



## TYPICAL APPLICATION



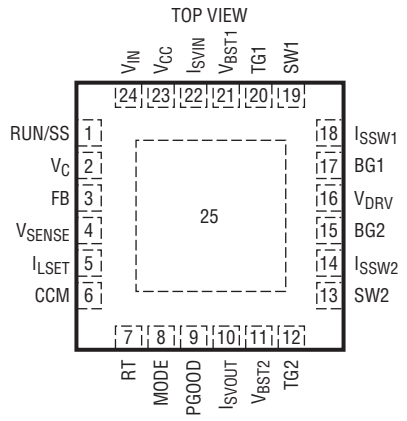



## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

Input Supply Voltage ($V_{IN}$) ..... –0.3V to 11V
$I_{SVOUT}$, $I_{SVIN}$ ..... –0.3V to 11V
SW1, SW2, $I_{SSW1}$, $I_{SSW2}$ Voltage:
  DC ..... –1V to 11V
  Pulsed, <1µs ..... –2V to 12V
RUN/SS, MODE, CCM, $V_{DRV}$, $V_{CC}$ Voltages .. –0.3V to 6V
PGOOD Voltage ..... –0.3V to 6V
$V_{BST1}$ Voltage ..... –0.3V to 16V
  With Respect to SW1 ..... –0.3V to 6V
$V_{BST2}$ Voltage ..... –0.3V to 16V
  With Respect to SW2 ..... –0.3V to 6V
Peak Driver Output Current < 10µs
(TG1, TG2, BG1, BG2) ..... 3A
$V_{CC}$ Average Output Current ..... 100mA
Operating Temperature Range (Note 2) .... –40°C to 85°C
Junction Temperature ..... 125°C
Storage Temperature Range ..... –65°C to 125°C

## PIN CONFIGURATION




UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 37°C/W 4 LAYER BOARD
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC3785EUF-1#PBF | LTC3785EUF-1#TRPBF | 37851 | 24-Lead (4mm × 4mm) Plastic QFN | –40°C to 85°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = $I_{SVOUT}$ = $V_{DRV}$ = $V_{BST1}$ = $V_{BST2}$ = 3.6V, $R_T$ = 49.9k, $R_{ILSET}$ = 59k.**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **$V_{IN}$ Supply** | | | | | | |
| Input Operating Voltage | | ● | 2.7 | | 10 | V |
| Quiescent Current—Burst Mode Operation | $V_C$ = 0V, MODE = 3.6V (Note 4) | | | 86 | 200 | µA |
| Quiescent Current—Shutdown | RUN/SS = 0V, $I_{SVOUT}$ = 3.6V | | | 15 | 25 | µA |
| Quiescent Current—Active | MODE = 0V (Note 4) | | | 0.8 | 1.5 | mA |
| **Error Amp** | | | | | | |
| Feedback Voltage | (Note 5) | ● | 1.200 | 1.225 | 1.25 | V |
| Feedback Input Current | | | | 1 | 500 | nA |
| Error Amp Source Current | | | | –500 | | µA |
| Error Amp Sink Current | | | | 900 | | µA |
| Error Amp $A_{VOL}$ | | | | 90 | | dB |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = $I_{SVOUT}$ = $V_{DRV}$ = $V_{BST1}$ = $V_{BST2}$ = 3.6V, $R_T$ = 49.9k, $R_{ILSET}$ = 59k.**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **$V_{CC}$ Regulator** | | | | | | |
| $V_{CC}$ Maximum Regulating Voltage | $V_{IN}$ = 5V, $I_{VCC}$ = –20mA | ● | 4.15 | 4.35 | 4.55 | V |
| $V_{CC}$ Regulation Voltage | $V_{IN}$ = 3.6V, $I_{VCC}$ = –20mA | ● | 3.3 | 3.5 | 3.6 | V |
| $V_{CC}$ Regulator Sink Current | $I_{SVOUT}$ = $V_{CC}$ = 5V | | | 800 | | µA |
| **Run/Soft-Start** | | | | | | |
| RUN/SS Threshold | When IC is Enabled<br>When EA is at Maximum Boost Duty Cycle | ● | 0.35 | 0.7<br>1.9 | 1.1 | V<br>V |
| RUN/SS Input Current | RUN/SS = 0V | | | –1 | | µA |
| RUN/SS Discharge Current | During Current Limit | | | 20 | 30 | µA |
| **Current Limit** | | | | | | |
| Current Limit Sense Threshold | $I_{SVIN}$ to $I_{SSW1}$, $R_{ILSET}$ = 121k<br>$I_{SVIN}$ to $I_{SSW1}$, $R_{ILSET}$ = 59k | ●<br>● | 20<br>55 | 60<br>105 | 100<br>155 | mV<br>mV |
| Reverse Current Limit Sense Threshold | $I_{SSW2}$ to $I_{SVOUT}$, CCM > 2V<br>$I_{SSW2}$ to $I_{SVOUT}$, CCM < 0.4V | ●<br>● | –50 | –110<br>–15 | –170<br>–35 | mV<br>mV |
| Input Current | $I_{SVIN}$<br>$I_{SVOUT}$<br>$I_{SSW1}$, $I_{SSW2}$ | | | 80<br>10<br>0.1 | 150<br>20<br>5 | µA<br>µA<br>µA |
| CCM Input Threshold (High) | | ● | 2.2 | | | V |
| CCM Input Threshold (Low) | | ● | | | 0.4 | V |
| CCM Input Current | CMM = 3.6V | | | 0.01 | 1 | µA |
| **Burst Mode Operation** | | | | | | |
| Mode Threshold | | ● | 0.8 | 1.5 | 2.2 | V |
| Mode Input Current | | | | 0.01 | 1 | µA |
| $t_{ON}$ Time | | | | 1.4 | | µs |
| **Oscillator** | | | | | | |
| Frequency Accuracy | | ● | 370 | 509 | 650 | kHz |
| **Switching Characteristics** | | | | | | |
| Maximum Duty Cycle | Boost (% Switch BG2 On)<br>Buck (% Switch TG1 On) | ● | 80 | 90<br>99 | | %<br>% |
| TG1, TG2 Driver Impedance | | | | 2 | | Ω |
| BG1, BG2 Driver Impedance | | | | 2 | | Ω |
| TG1, TG2 Rise Time | $C_{LOAD}$ = 3300pF (Note 3) | | | 20 | | ns |
| BG1, BG2 Rise Time | $C_{LOAD}$ = 3300pF (Note 3) | | | 20 | | ns |
| TG1, TG2 Fall Time | $C_{LOAD}$ = 3300pF (Note 3) | | | 20 | | ns |
| BG1, BG2 Fall Time | $C_{LOAD}$ = 3300pF (Note 3) | | | 20 | | ns |
| Buck Driver Nonoverlap Time | TG1 to BG1 | | | 100 | | ns |
| Boost Driver Nonoverlap Time | TG2 to BG2 | | | 100 | | ns |
| **Power Good** | | | | | | |
| Undervoltage Threshold | $V_{SENSE}$ Falling, % Below FB Regulation Voltage | | –5 | –7.5 | –10.5 | % |
| Undervoltage Hysteresis | | | | 1.5 | | % |
| Overvoltage Threshold | $V_{SENSE}$ Rising % Above FB Regulation Voltage, MODE = 0V | | 5 | 7.5 | 10.5 | % |
| Overvoltage Hysteresis | | | | –2 | | % |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = $I_{SVOUT}$ = $V_{DRV}$ = $V_{BST1}$ = $V_{BST2}$ = 3.6V, $R_T$ = 49.9k, $R_{ILSET}$ = 59k.**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| PGOOD Output Low | $I_{PGOOD}$ = 500µA | | | 200 | 500 | mV |
| PGOOD Leakage | $V_{PGOOD}$ = 5.5V | | | | 5 | µA |
| $V_{SENSE}$ Input Current | $V_{SENSE}$ = Measured FB Voltage | | | 1 | 500 | nA |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3785E-1 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

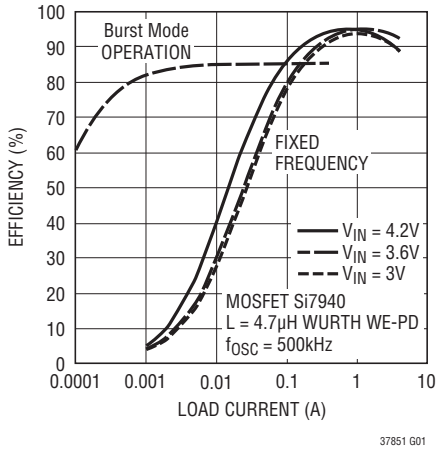
**Note 3:** Specification is guaranteed by design and not 100% tested in production.

**Note 4:** Current measurements are performed when the outputs are not switching.

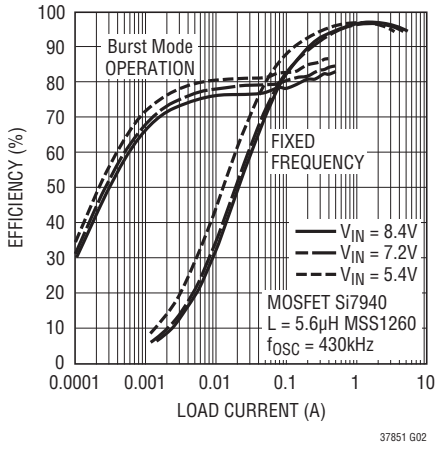
**Note 5:** The IC is tested in a feedback loop to make the measurement.

## TYPICAL PERFORMANCE CHARACTERISTICS

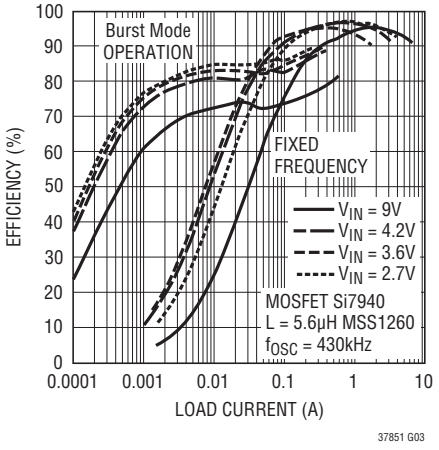
**Li-Ion to 3.3V Efficiency vs Load Current**



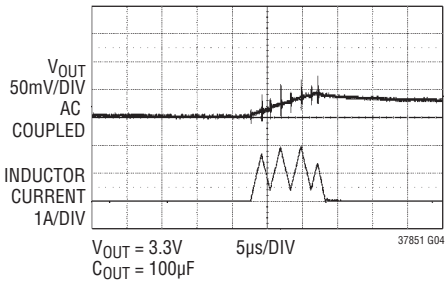

**Two Li-Ion to 7V Efficiency vs Load Current**



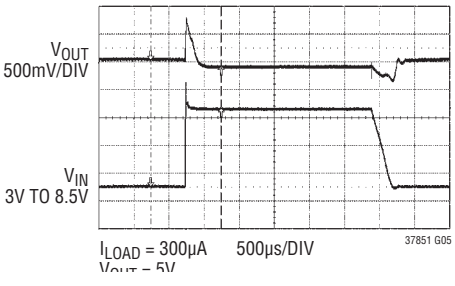

**Li-Ion/9V to 5V $V_{OUT}$ Efficiency vs Load Current**



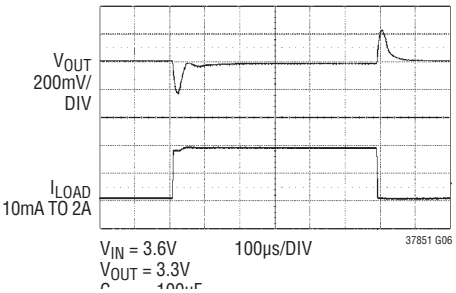

**Burst Mode Ripple**




**Line Transient Response**

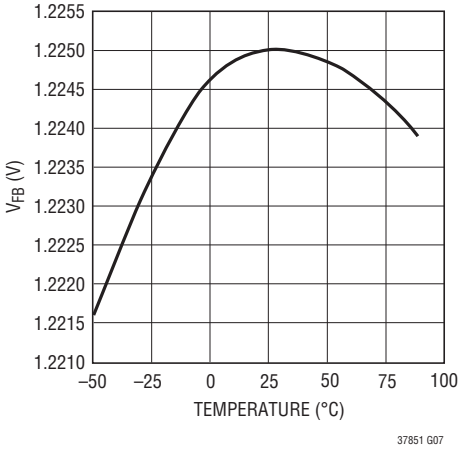



**$V_{OUT}$ Load Transient**

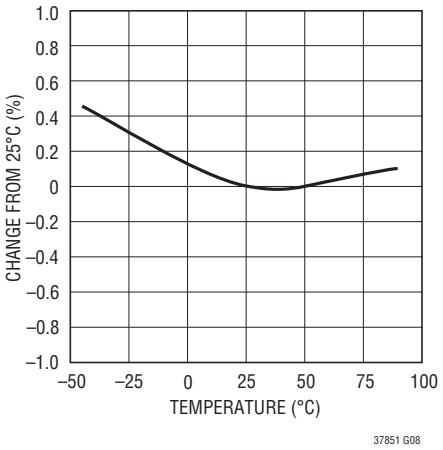


## TYPICAL PERFORMANCE CHARACTERISTICS

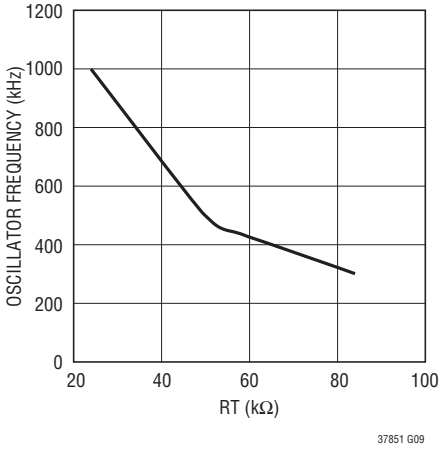
**$V_{FB}$ vs Temperature**



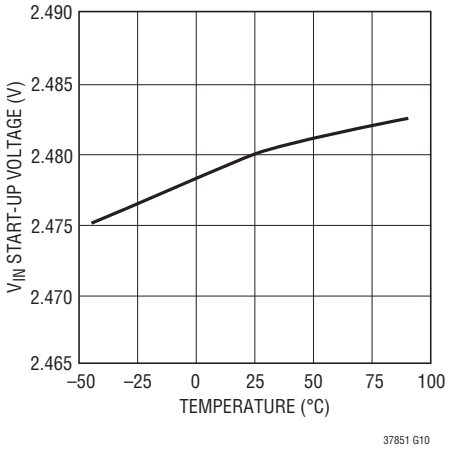

**Normalized Oscillator Frequency vs Temperature**



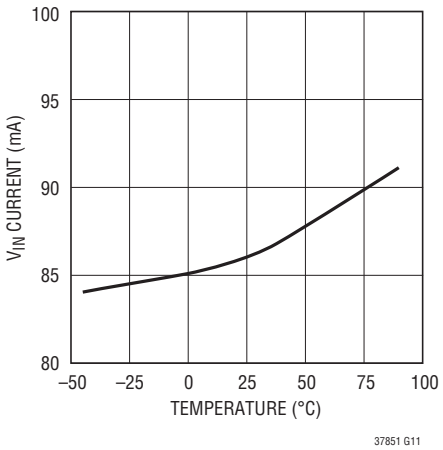

**Oscillator Frequency vs RT**



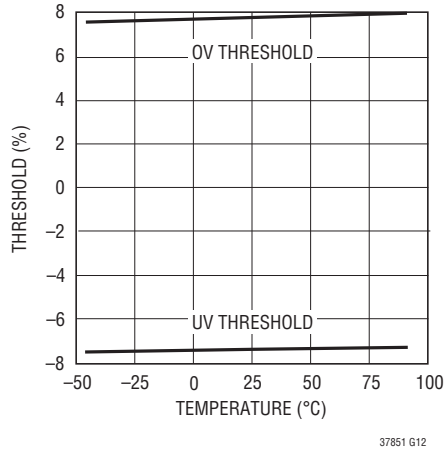

**$V_{IN}$ Start-Up Voltage vs Temperature**




**$V_{IN}$ Burst Quiescent Current vs Temperature**




**OV and UV Thresholds vs Temperature**




## PIN FUNCTIONS

**RUN/SS (Pin 1):** Run Control and Soft-Start Input. An internal 1µA charges the soft-start capacitor and will charge to approximately 2.5V. During a current limit fault, the soft-start capacitor will incrementally discharge. Once the pin drops below 1.225V the IC will enter fault mode, turning off the outputs for 32 times the soft-start time. If >5µA (at RUN/SS = 1.225V) is applied externally, the part will latch off after a fault is detected. If >40µA (at RUN/SS = 1.225V) is applied externally, current limit faults will not discharge the SS capacitor.

**$V_C$ (Pin 2):** Error Amp Output. A frequency compensation network is connected from this pin to the FB pin to compensate the loop. See the section Closing the Feedback Loop in the Applications Information section for guidelines.

**FB (Pin 3):** Feedback Pin. Connect resistor divider tap here. The feedback reference voltage is typically 1.225V The output voltage can be adjusted from 2.7V to 10V according to the following formula:

$$V_{OUT} = 1.225V \bullet \frac{R1+R2}{R2}$$

## PIN FUNCTIONS

**$V_{SENSE}$ (Pin 4):** Overvoltage and Undervoltage Sense. The overvoltage threshold is internally set 7.5% above the regulated FB voltage and the undervoltage threshold is internally set 7.5% below the FB regulated voltage. This pin can be tied to FB but to optimize the response time it is recommended that a separate voltage divider from $V_{OUT}$ be applied. The divider can be skewed from the feedback value to achieve the desired UV or OV threshold.

**$I_{LSET}$ (Pin 5):** Current Limit Set. A resistor from this pin to ground sets the current limit threshold from the $I_{SVIN}$ and $I_{SSW1}$ pins.

**CCM (Pin 6):** Continuous Conduction Mode Control Pin. When set low, the inductor current is allowed to go slightly negative (–15mV referenced to the $I_{SVOUT}$ – $I_{SSW2}$ pins). When driven high, the reverse current limit is set to the similar value of the forward current limit set by the $I_{LSET}$ pin.

**RT (Pin 7):** Oscillator Programming Pin. A resistor from this pin to GND sets the free-running frequency of the IC. $f_{OSC} \cong 2.5e10/RT$.

**MODE (Pin 8):** Burst Mode Control Pin.

- MODE = High: Enable Burst Mode Operation. In Burst Mode operation the operation is variable frequency, which provides a significant efficiency improvement at light loads. The Burst Mode operation will continue until the pin is driven low.
- MODE = Low: Disable Burst Mode operation and maintain low noise, constant frequency operation.

**PGOOD (Pin 9):** Open Drain Output. PGOOD is pulled to ground when the voltage on $V_{SENSE}$ is not within ±7.5% of its setpoint. PGOOD will also be pulled low when the part is in shutdown or input UVLO.

**$I_{SVOUT}$ (Pin 10):** Reverse Current Limit Comparator Noninverting Input. This pin is normally connected to the drain of the N-channel MOSFET D (TG2 driven).

**$V_{BST2}$ (Pin 11):** Boosted Floating Driver Supply for Boost Switch D. This pin will swing from a diode below $V_{CC}$ up to $V_{OUT} + V_{CC} – V_{DIODE}$.

**SW2 (Pin 13):** Ground Reference for Driver D. Gate drive from TG2 will reference to the common point of output switches C and D.

**$I_{SSW2}$ (Pin 14):** Reverse Current Limit Comparator Inverting Input. This pin is normally connected to the source of the N-channel MOSFET D (TG2 driven).

**$V_{DRV}$ (Pin 16):** Driver Supply for Ground Referenced Switches. Connect this pin to $V_{CC}$ potential.

**BG1, BG2 (Pins 17, 15):** Bottom gate driver pins drive the ground referenced N-channel MOSFET switches B and C.

**$I_{SSW1}$ (Pin 18):** Forward Current Limit Comparator Noninverting Input. This pin is normally connected to the source of the N-channel MOSFET A (TG1 driven).

**SW1 (Pin 19):** Ground Reference for Driver A. Gate drive from TG1 will reference to the common point of output switches A and B.

**TG1, TG2 (Pins 20, 12):** Top gate drive pins drive the top N-channel MOSFET switches A and D with a voltage swing equal to $V_{CC} – V_{DIODE}$ superimposed on the SW1 and SW2 nodes respectively.

**$V_{BST1}$ (Pin 21):** Boosted Floating Driver Supply for the Buck Switch A. This pin will swing from a diode below $V_{CC}$ up to $V_{IN} + V_{CC} – V_{DIODE}$.

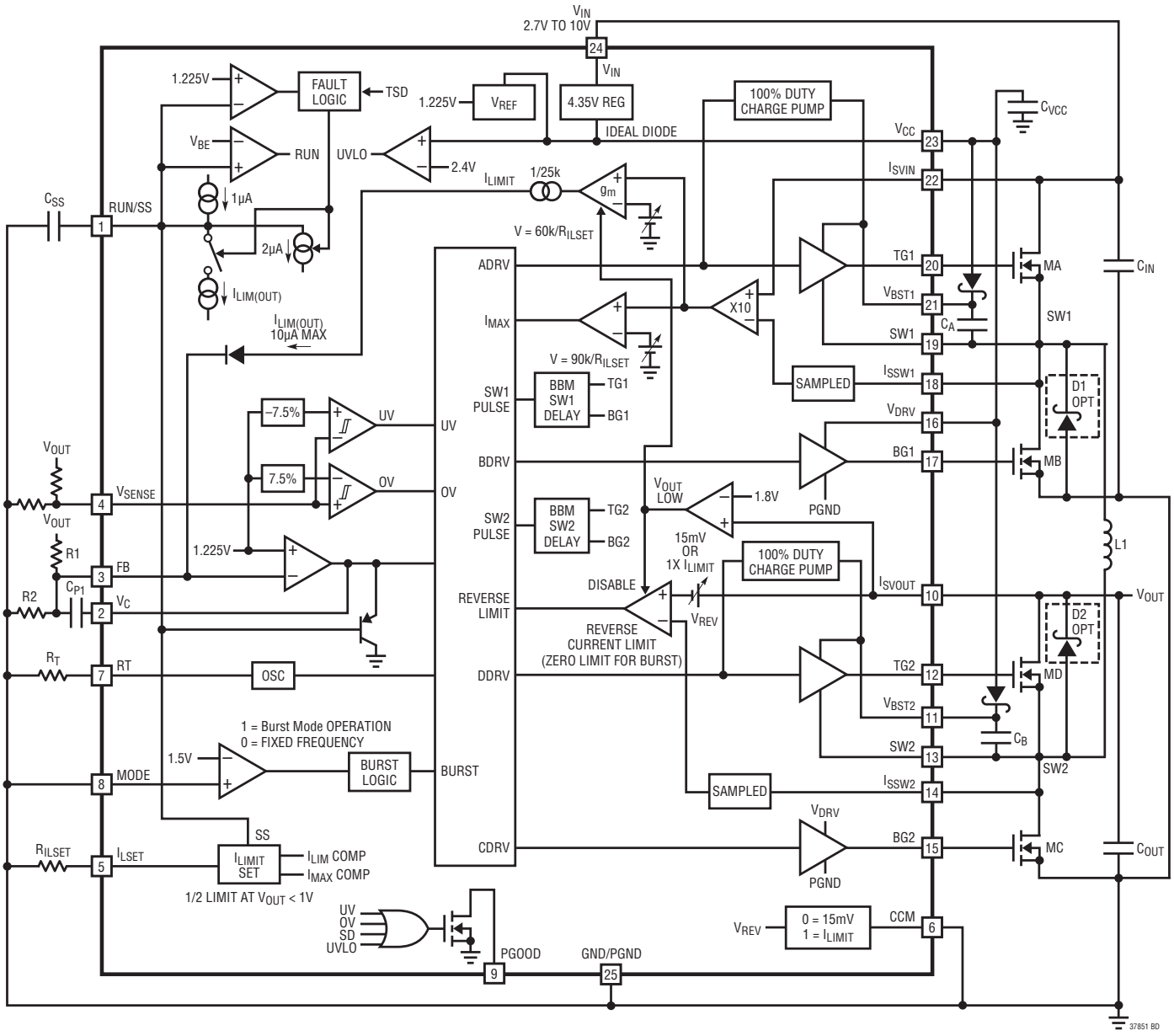
**$I_{SVIN}$ (Pin 22):** Forward Current Limit Comparator Inverting Input. This pin is normally connected to the drain of N-channel MOSFET A (TG1 driven).

**$V_{CC}$ (Pin 23):** Internal 4.35V LDO Regulator Output. The driver and control circuits are powered from this voltage to limit the maximum VGS drive voltage. Decouple this pin to power ground with at least a 4.7µF ceramic capacitor. For low $V_{IN}$ applications, $V_{CC}$ can be bootstrapped from $V_{OUT}$ through a Schottky diode.

**$V_{IN}$ (Pin 24):** Input Supply Pin for the $V_{CC}$ Regulator. A ceramic capacitor of at least 10µF is recommended close to the $V_{IN}$ and GND pins.

**Exposed Pad (Pin 25):** The GND and PGND pins are connected to the Exposed Pad which must be connected to the PCB ground for electrical contact and rated thermal performance.

## BLOCK DIAGRAM



## OPERATION

### MAIN CONTROL LOOP

The LTC3785-1 is a buck-boost voltage mode controller that provides an output voltage above, equal to or below the input voltage.

The LTC proprietary topology and control architecture also employs drain-to-source sensing (No $R_{SENSE}$) for forward and reverse current limiting. The controller provides all N-channel MOSFET output switch drive, facilitating single package multiple power switch technology along with lower $R_{DS(ON)}$. The error amp output voltage ($V_C$) determines the output duty cycle of the switches. Since the $V_C$ pin is a filtered signal, it provides rejection of high frequency noise.

The FB pin receives the voltage feedback signal, which is compared to the internal reference voltage by the error amplifier. The top MOSFET drivers are biased from a floating bootstrap capacitor, which is normally recharged during each off cycle through an external diode when the top MOSFET turns off. Optional Schottky diodes can be connected across synchronous switch B and D to provide a lower drop during the dead time and eliminate efficiency loss due to body diode reverse recovery.

The main control loop is shut down by pulling the RUN/SS pin low. An internal 1µA current source charges the RUN/SS pin and when the pin voltage is higher than 0.7V the IC is enabled. The $V_C$ voltage is then clamped to the RUN/SS voltage minus 0.7V while $C_{SS}$ is slowly charged during start-up. This soft-start clamping prevents inrush current draw from the input power supply.

### POWER SWITCH CONTROL

Figure 1 shows a simplified diagram of how the four power switches are connected to the inductor, $V_{IN}$, $V_{OUT}$ and GND. Figure 2 shows the regions of operation for the LTC3785-1 as a function of duty cycle D. The power switches are properly controlled so that the transfer between modes is continuous.

### Buck Region ($V_{IN} > V_{OUT}$)

Switch D is always on and switch C is always off during buck mode. When the error amp output voltage, $V_C$, is approximately above 0.1V, output A begins to switch. During

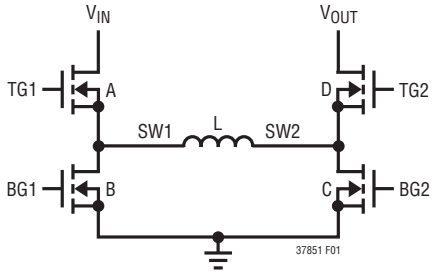



**Figure 1. Response Time Test Circuit**

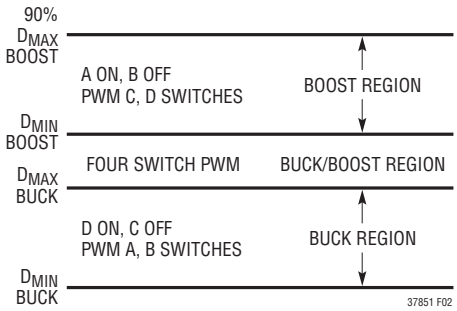



**Figure 1. Response Time Test Circuit**

the off time of switch A, synchronous switch B turns on for the remainder of the switching period. Switches A and B will alternate similar to a typical synchronous buck regulator. As the control voltage increases, the duty cycle of switch A increases until the max duty cycle of the converter in buck mode reaches $D_{MAX\_BUCK}$, given by:

$$D_{MAX\_BUCK} = 100 – D4(SW)\%$$

where D4(SW) = duty cycle % of the four switch range.

$$D4(SW) = (300ns \bullet f) \bullet 100\%$$

where f = operating frequency, Hz.

Beyond this point the four switch or buck-boost region is reached.

### Buck-Boost or Four Switch ($V_{IN} \sim V_{OUT}$)

When the error amp output voltage, $V_C$, is above approximately 0.65V, switch pair AD remain on for duty cycle $D_{MAX\_BUCK}$, and the switch pair AC begin to phase in. As switch pair AC phases in, switch pair BD phases out accordingly. When the $V_C$ voltage reaches the edge of the buck-boost range, approximately 0.7V, the AC switch pair completely phase out the BD pair, and the boost phase begins at duty cycle, D4(SW).

## OPERATION

The input voltage, $V_{IN}$, where the four switch region begins is given by:

$$V_{IN} = \frac{V_{OUT}}{1-(300ns \bullet f)} V$$

the point at which the four switch region ends is given by:

$$V_{IN} = V_{OUT}(1 - D) = V_{OUT}(1 - 300ns \bullet f)\ V$$

### Boost Region ($V_{IN} < V_{OUT}$)

Switch A is always on and switch B is always off during boost mode. When the error amp output voltage, $V_C$, is approximately above 0.7V, switch pair C and D will alternately switch to provide a boosted output voltage. This operation is typical to a synchronous boost regulator. The maximum duty cycle of the converter is limited to 90% typical.

### Burst Mode OPERATION

During Burst Mode operation, the LTC3785-1 delivers energy to the output until it is regulated and then goes into a sleep state where the outputs are off and the IC is consuming only 86µA. In Burst Mode operation, the output ripple has a variable frequency component, which is dependent upon load current

During the period where the converter is delivering energy to the output, the inductor will reach a peak current determined by an on time, $t_{ON}$, and will terminate at zero current for each cycle. The on time is given by:

$$t_{ON} = \frac{2.4}{V_{IN} \bullet f}$$

where f is the oscillator frequency.

The peak current is given by:

$$I_{PEAK} = \frac{V_{IN}}{L} \bullet t_{ON}$$

$$I_{PEAK} = \frac{2.4}{f \bullet L}$$

So the peak current is independent of $V_{IN}$ and inversely proportional to the f • L product optimizing the energy transfer for various applications.

In Burst Mode operation the maximum output current is given by:

$$I_{OUT(MAX,BURST)} \approx \frac{1.2 \bullet V_{IN}}{f \bullet L \bullet (V_{OUT} + V_{IN})}\ A$$

Burst Mode operation is user-controlled by driving the MODE pin high to enable and low to disable.

### $V_{CC}$ REGULATOR

An internal P-channel low dropout regulator produces 4.35V at the $V_{CC}$ pin from the $V_{IN}$ supply pin. $V_{CC}$ powers the drivers and internal circuitry of the LTC3785-1. The $V_{CC}$ pin regulator can supply a peak current of 100mA and must be bypassed to ground with a minimum of 4.7µF placed directly adjacent to the $V_{CC}$ and GND pins. Good bypassing is necessary to supply the high transient current required by the MOSFET gate drivers and to prevent interaction between channels. If desired, the $V_{CC}$ regulator can be connected to $V_{OUT}$ through a Schottky diode to provide higher gate drive in low input voltage applications. The $V_{CC}$ regulator can also be driven with an external 5V source directly (without a Schottky diode).

### TOPSIDE MOSFET DRIVER SUPPLY ($V_{BST1}$, $V_{BST2}$)

The external bootstrap capacitors connected to the $V_{BST1}$ and $V_{BST2}$ pins supply the gate drive voltage for the topside MOSFET switches A and D. When the top MOSFET switch A turns on, the switch node SW1 rises to $V_{IN}$ and the $V_{BST2}$ pin rises to approximately $V_{IN} + V_{CC}$. When the bottom MOSFET switch B turns on, the switch node SW1 drops low and the boost capacitor is charged through the diode connected to $V_{CC}$. When the top MOSFET switch D turns on, the switch node SW2 rises to $V_{OUT}$ and the $V_{BST2}$ pin rises to approximately $V_{OUT} + V_{CC}$. When the bottom MOSFET switch C turns on, the switch node SW2 drops low and the boost capacitor is charged through the diode connected to $V_{CC}$. The boost capacitors need to store about 100 times the gate charge required by the top MOSFET switch A and D. In most applications a 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate.

## OPERATION

### RUN/SOFT-START (RUN/SS)

The RUN/SS pin serves as the enable to the LTC3785-1, soft-start function, and fault programming. A 1µA current source charges the external capacitor. Once the RUN/SS voltage is above a diode drop(~0.7V) the IC is enabled. Once the IC is enabled, the RUN/SS voltage minus a diode drop (RUN/SS – 0.7V) clamps the output of the error amp ($V_C$) to limit duty cycle. The range of the duty cycle clamping is approximately 0.7V to 1.7V. The RUN/SS pin is clamped to approximately 2.2V. If current limit is reached the pin will begin to discharge with a current determined by the magnitude of inductor current overcurrent limit, but not to exceed 10µA. This function will be described in more detail in the Forward Current Limit section.

### OSCILLATOR

The frequency of operation is set through a resistor from the RT pin to ground where $f \cong (2.5e^{10}/RT)Hz$.

### ERROR AMP

The error amplifier is a voltage mode amplifier with a reference voltage of 1.225V internally connected to the non-inverting input. The loop compensation components are configured around the amplifier to provide loop compensation for the converter. The RUN/SS pin will clamp the error amp output, $V_C$, to provide a soft-start function.

### UNDERVOLTAGE AND OVERVOLTAGE PROTECTION

The LTC3785-1 incorporates overvoltage (OV) and undervoltage (UV) functions for fault protection and transient limitation. Both comparators are connected to the $V_{SENSE}$ pin, which usually has a similar voltage divider as the error amplifier without the compensation. The overvoltage threshold is 7.5% above the reference. The undervoltage threshold is 7.5% below the reference with both comparators having 1.5% hysteresis. During an overvoltage fault, all output switching stops until the fault ceases. During an undervoltage fault, the IC is commanded to run fixed frequency only (disabled Burst Mode operation). If the design requires a tightened threshold to one of the comparator thresholds the voltage divider on the $V_{SENSE}$ pin can be skewed to achieve the threshold. Since the range is a constant, tightening the UV threshold will loosen the OV threshold and vice versa.

### POWER GOOD COMPARATOR

The PGOOD pin is an open-drain output which indicates the status of the buck-boost converter output. The output voltage is monitored at $V_{SENSE}$ via a resistor divider tap from $V_{OUT}$ to GND. The values used for this resistor divider are typically selected to be the same as those used in the error amplifier feedback divider. If the voltage on $V_{SENSE}$ either falls 7.5% below (UV condition) or rises 7.5% above (OV condition) the regulation voltage, the PGOOD open-drain output will pull low signaling the output is out of regulation. Once an out of regulation condition is triggered, the voltage on $V_{SENSE}$ must rise 1.5% above the UV threshold or fall 2% below the OV threshold before the pull-down will turn off. In addition, there is a 15µs deglitch delay to help prevent false trips due to voltage transients caused by line or load steps. Depending upon the application, this delay may be insufficient. A capacitor can be placed from $V_{SENSE}$ to GND to add additional deglitch filtering, ensuring PGOOD doesn't trip during a transient. The PGOOD output will also pull low during shutdown and input undervoltage lockout to indicate these fault conditions.

### FORWARD CURRENT LIMIT

The LTC3785-1 is designed to sense the input current by sampling the voltage across MOSFET A during the on time of the switch (TG1 = High). The sense pins are $I_{SVIN}$ and $I_{SSW1}$. A current sense resistor can be used if increased accuracy is required. The current limit threshold can be programmed with a resistor on the $I_{LSET}$ pin. Once the desired current limit has been chosen, $R_{ILSET}$ can be determined by the following formula:

$$R_{ILSET} = \frac{6000}{R_{DS(ON)A} \bullet I_{LIMIT}}\ \Omega$$

where $R_{DS(ON)A} = R_{DS(ON)}$ of N-channel MOSFET switch A and $I_{LIMIT}$ = current limit in Amps.

Once the voltage between $I_{SVIN}$ and $I_{SSW1}$ exceeds the threshold, current will be sourced out of FB to take control

## OPERATION

of the voltage loop, resulting in a lower output voltage to regulate the input current. This fault condition causes the RUN/SS capacitor to begin discharging. The level of the discharge current depends on how much the current exceeds the programmed threshold. Figure 3 is a simplified diagram of the current sense and fault circuitry. If the current limit fault duration is long enough to discharge the RUN/SS capacitor below 1.225V, the fault latch is set and will cycle the RUN/SS capacitor 16 times (1µA charging and 1µA discharging of the RUN/SS capacitor) to create an off time of 32 times the soft-start time before the outputs are allowed to switch to restart the output voltage. If the current limit fault level exceeds 150% of the programmed $I_{LIMIT}$ level at any time, the $I_{MAX}$ comparator is tripped and output switches B and D are turned on to discharge the inductor current for the remainder of the cycle.

To have the power converter latch off on a fault, a pull-up current between 4µA and 7µA on the RUN/SS pin will allow the RUN/SS capacitor to discharge during an extended fault, but will prevent cycling of the fault which will cause the converter to stay off. One method to implement this is by placing a diode (anode tied to $V_{OUT}$) and a resistor from $V_{OUT}$ to the RUN/SS pin. The current sourced into RUN/SS will be $V_{OUT}$ – 0.7 divided by the resistor value. To ignore all faults source greater than 40µA into the RUN/SS pin (At 1.225V on the RUN/SS pin). Since the maximum fault current is limited, this will prevent any discharging of the RUN/SS capacitor, the soft-start capacitor will need to be sized accordingly to accommodate the extra charging current at start-up.

During an output short-circuit or if $V_{OUT}$ is less than 1.8V, the current limit folds back to 50% of the programmed level.

### REVERSE CURRENT LIMIT

The LTC3785-1 can be programmed to provide full class D operation or allowed to source and sink current equal to the current limit set value. This is achieved by asserting a high level on the CCM pin. To minimize the reverse output current, the CCM pin should be driven low or strapped to ground. During this mode only, –15mV typical is allowed across output switch D and is sensed with the $I_{SVOUT}$ and $I_{SSW2}$ pins.

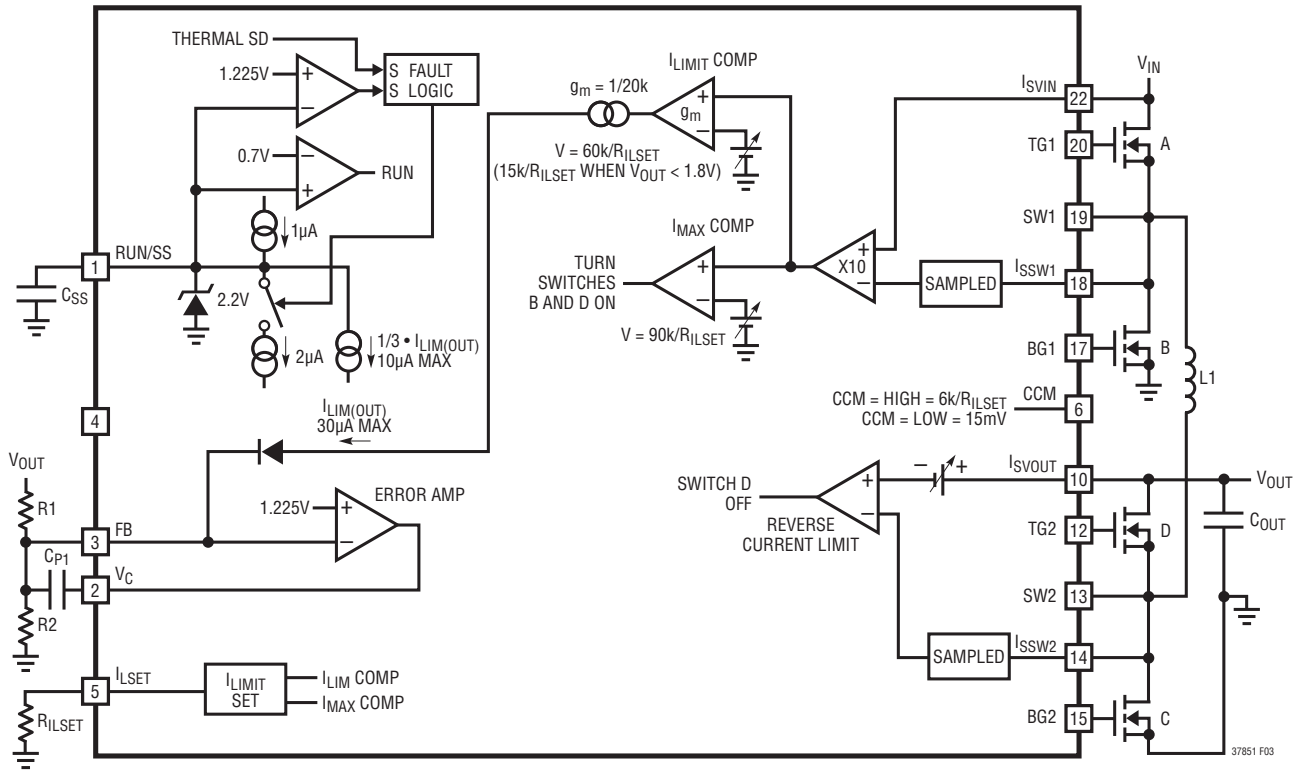



**Figure 3. Block Diagram of Current Limit Fault Circuitry**

## APPLICATIONS INFORMATION

### INDUCTOR SELECTION

The high frequency operation of the LTC3785-1 allows the use of small surface mount inductors. The inductor current ripple is typically set 20% to 40% of the maximum inductor current. For a given ripple the inductance terms are given as follows:

$$L > \frac{V_{IN(MIN)}^2 \bullet \left(V_{OUT} - V_{IN(MIN)}\right) \bullet 100}{f \bullet I_{OUT(MAX)} \bullet \%Ripple \bullet V_{OUT}^2}, \text{ (Boost Mode)}$$

$$L > \frac{V_{OUT} \bullet \left(V_{IN(MAX)} - V_{OUT}\right) \bullet 100}{f \bullet I_{OUT(MAX)} \bullet \%Ripple \bullet V_{IN(MAX)}}, \text{ (Buck Mode)}$$

where:

f = Operating frequency, Hz

%Ripple = Allowable inductor current ripple, %

$V_{IN(MIN)}$ = Minimum input voltage (limit to $V_{OUT}/2$ minimum for worst-case), V

$V_{IN(MAX)}$ = Maximum input voltage, V

$V_{OUT}$ = Output voltage, V

$I_{OUT(MAX)}$ = Maximum output load current, A

For high efficiency choose an inductor with a high frequency core material, such as ferrite, to reduce core loses. The inductor should have low ESR (equivalent series resistance) to reduce the $I^2R$ losses, and must be able to handle the peak inductor current without saturating. Molded chokes or chip inductors usually do not have enough core to support the peak inductor currents in the 3A to 6A region. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor.

### $C_{IN}$ AND $C_{OUT}$ SELECTION

In boost mode, input current is continuous. In buck mode, input current is discontinuous. In buck mode, the selection of input capacitor, $C_{IN}$, is driven by the need to filter the input square wave current. Use a low ESR capacitor, sized to handle the maximum RMS current. For buck operation, the maximum RMS capacitor current is given by:

$$I_{RMS} \sim I_{OUT(MAX)} \bullet \sqrt{\frac{V_{OUT}}{V_{IN}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to derate the capacitor. In boost mode, the discontinuous current shifts from the input to the output, so $C_{OUT}$ must be capable of reducing the output voltage ripple. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady ripple due to charging and discharging the bulk capacitance is given by:

$$V_{RIPPLE\_BOOST} = \frac{I_{OUT(MAX)} \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{C_{OUT} \bullet V_{OUT} \bullet f}$$

$$V_{RIPPLE\_BUCK} = \frac{V_{OUT} \bullet \left(V_{IN(MAX)} - V_{OUT}\right)}{8 \bullet L \bullet C_{OUT} \bullet V_{IN(MAX)} \bullet f^2}$$

where $C_{OUT}$= output filter capacitor, F

The steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{BOOST,ESR} = I_{L(MAX,BOOST)} \bullet ESR$$

$$\Delta V_{BUCK,ESR} = \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \bullet V_{OUT}}{L \bullet f \bullet V_{IN}} \bullet ESR$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient. Capacitors are now available with low ESR and high ripple current ratings such as OS-CON and POSCAP.

### POWER N-CHANNEL MOSFET SELECTION AND EFFICIENCY CONSIDERATIONS

The LTC3785-1 requires four external N-channel power MOSFETs, two for the top switches (switches A and D, shown in Figure 1) and two for the bottom switches

## APPLICATIONS INFORMATION

(switches B and C shown in Figure 1). Important parameters for the power MOSFETs are the breakdown voltage $V_{BR(DSS)}$, threshold voltage $V_{GS(TH)}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance $C_{RSS}$ and maximum current $I_{DS(MAX)}$. The drive voltage is set by the 4.35V $V_{CC}$ supply. Consequently, logic-level threshold MOSFETs must be used in LTC3785-1 applications. If the input voltage is expected to drop below 5V, then sub-logic threshold MOSFETs should be considered. In order to select the power MOSFETs, the power dissipated by the device must be known.

For switch A, the maximum power dissipation happens in boost mode, when it remains on all the time. Its maximum power dissipation at maximum output current is given by:

$$PA(BOOST) = \left(\frac{V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}\right)^2 \bullet \rho T \bullet R_{DS(ON)}$$

where $\rho T$ is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically about 0.4%/°C as shown in Figure 4. For a maximum junction temperature of 125°C, using a value $\rho T$ = 1.5 is reasonable.

Switch B operates in buck mode as the synchronous rectifier. Its power dissipation at maximum output current is given by:

$$PB(BUCK) = \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^2 \bullet \rho T \bullet R_{DS(ON)}$$

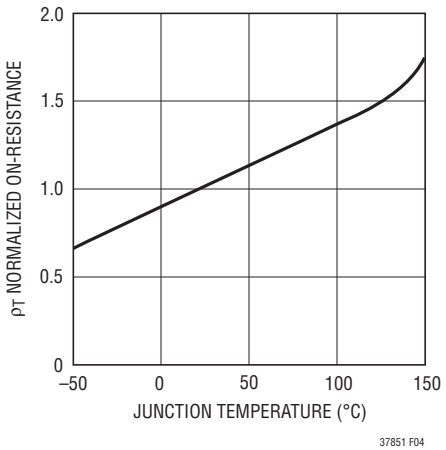



**Figure 4. Normalized $R_{DS(ON)}$ vs Temperature**

Switch C operates in boost mode as the control switch. Its power dissipation at maximum current is given by:

$$PC(BOOST) = \frac{(V_{OUT} - V_{IN}) \bullet V_{OUT}}{V_{IN}^2} \bullet I_{OUT(MAX)}^2 \bullet \rho T \bullet R_{DS(ON)} + k \bullet V_{OUT}^3 \bullet \frac{I_{OUT(MAX)}}{V_{IN}} \bullet C_{RSS} \bullet f$$

where $C_{RSS}$ is usually specified by the MOSFET manufacturers. The constant k, which accounts for the loss caused by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.0.

For switch D, the maximum power dissipation happens in boost mode when its duty cycle is higher than 50%. Its maximum power dissipation at maximum output current is given by:

$$PD(BOOST) = \frac{V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^2 \bullet \rho T \bullet R_{DS(ON)}$$

Typically, switch A has the highest power dissipation and switch B has the lowest power dissipation unless a short occurs at the output. From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P \bullet R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in the equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the case to the ambient temperature ($R_{TH(CA)}$). This value of $T_J$ can then be compared to the original, assumed value used in the iterative calculation process.

### SCHOTTKY DIODE (D1, D2) SELECTION

Optional Schottky diodes D1 and D2 shown in the Block Diagram conduct during the dead time between the conduction of the power MOSFET switches. They are intended to prevent the body diode of synchronous switches B and D from turning on and storing charge during the dead time. In particular, D2 significantly reduces reverse recovery current between switch D turn off and switch C turn on, which improves converter efficiency and reduces switch C voltage stress. In order for D2 to be effective, it must be located in very close proximity to SWD.

## APPLICATIONS INFORMATION

### CLOSING THE FEEDBACK LOOP

The LTC3785-1 incorporates voltage mode control. The control to output gain is given by:

$$G_{Buck} = 1.6 \bullet V_{IN}, \text{ Buck Mode}$$

$$G_{BOOST} = \frac{1.6 \bullet V_{OUT}^2}{V_{IN}}, \text{ Boost Mode}$$

The output filter exhibits a double-pole response and is given by:

$$f_{FILTER\_POLE} = \frac{1}{2 \bullet \pi \bullet \sqrt{L \bullet C_{OUT}}}$$

where $C_{OUT}$ is the output filter capacitor.

The output filter zero is given by:

$$f_{FILTER\_ZERO} = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}}$$

where $R_{ESR}$ is the capacitor equivalent series resistance.

A troublesome feature in boost mode is the right half plane zero (RHP), and is given by:

$$f_{RHPZ} = \frac{V_{IN}^2}{2 \bullet \pi \bullet I_{OUT} \bullet L \bullet V_{OUT}}$$

The loop gain is typically rolled off before the RHP zero frequency.

A simple type I compensation network (Figure 5) can be incorporated to stabilize the loop but at a cost of reduced bandwidth and slower transient response. To ensure proper phase margin, the loop must cross over almost a decade before the L-C double pole.

The unity gain frequency of the error amplifier with the type 1 compensation is given by:

$$f_{UG} = \frac{1}{2 \bullet \pi \bullet R1 \bullet C_{P1}}$$

Most applications demand an improved transient response to allow a smaller output filter capacitor. To achieve a higher bandwidth, type III compensation is required as shown in Figure 6. Two zeros are required to compensate for the double pole response.

$$f_{POLE1} \approx \frac{1}{2 \bullet \pi \bullet 32e3 \bullet C_{P1} \bullet R1} \text{ (a very low frequency)}$$

$$f_{ZERO1} = \frac{1}{2 \bullet \pi \bullet R_Z \bullet C_{P1}}$$

$$f_{ZERO2} = \frac{1}{2 \bullet \pi \bullet R1 \bullet C_{Z1}}$$

$$f_{POLE2} \approx \frac{1}{2 \bullet \pi \bullet R_Z \bullet C_{P2}}$$

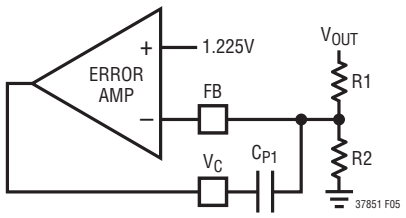



Figure 5. Error Amplifier with Type I Compensation

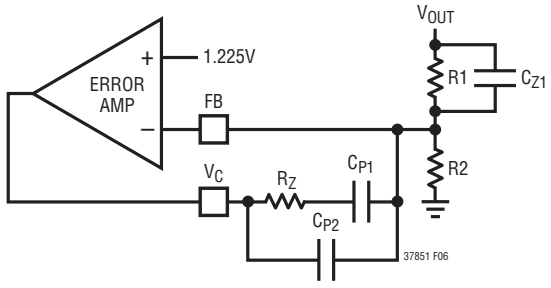



Figure 6. Error Amplifier with Type III Compensation

# APPLICATIONS INFORMATION

## EFFICIENCY CONSIDERATIONS

The percentage efficiency of a switching regulator is equal to the output power divided by the input power times 100%.

It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in circuits produce losses, four main sources account for most of the losses in LTC3785-1 application circuits:

1. DC $I^2R$ losses. These arise from the resistances of the MOSFETs, sensing resistor (if used), inductor and PC board traces and cause the efficiency to drop at high output currents.
2. Transition loss. This loss arises from the brief voltage transition time of switch A or switch C. It depends upon the switch voltage, inductor current, driver strength and MOSFET capacitance, among other factors.

   Transition Loss ~ $V_{SW}^2 \bullet I_L \bullet C_{RSS} \bullet f$

   where $C_{RSS}$ is the reverse transfer capacitance.
3. $C_{IN}$ and $C_{OUT}$ loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator in buck mode. The output capacitor has the more difficult job of filtering the large RMS output current in boost mode. Both $C_{IN}$ and $C_{OUT}$ are required to have low ESR to minimize the AC $I^2R$ loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.
4. Other losses. Optional Schottky diodes D1 and D2 are responsible for conduction losses during dead time and light load conduction periods. Core loss is the predominant inductor loss at light loads. Turning on switch C causes reverse recovery current loss in boost mode. When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased. If there is no change in input current, then there is no change in efficiency.
5. $V_{CC}$ regulator loss. In applications where the input voltage is above 5V, such as two Li-Ion cells, the $V_{CC}$ regulator will dissipate some power due the differential voltage and the average output current to the drive the gates of the output switches. The $V_{CC}$ pin can be driven directly from a high efficiency external 5V source if desired to incrementally improve overall efficiency at lighter loads.

## DESIGN EXAMPLE

As a design example, assume $V_{IN}$ = 2.7V to 10V (3.6V nominal Li-Ion with 9V adapter), $V_{OUT}$ = 3.3V (5%), $I_{OUT(MAX)}$ = 3A and f = 500kHz.

### Determine the Inductor Value

Setting the Inductor Ripple to 40% and using the equations in the Inductor Selection section gives:

$$L > \frac{(2.7)^2 \bullet (3.3-2.7) \bullet 100}{500 \bullet 10^3 \bullet 3 \bullet 40 \bullet (3.3)^2} = 0.67\mu H$$

$$L > \frac{3.3 \bullet (10-3.3) \bullet 100}{500 \bullet 10^3 \bullet 3 \bullet 40 \bullet 10} = 3.7\mu H$$

So the worst-case ripple for this application is during buck mode so a standard inductor value of 3.3µH is chosen.

### Determine the Proper Inductor Type Selection

The highest inductor current is during boost mode and is given by:

$$I_{L(MAX\_AV)} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet \eta}$$

where $\eta$ = estimated efficiency in this mode (use 80%).

$$I_{L(MAX\_AV)} = \frac{3.3 \bullet 3}{2.7 \bullet 0.8} = 4.6A$$

## APPLICATIONS INFORMATION

To limit the maximum efficiency loss of the inductor ESR to below 5% the equation is:

$$ESR_{L(MAX)} \sim \frac{V_{OUT} \bullet I_{OUT} \bullet \%Loss}{I_{L(MAX\_AV)}^2 \bullet 100} = 24m\Omega$$

A suitable inductor for this application could be a Coiltronics CD1-3R8 which has a rating DC current of 6A and ESR of 13mΩ.

### Choose a Proper MOSFET Switch

Using the same guidelines for ESR of the inductor, one suitable MOSFET could be the Siliconix Si7940DP which is a dual MOSFET in a surface mount package with 25mΩ at 2.5V and a total gate charge of 12nC.

Checking the power dissipation of each switch will ensure reliable operation since the thermal resistance of the package is 60°C/W.

The maximum power dissipation of switch A and C occurs in boost mode. Assuming a junction temperature of $T_J$ = 100°C with $\rho_{100C}$ = 1.3, the power dissipation at $V_{IN}$ = 2.7, and using the equations from the Efficiency Considerations section:

$$PA(BOOST) = \left(\frac{3.3}{2.7} \bullet 3\right)^2 \bullet 1.3 \bullet 0.025 = 0.43W$$

$$PC(BOOST) = \frac{(3.3 - 2.7) \bullet 3.3}{2.7^2} \bullet 3^2 \bullet 1.3 \bullet 0.025 + 1 \bullet 3.3^3 \bullet \frac{3}{2.7} \bullet 0.45 - 9 \bullet 500 \bullet 10^3 = 0.09W$$

The maximum power dissipation of switch B and D occurs in buck mode and is given by:

$$PB(BUCK) = \frac{10 - 3.3}{10} \bullet 3^2 \bullet 1.3 \bullet 0.025 = 0.20W$$

$$PD(BOOST) = \frac{3.3}{10} \bullet 3^2 \bullet 1.3 \bullet 0.025 = 0.10W$$

Now to double check the $T_J$ of the package with 50°C ambient. Since this is a dual NMOS package we can add switches A + B and C + D worst-case. For applications where the MOSFETs are in separate packages each device's maximum $T_J$ would have to be calculated.

$$T_{J(PKG1)} = T_A + \theta_{JA}(PA + PB)$$
$$= 50 + 60 \bullet (0.43 + 0.20) = 88°C$$

$$T_{J(PKG2)} = T_A + \theta_{JA}(PC + PD)$$
$$= 50 + 60 \bullet (0.09 + 0.10) = 60°C$$

### Set The Maximum Current Limit

The equation for setting the maximum current limit of the IC is given by:

$$R_{ILSET} = \frac{6000}{R_{DS(ON)A} \bullet I_{LIMIT}}\ \Omega$$

The maximum current is set 25% above $I_{L(PEAK)}$ to account for worst-case variation at 100°C = 6A.

$$R_{ILSET} = \frac{6000}{0.025 \bullet 6} = 42k$$

### Choose the Input and Output Capacitance

The input capacitance should filter current ripple which is worst-case in buck mode. Since the input current could reach 6A, a capacitor ESR of 10mΩ or less will yield an input ripple of 60mV.

The output capacitance should filter current ripple which is worst in boost mode, but is usually dictated by the loop response, the maximum load transient and the allowable transient response.

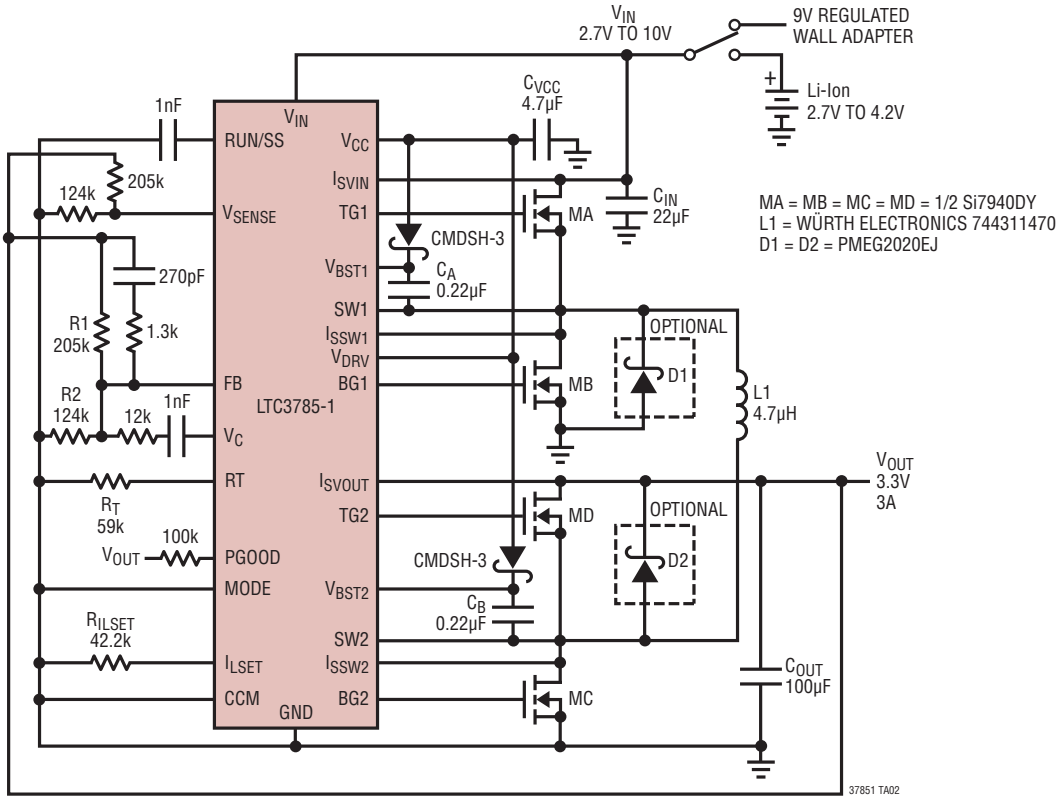
## APPLICATIONS INFORMATION

### PC BOARD LAYOUT CHECKLIST

The basic PC board layout requires a dedicated ground plane layer. Also, for high current, a multilayer board provides heat sinking for power components.

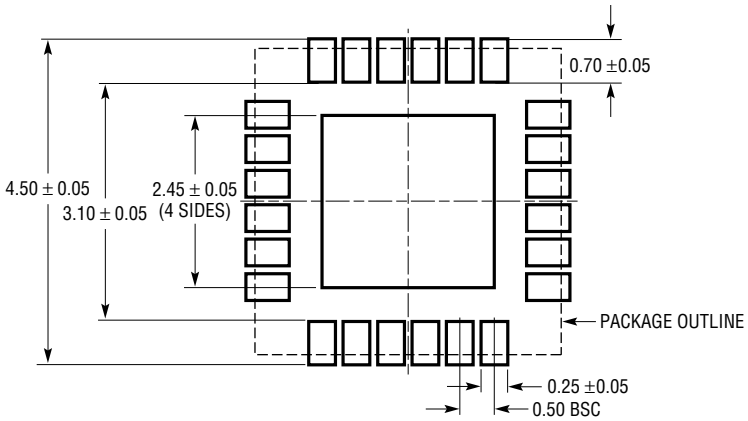
- The ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs.
- Place $C_{IN}$, switch A, switch B and D1 in one compact area. Place $C_{OUT}$, switch C, switch D and D2 in one compact area.
- Use immediate vias to connect the components (including the LTC3785-1's GND/PGND pin) to the ground plane. Use several large vias for each power component.
- Use planes for $V_{IN}$ and $V_{OUT}$ to maintain good voltage filtering and to keep power losses low.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to any DC net ($V_{IN}$ or GND). When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3785-1.
- Segregate the signal and power grounds. All small-signal components should return to the GND pin at one point. The sources of switch B and switch C should also connect to one point at the GND of the IC.
- Place switch B and switch C as close to the controller as possible, keeping the PGND, BG and SW traces short.
- Keep the high dV/dT SW1, SW2, $V_{BST1}$, $V_{BST2}$, TG1 and TG2 nodes away from sensitive small-signal nodes.
- The path formed by switch A, switch B, D1 and the $C_{IN}$ capacitor should have short leads and PC trace lengths. The path formed by switch C, switch D, D2 and the $C_{OUT}$ capacitor also should have short leads and PC trace lengths.
- The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor.
- Connect the $V_{CC}$ decoupling capacitor $C_{VCC}$ closely to the $V_{CC}$ and PGND pins.
- Connect the top driver boost capacitor $C_A$ closely to the $V_{BST1}$ and SW1 pins. Connect the top driver boost capacitor $C_B$ closely to the $V_{BST2}$ and SW2 pins.
- Connect the input capacitors $C_{IN}$ and output capacitors $C_{OUT}$ close to the power MOSFETs. These capacitors carry the MOSFET AC current in boost and buck mode.
- Connect FB and $V_{SENSE}$ pin resistive dividers to the (+) terminals of $C_{OUT}$ and signal ground. If a small $V_{SENSE}$ decoupling capacitor is used, it should be as close as possible to the LTC3785-1 GND pin.
- Route $I_{SVIN}$ and $I_{SSW1}$ leads together with minimum PC trace spacing. Ensure accurate current sensing with Kelvin connections across MOSFET A or sense resistor.
- Route $I_{SVOUT}$ and $I_{SSW2}$ leads together with minimum PC trace spacing. Ensure accurate current sensing with Kelvin connections across MOSFET D or sense resistor.
- Connect the feedback network close to IC, between the $V_C$ and FB pins.

## TYPICAL APPLICATION

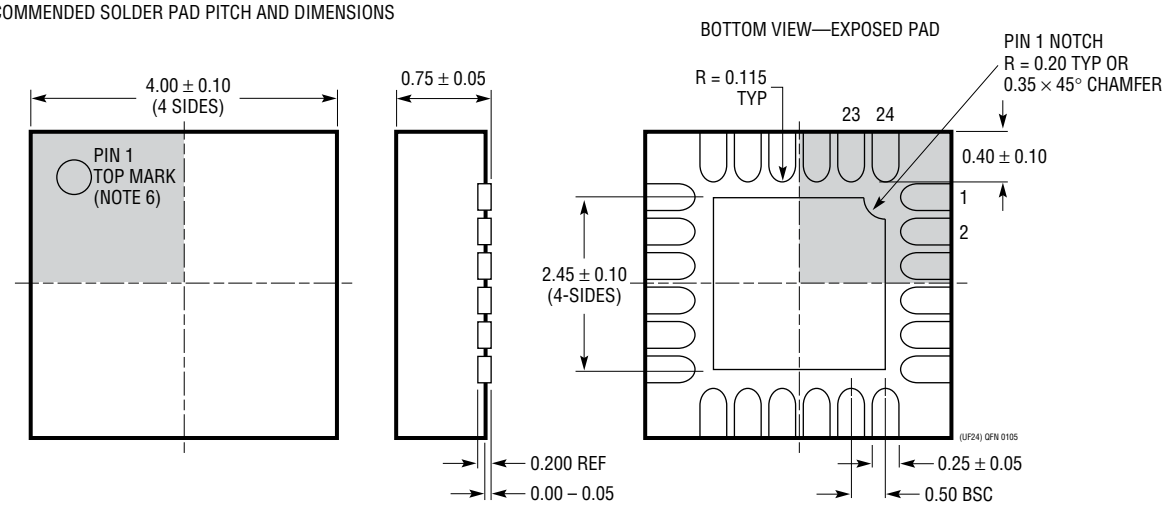


# PACKAGE DESCRIPTION

**UF Package**
**24-Lead Plastic QFN (4mm × 4mm)**
(Reference LTC DWG # 05-08-1697 Rev B)



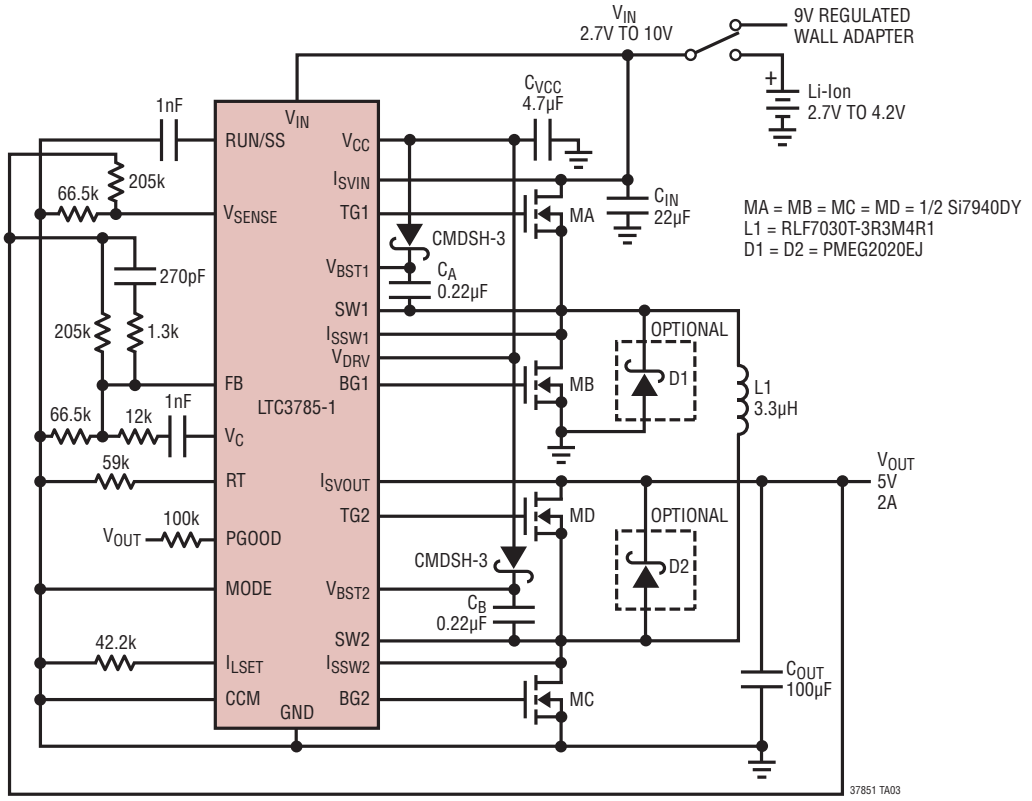

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS




NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

## TYPICAL APPLICATION

**Li-Ion/9V Wall Adapter to 5V/2A**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC3443 | 1.2A $I_{OUT}$, 600kHz, Synchronous Buck-Boost DC/DC Converter | $V_{IN}$: 2.4V to 5.5V, $V_{OUT}$: 2.4V to 5.25V, $I_Q$ = 28µA, $I_{SD}$ < 1µA, MS Package |
| LTC3444 | 500mA $I_{OUT}$, 1.5MHz Synchronous Buck-Boost DC/DC Converter | $V_{IN}$: 2.7V to 5.5V, $V_{OUT}$: 0.5V to 5.25V, Optimized for WCDMA RF Amplifier Bias |
| LTC3531/ LTC3531-3/ LTC3531-3.3 | 200mA $I_{OUT}$, Synchronous Buck-Boost DC/DC Converter | $V_{IN}$: 1.8V to 5.5V, $V_{OUT}$: 2V to 5V, $I_Q$ = 35µA, $I_{SD}$ < 1µA, MS, DFN Packages |
| LTC3532 | 500mA $I_{OUT}$, 2MHz, Synchronous Buck-Boost DC/DC Converter | $V_{IN}$: 2.4V to 5.5V, $V_{OUT}$: 2.4V to 5.25V, $I_Q$ = 35µA, $I_{SD}$ < 1µA, MS, DFN Packages |
| LTC3533 | 2A Wide Input Voltage Synchronous Buck-Boost DC/DC Converter | $V_{IN}$: 1.8V to 5.5V, $V_{OUT}$: 1.8V to 5.25V, $I_Q$ = 40µA, $I_{SD}$ < 1µA, DFN Package |
| LTC3780 | High Efficiency, Synchronous, 4-Switch Buck-Boost Controller | $V_{IN}$: 4V to 36V, $V_{OUT}$: 0.8V to 30V, $I_Q$ = 1.5mA, $I_{SD}$ < 55µA, SSOP-24, QFN-32 Packages |
| LTC3785 | 10V, High Efficiency, Synchronous, No $R_{SENSE}$, Buck-Boost Controller | $V_{IN}$: 2.7V to 10V, $V_{OUT}$: 2.7V to 10V, $I_Q$ = 86mA, $I_{SD}$ < 15µA, QFN-24 Package |
| LTM4605 | 5A to 12A Buck-Boost µModule | 4.5V ≤ $V_{IN}$ ≤ 20V, 0.8V ≤ $V_{OUT}$ ≤ 16V, 15mm × 15mm × 2.8mm LGA Package |
| LTM4607 | 5A to 12A Buck-Boost µModule | 4.5V ≤ $V_{IN}$ ≤ 36V, 0.8V ≤ $V_{OUT}$ ≤ 24V, 15mm × 15mm × 2.8mm LGA Package |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