Dual/Quad Low Noise, High Speed Precision Op Amps

FEATURES

- 100% Tested Low Voltage Noise:
  2.7nV/√Hz Typ
  4.2nV/√Hz Max
- Slew Rate: 4.5V/μs Typ
- Gain-Bandwidth Product: 12.5MHz Typ
- Offset Voltage,
  Prime Grade: 70μV Max
  Low Grade: 100μV Max
- High Voltage Gain: 5 Million Min
- Supply Current Per Amplifier: 2.75mA Max
- Common Mode Rejection: 112dB Min
- Power Supply Rejection: 116dB Min
- Available in 8-Pin SO Package

APPLICATIONS

- Two and Three Op Amp Instrumentation Amplifiers
- Low Noise Signal Processing
- Active Filters
- Microvolt Accuracy Threshold Detection
- Strain Gauge Amplifiers
- Direct Coupled Audio Gain Stages
- Tape Head Preamplifiers
- Infrared Detectors

DESCRIPTION

The LT®1124 dual and LT1125 quad are high performance op amps that offer higher gain, slew rate and bandwidth than the industry standard OP-27 and competing OP-270/OP-470 op amps. In addition, the LT1124/LT1125 have lower I_B and I_{OS} than the OP-27; lower V_{OS} and noise than the OP-270/OP-470.

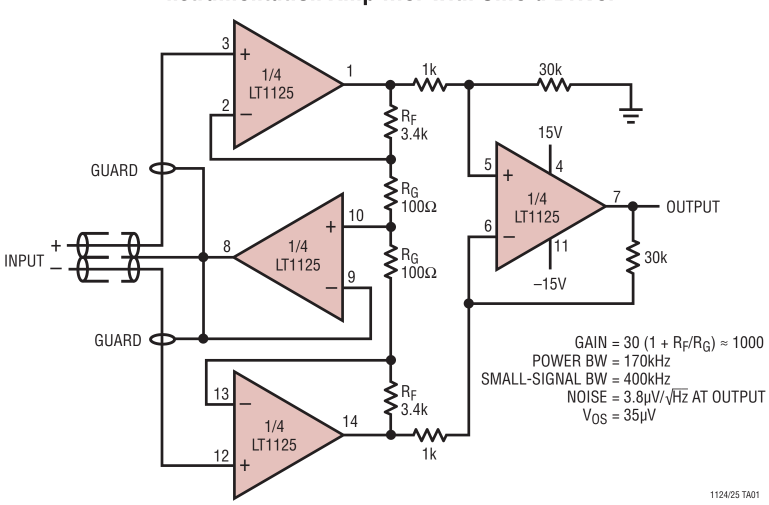
In the design, processing and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Slew rate, gain bandwidth and 1kHz noise are 100% tested for each individual amplifier. Consequently, the specifications of even the lowest cost grades (the LT1124C and the LT1125C) have been spectacularly improved compared to equivalent grades of competing amplifiers.

Power consumption of the LT1124 is one-half of two OP-27s. Low power and high performance in an 8-pin SO package make the LT1124 a first choice for surface mounted systems and where board space is restricted.

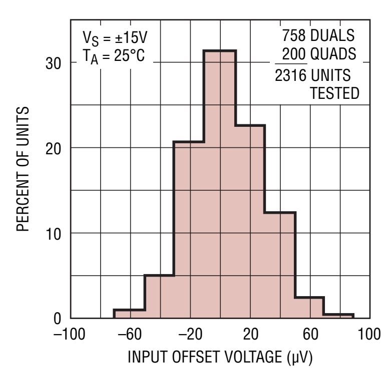
For a decompensated version of these devices, with three times higher slew rate and bandwidth, please see the LT1126/LT1127 data sheet.

TYPICAL APPLICATION

Instrumentation Amplifier with Shield Driver



Input Offset Voltage Distribution (All Packages, LT1124 and LT1125)



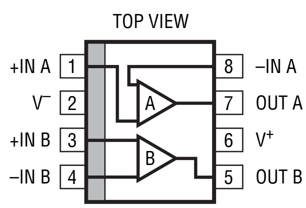
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage .... ±22V
Input Voltages .... Equal to Supply Voltage
Output Short-Circuit Duration .... Indefinite
Differential Input Current (Note 6) .... ±25mA
Lead Temperature (Soldering, 10 sec) .... 300°C
Storage Temperature Range .... –65°C to 150°C

Operating Temperature Range
- LT1124AC/LT1124C
- LT1125AC/LT1125C (Note 10) .... –40°C to 85°C
- LT1124AI/LT1124I .... –40°C to 85°C
- LT1124AMP/LT1125MP .... –55°C to 125°C
- LT1124AM/LT1124M
- LT1125AM/LT1125M
- **OBSOLETE** .... –55°C to 125°C

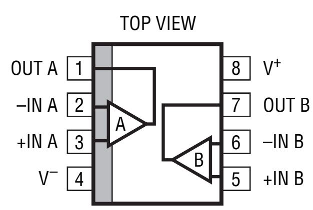
PIN CONFIGURATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 140°C, θ_{JA} = 190°C/W

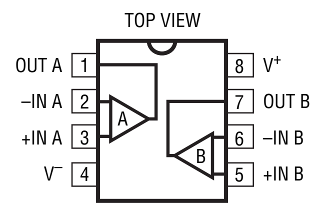
NOTE: THIS PIN CONFIGURATION DIFFERS FROM THE 8-PIN PDIP CONFIGURATION. INSTEAD, IT FOLLOWS THE ROTATED LT1013DS8 SO PACKAGE PIN LOCATIONS



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 190°C/W

OBSOLETE PINOUT



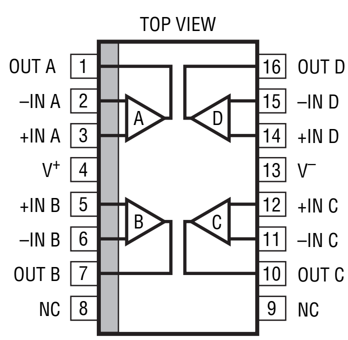
N8 PACKAGE
8-LEAD PDIP

T_{JMAX} = 140°C, θ_{JA} = 130°C/W

J8 PACKAGE
8-LEAD CERAMIC DIP

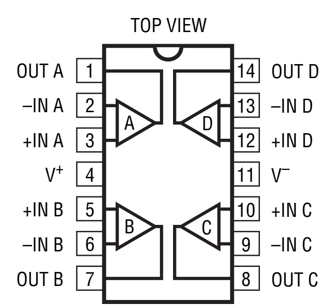
T_{JMAX} = 160°C, θ_{JA} = 100°C/W

OBSOLETE PACKAGE
Consider the N8 for Alternate Source



SW PACKAGE
16-LEAD PLASTIC SO WIDE

T_{JMAX} = 140°C, θ_{JA} = 130°C/W



N PACKAGE
14-LEAD PDIP

T_{JMAX} = 140°C, θ_{JA} = 110°C/W (N)

J PACKAGE
14-LEAD CERAMIC DIP

T_{JMAX} = 160°C, θ_{JA} = 80°C/W

OBSOLETE PACKAGE
Consider the N for Alternate Source

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1124CS8#PBF	LT1124CS8#TRPBF	1124	8-Lead Plastic SO, Rotated Pinout	0°C to 70°C
LT1124AIS8#PBF	LT1124AIS8#TRPBF	1124AI	8-Lead Plastic SO, Rotated Pinout	–40°C to 85°C
LT1124IS8#PBF	LT1124IS8#TRPBF	1124I	8-Lead Plastic SO, Rotated Pinout	–40°C to 85°C
LT1124AMPS8#PBF	LT1124AMPS8#TRPBF	124AMP	8-Lead Plastic SO, Rotated Pinout	–55°C to 125°C
LT1124CS8-1#PBF	LT1124CS8-1#TRPBF	11241	8-Lead Plastic SO, Standard Pinout	0°C to 70°C
LT1124AIS8-1#PBF	LT1124AIS8-1#TRPBF	11241	8-Lead Plastic SO, Standard Pinout	–40°C to 85°C
LT1124IS8-1#PBF	LT1124IS8-1#TRPBF	11241	8-Lead Plastic SO, Standard Pinout	–40°C to 85°C
LT1124AMPS8-1#PBF	LT1124AMPS8-1#TRPBF	11241	8-Lead Plastic SO, Standard Pinout	–55°C to 125°C
OBSOLETE PINOUT				
LT1125CSW#PBF	LT1125CSW#TRPBF	LT1125CSW	16-Lead Plastic SO Wide	0°C to 70°C
LT1125MPSW	LT1125MPSW#TR	LT1125MPSW	16-Lead Plastic SO Wide	–55°C to 125°C
LT1124ACN8#PBF	LT1124ACN8#TRPBF	LT1124ACN8	8-Lead PDIP	0°C to 70°C
LT1124CN8#PBF	LT1124CN8#TRPBF	LT1124CN8	8-Lead PDIP	0°C to 70°C
LT1125ACN#PBF	LT1125ACN#TRPBF	LT1125ACN	14-Lead PDIP	0°C to 70°C
LT1125CN#PBF	LT1125CN#TRPBF	LT1125CN	14-Lead PDIP	0°C to 70°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**SPECIFIED TEMPERATURE RANGE**
LT1124CS8	LT1124CS8#TR	1124	8-Lead Plastic SO, Rotated Pinout	0°C to 70°C
LT1124AIS8	LT1124AIS8#TR	1124AI	8-Lead Plastic SO, Rotated Pinout	–40°C to 85°C
LT1124IS8	LT1124IS8#TR	1124I	8-Lead Plastic SO, Rotated Pinout	–40°C to 85°C
LT1125CSW	LT1125CSW#TR	LT1125CSW	16-Lead Plastic SO Wide	0°C to 70°C
LT1124ACN8	LT1124ACN8#TR	LT1124ACN8	8-Lead PDIP	0°C to 70°C
LT1124CN8	LT1124CN8#TR	LT1124CN8	8-Lead PDIP	0°C to 70°C
LT1125ACN	LT1125ACN#TR	LT1125ACN	14-Lead PDIP	0°C to 70°C
LT1125CN	LT1125CN#TR	LT1125CN	14-Lead PDIP	0°C to 70°C
LT1124CJ8	LT1124CJ8#TR	LT1124CJ8	8-Lead CERAMIC DIP	0°C to 70°C
LT1124AMJ8	LT1124AMJ8#TR	LT1124AMJ8	8-Lead CERAMIC DIP	–55°C to 125°C
LT1124MJ8	LT1124MJ8#TR	LT1124MJ8	8-Lead CERAMIC DIP	–55°C to 125°C
LT1125CJ	LT1125CJ#TR	LT1125CJ	14-Lead CERAMIC DIP	0°C to 70°C
LT1125AMJ	LT1125AMJ#TR	LT1125AMJ	14-Lead CERAMIC DIP	–55°C to 125°C
LT1125MJ	LT1125MJ#TR	LT1125MJ	14-Lead CERAMIC DIP	–55°C to 125°C
OBSOLETE PACKAGE				

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = ±15V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)	LT1124AC/AI/AM LT1125AC/AM MIN	TYP	MAX	LT1124C/I/M LT1125C/M MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1124 LT1125		20 25	70 90		25 30	100 140	µV µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long-Term Input Offset Voltage Stability			0.3			0.3		µV/Mo
I_{OS}	Input Offset Current	LT1124 LT1125		5 6	15 20		6 7	20 30	nA nA
I_B	Input Bias Current			±7	±20		±8	±30	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Notes 8, 9)		70	200		70		nV_{P-P}
	Input Noise Voltage Density	f_O = 10Hz (Note 5) f_O = 1000Hz (Note 3)		3.0 2.7	5.5 4.2		3.0 2.7	5.5 4.2	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f_O = 10Hz f_O = 1000Hz		1.3 0.3			1.3 0.3		$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
V_{CM}	Input Voltage Range		±12	±12.8		±12	±12.8		V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±12V	112	126		106	124		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4V to ±18V	116	126		110	124		dB
A_{VOL}	Large-Signal Voltage Gain	R_L ≥ 10k, V_{OUT} = ±10V R_L ≥ 2k, V_{OUT} = ±10V	5 2	17 4		3.0 1.5	15 3		V/µV V/µV
V_{OUT}	Maximum Output Voltage Swing	R_L ≥ 2k	±13	±13.8		±12.5	±13.8		V
SR	Slew Rate	R_L ≥ 2k (Notes 3, 7)	3	4.5		2.7	4.5		V/µs
GBW	Gain-Bandwidth Product	f_O = 100kHz (Note 3)	9	12.5		8	12.5		MHz
Z_O	Open-Loop Output Resistance	V_{OUT} = 0, I_{OUT} = 0		75			75		Ω
I_S	Supply Current per Amplifier			2.3	2.75		2.3	2.75	mA
	Channel Separation	f ≤ 10Hz (Note 9) V_{OUT} = ±10V, R_L = 2k	134	150		130	150		dB

The ● denotes the specifications which apply over the –55°C ≤ T_A ≤ 125°C temperature range, V_S = ±15V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)		LT1124AM LT1125AM MIN	TYP	MAX	LT1124M LT1125M MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1124 LT1125	● ●		50 55	170 190		60 70	250 290	µV µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 5)	●		0.3	1.0		0.4	1.5	µV/°C
I_{OS}	Input Offset Current	LT1124 LT1125	● ●		18 18	45 55		20 20	60 70	nA nA
I_B	Input Bias Current		●		±18	±55		±20	±70	nA
V_{CM}	Input Voltage Range		●	±11.3	±12		±11.3	±12		V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±11.3V	●	106	122		100	120		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4V to ±18V	●	110	122		104	120		dB
A_{VOL}	Large-Signal Voltage Gain	R_L ≥ 10k, V_{OUT} = ±10V R_L ≥ 2k, V_{OUT} = ±10V	● ●	3 1	10 3		2.0 0.7	10 2		V/µV V/µV
V_{OUT}	Maximum Output Voltage Swing	R_L ≥ 2k	●	±12.5	±13.6		±12	±13.6		V
SR	Slew Rate	R_L ≥ 2k (Notes 3, 7)	●	2.3	3.8		2	3.8		V/µs
I_S	Supply Current per Amplifier		●		2.5	3.25		2.5	3.25	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the 0°C ≤ T_A ≤ 70°C temperature range, V_S = ±15V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)		LT1124AC LT1125AC MIN	TYP	MAX	LT1124C LT1125C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1124 LT1125	● ●		35 40	120 140		45 50	170 210	μV μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 5)	●		0.3	1		0.4	1.5	μV/°C
I_{OS}	Input Offset Current	LT1124 LT1125	● ●		6 7	25 35		7 8	35 45	nA nA
I_B	Input Bias Current		●		±8	±35		±9	±45	nA
V_{CM}	Input Voltage Range		●	±11.5	±12.4		±11.5	±12.4		V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±11.5V	●	109	125		102	122		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4V to ±18V	●	112	125		107	122		dB
A_{VOL}	Large-Signal Voltage Gain	R_L ≥ 10k, V_{OUT} = ±10V R_L ≥ 2k, V_{OUT} = ±10V	● ●	4.0 1.5	15 3.5		2.5 1.0	14 2.5		V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	R_L ≥ 2k	●	±12.5	±13.7		±12	±13.7		V
SR	Slew Rate	R_L ≥ 2k (Notes 3, 7)	●	2.6	4		2.4	4		V/μs
I_S	Supply Current per Amplifier		●		2.4	3		2.4	3	mA

The ● denotes the specifications which apply over the –40°C ≤ T_A ≤ 85°C temperature range, V_S = ±15V, unless otherwise noted. (Note 10)

SYMBOL	PARAMETER	CONDITIONS (Note 2)		LT1124AC/AI LT1125AC MIN	TYP	MAX	LT1124C/I LT1125C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1124 LT1125	● ●		40 45	140 160		50 55	200 240	μV μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 5)	●		0.3	1		0.4	1.5	μV/°C
I_{OS}	Input Offset Current	LT1124 LT1125	● ●		15 15	40 50		17 17	55 65	nA nA
I_B	Input Bias Current		●		±15	±50		±17	±65	nA
V_{CM}	Input Voltage Range		●	±11.4	±12.2		±11.4	±12.2		V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±11.4V	●	107	124		101	121		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4V to ±18V	●	111	124		106	121		dB
A_{VOL}	Large-Signal Voltage Gain	R_L ≥ 10k, V_{OUT} = ±10V R_L ≥ 2k, V_{OUT} = ±10V	● ●	3.5 1.2	12 3.2		2.2 0.8	12 2.3		V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	R_L ≥ 2k	●	±12.5	±13.6		±12	±13.6		V
SR	Slew Rate	R_L ≥ 2k (Notes 3, 7)	●	2.4	3.9		2.1	3.9		V/μs
I_S	Supply Current per Amplifier		●		2.4	3.25		2.4	3.25	mA

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1125s (or 100 LT1124s) typically 240 op amps (or 120) will be better than the indicated specification.

Note 3: This parameter is 100% tested for each individual amplifier.

Note 4: This parameter is sample tested only.

Note 5: This parameter is not 100% tested.

Note 6: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±1.4V, the input current should be limited to 25mA.

Note 7: Slew rate is measured in $A_V = -1$; input signal is ±7.5V, output measured at ±2.5V.

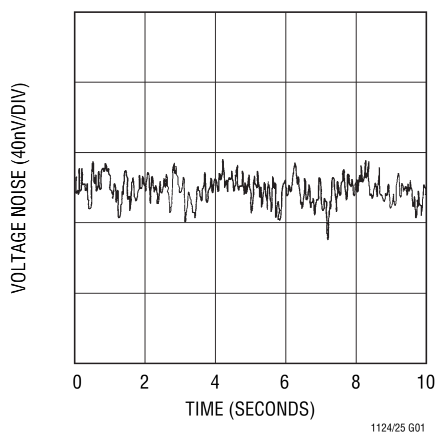
Note 8: 0.1Hz to 10Hz noise can be inferred from the 10Hz noise voltage density test. See the test circuit and frequency response curve for 0.1Hz to 10Hz tester in the Applications Information section of the LT1007 or LT1028 data sheets.

Note 9: This parameter is guaranteed but not tested.

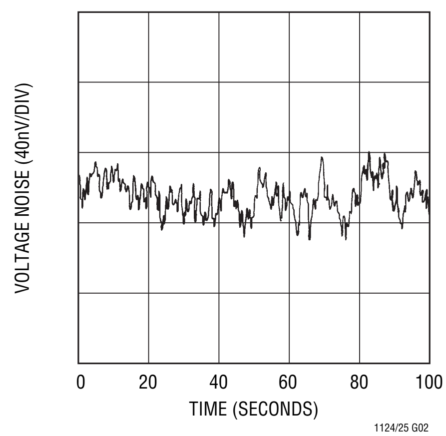
Note 10: The LT1124C/LT1125C and LT1124AC/LT1125AC are guaranteed to meet specified performance from 0°C to 70°C and are designed, characterized and expected to meet these extended temperature limits, but are not tested at –40°C and 85°C. The LT1124AI and LT1124I are guaranteed to meet the extended temperature limits.

TYPICAL PERFORMANCE CHARACTERISTICS

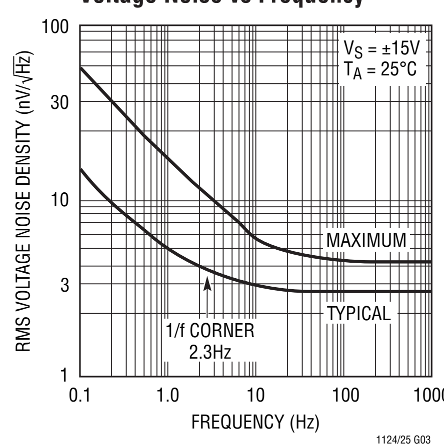
0.1Hz to 10Hz Voltage Noise



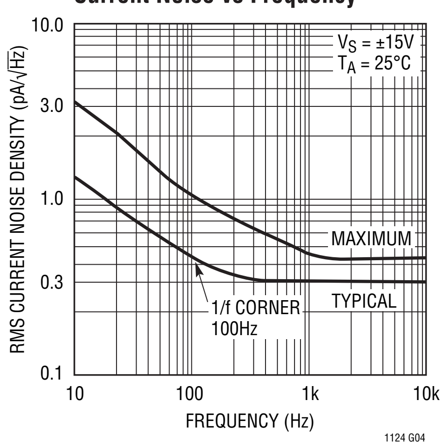
0.01Hz to 1Hz Voltage Noise



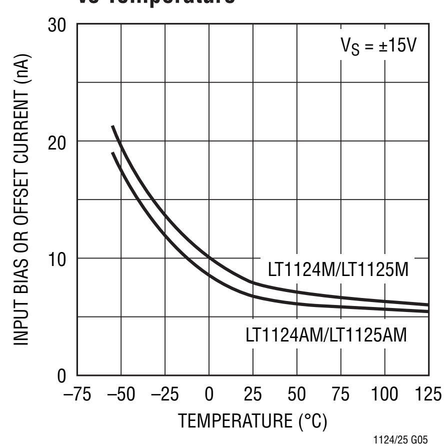
Voltage Noise vs Frequency



Current Noise vs Frequency

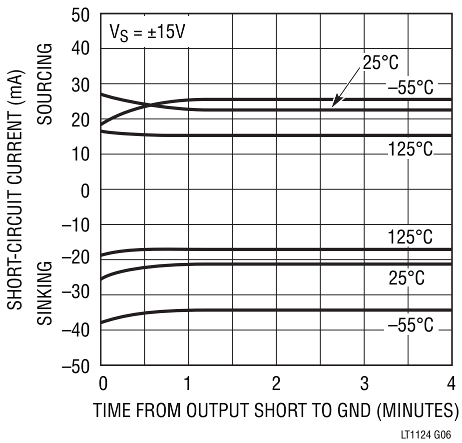


Input Bias or Offset Current vs Temperature

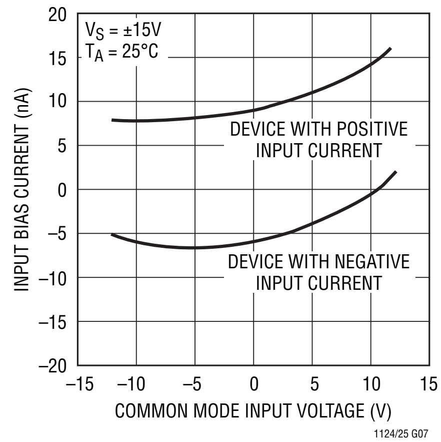


TYPICAL PERFORMANCE CHARACTERISTICS

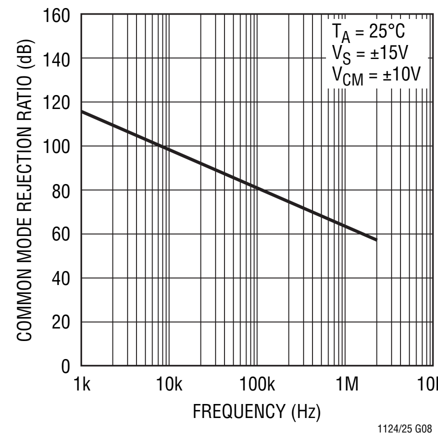
Output Short-Circuit Current vs Time



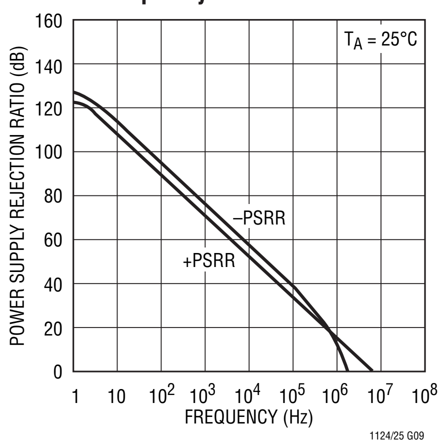
Input Bias Current Over the Common Mode Range



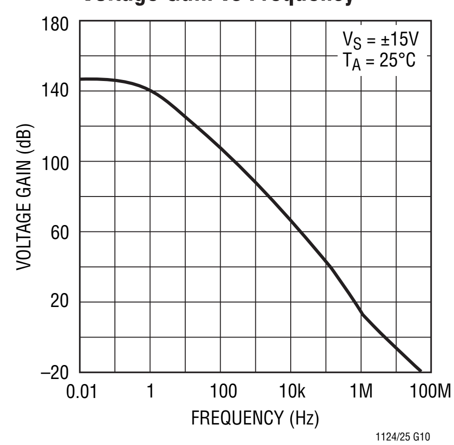
Common Mode Rejection Ratio vs Frequency



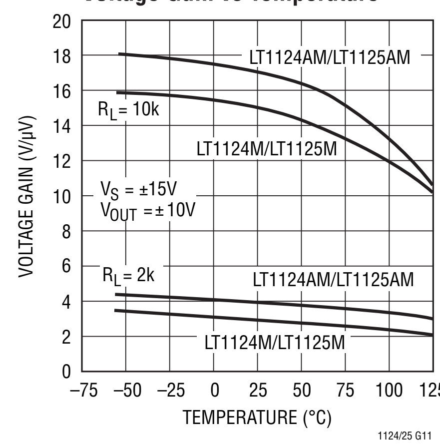
Power Supply Rejection Ratio vs Frequency



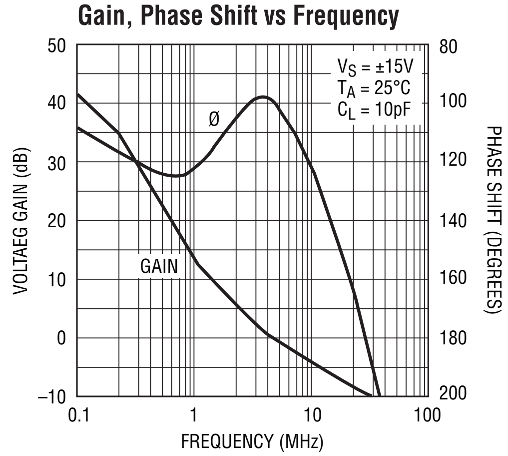
Voltage Gain vs Frequency



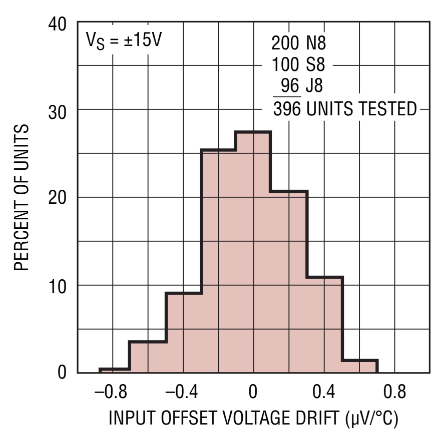
Voltage Gain vs Temperature



Gain, Phase Shift vs Frequency

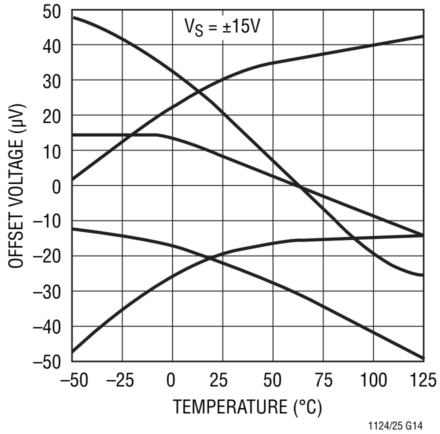


Input Offset Voltage Drift Distribution

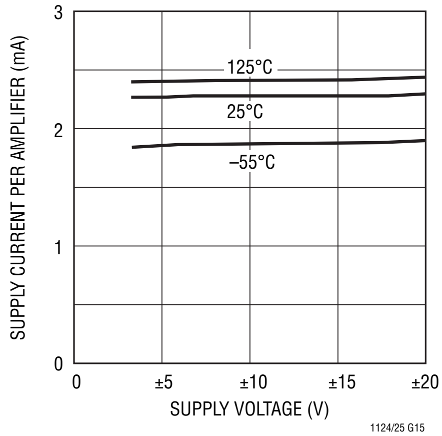


TYPICAL PERFORMANCE CHARACTERISTICS

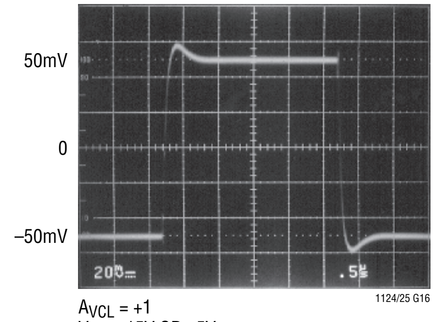
Offset Voltage Drift with Temperature of Representative Units



Supply Current vs Supply Voltage

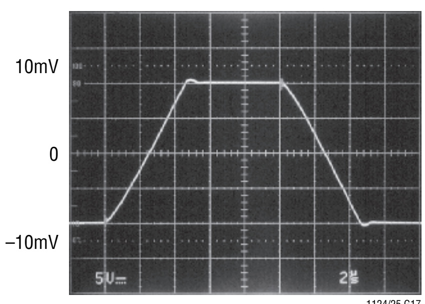


Small-Signal Transient Response



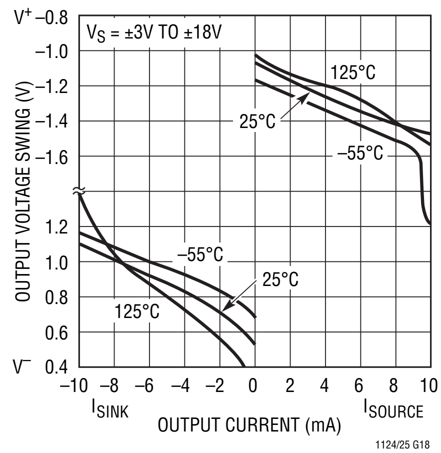
A_{VCL} = +1
V_S = ±15V OR ±5V
C_L = 15pF

Large-Signal Transient Response

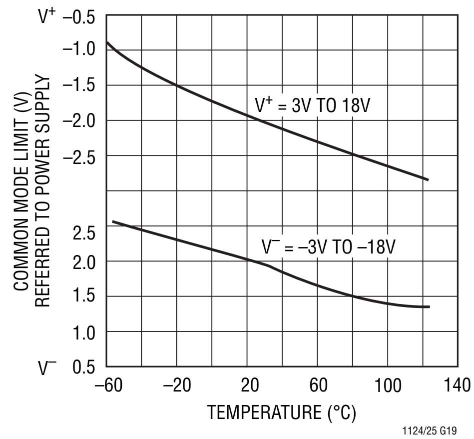


A_{VCL} = –1
V_S = ±15V

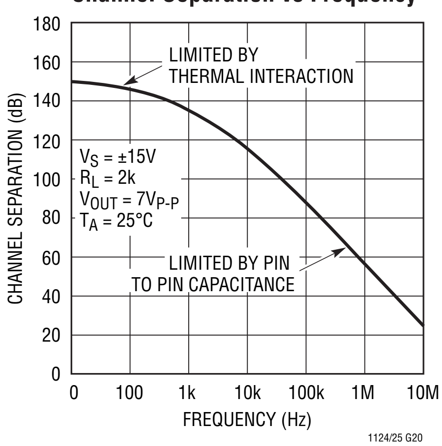
Output Voltage Swing vs Load Current



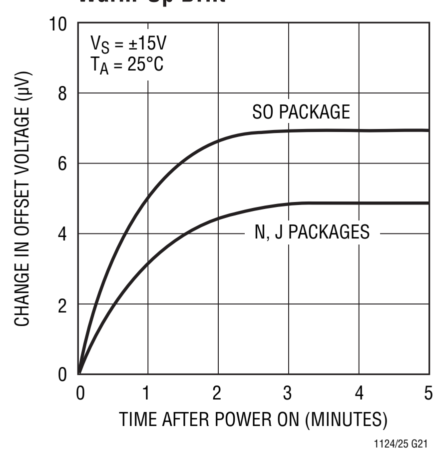
Common Mode Limit vs Temperature



Channel Separation vs Frequency

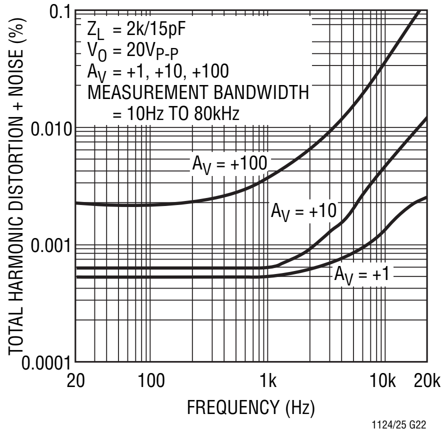


Warm-Up Drift

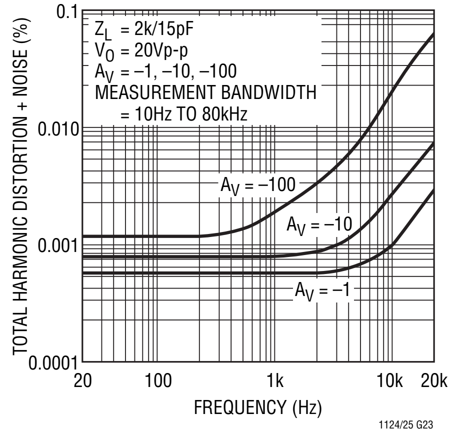


TYPICAL PERFORMANCE CHARACTERISTICS

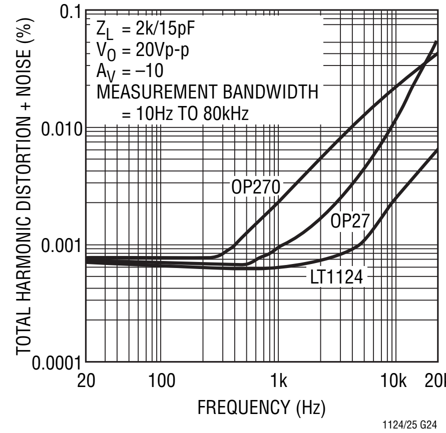
Total Harmonic Distortion and Noise vs Frequency for Noninverting Gain



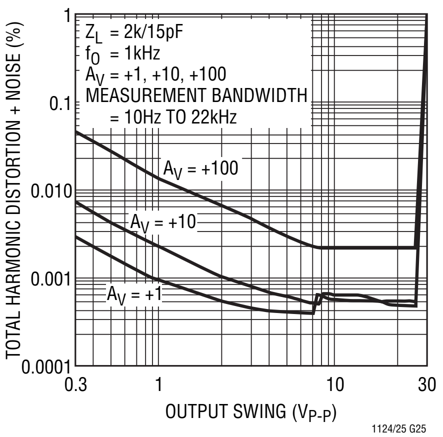
Total Harmonic Distortion and Noise vs Frequency for Inverting Gain



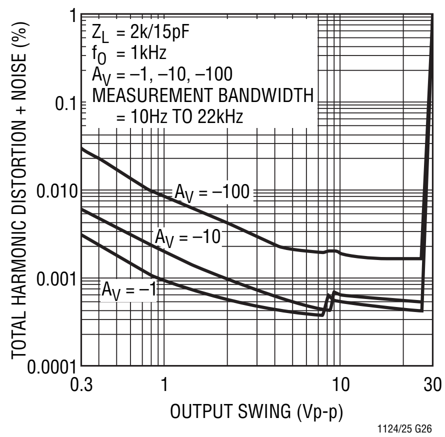
Total Harmonic Distortion and Noise vs Frequency for Competitive Devices



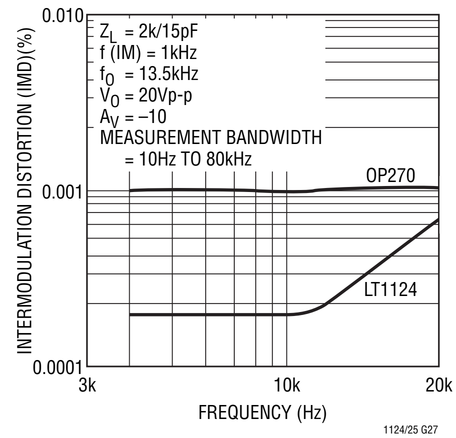
Total Harmonic Distortion and Noise vs Output Amplitude for Noninverting Gain



Total Harmonic Distortion and Noise vs Output Amplitude for Inverting Gain



Intermodulation Distortion (CCIF Method)* vs Frequency LT1124 and OP270



APPLICATIONS INFORMATION

The LT1124 may be inserted directly into OP-270 sockets. The LT1125 plugs into OP-470 sockets. Of course, all standard dual and quad bipolar op amps can also be replaced by these devices.

Matching Specifications

In many applications the performance of a system depends on the matching between two op amps, rather than the individual characteristics of the two devices. The three op amp instrumentation amplifier configuration shown in this data sheet is an example. Matching characteristics are not 100% tested on the LT1124/LT1125.

Some specifications are guaranteed by definition. For example, 70µV maximum offset voltage implies that mismatch cannot be more than 140µV. 112dB (= 2.5µV/V) CMRR means that worst-case CMRR match is 106dB (5µV/V). However, Table 1 can be used to estimate the expected matching performance between the two sides of the LT1124, and between amplifiers A and D, and between amplifiers B and C of the LT1125.

Offset Voltage and Drift

Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier unless proper care is exercised. Air currents should be minimized, package leads should be short, the two input leads should be close together and maintained at the same temperature.

The circuit shown in Figure 1 to measure offset voltage is also used as the burn-in configuration for the LT1124/LT1125, with the supply voltages increased to ±16V.

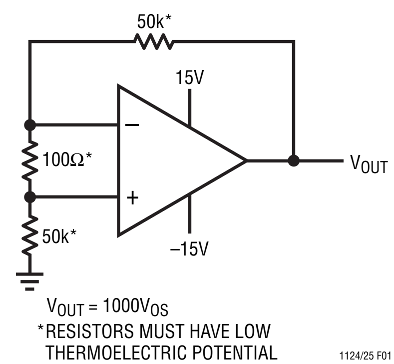


Figure 1. Test Circuit for Offset Voltage and Offset Voltage Drift with Temperature

Table 1. Expected Match

		LT1124AC/AM LT1125AC/AM		LT1124C/M LT1125C/M		
PARAMETER		**50% YIELD**	**98% YIELD**	**50% YIELD**	**98% YIELD**	**UNITS**
V_{OS} Match, ΔV_{OS}	LT1124	20	110	30	130	µV
	LT1125	30	150	50	180	µV
Temperature Coefficient Match		0.35	1.0	0.5	1.5	µV/°C
Average Noninverting I_B		6	18	7	25	nA
Match of Noninverting I_B		7	22	8	30	nA
CMRR Match		126	115	123	112	dB
PSRR Match		127	118	127	114	dB

APPLICATIONS INFORMATION

High Speed Operation

When the feedback around the op amp is resistive (R_F), a pole will be created with R_F, the source resistance and capacitance (R_S, C_S), and the amplifier input capacitance ($C_{IN} \approx 2pF$). In low closed loop gain configurations and with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem (see Figure 2). With $R_S (C_S + C_{IN}) = R_F C_F$, the effect of the feedback pole is completely removed.

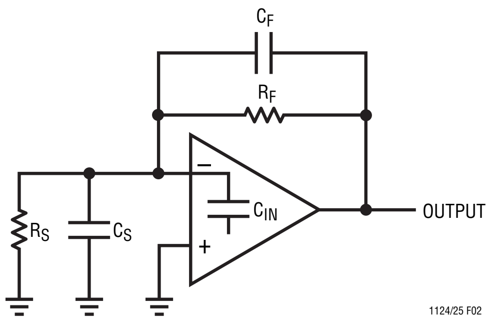


Figure 2. High Speed Operation

Unity Gain Buffer Applications

When $R_F \leq 100\Omega$ and the input is driven with a fast, large signal pulse (>1V), the output waveform will look as shown in Figure 3.

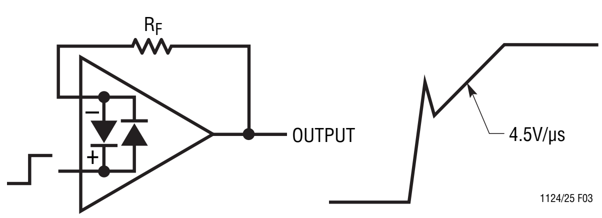


Figure 3. Unity-Gain Buffer Applications

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short circuit protection, will be drawn by the signal generator. With $R_F \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V) and the amplifier stays in its active mode and a smooth transition will occur.

Noise Testing

Each individual amplifier is tested to $4.2nV/\sqrt{Hz}$ voltage noise; i.e., for the LT1124 two tests, for the LT1125 four tests are performed. Noise testing for competing multiple op amps, if done at all, may be sample tested or tested using the circuit shown in Figure 4.

$$e_{n\,OUT} = \sqrt{(e_{nA})^2 + (e_{nB})^2 + (e_{nC})^2 + (e_{nD})^2}$$

If the LT1125 were tested this way, the noise limit would be $\sqrt{4 \bullet (4.2nV/\sqrt{Hz})^2} = 8.4nV/\sqrt{Hz}$. But is this an effective screen? What if three of the four amplifiers are at a typical $2.7nV/\sqrt{Hz}$, and the fourth one was contaminated and has $6.9nV/\sqrt{Hz}$ noise?

$$\text{RMS Sum} = \sqrt{(2.7)^2 + (2.7)^2 + (2.7)^2 + (6.9)^2} = 8.33nV/\sqrt{Hz}$$

This passes an $8.4nV/\sqrt{Hz}$ spec, yet one of the amplifiers is 64% over the LT1125 spec limit. Clearly, for proper noise measurement, the op amps have to be tested individually.

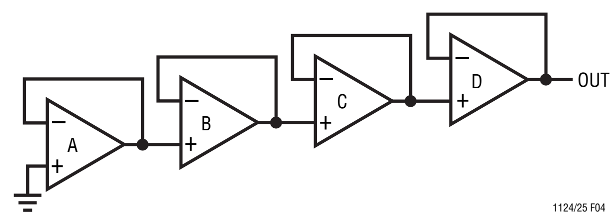


Figure 4. Competing Quad Op Amp Noise Test Method

PERFORMANCE COMPARISON

Table 2 summarizes the performance of the LT1124/LT1125 compared to the low cost grades of alternate approaches.

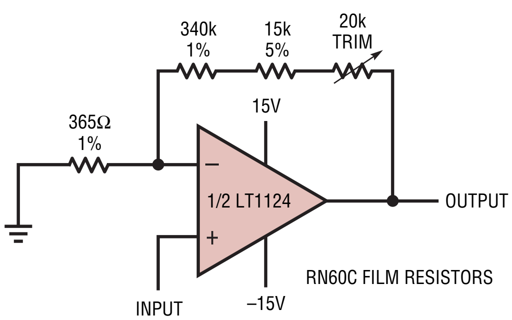
The comparison shows how the specs of the LT1124/LT1125 not only stand up to the industry standard OP-27, but in most cases are superior. Normally dual and quad performance is degraded when compared to singles, for the LT1124/LT1125 this is not the case.

Table 2. Guaranteed Performance, V_S = ±15V, T_A = 25°C, Low Cost Devices

PARAMETER/UNITS		LT1124CN8 LT1125CN	OP-27 GP	OP-270 GP	OP-470 GP	UNITS
Voltage Noise, 1kHz		4.2 100% Tested	4.5 Sample Tested	– No Limit	5.0 Sample Tested	nV/√Hz
Slew Rate		2.7 100% Tested	1.7 Not Tested	1.7	1.4	V/μs
Gain-Bandwidth Product		8.0 100% Tested	5.0 Not Tested	– No Limit	– No Limit	MHz
Offset Voltage	LT1124 LT1125	100 140	100 –	250 –	– 1000	μV μV
Offset Current	LT1124 LT1125	20 30	75 –	20 –	– 30	nA nA
Bias Current		30	80	60	60	nA
Supply Current/Amp		2.75	5.67	3.25	2.75	mA
Voltage Gain, R_L = 2k		1.5	0.7	0.35	0.4	V/μV
Common Mode Rejection Ratio		106	100	90	100	dB
Power Supply Rejection Ratio		110	94	104	105	dB
SO-8 Package		Yes – LT1124	Yes	No	–	

TYPICAL APPLICATIONS

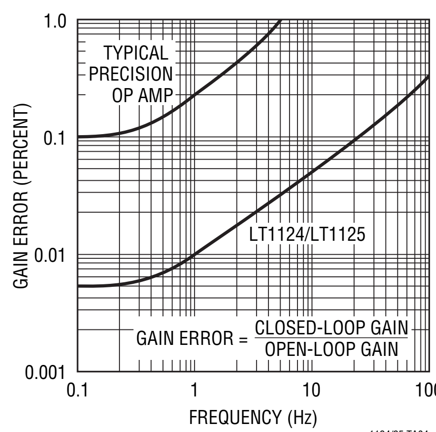
Gain 1000 Amplifier with 0.01% Accuracy, DC to 1Hz



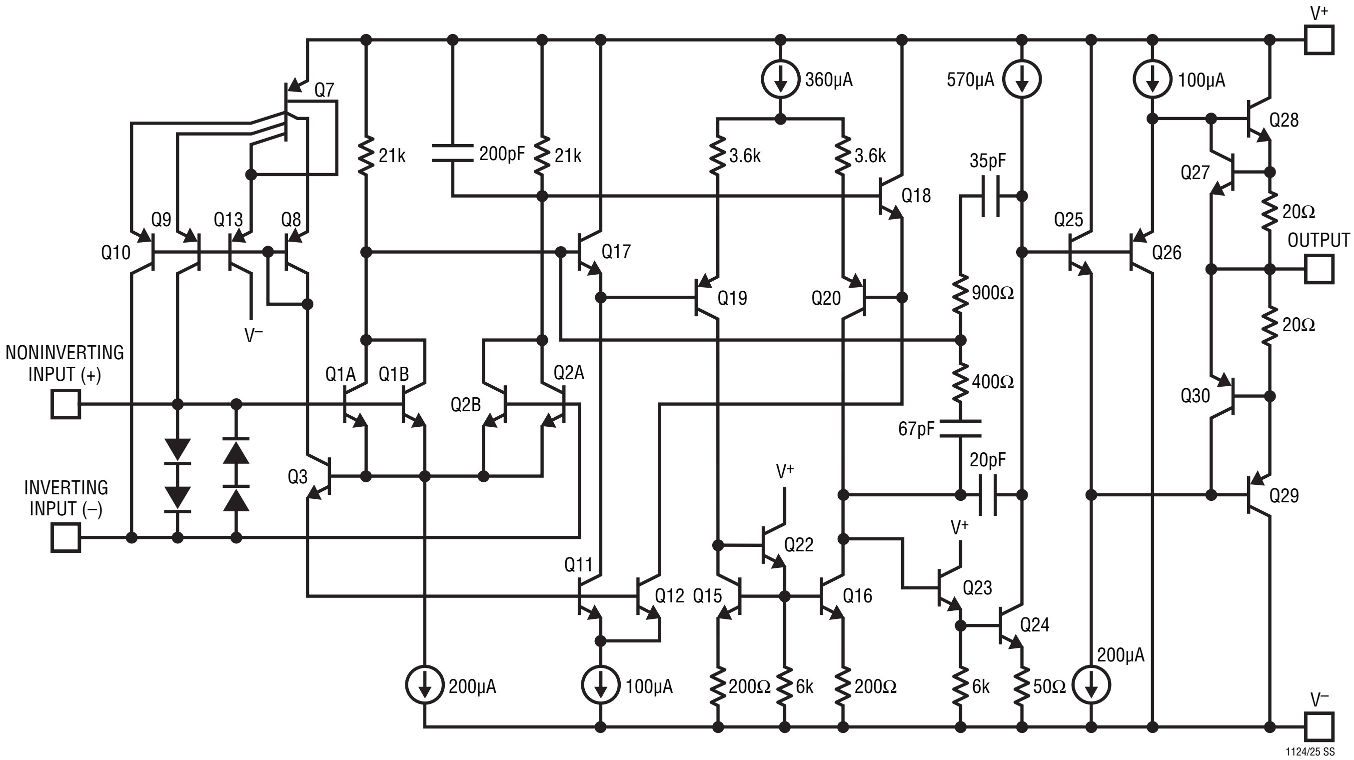
THE HIGH GAIN AND WIDE BANDWIDTH OF THE LT1124/LT1125, IS USEFUL IN LOW FREQUENCY HIGH CLOSED-LOOP GAIN AMPLIFIER APPLICATIONS. A TYPICAL PRECISION OP AMP MAY HAVE AN OPEN-LOOP GAIN OF ONE MILLION WITH 500kHz BANDWIDTH. AS THE GAIN ERROR PLOT SHOWS, THIS DEVICE IS CAPABLE OF 0.1% AMPLIFYING ACCURACY UP TO 0.3Hz ONLY. EVEN INSTRUMENTATION RANGE SIGNALS CAN VARY AT A FASTER RATE. THE LT1124/LT1125 "GAIN PRECISION — BANDWIDTH PRODUCT" IS 75 TIMES HIGHER, AS SHOWN.

1124/25 TA03

Gain Error vs Frequency Closed-Loop Gain = 1000



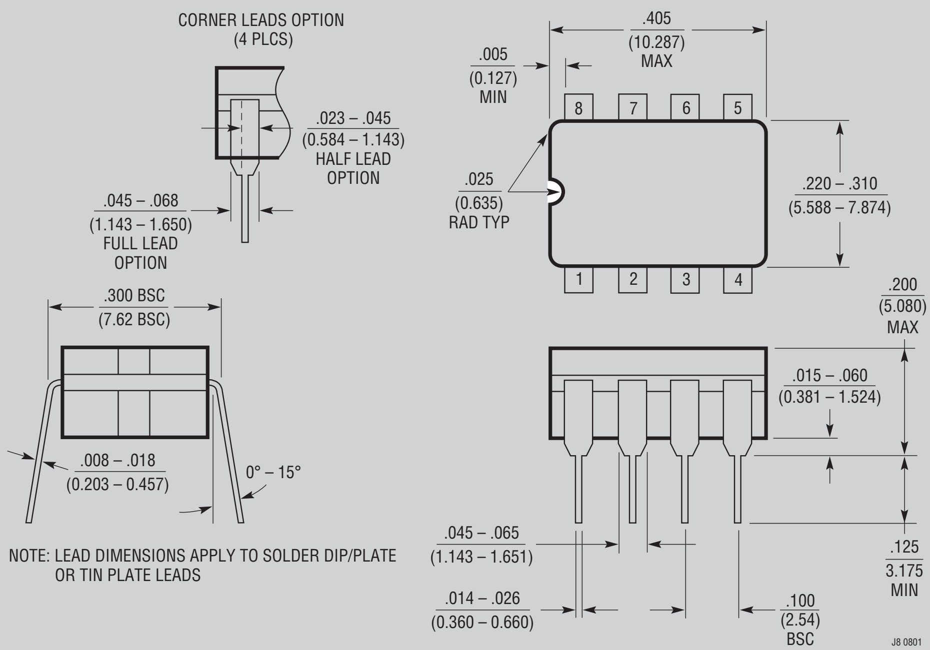
SCHEMATIC DIAGRAM (1/2 LT1124, 1/4 LT1125)



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

J8 Package
8-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)

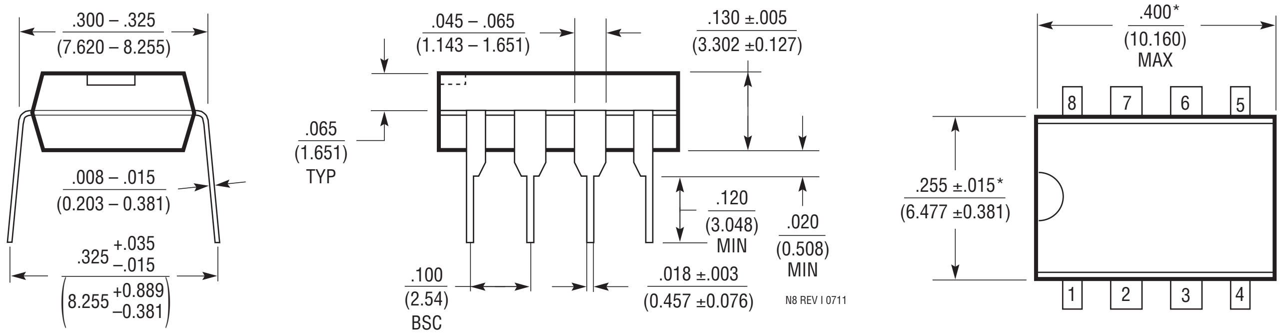


OBSOLETE PACKAGE

PACKAGE DESCRIPTION

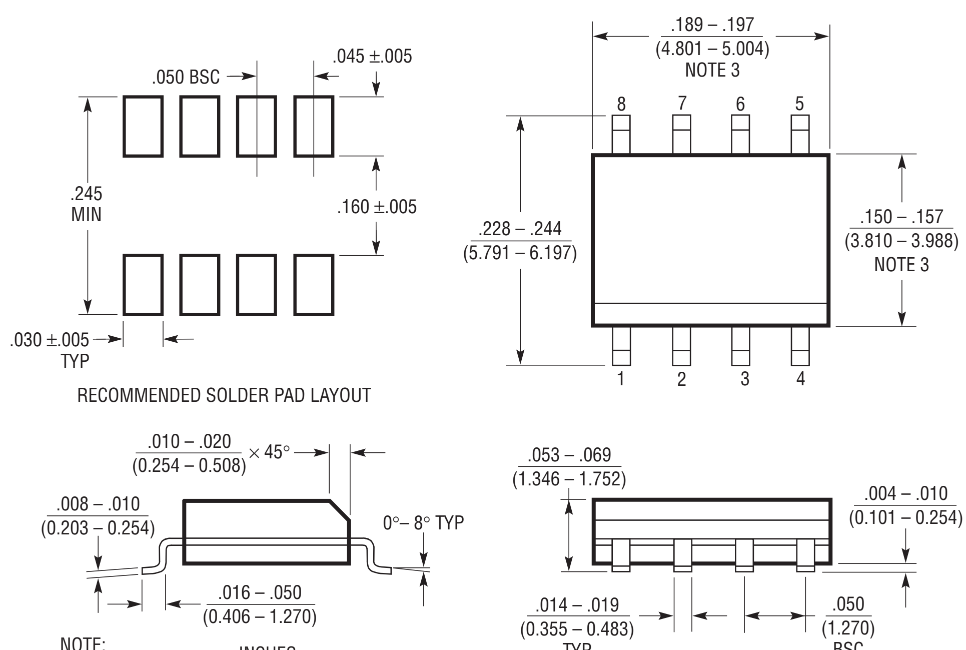
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510 Rev I)



NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

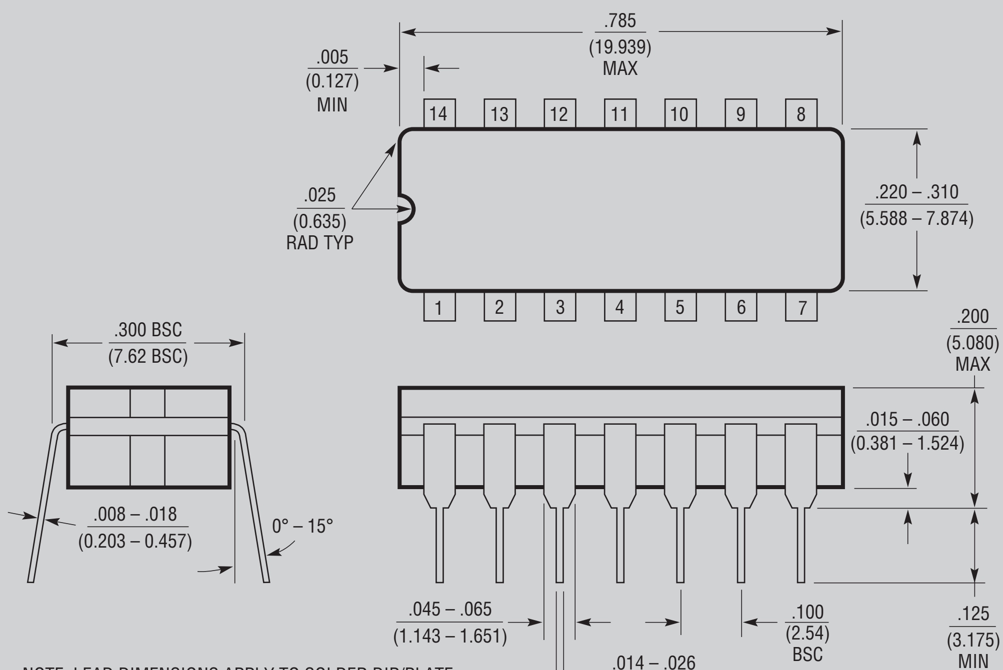
SO8 REV G 0212

11245ff

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

J Package
14-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)



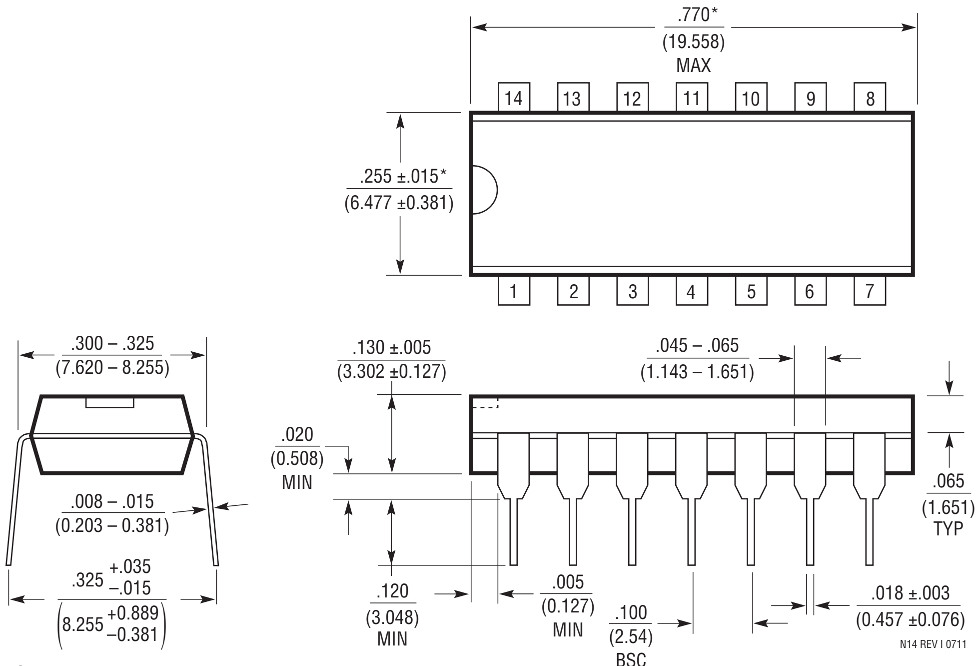
NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE
OR TIN PLATE LEADS

OBSOLETE PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

N Package
14-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510 Rev I)

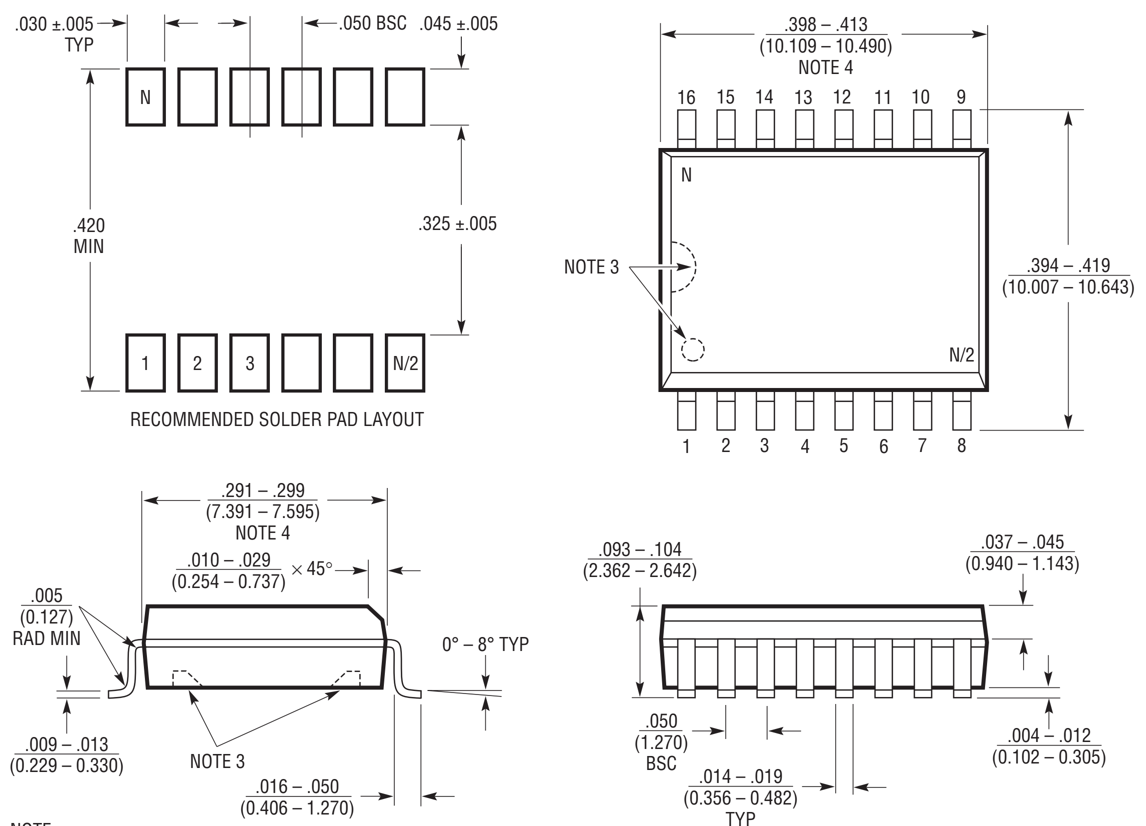


NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

SW Package
16-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

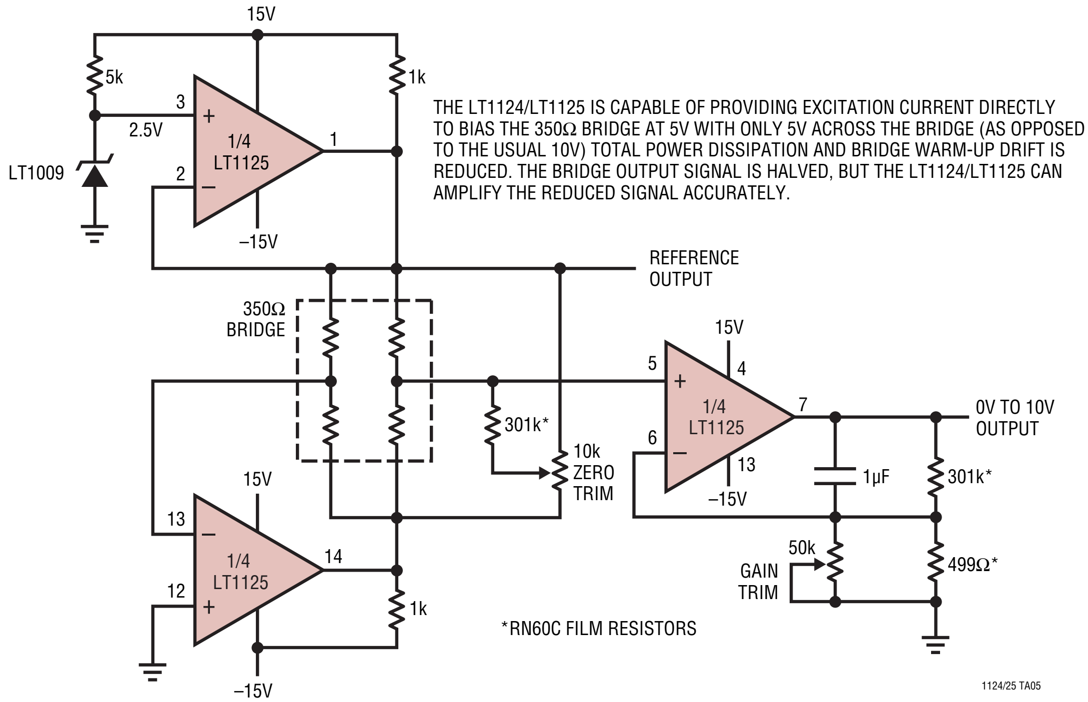
S16 (WIDE) 0502

REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
D	09/10	LT1124-1 added. Reflected throughout the data sheet.	1 to 18
E	10/10	Revised part marking for LT1124AMPS8-1 in Order Information section.	3
F	01/14	LT1124-1 removed.	1 to 3

TYPICAL APPLICATION

Strain Gauge Signal Conditioner with Bridge Excitation



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1007	Single Low Noise, Precision Op Amp	2.5nV/√Hz 1kHz Voltage Noise
LT1028/LT1128	Single Low Noise, Precision Op Amps	0.85nV/√Hz Voltage Noise
LT1112/LT1114	Dual/Quad Precision Picoamp Input	250pA Max I_B
LT1113	Dual Low Noise JFET Op Amp	4.5nV/√Hz Voltage Noise, 10fA/√Hz Current Noise
LT1126/LT1127	Decompensated LT1124/LT1125	11V/µs Slew Rate
LT1169	Dual Low Noise JFET Op Amp	6nV/√Hz Voltage Noise, 1fA/√Hz Current Noise, 10pA Max I_B
LT1792	Single LT1113	4.2nV/√Hz Voltage Noise, 10fA/√Hz Current Noise
LT1793	Single LT1169	6nV/√Hz Voltage Noise, 1fA/√Hz Current Noise, 10pA Max I_B

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