General-Purpose CMOS Rail-to-Rail Amplifiers

AD8541/AD8542/AD8544

FEATURES

Single-supply operation: 2.7 V to 5.5 V
Low supply current: 45 μA/amplifier
Wide bandwidth: 1 MHz
No phase reversal
Low input currents: 4 pA
Unity gain stable
Rail-to-rail input and output

APPLICATIONS

ASIC input or output amplifiers
Sensor interfaces
Piezoelectric transducer amplifiers
Medical instrumentation
Mobile communications
Audio outputs
Portable systems

GENERAL DESCRIPTION

The AD8541/AD8542/AD8544 are single, dual, and quad rail-to-rail input and output, single-supply amplifiers featuring very low supply current and 1 MHz bandwidth. All are guaranteed to operate from a 2.7 V single supply as well as a 5 V supply. These parts provide 1 MHz bandwidth at a low current consumption of 45 μA per amplifier.

Very low input bias currents enable the AD8541/AD8542/AD8544 to be used for integrators, photodiode amplifiers, piezoelectric sensors, and other applications with high source impedance. The supply current is only 45 μA per amplifier, ideal for battery operation.

Rail-to-rail inputs and outputs are useful to designers buffering ASICs in single-supply systems. The AD8541/AD8542/AD8544 are optimized to maintain high gains at lower supply voltages, making them useful for active filters and gain stages.

The AD8541/AD8542/AD8544 are specified over the extended industrial temperature range (–40°C to +125°C). The AD8541 is available in 5-lead SOT-23, 5-lead SC70, and 8-lead SOIC packages. The AD8542 is available in 8-lead SOIC, 8-lead MSOP, and 8-lead TSSOP surface-mount packages. The AD8544 is available in 14-lead narrow SOIC and 14-lead TSSOP surface-mount packages. All MSOP, SC70, and SOT versions are available in tape and reel only.

PIN CONFIGURATIONS

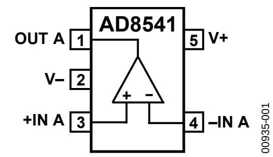

Figure 1. 5-Lead SC70 and 5-Lead SOT-23 (KS and RJ Suffixes)

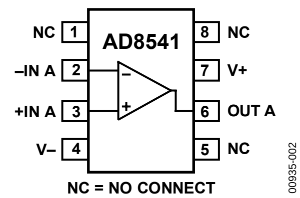

Figure 2. 8-Lead SOIC (R Suffix)

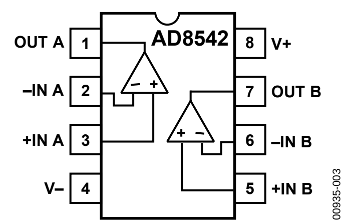

Figure 3. 8-Lead SOIC, 8-Lead MSOP, and 8-Lead TSSOP (R, RM, and RU Suffixes)

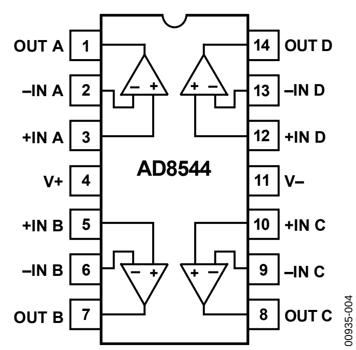

Figure 4. 14-Lead SOIC and 14-Lead TSSOP (R and RU Suffixes)

Rev. F

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1/03—Rev. B to Rev. C

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_S = 2.7 V, V_{CM} = 1.35 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	6	mV
		−40°C ≤ T_A ≤ +125°C			7	mV
Input Bias Current	I_B			4	60	pA
		−40°C ≤ T_A ≤ +85°C			100	pA
		−40°C ≤ T_A ≤ +125°C			1000	pA
Input Offset Current	I_{OS}			0.1	30	pA
		−40°C ≤ T_A ≤ +85°C			50	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
Input Voltage Range			0		2.7	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.7 V	40	45		dB
		−40°C ≤ T_A ≤ +125°C	38			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, V_O = 0.5 V to 2.2 V	100	500		V/mV
		−40°C ≤ T_A ≤ +85°C	50			V/mV
		−40°C ≤ T_A ≤ +125°C	2			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		4		μV/°C
Bias Current Drift	$\Delta I_B/\Delta T$	−40°C ≤ T_A ≤ +85°C		100		fA/°C
		−40°C ≤ T_A ≤ +125°C		2000		fA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		25		fA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	2.575	2.65		V
		−40°C ≤ T_A ≤ +125°C	2.550			V
Output Voltage Low	V_{OL}	I_L = 1 mA		35	100	mV
		−40°C ≤ T_A ≤ +125°C			125	mV
Output Current	I_{OUT}	V_{OUT} = V_S − 1 V		15		mA
	I_{SC}			±20		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 200 kHz, A_V = 1		50		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.5 V to 6 V	65	76		dB
		−40°C ≤ T_A ≤ +125°C	60			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		38	55	μA
		−40°C ≤ T_A ≤ +125°C			75	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ	0.4	0.75		V/μs
Settling Time	t_S	To 0.1% (1 V step)		5		μs
Gain Bandwidth Product	GBP			980		kHz
Phase Margin	Φ_M			63		Degrees
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		40		nV/√Hz
	e_n	f = 10 kHz		38		nV/√Hz
Current Noise Density	i_n			<0.1		pA/√Hz

V_S = 3.0 V, V_{CM} = 1.5 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	6	mV
		−40°C ≤ T_A ≤ +125°C			7	mV
Input Bias Current	I_B			4	60	pA
		−40°C ≤ T_A ≤ +85°C			100	pA
		−40°C ≤ T_A ≤ +125°C			1000	pA
Input Offset Current	I_{OS}			0.1	30	pA
		−40°C ≤ T_A ≤ +85°C			50	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 3 V	40	45		dB
		−40°C ≤ T_A ≤ +125°C	38			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, V_O = 0.5 V to 2.2 V	100	500		V/mV
		−40°C ≤ T_A ≤ +85°C	50			V/mV
		−40°C ≤ T_A ≤ +125°C	2			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		4		μV/°C
Bias Current Drift	$\Delta I_B/\Delta T$	−40°C ≤ T_A ≤ +85°C		100		fA/°C
		−40°C ≤ T_A ≤ +125°C		2000		fA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		25		fA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	2.875	2.955		V
		−40°C ≤ T_A ≤ +125°C	2.850			V
Output Voltage Low	V_{OL}	I_L = 1 mA		32	100	mV
		−40°C ≤ T_A ≤ +125°C			125	mV
Output Current	I_{OUT}	V_{OUT} = V_S − 1 V		18		mA
	I_{SC}			±25		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 200 kHz, A_V = 1		50		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.5 V to 6 V	65	76		dB
		−40°C ≤ T_A ≤ +125°C	60			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		40	60	μA
		−40°C ≤ T_A ≤ +125°C			75	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ	0.4	0.8		V/μs
Settling Time	t_S	To 0.01% (1 V step)		5		μs
Gain Bandwidth Product	GBP			980		kHz
Phase Margin	Φ_M			64		Degrees
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		42		nV/√Hz
	e_n	f = 10 kHz		38		nV/√Hz
Current Noise Density	i_n			<0.1		pA/√Hz

V_S = 5.0 V, V_{CM} = 2.5 V, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	6	mV
		−40°C ≤ T_A ≤ +125°C			7	mV
Input Bias Current	I_B			4	60	pA
		−40°C ≤ T_A ≤ +85°C			100	pA
		−40°C ≤ T_A ≤ +125°C			1000	pA
Input Offset Current	I_{OS}			0.1	30	pA
		−40°C ≤ T_A ≤ +85°C			50	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	40	48		dB
		−40°C ≤ T_A ≤ +125°C	38			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, V_O = 0.5 V to 2.2 V	20	40		V/mV
		−40°C ≤ T_A ≤ +85°C	10			V/mV
		−40°C ≤ T_A ≤ +125°C	2			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		4		μV/°C
Bias Current Drift	$\Delta I_B/\Delta T$	−40°C ≤ T_A ≤ +85°C		100		fA/°C
		−40°C ≤ T_A ≤ +125°C		2000		fA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		25		fA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	4.9	4.965		V
		−40°C ≤ T_A ≤ +125°C	4.875			V
Output Voltage Low	V_{OL}	I_L = 1 mA		25	100	mV
		−40°C ≤ T_A ≤ +125°C			125	mV
Output Current	I_{OUT}	V_{OUT} = V_S − 1 V		30		mA
	I_{SC}			±60		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 200 kHz, A_V = 1		45		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.5 V to 6 V	65	76		dB
		−40°C ≤ T_A ≤ +125°C	60			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		45	65	μA
		−40°C ≤ T_A ≤ +125°C			85	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 200 pF	0.45	0.92		V/μs
Full Power Bandwidth	BW_P	1% distortion		70		kHz
Settling Time	t_S	To 0.1% (1 V step)		6		μs
Gain Bandwidth Product	GBP			1000		kHz
Phase Margin	Φ_M			67		Degrees
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		42		nV/√Hz
	e_n	f = 10 kHz		38		nV/√Hz
Current Noise Density	i_n			<0.1		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage (V_S)	6 V
Input Voltage	GND to V_S
Differential Input Voltage[1]	±6 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] For supplies less than 6 V, the differential input voltage is equal to $\pm V_S$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

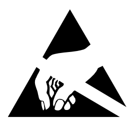
THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5.

Package Type	θ_{JA}	θ_{JC}	Unit
5-Lead SC70 (KS)	376	126	°C/W
5-Lead SOT-23 (RJ)	230	146	°C/W
8-Lead SOIC (R)	158	43	°C/W
8-Lead MSOP (RM)	210	45	°C/W
8-Lead TSSOP (RU)	240	43	°C/W
14-Lead SOIC (R)	120	36	°C/W
14-Lead TSSOP (RU)	240	43	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

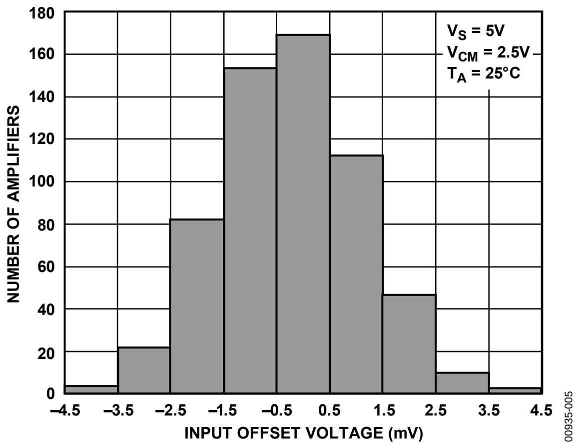


Figure 5. Input Offset Voltage Distribution

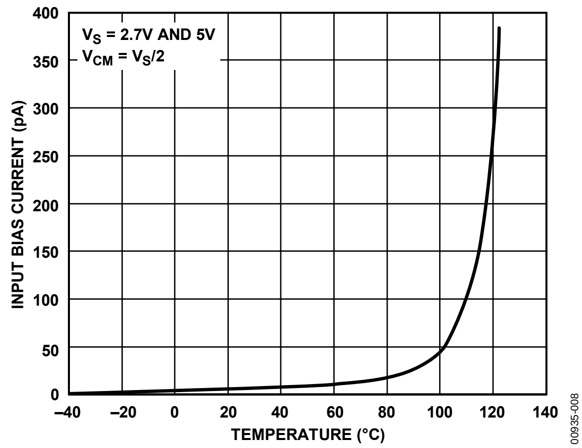


Figure 8. Input Bias Current vs. Temperature

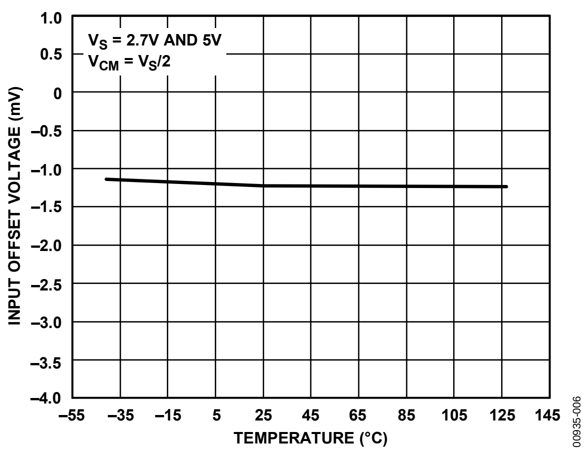


Figure 6. Input Offset Voltage vs. Temperature

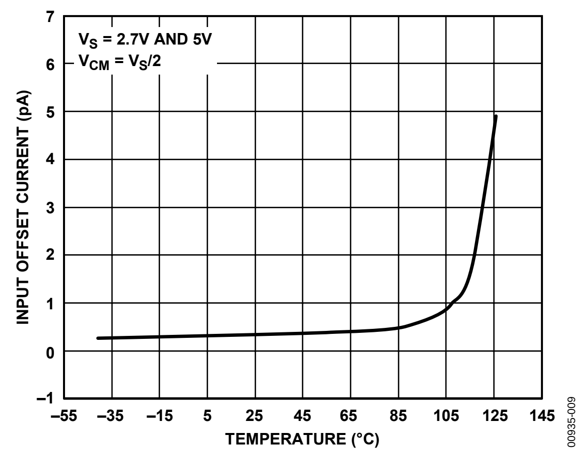


Figure 9. Input Offset Current vs. Temperature

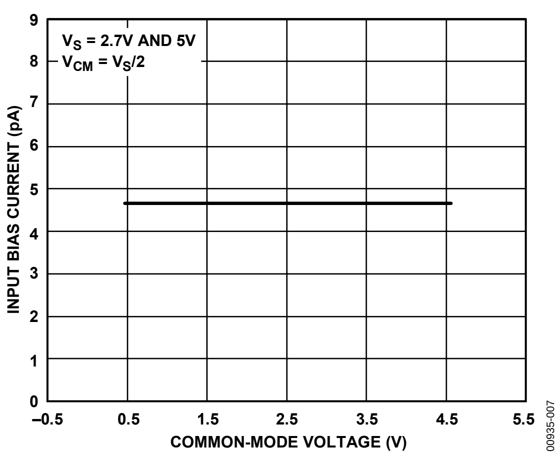


Figure 7. Input Bias Current vs. Common-Mode Voltage

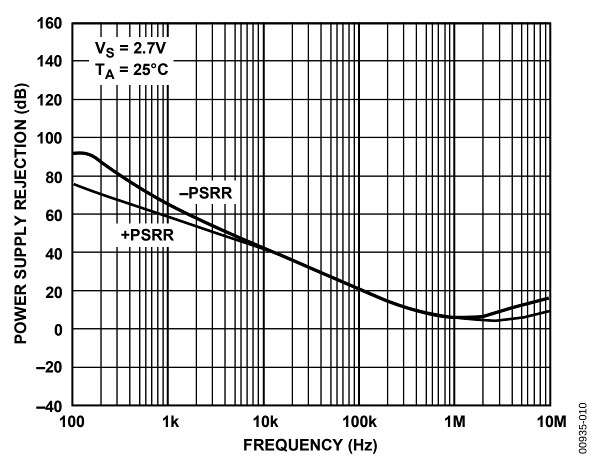


Figure 10. Power Supply Rejection vs. Frequency

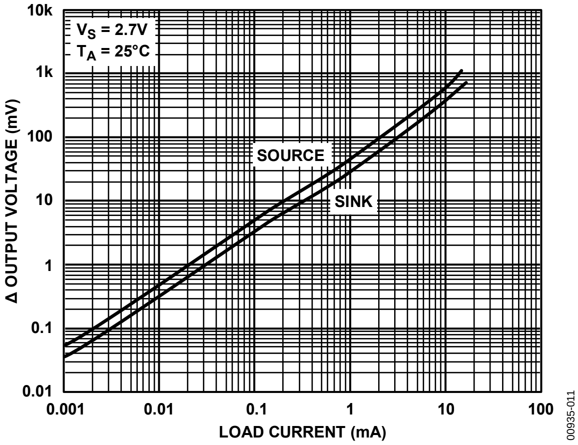


Figure 11. Output Voltage to Supply Rail vs. Load Current

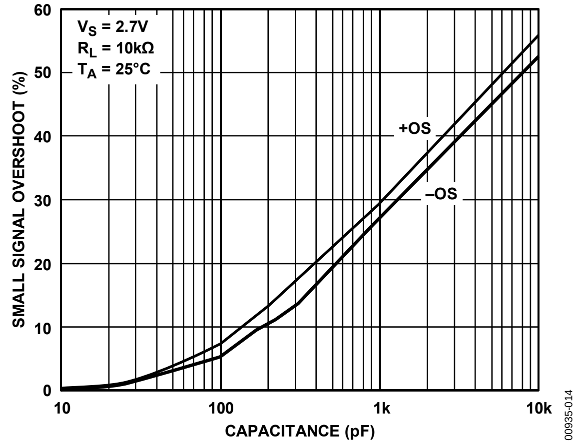


Figure 14. Small Signal Overshoot vs. Load Capacitance

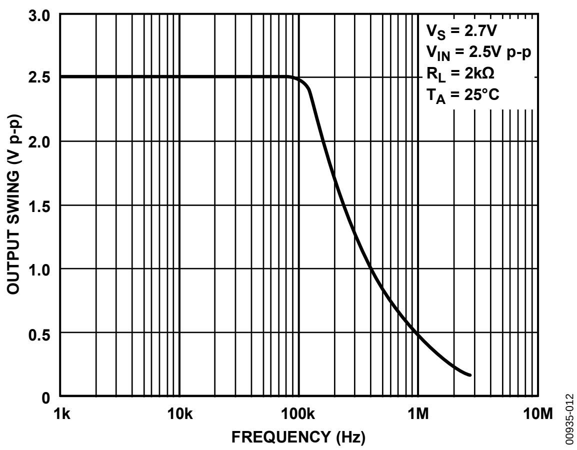


Figure 12. Closed-Loop Output Voltage Swing vs. Frequency

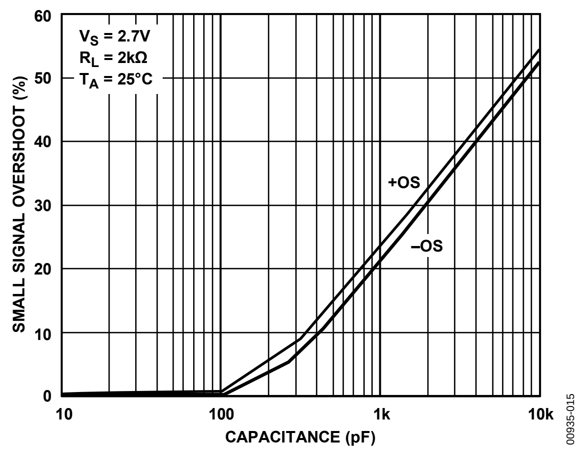


Figure 15. Small Signal Overshoot vs. Load Capacitance

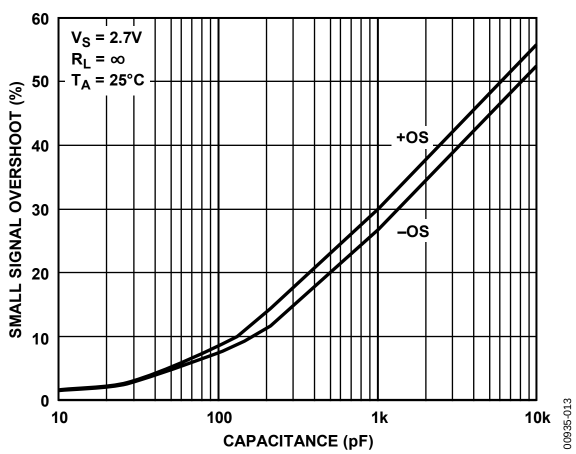


Figure 13. Small Signal Overshoot vs. Load Capacitance

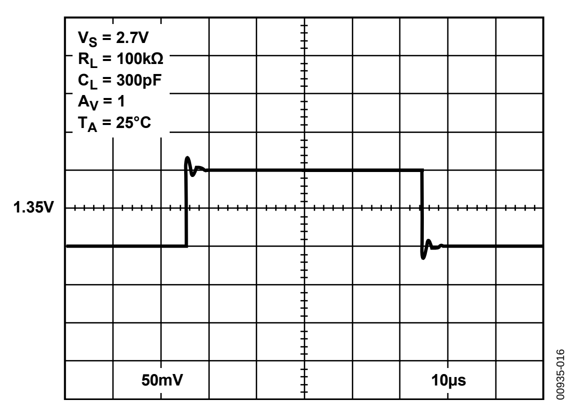


Figure 16. Small Signal Transient Response

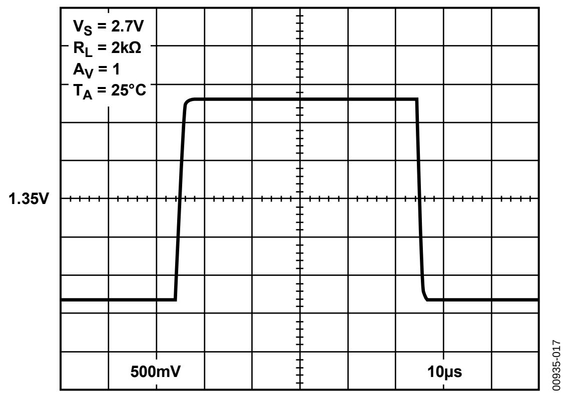


Figure 17. Large Signal Transient Response

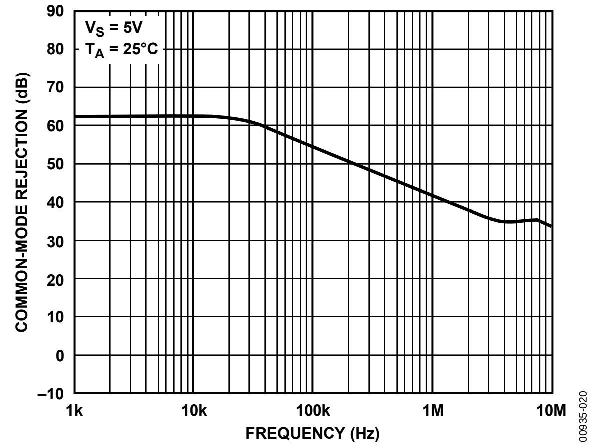


Figure 20. Common-Mode Rejection vs. Frequency

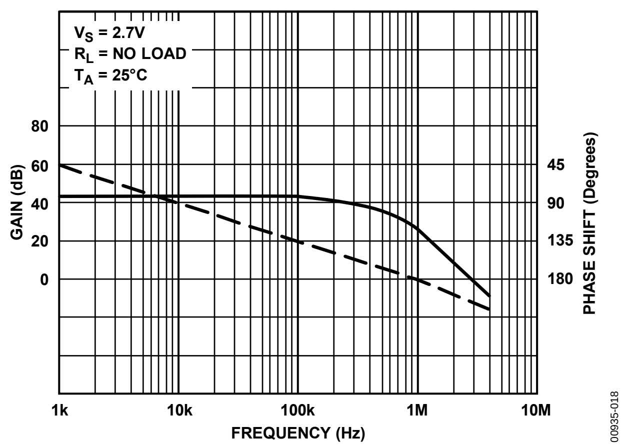


Figure 18. Open-Loop Gain and Phase vs. Frequency

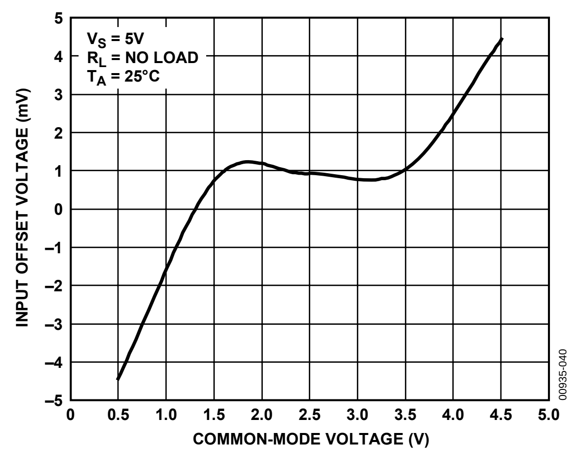


Figure 21. Input Offset Voltage vs. Common-Mode Voltage

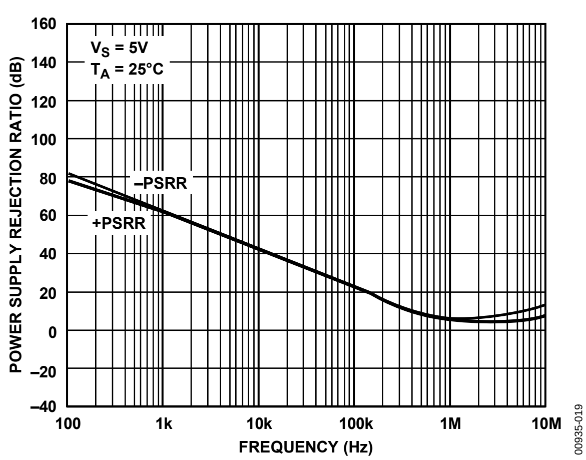


Figure 19. Power Supply Rejection Ratio vs. Frequency

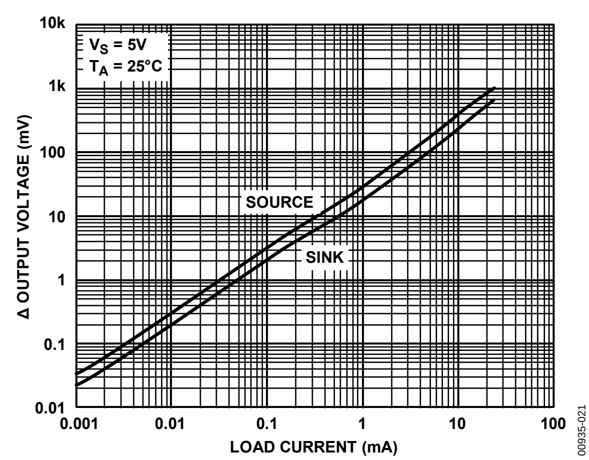


Figure 22. Output Voltage to Supply Rail vs. Load Current

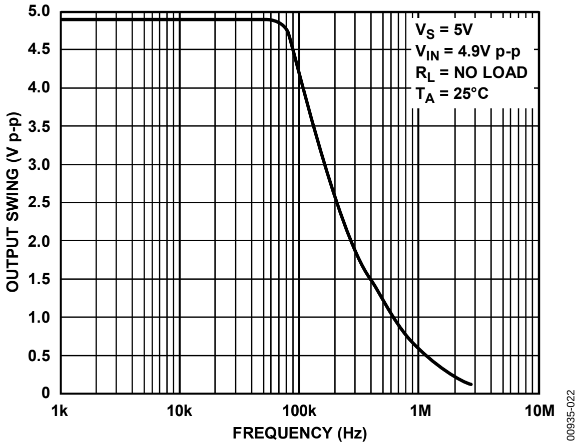


Figure 23. Closed-Loop Output Voltage Swing vs. Frequency,

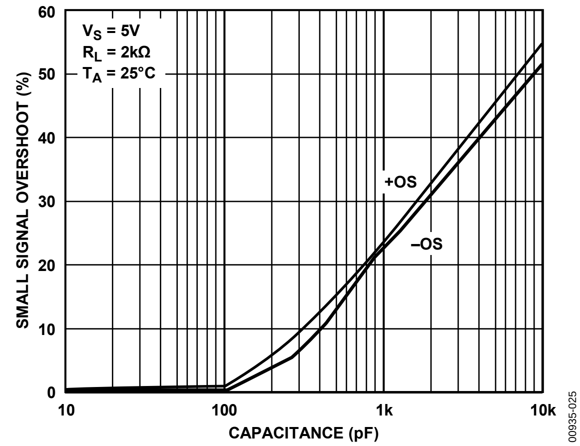


Figure 26. Small Signal Overshoot vs. Load Capacitance

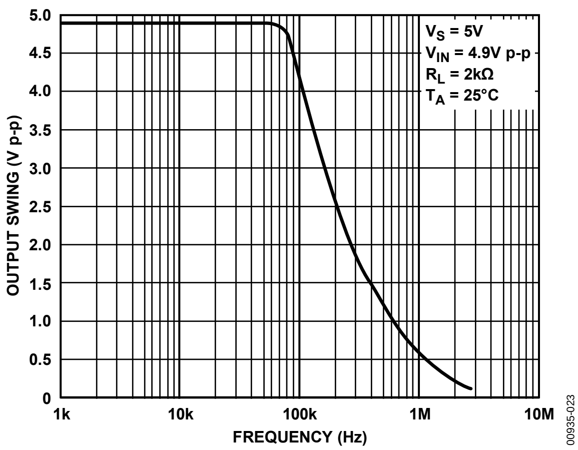


Figure 24. Closed-Loop Output Voltage Swing vs. Frequency

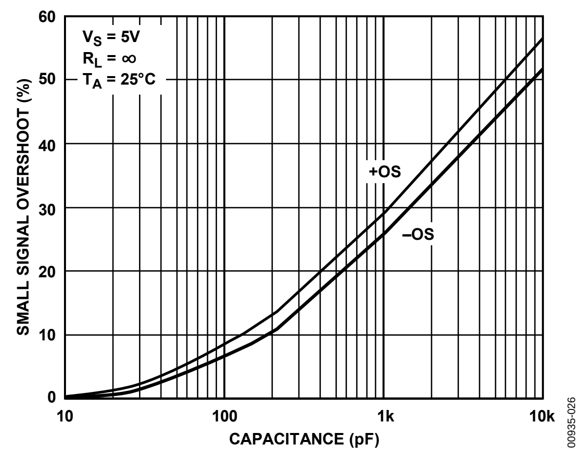


Figure 27. Small Signal Overshoot vs. Load Capacitance

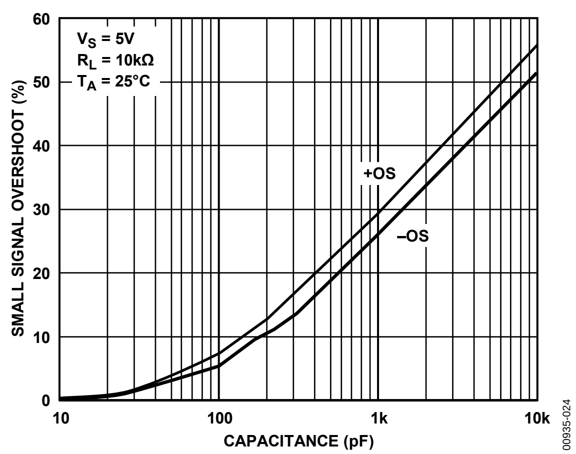


Figure 25. Small Signal Overshoot vs. Load Capacitance

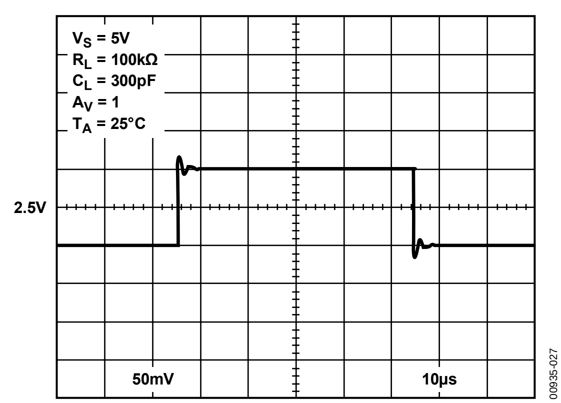


Figure 28. Small Signal Transient Response

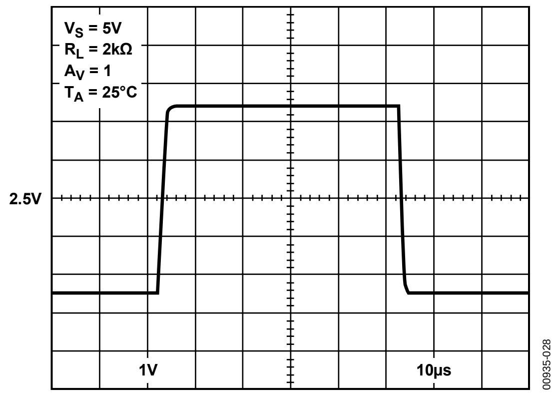


Figure 29. Large Signal Transient Response

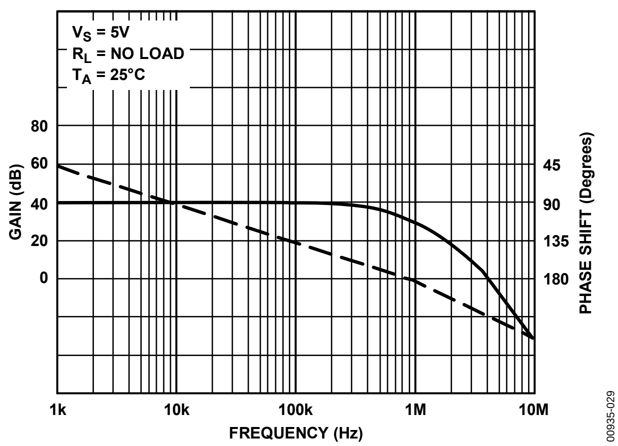


Figure 30. Open-Loop Gain and Phase vs. Frequency

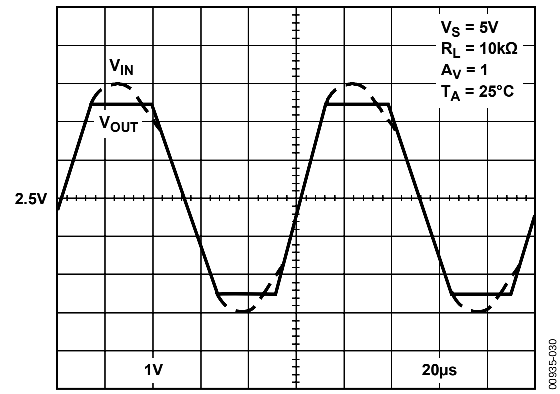


Figure 31. No Phase Reversal

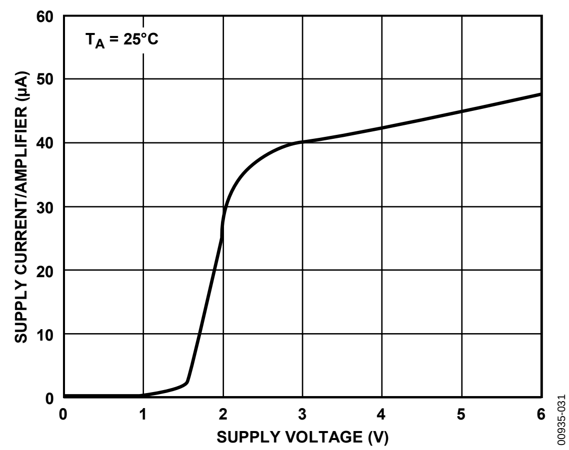


Figure 32. Supply Current per Amplifier vs. Supply Voltage

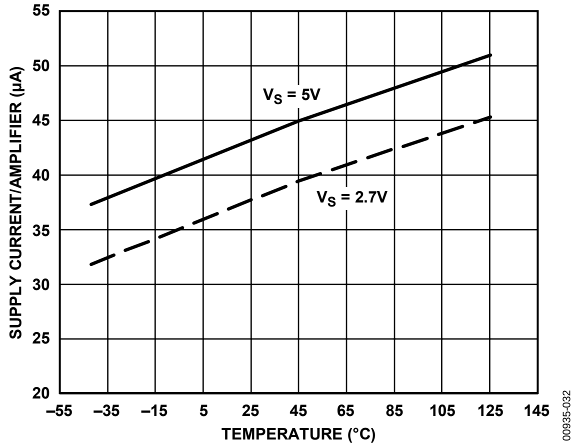


Figure 33. Supply Current per Amplifier vs. Temperature

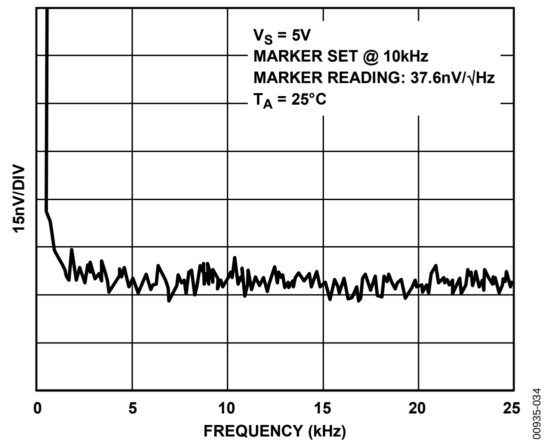


Figure 35. Voltage Noise

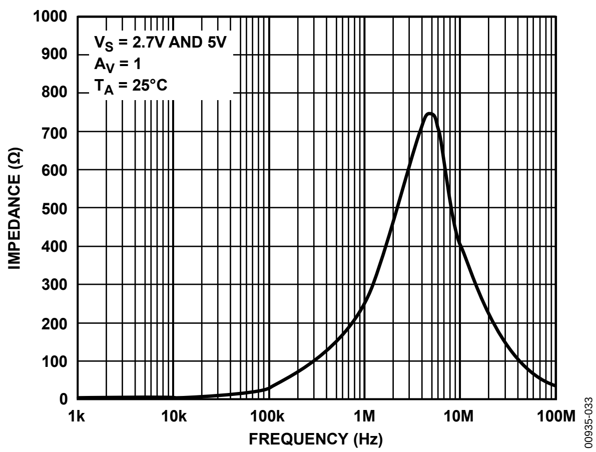


Figure 34. Closed-Loop Output Impedance vs. Frequency

THEORY OF OPERATION

NOTES ON THE AD854X AMPLIFIERS

The AD8541/AD8542/AD8544 amplifiers are improved performance, general-purpose operational amplifiers. Performance has been improved over previous amplifiers in several ways, including lower supply current for 1 MHz gain bandwidth, higher output current, and better performance at lower voltages.

Lower Supply Current for 1 MHz Gain Bandwidth

The AD854x series typically uses 45 µA of current per amplifier, which is much less than the 200 µA to 700 µA used in earlier generation parts with similar performance. This makes the AD854x series a good choice for upgrading portable designs for longer battery life. Alternatively, additional functions and performance can be added at the same current drain.

Higher Output Current

At 5 V single supply, the short-circuit current is typically 60 µA. Even 1 V from the supply rail, the AD854x amplifiers can provide a 30 mA output current, sourcing, or sinking.

Sourcing and sinking are strong at lower voltages, with 15 mA available at 2.7 V and 18 mA at 3.0 V. For even higher output currents, see the AD8531/AD8532/AD8534 parts for output currents to 250 mA. Information on these parts is available from your Analog Devices, Inc. representative, and data sheets are available at www.analog.com.

Better Performance at Lower Voltages

The AD854x family of parts was designed to provide better ac performance at 3.0 V and 2.7 V than previously available parts. Typical gain bandwidth product is close to 1 MHz at 2.7 V. Voltage gain at 2.7 V and 3.0 V is typically 500,000. Phase margin is typically over 60°C, making the part easy to use.

APPLICATIONS

NOTCH FILTER

The AD854x have very high open-loop gain (especially with a supply voltage below 4 V), which makes it useful for active filters of all types. For example, Figure 36 illustrates the AD8542 in the classic twin-T notch filter design. The twin-T notch is desired for simplicity, low output impedance, and minimal use of op amps. In fact, this notch filter can be designed with only one op amp if Q adjustment is not required. Simply remove U2 as illustrated in Figure 37. However, a major drawback to this circuit topology is ensuring that all the Rs and Cs closely match. The components must closely match or notch frequency offset and drift causes the circuit to no longer attenuate at the ideal notch frequency. To achieve desired performance, 1% or better component tolerances or special component screens are usually required. One method to desensitize the circuit-to-component mismatch is to increase R2 with respect to R1, which lowers Q. A lower Q increases attenuation over a wider frequency range but reduces attenuation at the peak notch frequency.

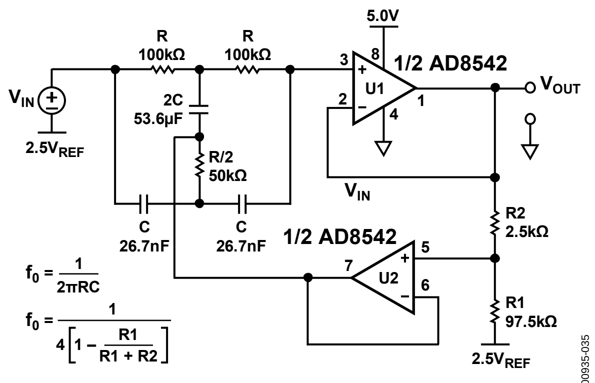


Figure 36. 60 Hz Twin-T Notch Filter, Q = 10

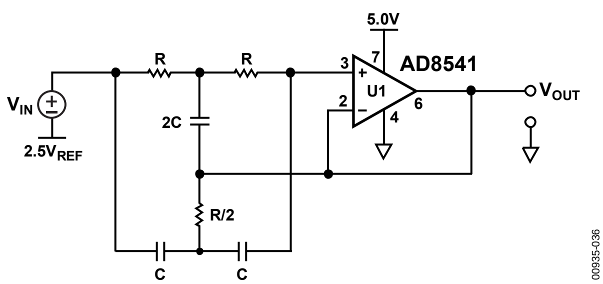


Figure 37. 60 Hz Twin-T Notch Filter, Q = ∞ (Ideal)

Figure 38 is an example of the AD8544 in a notch filter circuit. The frequency dependent negative resistance (FDNR) notch filter has fewer critical matching requirements than the twin-T notch, where as the Q of the FDNR is directly proportional to a single resistor R1. Although matching component values is still important, it is also much easier and/or less expensive to accomplish in the FDNR circuit. For example, the twin-T notch uses three capacitors with two unique values, whereas the FDNR circuit uses only two capacitors, which may be of the same value. U3 is simply a buffer that is added to lower the output impedance of the circuit.

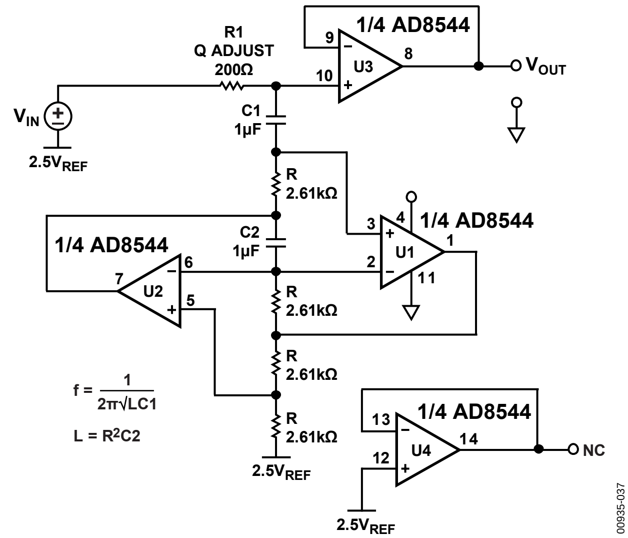


Figure 38. FDNR 60 Hz Notch Filter with Output Buffer

COMPARATOR FUNCTION

A comparator function is a common application for a spare op amp in a quad package. Figure 39 illustrates ¼ of the AD8544 as a comparator in a standard overload detection application. Unlike many op amps, the AD854x family can double as comparators because this op amp family has a rail-to-rail differential input range, rail-to-rail output, and a great speed vs. power ratio. R2 is used to introduce hysteresis. The AD854x, when used as comparators, have 5 µs propagation delay at 5 V and 5 µs overload recovery time.

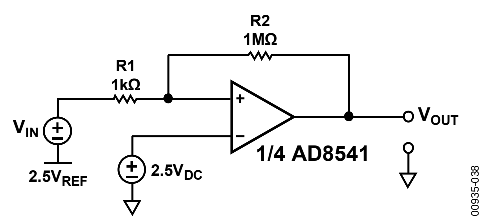


Figure 39. AD854x Comparator Application—Overload Detector

PHOTODIODE APPLICATION

The AD854x family has very high impedance with an input bias current typically around 4 pA. This characteristic allows the AD854x op amps to be used in photodiode applications and other applications that require high input impedance. Note that the AD854x has significant voltage offset that can be removed by capacitive coupling or software calibration.

Figure 40 illustrates a photodiode or current measurement application. The feedback resistor is limited to 10 MΩ to avoid excessive output offset. In addition, a resistor is not needed on the noninverting input to cancel bias current offset because the bias current-related output offset is not significant when compared to the voltage offset contribution. For best performance, follow the standard high impedance layout techniques, which include the following:

- Shielding the circuit.
- Cleaning the circuit board.
- Putting a trace connected to the noninverting input around the inverting input.
- Using separate analog and digital power supplies.

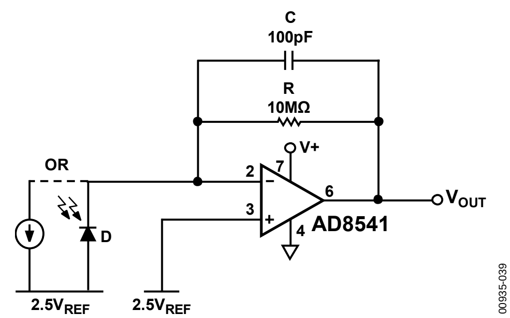
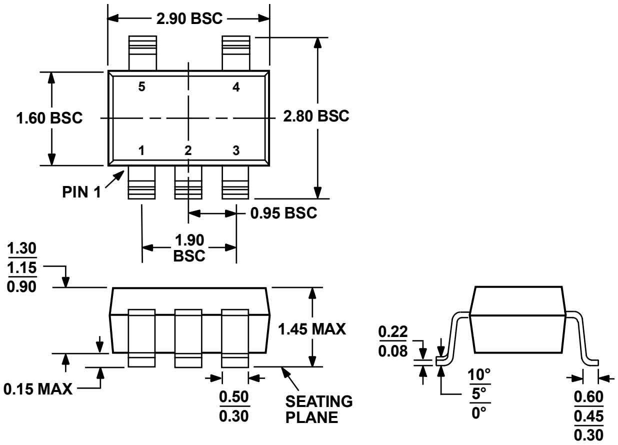


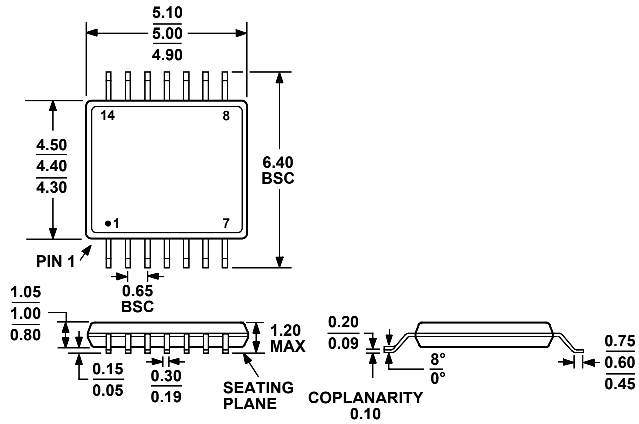
Figure 40. High Input Impedance Application—Photodiode Amplifier

OUTLINE DIMENSIONS



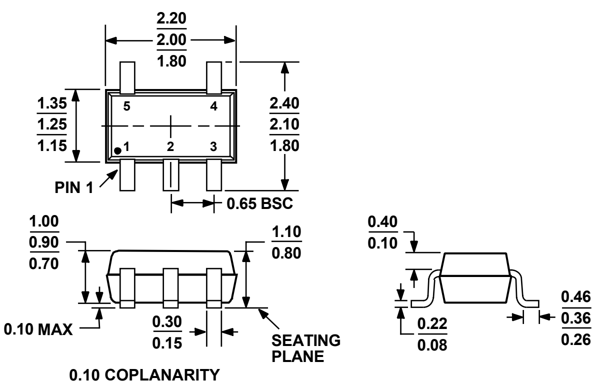
COMPLIANT TO JEDEC STANDARDS MO-178-AA

Figure 41. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters



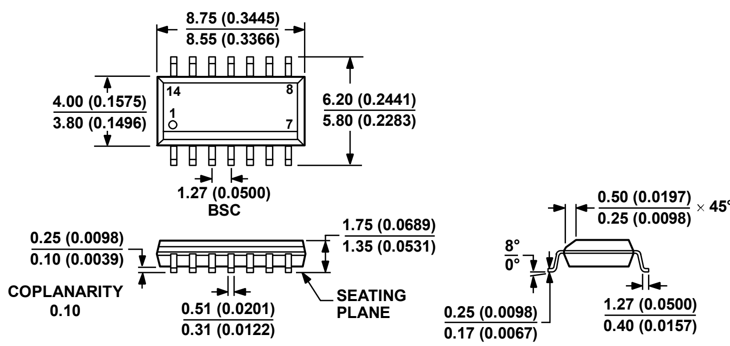
COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 42. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-203-AA

Figure 43. 5-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-5)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 44. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)

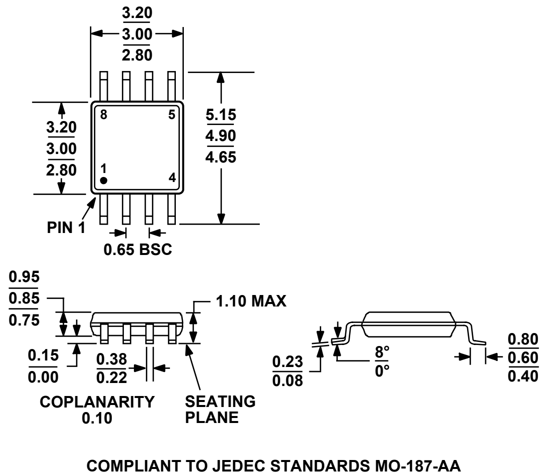


Figure 45. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

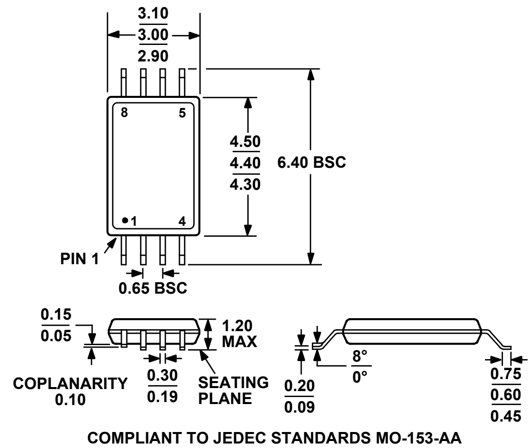


Figure 46. 8-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-8)
Dimensions shown in millimeters

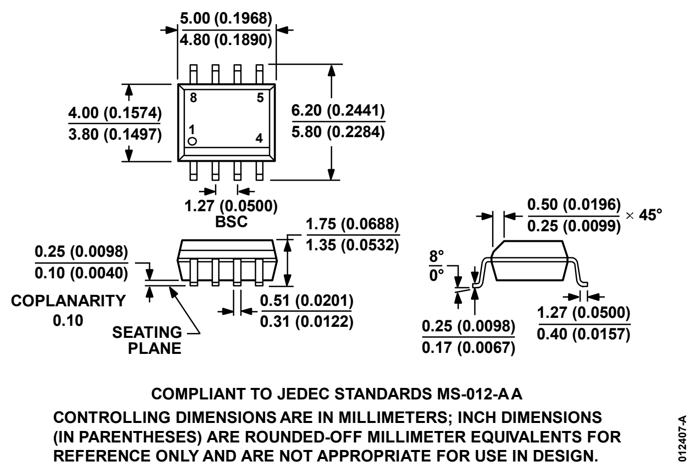


Figure 47. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8541AKS-R2	–40°C to +125°C	5-Lead SC70	KS-5	A4B
AD8541AKS-REEL7	–40°C to +125°C	5-Lead SC70	KS-5	A4B
AD8541AKSZ-R2[1]	–40°C to +125°C	5-Lead SC70	KS-5	A12
AD8541AKSZ-REEL7[1]	–40°C to +125°C	5-Lead SC70	KS-5	A12
AD8541ART-R2	–40°C to +125°C	5-Lead SOT-23	RJ-5	A4A
AD8541ART-REEL	–40°C to +125°C	5-Lead SOT-23	RJ-5	A4A
AD8541ART-REEL7	–40°C to +125°C	5-Lead SOT-23	RJ-5	A4A
AD8541ARTZ-R2[1]	–40°C to +125°C	5-Lead SOT-23	RJ-5	A4A#
AD8541ARTZ-REEL[1]	–40°C to +125°C	5-Lead SOT-23	RJ-5	A4A#
AD8541ARTZ-REEL7[1]	–40°C to +125°C	5-Lead SOT-23	RJ-5	A4A#
AD8541AR	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8541AR-REEL	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8541AR-REEL7	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8541ARZ[1]	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8541ARZ-REEL[1]	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8541ARZ-REEL7[1]	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8542AR	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8542AR-REEL	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8542AR-REEL7	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8542ARZ[1]	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8542ARZ-REEL[1]	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8542ARZ-REEL7[1]	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8542ARM-R2	–40°C to +125°C	8-Lead MSOP	RM-8	AVA
AD8542ARM-REEL	–40°C to +125°C	8-Lead MSOP	RM-8	AVA
AD8542ARMZ-R2[1]	–40°C to +125°C	8-Lead MSOP	RM-8	AVA#
AD8542ARMZ-REEL[1]	–40°C to +125°C	8-Lead MSOP	RM-8	AVA#
AD8542ARU	–40°C to +125°C	8-Lead TSSOP	RU-8	
AD8542ARU-REEL	–40°C to +125°C	8-Lead TSSOP	RU-8	
AD8542ARUZ[1]	–40°C to +125°C	8-Lead TSSOP	RU-8	
AD8542ARUZ-REEL[1]	–40°C to +125°C	8-Lead TSSOP	RU-8	
AD8544AR	–40°C to +125°C	14-Lead SOIC_N	R-14	
AD8544AR-REEL	–40°C to +125°C	14-Lead SOIC_N	R-14	
AD8544AR-REEL7	–40°C to +125°C	14-Lead SOIC_N	R-14	
AD8544ARZ[1]	–40°C to +125°C	14-Lead SOIC_N	R-14	
AD8544ARZ-REEL[1]	–40°C to +125°C	14-Lead SOIC_N	R-14	
AD8544ARZ-REEL7[1]	–40°C to +125°C	14-Lead SOIC_N	R-14	
AD8544ARU	–40°C to +125°C	14-Lead TSSOP	RU-14	
AD8544ARU-REEL	–40°C to +125°C	14-Lead TSSOP	RU-14	
AD8544ARUZ[1]	–40°C to +125°C	14-Lead TSSOP	RU-14	
AD8544ARUZ-REEL[1]	–40°C to +125°C	14-Lead TSSOP	RU-14	

[1] Z = RoHS Compliant Part; # denotes RoHS compliant product may be top or bottom marked.

NOTES

NOTES

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