10MHz, 6V/µs, Dual/Quad Rail-to-Rail Input and Output Precision C-Load Op Amps

FEATURES

- **Rail-to-Rail Input and Output**
- **475µV Max V_{OS} from V^+ to V^-**
- **Gain-Bandwidth Product: 10MHz**
- **Slew Rate: 6V/µs**
- **Low Supply Current per Amplifier: 1.7mA**
- Input Offset Current: 65nA Max
- Input Bias Current: 650nA Max
- Open-Loop Gain: 1000V/mV Min
- Low Input Noise Voltage: $12nV/\sqrt{Hz}$ Typ
- Wide Supply Range: 2.2V to ±15V
- Large Output Drive Current: 30mA
- Stable for Capacitive Loads Up to 10,000pF
- Dual in 8-Pin PDIP and SO Package
- Quad in Narrow 14-Pin SO

APPLICATIONS

- Driving A-to-D Converters
- Active Filters
- Rail-to-Rail Buffer Amplifiers
- Low Voltage Signal Processing
- Battery-Powered Systems

DESCRIPTION

The LT®1498/LT1499 are dual/quad, rail-to-rail input and output precision C-Load™ op amps with a 10MHz gain-bandwidth product and a 6V/µs slew rate.

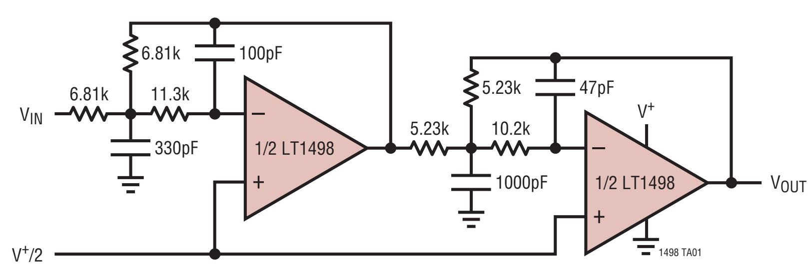
The LT1498/LT1499 are designed to maximize input dynamic range by delivering precision performance over the full supply voltage. Using a patented technique, both input stages of the LT1498/LT1499 are trimmed, one at the negative supply and the other at the positive supply. The resulting guaranteed common mode rejection is much better than other rail-to-rail input op amps. When used as a unity-gain buffer in front of single supply 12-bit A-to-D converters, the LT1498/LT1499 are guaranteed to add less than 1LSB of error even in single 3V supply systems.

With 110dB of supply rejection, the LT1498/LT1499 maintain their performance over a supply range of 2.2V to 36V and are specified for 3V, 5V and ±15V supplies. The inputs can be driven beyond the supplies without damage or phase reversal of the output. These op amps remain stable while driving capacitive loads up to 10,000pF.

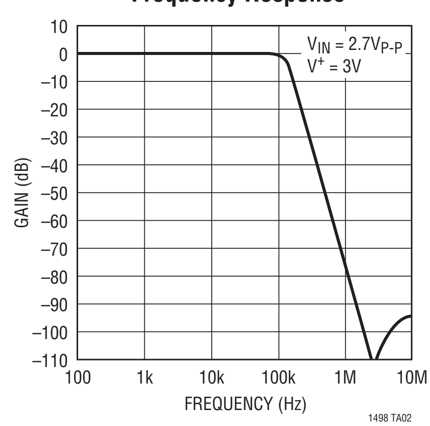
The LT1498 is available with the standard dual op amp configuration in 8-pin PDIP and SO packaging. The LT1499 features the standard quad op amp configuration and is available in a 14-pin plastic SO package. These devices can be used as plug-in replacements for many standard op amps to improve input/output range and precision.

TYPICAL APPLICATION

Single Supply 100kHz 4th Order Butterworth Filter



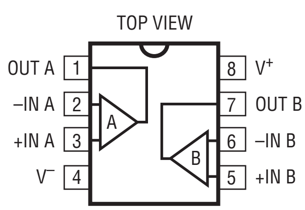
Frequency Response



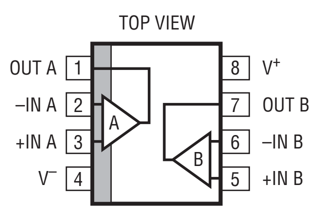
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 36V
Input Current .... ±10mA
Output Short-Circuit Duration (Note 2) .... Continuous
Operating Temperature Range
LT1498/LT1499 .... –40°C to 85°C
LT1498H/LT1499H .... –40°C to 125°C
LT1498MP .... –55°C to 125°C
Specified Temperature Range (Note 4)
LT1498/LT1499 .... –40°C to 85°C
LT1498H/LT1499H .... –40°C to 125°C
LT1498MP .... –55°C to 125°C
Junction Temperature .... 150°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

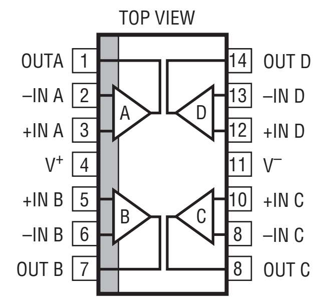
PIN CONFIGURATION



N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 130°C/W



S PACKAGE
14-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1498CN8#PBF	LT1498CN8#TRPBF	LT1498CN8	8-Lead Plastic PDIP	0°C to 70°C
LT1498CS8#PBF	LT1498CS8#TRPBF	1498	8-Lead Plastic SO	0°C to 70°C
LT1498IN8#PBF	LT1498IN8#TRPBF	LT1498IN8	8-Lead Plastic PDIP	–40°C to 85°C
LT1498IS8#PBF	LT1498IS8#TRPBF	1498I	8-Lead Plastic SO	–40°C to 85°C
LT1498HS8#PBF	LT1498HS8#TRPBF	1498H	8-Lead Plastic SO	–40°C to 125°C
LT1498MPS8#PBF	LT1498MPS8#TRPBF	1498MP	8-Lead Plastic SO	–55°C to 125°C
LT1499CS#PBF	LT1499CS#TRPBF	LT1499CS	14-Lead Plastic SO	0°C to 70°C
LT1499IS#PBF	LT1499IS#TRPBF	LT1499IS	14-Lead Plastic SO	–40°C to 85°C
LT1499HS#PBF	LT1499HS#TRPBF	LT1499HS	14-Lead Plastic SO	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = 5V, 0V$; $V_S = 3V, 0V$; $V_{CM} = V_{OUT}$ = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$ $V_{CM} = V^-$		150 150	475 475	µV µV
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ to V^+		150	425	µV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^+, V^-$ (Note 5)		200	750	µV
I_B	Input Bias Current	$V_{CM} = V^+$ $V_{CM} = V^-$	0 –650	250 –250	650 0	nA nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^-$ to V^+		500	1300	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+$ (Note 5) $V_{CM} = V^-$ (Note 5)	0 –100	10 –10	100 0	nA nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$ $V_{CM} = V^-$		5 5	65 65	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^-$ to V^+		10	130	nA
	Input Noise Voltage	0.1Hz to 10Hz		400		nV_{P-P}
e_n	Input Noise Voltage Density	f = 1kHz		12		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 1kHz		0.3		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance			5		pF
A_{VOL}	Large-Signal Voltage Gain	$V_S = 5V$, $V_O = 75mV$ to $4.8V$, $R_L = 10k$ $V_S = 3V$, $V_O = 75mV$ to $2.8V$, $R_L = 10k$	600 500	3800 2000		V/mV V/mV
CMRR	Common Mode Rejection Ratio	$V_S = 5V$, $V_{CM} = V^-$ to V^+ $V_S = 3V$, $V_{CM} = V^-$ to V^+	81 76	90 86		dB dB
	CMRR Match (Channel-to-Channel) (Note 5)	$V_S = 5V$, $V_{CM} = V^-$ to V^+ $V_S = 3V$, $V_{CM} = V^-$ to V^+	75 70	91 86		dB dB
PSRR	Power Supply Rejection Ratio	$V_S = 2.2V$ to $12V$, $V_{CM} = V_O = 0.5V$	88	105		dB
	PSRR Match (Channel-to-Channel) (Note 5)	$V_S = 2.2V$ to $12V$, $V_{CM} = V_O = 0.5V$	82	103		dB
V_{OL}	Output Voltage Swing (Low) (Note 6)	No Load $I_{SINK} = 0.5mA$ $I_{SINK} = 2.5mA$		14 35 90	30 70 200	mV mV mV
V_{OH}	Output Voltage Swing (High) (Note 6)	No Load $I_{SOURCE} = 0.5mA$ $I_{SOURCE} = 2.5mA$		2.5 50 140	10 100 250	mV mV mV
I_{SC}	Short-Circuit Current	$V_S = 5V$ $V_S = 3V$	±12.5 ±12.0	±24 ±19		mA mA
I_S	Supply Current per Amplifier			1.7	2.2	mA
GBW	Gain-Bandwidth Product (Note 7)		6.8	10.5		MHz
SR	Slew Rate (Note 8)	$V_S = 5V$, $A_V = –1$, R_L = Open, $V_O = 4V$ $V_S = 3V$, $A_V = –1$, R_L = Open	2.6 2.3	4.5 4.0		V/µs V/µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range 0°C < T_A < 70°C. V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$ $V_{CM} = V^- + 0.1V$	● ●		175 175	650 650	µV µV
V_{OS} TC	Input Offset Voltage Drift (Note 3)	 $V_{CM} = V^+$	● ●		0.5 1.5	2.5 4.0	µV/°C µV/°C
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^- + 0.1V$ to V^+	●		170	600	µV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^- + 0.1V$, V^+ (Note 5)	●		200	900	µV
I_B	Input Bias Current	$V_{CM} = V^+$ $V_{CM} = V^- + 0.1V$	● ●	0 –780	275 –275	780 0	nA nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^- + 0.1V$ to V^+	●		550	1560	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+$ (Note 5) $V_{CM} = V^- + 0.1V$ (Note 5)	● ●	0 –170	15 –15	170 0	nA nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$ $V_{CM} = V^- + 0.1V$	● ●		10 10	85 85	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^- + 0.1V$ to V^+	●		20	170	nA
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 75mV to 4.8V, R_L = 10k V_S = 3V, V_O = 75mV to 2.8V, R_L = 10k	● ●	500 400	2500 2000		V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, $V_{CM} = V^- + 0.1V$ to V^+ V_S = 3V, $V_{CM} = V^- + 0.1V$ to V^+	● ●	78 73	89 85		dB dB
	CMRR Match (Channel-to-Channel) (Note 5)	V_S = 5V, $V_{CM} = V^- + 0.1V$ to V^+ V_S = 3V, $V_{CM} = V^- + 0.1V$ to V^+	● ●	74 69	90 86		dB dB
PSRR	Power Supply Rejection Ratio	V_S = 2.3V to 12V, $V_{CM} = V_O$ = 0.5V	●	86	102		dB
	PSRR Match (Channel-to-Channel) (Note 5)	V_S = 2.3V to 12V, $V_{CM} = V_O$ = 0.5V	●	80	102		dB
V_{OL}	Output Voltage Swing (Low) (Note 6)	No Load I_{SINK} = 0.5mA I_{SINK} = 2.5mA	● ● ●		17 40 110	35 80 220	mV mV mV
V_{OH}	Output Voltage Swing (High) (Note 6)	No Load I_{SOURCE} = 0.5mA I_{SOURCE} = 2.5mA	● ● ●		3.5 55 160	15 120 300	mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V	● ●	±12 ±10	±23 ±20		mA mA
I_S	Supply Current per Amplifier		●		1.9	2.6	mA
GBW	Gain-Bandwidth Product (Note 7)		●	6.1	9		MHz
SR	Slew Rate (Note 8)	V_S = 5V, A_V = –1, R_L = Open, V_O = 4V V_S = 3V, A_V = –1, R_L = Open	● ●	2.5 2.2	4.0 3.5		V/µs V/µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range $-40°C < T_A < 85°C$. V_S = 5V, 0V; V_S = 3V, 0V; $V_{CM} = V_{OUT}$ = half supply, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$ $V_{CM} = V^- + 0.1V$	● ●		250 250	750 750	μV μV
V_{OS} TC	Input Offset Voltage Drift (Note 3)	 $V_{CM} = V^+$	● ●		0.5 1.5	2.5 4.0	μV/°C μV/°C
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^- + 0.1V$ to V^+	●		250	650	μV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^- + 0.1V$, V^+ (Note 5)	●		300	1500	μV
I_B	Input Bias Current	$V_{CM} = V^+$ $V_{CM} = V^- + 0.1V$	● ●	0 –975	350 –350	975 0	nA nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^- + 0.1V$ to V^+	●		700	1950	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+$ (Note 5) $V_{CM} = V^- + 0.1V$ (Note 5)	● ●	0 –180	30 –30	180 0	nA nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$ $V_{CM} = V^- + 0.1V$	● ●		15 15	110 110	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^- + 0.1V$ to V^+	●		30	220	nA
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 75mV to 4.8V, R_L = 10k V_S = 3V, V_O = 75mV to 2.8V, R_L = 10k	● ●	400 300	2500 2000		V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, $V_{CM} = V^- + 0.1V$ to V^+ V_S = 3V, $V_{CM} = V^- + 0.1V$ to V^+	● ●	77 73	86 81		dB dB
	CMRR Match (Channel-to-Channel) (Note 5)	V_S = 5V, $V_{CM} = V^- + 0.1V$ to V^+ V_S = 3V, $V_{CM} = V^- + 0.1V$ to V^+	● ●	72 69	86 83		dB dB
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 12V, $V_{CM} = V_O$ = 0.5V	●	86	100		dB
	PSRR Match (Channel-to-Channel) (Note 5)	V_S = 2.5V to 12V, $V_{CM} = V_O$ = 0.5V	●	80	100		dB
V_{OL}	Output Voltage Swing (Low) (Note 6)	No Load I_{SINK} = 0.5mA I_{SINK} = 2.5mA	● ● ●		18 45 110	40 80 220	mV mV mV
V_{OH}	Output Voltage Swing (High) (Note 6)	No Load I_{SOURCE} = 0.5mA I_{SOURCE} = 2.5mA	● ● ●		3.5 60 170	15 120 300	mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V	● ●	±7.5 ±7.5	±15 ±15		mA mA
I_S	Supply Current per Amplifier		●		2.0	2.7	mA
GBW	Gain-Bandwidth Product (Note 7)		●	5.8	8.5		MHz
SR	Slew Rate (Note 8)	V_S = 5V, A_V = –1, R_L = Open, V_O = 4V V_S = 3V, A_V = –1, R_L = Open	● ●	2.2 1.9	3.6 3.2		V/μs V/μs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range –40°C < T_A < 125°C. V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+ - 0.5V$ $V_{CM} = V^- + 0.5V$	● ●		300 300	1100 1100	µV µV
V_{OS} TC	Input Offset Voltage Drift (Note 3)	 $V_{CM} = V^+ - 0.5V$	● ●		0.5 1.5		µV/°C µV/°C
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^- + 0.5V$ to $V^+ - 0.5V$	●		250	2300	µV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^- + 0.5V$, $V^+ - 0.5V$ (Note 5)	●		300	1900	µV
I_B	Input Bias Current	$V_{CM} = V^+ - 0.5V$ $V_{CM} = V^- + 0.5V$	● ●	0 –1100	450 –450	1100 0	nA nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^- + 0.5V$ to $V^+ - 0.5V$	●		900	2200	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+ - 0.5V$ (Note 5) $V_{CM} = V^- + 0.5V$ (Note 5)	● ●	0 –400	40 –40	400 0	nA nA
I_{OS}	Input Offset Current	$V_{CM} = V^+ - 0.5V$ $V_{CM} = V^- + 0.5V$	● ●		40 40	300 300	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^- + 0.5V$ to $V^+ - 0.5V$	●		80	600	nA
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 10k V_S = 3V, V_O = 0.5V to 2.5V, R_L = 10k	● ●	40 20	210 210		V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, $V_{CM} = V^- + 0.5V$ to $V^+ - 0.5V$ V_S = 3V, $V_{CM} = V^- + 0.5V$ to $V^+ - 0.5V$	● ●	66 62	80 75		dB dB
	CMRR Match (Channel-to-Channel) (Note 5)	V_S = 5V, $V_{CM} = V^- + 0.5V$ to $V^+ - 0.5V$ V_S = 3V, $V_{CM} = V^- + 0.5V$ to $V^+ - 0.5V$	● ●	62 58	80 75		dB dB
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 12V, V_{CM} = V_O = 0.5V	●	86	100		dB
	PSRR Match (Channel-to-Channel) (Note 5)	V_S = 2.5V to 12V, V_{CM} = V_O = 0.5V	●	80	100		dB
V_{OL}	Output Voltage Swing (Low) (Note 6)	No Load I_{SINK} = 0.5mA I_{SINK} = 2.5mA	● ● ●		22 45 110	50 80 220	mV mV mV
V_{OH}	Output Voltage Swing (High) (Note 6)	No Load I_{SOURCE} = 0.5mA I_{SOURCE} = 2.5mA	● ● ●		3.5 60 170	20 120 350	mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V	● ●	±5 ±5	±15 ±15		mA mA
I_S	Supply Current per Amplifier		●		2.4	3.0	mA
GBW	Gain-Bandwidth Product (Note 7)		●	5.8	8.5		MHz
SR	Slew Rate (Note 8)	V_S = 5V, A_V = –1, R_L = Open, V_O = 4V V_S = 3V, A_V = –1, R_L = Open	● ●	2.0 1.7	3.6 3.2		V/µs V/µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range $-55°C < T_A < 125°C$. V_S = 5V, 0V; V_S = 3V, 0V; $V_{CM} = V_{OUT}$ = half supply, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+ - 0.5V$ $V_{CM} = V^- + 0.5V$	● ●		300 300	1100 1100	µV µV
V_{OS} TC	Input Offset Voltage Drift (Note 3)	 $V_{CM} = V^+ - 0.5V$	● ●		0.5 1.5		µV/°C µV/°C
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^- + 0.5V$ to $V^+ - 0.5V$	●		250	2300	µV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^- + 0.5V$, $V^+ - 0.5V$ (Note 5)	●		300	1900	µV
I_B	Input Bias Current	$V_{CM} = V^+ - 0.5V$ $V_{CM} = V^- + 0.5V$	● ●	0 –1100	450 –450	1100 0	nA nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^- + 0.5V$ to $V^+ - 0.5V$	●		900	2200	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+ - 0.5V$ (Note 5) $V_{CM} = V^- + 0.5V$ (Note 5)	● ●	0 –400	40 –40	400 0	nA nA
I_{OS}	Input Offset Current	$V_{CM} = V^+ - 0.5V$ $V_{CM} = V^- + 0.5V$	● ●		40 40	300 300	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^- + 0.5V$ to $V^+ - 0.5V$	●		80	600	nA
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 10k V_S = 3V, V_O = 0.5V to 2.5V, R_L = 10k	● ●	40 20	210 210		V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, $V_{CM} = V^- + 0.5V$ to $V^+ - 0.5V$ V_S = 3V, $V_{CM} = V^- + 0.5V$ to $V^+ - 0.5V$	● ●	66 62	80 75		dB dB
	CMRR Match (Channel-to-Channel) (Note 5)	V_S = 5V, $V_{CM} = V^- + 0.5V$ to $V^+ - 0.5V$ V_S = 3V, $V_{CM} = V^- + 0.5V$ to $V^+ - 0.5V$	● ●	62 58	80 75		dB dB
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 12V, $V_{CM} = V_O$ = 0.5V	●	86	100		dB
	PSRR Match (Channel-to-Channel) (Note 5)	V_S = 2.5V to 12V, $V_{CM} = V_O$ = 0.5V	●	80	100		dB
V_{OL}	Output Voltage Swing (Low) (Note 6)	No Load I_{SINK} = 0.5mA I_{SINK} = 2.5mA	● ● ●		22 45 110	50 80 220	mV mV mV
V_{OH}	Output Voltage Swing (High) (Note 6)	No Load I_{SOURCE} = 0.5mA I_{SOURCE} = 2.5mA	● ● ●		3.5 60 170	20 120 350	mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V	● ●	±5 ±5	±15 ±15		mA mA
I_S	Supply Current per Amplifier		●		2.4	3.0	mA
GBW	Gain-Bandwidth Product (Note 7)		●	5.8	8.5		MHz
SR	Slew Rate (Note 8)	V_S = 5V, A_V = –1, R_L = Open, V_O = 4V V_S = 3V, A_V = –1, R_L = Open	● ●	2.0 1.7	3.6 3.2		V/µs V/µs

ELECTRICAL CHARACTERISTICS $T_A = 25°C$. $V_S = ±15V$, $V_{CM} = 0V$, $V_{OUT} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$ $V_{CM} = V^-$		200 200	800 800	μV μV
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ to V^+		150	650	μV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^+$, V^- (Note 5)		250	1400	μV
I_B	Input Bias Current	$V_{CM} = V^+$ $V_{CM} = V^-$	0 –715	250 –250	715 0	nA nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^-$ to V^+		500	1430	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+$ (Note 5) $V_{CM} = V^-$ (Note 5)	0 –120	12 –12	120 0	nA nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$ $V_{CM} = V^-$		6 6	70 70	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^-$ to V^+		12	140	nA
	Input Noise Voltage	0.1Hz to 10Hz		400		nV_{P-P}
e_n	Input Noise Voltage Density	f = 1kHz		12		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 1kHz		0.3		$pA/\sqrt{Hz}$
A_{VOL}	Large-Signal Voltage Gain	V_O = –14.5V to 14.5V, R_L = 10k V_O = –10V to 10V, R_L = 2k	1000 500	5200 2300		V/mV V/mV
	Channel Separation	V_O = –10V to 10V, R_L = 2k	116	130		dB
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^-$ to V^+	93	106		dB
	CMRR Match (Channel-to-Channel) (Note 5)	$V_{CM} = V^-$ to V^+	87	103		dB
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	89	110		dB
	PSRR Match (Channel-to-Channel) (Note 5)	V_S = ±5V to ±15V	83	105		dB
V_{OL}	Output Voltage Swing (Low) (Note 6)	No Load I_{SINK} = 0.5mA I_{SINK} = 10mA		18 40 230	30 80 500	mV mV mV
V_{OH}	Output Voltage Swing (High) (Note 6)	No Load I_{SOURCE} = 0.5mA I_{SOURCE} = 10mA		2.5 55 420	10 120 800	mV mV mV
I_{SC}	Short-Circuit Current		±15	±30		mA
I_S	Supply Current per Amplifier			1.8	2.5	mA
GBW	Gain-Bandwidth Product (Note 7)		6.8	10.5		MHz
SR	Slew Rate	A_V = –1, R_L = Open, V_O = ±10V Measure at V_O = ±5V	3.5	6		V/μs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range $0°C < T_A < 70°C$. $V_S = ±15V$, $V_{CM} = 0V$, $V_{OUT} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$ $V_{CM} = V^- + 0.1V$	● ●		200 200	900 900	µV µV
V_{OS} TC	Input Offset Voltage Drift (Note 3)	 $V_{CM} = V^+$	● ●		1.0 2.0	3.5 5.0	µV/°C µV/°C
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^- + 0.1V$ to V^+	●		200	750	µV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^- + 0.1V$, V^+ (Note 5)	●		350	1500	µV
I_B	Input Bias Current	$V_{CM} = V^+$ $V_{CM} = V^- + 0.1V$	● ●	0 –875	300 –300	875 0	nA nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^- + 0.1V$ to V^+	●		600	1750	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+$ (Note 5) $V_{CM} = V^- + 0.1V$ (Note 5)	● ●	0 –180	20 –20	180 0	nA nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$ $V_{CM} = V^- + 0.1V$	● ●		15 15	90 90	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^- + 0.1V$ to V^+	●		30	180	nA
A_{VOL}	Large-Signal Voltage Gain	$V_O = –14.5V$ to $14.5V$, $R_L = 10k$ $V_O = –10V$ to $10V$, $R_L = 2k$	● ●	900 400	5000 2000		V/mV V/mV
	Channel Separation	$V_O = –10V$ to $10V$, $R_L = 2k$	●	112	125		dB
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^- + 0.1V$ to V^+	●	92	103		dB
	CMRR Match (Channel-to-Channel) (Note 5)	$V_{CM} = V^- + 0.1V$ to V^+	●	86	103		dB
PSRR	Power Supply Rejection Ratio	$V_S = ±5V$ to $±15V$	●	88	103		dB
	PSRR Match (Channel-to-Channel) (Note 5)	$V_S = ±5V$ to $±15V$	●	82	103		dB
V_{OL}	Output Voltage Swing (Low) (Note 6)	No Load $I_{SINK} = 0.5mA$ $I_{SINK} = 10mA$	● ● ●		18 45 270	40 90 520	mV mV mV
V_{OH}	Output Voltage Swing (High) (Note 6)	No Load $I_{SOURCE} = 0.5mA$ $I_{SOURCE} = 10mA$	● ● ●		3.5 60 480	15 120 1000	mV mV mV
I_{SC}	Short-Circuit Current		●	±12	±28		mA
I_S	Supply Current per Amplifier		●		1.9	2.8	mA
GBW	Gain-Bandwidth Product (Note 7)		●	6.1	9		MHz
SR	Slew Rate	$A_V = –1$, $R_L = $ Open, $V_O = ±10V$ Measured at $V_O = ±5V$	●	3.4	5.3		V/µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range $-40°C < T_A < 85°C$. $V_S = ±15V$, $V_{CM} = 0V$, $V_{OUT} = 0V$, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$ $V_{CM} = V^- + 0.1V$	● ●		300 300	950 950	µV µV
V_{OS} TC	Input Offset Voltage Drift (Note 3)	 $V_{CM} = V^+$	● ●		1.0 2.0	3.5 5.0	µV/°C µV/°C
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^- + 0.1V$ to V^+	●		250	850	µV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^- + 0.1V$, V^+ (Note 5)	●		350	1800	µV
I_B	Input Bias Current	$V_{CM} = V^+$ $V_{CM} = V^- + 0.1V$	● ●	0 –1050	350 –350	1050 0	nA nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^- + 0.1V$ to V^+	●		700	2100	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+$ (Note 5) $V_{CM} = V^- + 0.1V$ (Note 5)	● ●	0 –200	20 –20	200 0	nA nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$ $V_{CM} = V^- + 0.1V$	● ●		15 15	115 115	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^- + 0.1V$ to V^+	●		30	230	nA
A_{VOL}	Large-Signal Voltage Gain	$V_O = -14.5V$ to $14.5V$, $R_L = 10k$ $V_O = -10V$ to $10V$, $R_L = 2k$	● ●	800 350	5000 2000		V/mV V/mV
	Channel Separation	$V_O = -10V$ to $10V$, $R_L = 2k$	●	110	120		dB
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^- + 0.1V$ to V^+	●	90	101		dB
	CMRR Match (Channel-to-Channel) (Note 5)	$V_{CM} = V^- + 0.1V$ to V^+	●	86	100		dB
PSRR	Power Supply Rejection Ratio	$V_S = ±5V$ to $±15V$	●	88	100		dB
	PSRR Match (Channel-to-Channel) (Note 5)	$V_S = ±5V$ to $±15V$	●	82	100		dB
V_{OL}	Output Voltage Swing (Low) (Note 6)	No Load $I_{SINK} = 0.5mA$ $I_{SINK} = 10mA$	● ● ●		25 50 275	50 100 520	mV mV mV
V_{OH}	Output Voltage Swing (High) (Note 6)	No Load $I_{SOURCE} = 0.5mA$ $I_{SOURCE} = 10mA$	● ● ●		3.5 65 500	15 120 1000	mV mV mV
I_{SC}	Short-Circuit Current		●	±10	±18		mA
I_S	Supply Current per Amplifier		●		2.0	3.0	mA
GBW	Gain-Bandwidth Product (Note 7)		●	5.8	8.5		MHz
SR	Slew Rate	$A_V = -1$, R_L = Open, $V_O = ±10V$ Measure at $V_O = ±5V$	●	3	4.75		V/µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range –40°C < T_A < 125°C. V_S = ±15V, V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+ – 0.5V$ $V_{CM} = V^– + 0.5V$	● ●		350 350	1300 1300	µV µV
V_{OS} TC	Input Offset Voltage Drift (Note 3)	 $V_{CM} = V^+ – 0.5V$	● ●		1.0 2.0		µV/°C µV/°C
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^– + 0.5V$ to $V^+ – 0.5V$	●		250	1500	µV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^– + 0.5V, V^+ – 0.5V$ (Note 5)	●		400	2200	µV
I_B	Input Bias Current	$V_{CM} = V^+ – 0.5V$ $V_{CM} = V^– + 0.5V$	● ●	0 –1200	500 –500	1200 0	nA nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^– + 0.5V$ to $V^+ – 0.5V$	●		1000	2400	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+ – 0.5V$ (Note 5) $V_{CM} = V^– + 0.5V$ (Note 5)	● ●	0 –400	40 –40	400 0	nA nA
I_{OS}	Input Offset Current	$V_{CM} = V^+ – 0.5V$ $V_{CM} = V^– + 0.5V$	● ●		40 40	300 300	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^– + 0.5V$ to $V^+ – 0.5V$	●		80	600	nA
A_{VOL}	Large-Signal Voltage Gain	V_O = –14.5V to 14.5V, R_L = 10k	●	40	400		V/mV
	Channel Separation	V_O = –10V to 10V, R_L = 2k	●	110	120		dB
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^– + 0.5V$ to $V^+ – 0.5V$	●	86	100		dB
	CMRR Match (Channel-to-Channel) (Note 5)	$V_{CM} = V^– + 0.5V$ to $V^+ – 0.5V$	●	80	100		dB
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	●	88	100		dB
	PSRR Match (Channel-to-Channel) (Note 5)	V_S = ±5V to ±15V	●	80	100		dB
V_{OL}	Output Voltage Swing (Low) (Note 6)	No Load I_{SINK} = 0.5mA I_{SINK} = 10mA	● ● ●		25 50 275	75 100 520	mV mV mV
V_{OH}	Output Voltage Swing (High) (Note 6)	No Load I_{SOURCE} = 0.5mA I_{SOURCE} = 10mA	● ● ●		3.5 65 500	20 120 1400	mV mV mV
I_{SC}	Short-Circuit Current		●	±7.5	±12		mA
I_S	Supply Current per Amplifier		●		2.5	3.2	mA
GBW	Gain-Bandwidth Product (Note 7)		●	5.8	8.5		MHz
SR	Slew Rate	A_V = –1, R_L = Open, V_O = ±10V Measure at V_O = ±5V	●	2.2	4.75		V/µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range –55°C < T_A < 125°C. V_S = ±15V, V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+ – 0.5V$ $V_{CM} = V^- + 0.5V$	● ●		350 350	1300 1300	μV μV
V_{OS} TC	Input Offset Voltage Drift (Note 3)	 $V_{CM} = V^+ – 0.5V$	● ●		1.0 2.0		μV/°C μV/°C
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^- + 0.5V$ to $V^+ – 0.5V$	●		250	1500	μV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^- + 0.5V$, $V^+ – 0.5V$ (Note 5)	●		400	2200	μV
I_B	Input Bias Current	$V_{CM} = V^+ – 0.5V$ $V_{CM} = V^- + 0.5V$	● ●	0 –1200	500 –500	1200 0	nA nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^- + 0.5V$ to $V^+ – 0.5V$	●		1000	2400	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+ – 0.5V$ (Note 5) $V_{CM} = V^- + 0.5V$ (Note 5)	● ●	0 –400	40 –40	400 0	nA nA
I_{OS}	Input Offset Current	$V_{CM} = V^+ – 0.5V$ $V_{CM} = V^- + 0.5V$	● ●		40 40	300 300	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^- + 0.5V$ to $V^+ – 0.5V$	●		80	600	nA
A_{VOL}	Large-Signal Voltage Gain	V_O = –14.5V to 14.5V, R_L = 10k	●	40	400		V/mV
	Channel Separation	V_O = –10V to 10V, R_L = 2k	●	110	120		dB
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^- + 0.5V$ to $V^+ – 0.5V$	●	86	100		dB
	CMRR Match (Channel-to-Channel) (Note 5)	$V_{CM} = V^- + 0.5V$ to $V^+ – 0.5V$	●	80	100		dB
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	●	88	100		dB
	PSRR Match (Channel-to-Channel) (Note 5)	V_S = ±5V to ±15V	●	80	100		dB
V_{OL}	Output Voltage Swing (Low) (Note 6)	No Load I_{SINK} = 0.5mA I_{SINK} = 10mA	● ● ●		25 50 275	75 100 520	mV mV mV
V_{OH}	Output Voltage Swing (High) (Note 6)	No Load I_{SOURCE} = 0.5mA I_{SOURCE} = 10mA	● ● ●		3.5 65 500	20 120 1400	mV mV mV
I_{SC}	Short-Circuit Current		●	±7.5	±12		mA
I_S	Supply Current per Amplifier		●		2.5	3.2	mA
GBW	Gain-Bandwidth Product (Note 7)		●	5.8	8.5		MHz
SR	Slew Rate	A_V = –1, R_L = Open, V_O = ±10V Measure at V_O = ±5V	●	2.2	4.75		V/μs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 3: This parameter is not 100% tested.

Note 4: The LT1498C/LT1499C are guaranteed to meet specified performance from 0°C to 70°C. The LT1498C/LT1499C are designed, characterized and expected to meet specified performance from –40°C to 85°C but are not tested or QA sampled at these temperatures. The LT1498I/LT1499I are guaranteed to meet specified performance from –40°C to 85°C. The LT1498H/LT1499H are guaranteed to meet specified performance from –40°C to 125°C. The LT1498MP is guaranteed to meet specified performance from –55°C to 125°C.

Note 5: Matching parameters are the difference between amplifiers A and D and between B and C on the LT1499; between the two amplifiers on the LT1498.

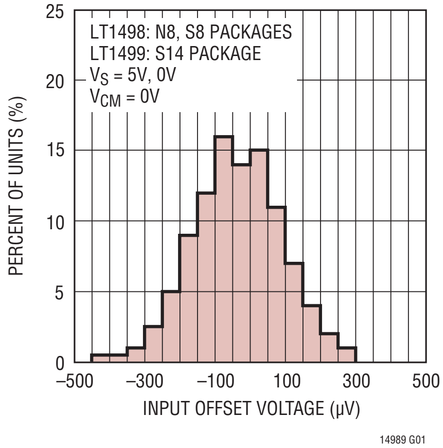
Note 6: Output voltage swings are measured between the output and power supply rails.

Note 7: V_S = 3V, V_S = ±15V GBW limit guaranteed by correlation to 5V tests.

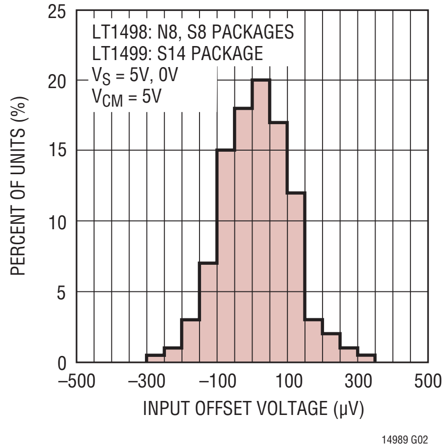
Note 8: V_S = 3V, V_S = 5V slew rate limit guaranteed by correlation to ±15V tests.

TYPICAL PERFORMANCE CHARACTERISTICS

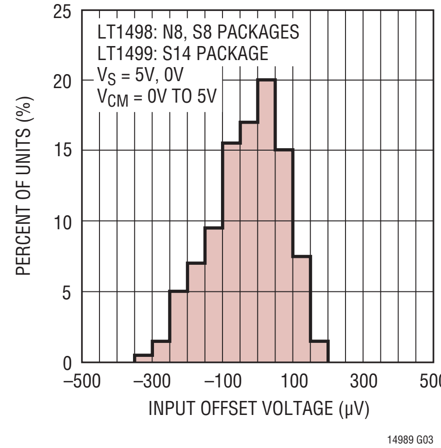
V_{OS} Distribution, V_{CM} = 0V (PNP Stage)



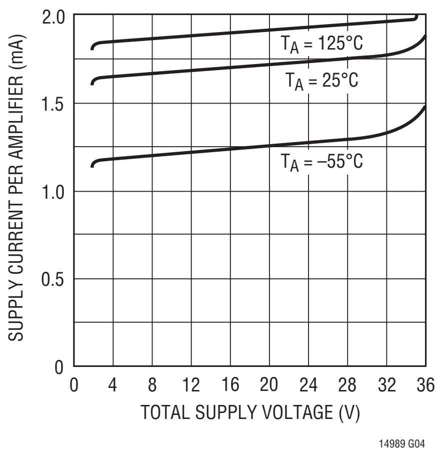
V_{OS} Distribution V_{CM} = 5V (NPN Stage)



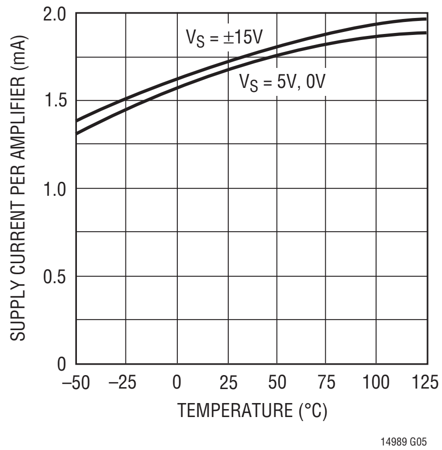
ΔV_{OS} Shift for V_{CM} = 0V to 5V



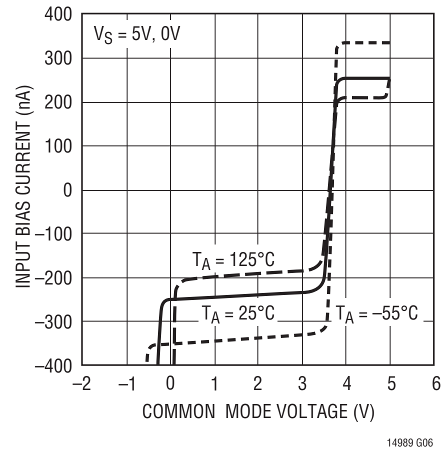
Supply Current vs Supply Voltage



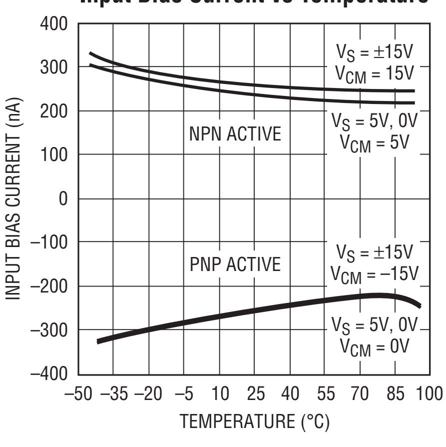
Supply Current vs Temperature



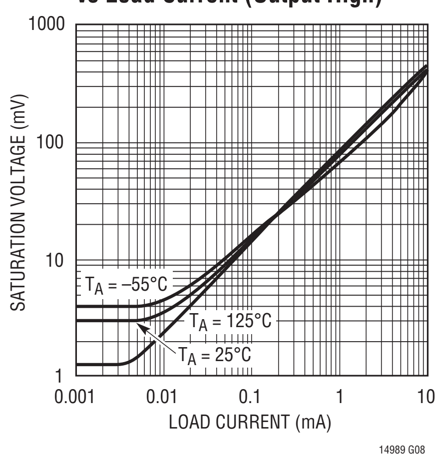
Input Bias Current vs Common Mode Voltage



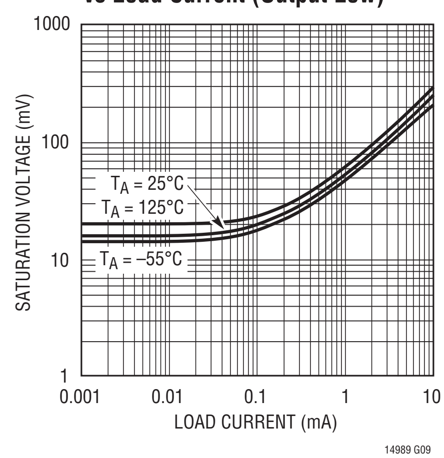
Input Bias Current vs Temperature



Output Saturation Voltage vs Load Current (Output High)

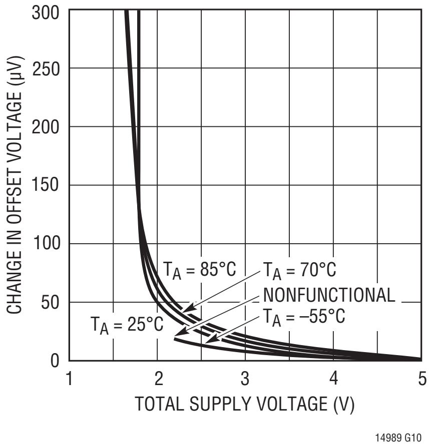


Output Saturation Voltage vs Load Current (Output Low)

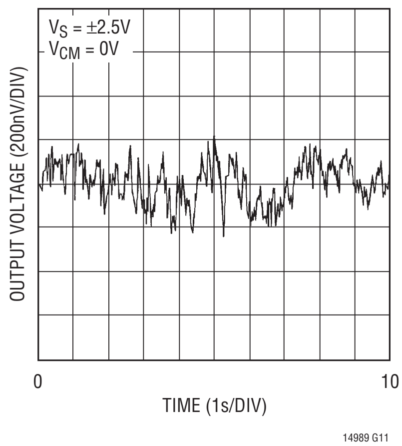


TYPICAL PERFORMANCE CHARACTERISTICS

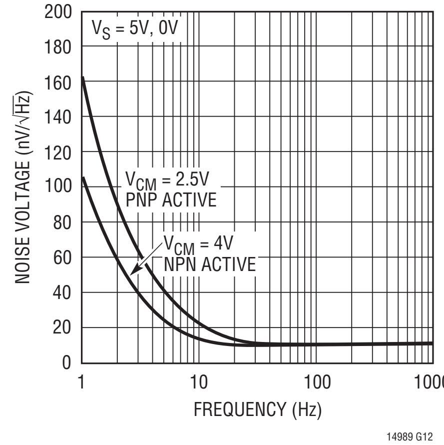
Minimum Supply Voltage



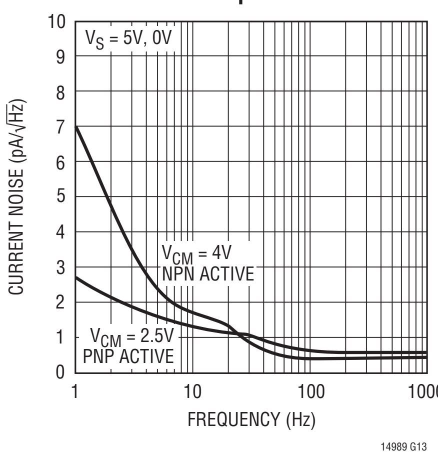
0.1Hz to 10Hz Output Voltage Noise



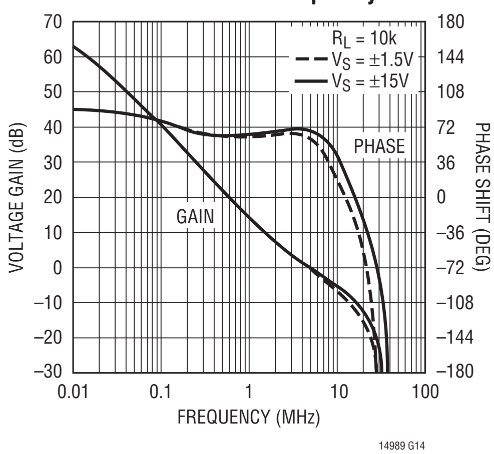
Noise Voltage Spectrum



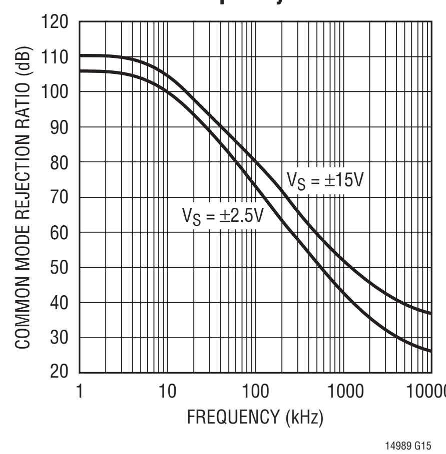
Noise Current Spectrum



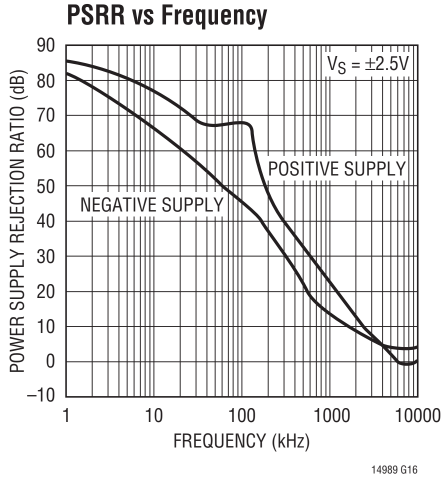
Gain and Phase vs Frequency



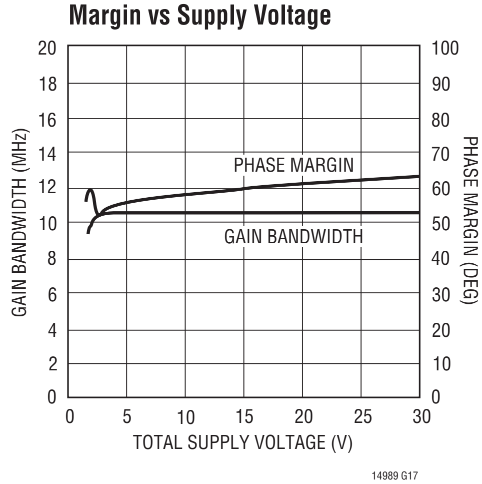
CMRR vs Frequency



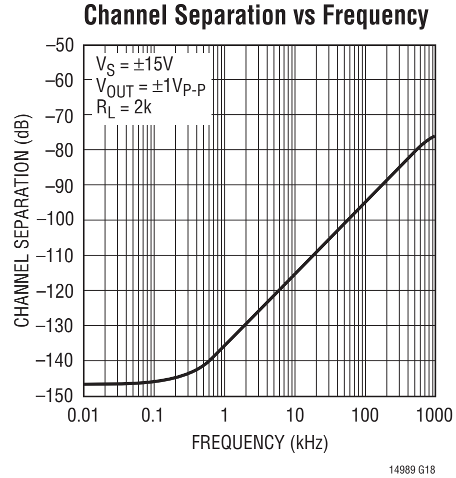
PSRR vs Frequency



Gain Bandwidth and Phase Margin vs Supply Voltage

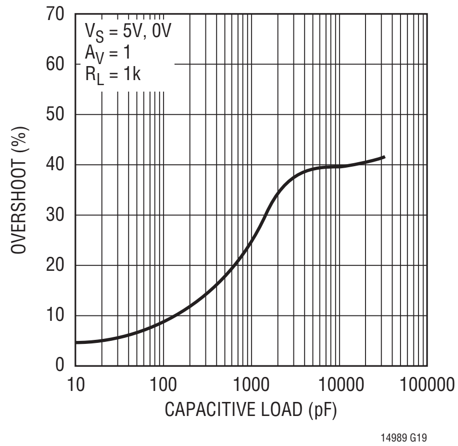


Channel Separation vs Frequency

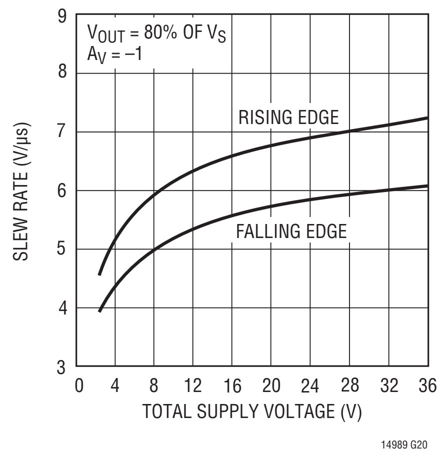


TYPICAL PERFORMANCE CHARACTERISTICS

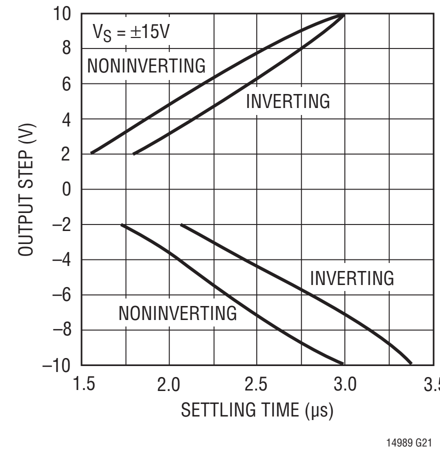
Capacitive Load Handling



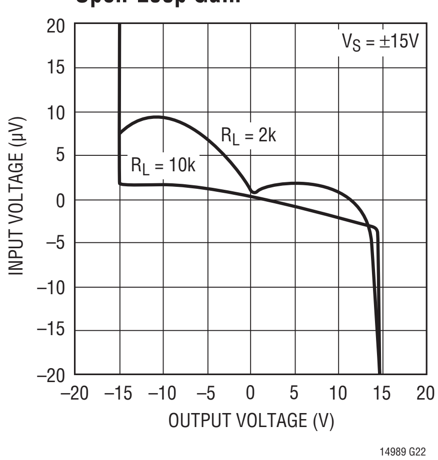
Slew Rate vs Supply Voltage



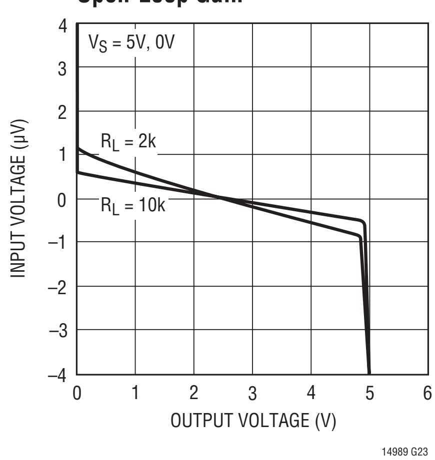
Output Step vs Settling Time to 0.01%



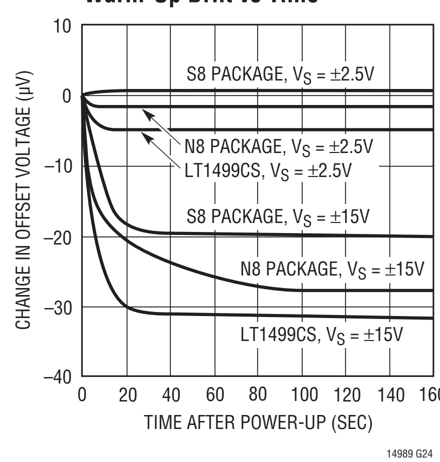
Open-Loop Gain



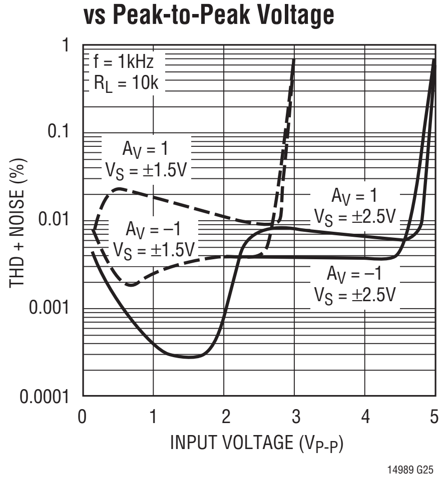
Open-Loop Gain



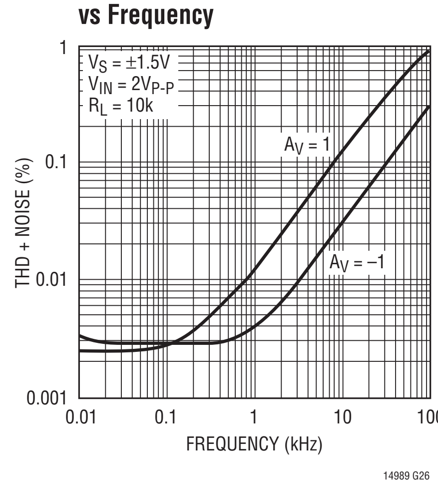
Warm-Up Drift vs Time



Total Harmonic Distortion + Noise vs Peak-to-Peak Voltage



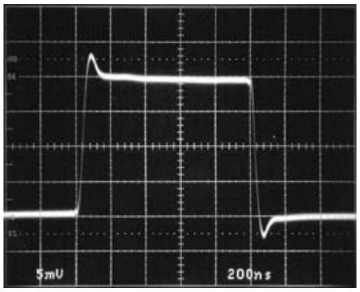
Total Harmonic Distortion + Noise vs Frequency



TYPICAL PERFORMANCE CHARACTERISTICS

5V Small-Signal Response

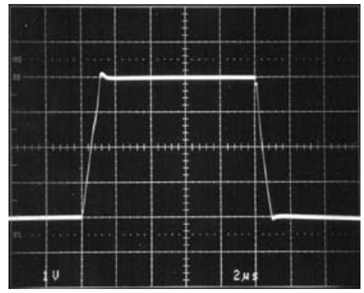
5mV/DIV



V_S = 5V 200ns/DIV 14989 G27
A_V = 1
V_{IN} = 20mV_{P-P} AT 50kHz
R_L = 1k

5V Large-Signal Response

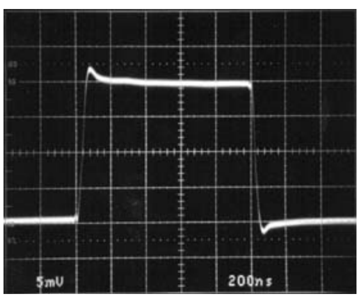
1V/DIV



V_S = 5V 2μs/DIV 14989 G28
A_V = 1
V_{IN} = 4V_{P-P} AT 10kHz
R_L = 1k

±15V Small-Signal Response

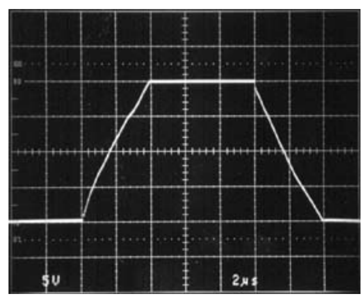
5mV/DIV



V_S = ±15V 200ns/DIV 14989 G29
A_V = 1
V_{IN} = 20mV_{P-P} AT 50kHz
R_L = 1k

±15V Large-Signal Response

5V/DIV



V_S = ±15V 2μs/DIV 14989 G30
A_V = 1
V_{IN} = 20V_{P-P} AT 10kHz
R_L = 1k

APPLICATIONS INFORMATION

Rail-to-Rail Input and Output

The LT1498/LT1499 are fully functional for an input and output signal range from the negative supply to the positive supply. Figure 1 shows a simplified schematic of the amplifier. The input stage consists of two differential amplifiers, a PNP stage (Q1/Q2) and an NPN stage (Q3/Q4) which are active over different ranges of input common mode voltage. A complementary common emitter output stage (Q14/Q15) is employed allowing the output to swing from rail-to-rail. The devices are fabricated on Linear Technology's proprietary complementary bipolar process to ensure very similar DC and AC characteristics for the output devices (Q14/Q15).

The PNP differential input pair is active for input common mode voltages, V_{CM}, between the negative supply to approximately 1.3V below the positive supply. As V_{CM} moves further toward the positive supply, the transistor (Q5) will steer the tail current, I_1, to the current mirror (Q6/Q7) activating the NPN differential pair, and the PNP differential pair becomes inactive for the rest of the input common mode range up to the positive supply.

The output is configured with a pair of complementary common emitter stages that enables the output to swing from rail to rail. Capacitors (C1 and C2) form local feedback loops that lower the output impedance at high frequencies.

Input Offset Voltage

The offset voltage changes depending upon which input stage is active. The input offsets are random, but are trimmed to less than 475µV. To maintain the precision characteristics of the amplifier, the change of V_{OS} over the entire input common mode range (CMRR) is guaranteed to be less than 425µV on a single 5V supply.

Input Bias Current

The input bias current polarity also depends on the input common mode voltage, as described in the previous section. When the PNP differential pair is active, the input bias currents flow out of the input pins; they flow in opposite direction when the NPN input stage is active. The offset error due to input bias current can be minimized by equalizing the noninverting and inverting input source impedances. This will reduce the error since the input offset currents are much less than the input bias currents.

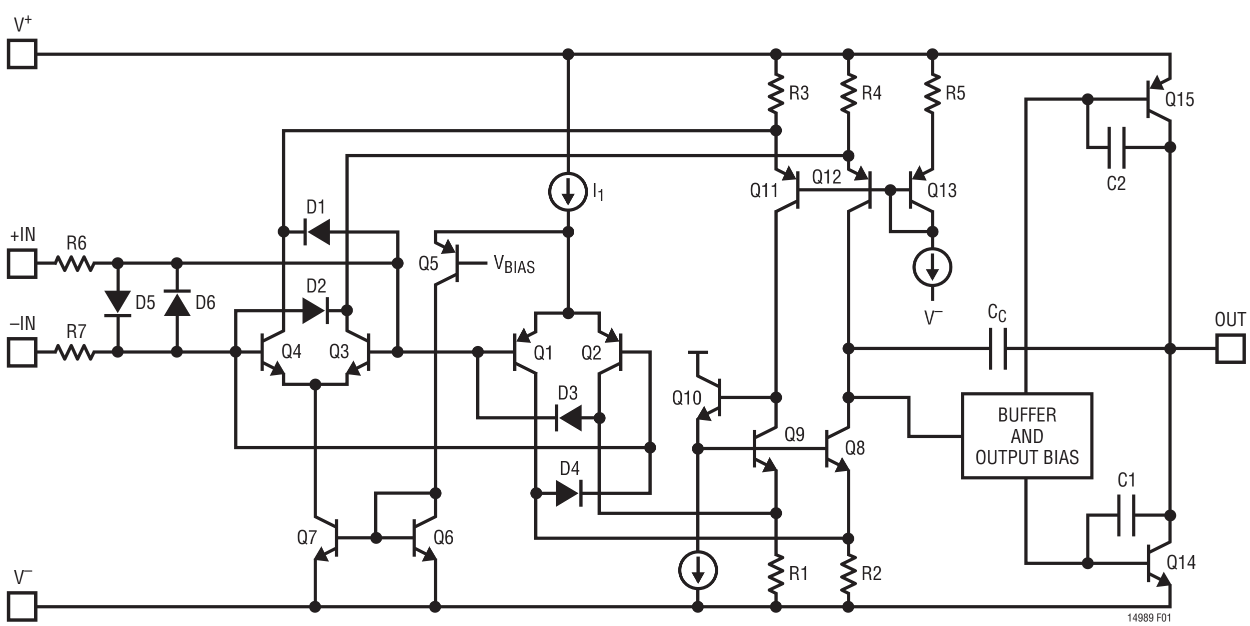


Figure 1. LT1498 Simplified Schematic Diagram

APPLICATIONS INFORMATION

Overdrive Protection

To prevent the output from reversing polarity when the input voltage exceeds the power supplies, two pair of crossing diodes D1 to D4 are employed. When the input voltage exceeds either power supply by approximately 700mV, D1/D2 or D3/D4 will turn on, forcing the output to the proper polarity. For the phase reversal protection to work properly, the input current must be less than 5mA. If the amplifier is to be severely overdriven, an external resistor should be used to limit the overdrive current.

Furthermore, the LT1498/LT1499's input stages are protected by a pair of back-to-back diodes, D5/D6. When a differential voltage of more than 0.7V is applied to the inputs, these diodes will turn on, preventing the Zener breakdown of the input transistors. The current in D5/D6 should be limited to less than 10mA. Internal resistors R6 and R7 (700Ω total) limit the input current for differential input signals of 7V or less. For larger input levels, a resistor in series with either or both inputs should be used to limit the current. Worst-case differential input voltage usually occurs when the output is shorted to ground. In addition, the amplifier is protected against ESD strikes up to 3kV on all pins.

Capacitive Load

The LT1498/LT1499 are designed for ease of use. The amplifier can drive a capacitive load of more than 10nF without oscillation at unity gain. When driving a heavy capacitive load, the bandwidth is reduced to maintain stability. Figures 2a and 2b illustrate the stability of the device for small-signal and large-signal conditions with capacitive loads. Both the small-signal and large-signal transient response with a 10nF capacitive load are well behaved.

Feedback Components

To minimize the loading effect of feedback, it is possible to use the high value feedback resistors to set the gain. However, care must be taken to insure that the pole formed by the feedback resistors and the total input capacitance at the inverting input does not degrade the stability of the amplifier. For instance, the LT1498/LT1499 in a noninverting gain of 2, set with two 30k resistors, will probably oscillate with 10pF total input capacitance (5pF input capacitance + 5pF board capacitance). The amplifier has a 2.5MHz crossing frequency and a 60° phase margin at 6dB of gain. The feedback resistors and the total input capacitance create a pole at 1.06MHz that induces 67° of phase shift at 2.5MHz! The solution is simple, either lower the value of the resistors or add a feedback capacitor of 10pF of more.

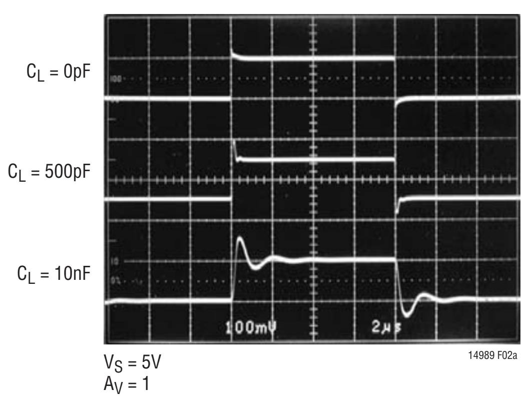


Figure 2a. LT1498 Small-Signal Response

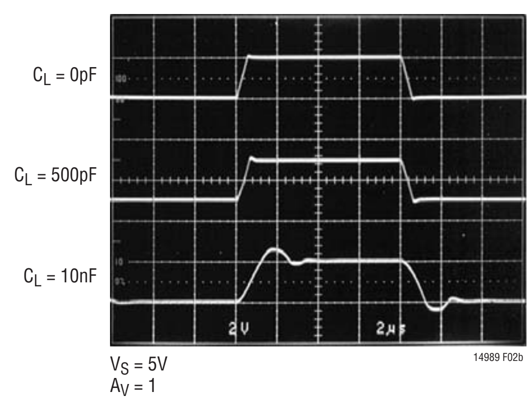
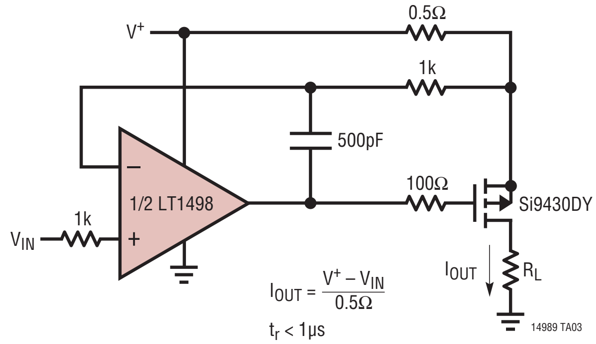


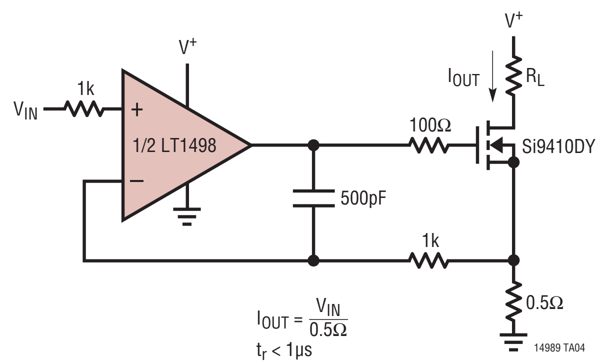
Figure 2b. LT1498 Large-Signal Response

TYPICAL APPLICATIONS

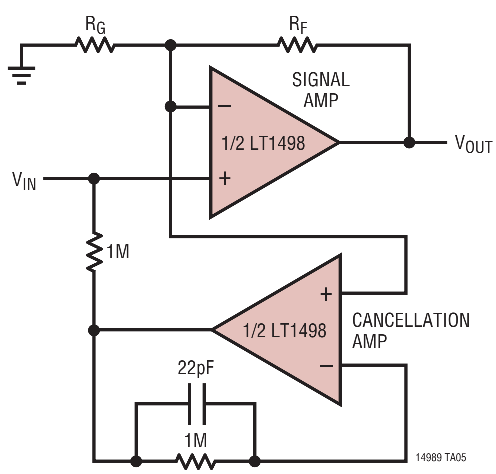
1A Voltage Controlled Current Source



1A Voltage Controlled Current Sink



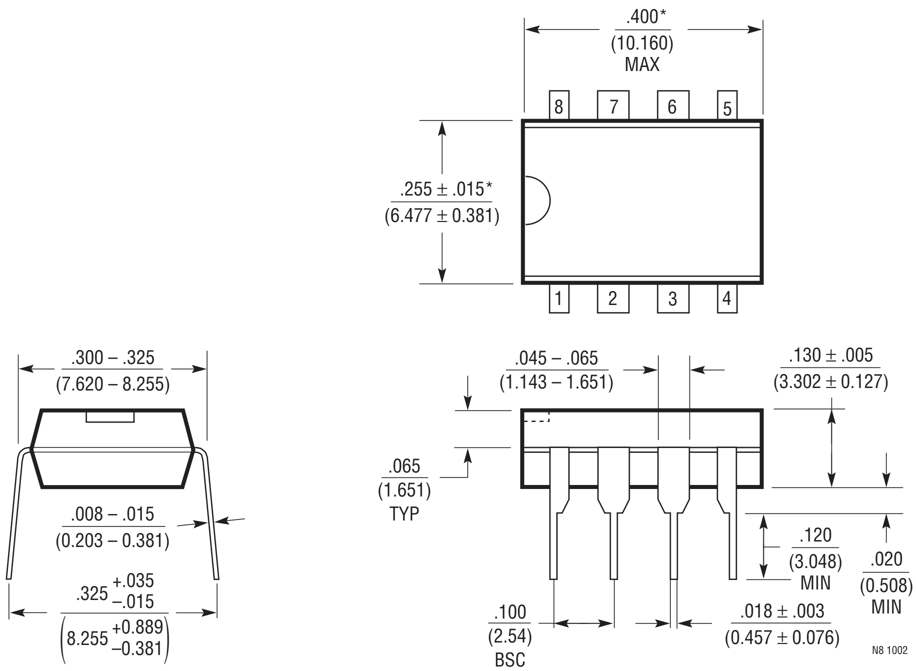
Input Bias Current Cancellation



INPUT BIAS CURRENT LESS THAN 50nA
FOR 500mV ≤ V_{IN} ≤ (V^+ – 500mV)

PACKAGE DESCRIPTION

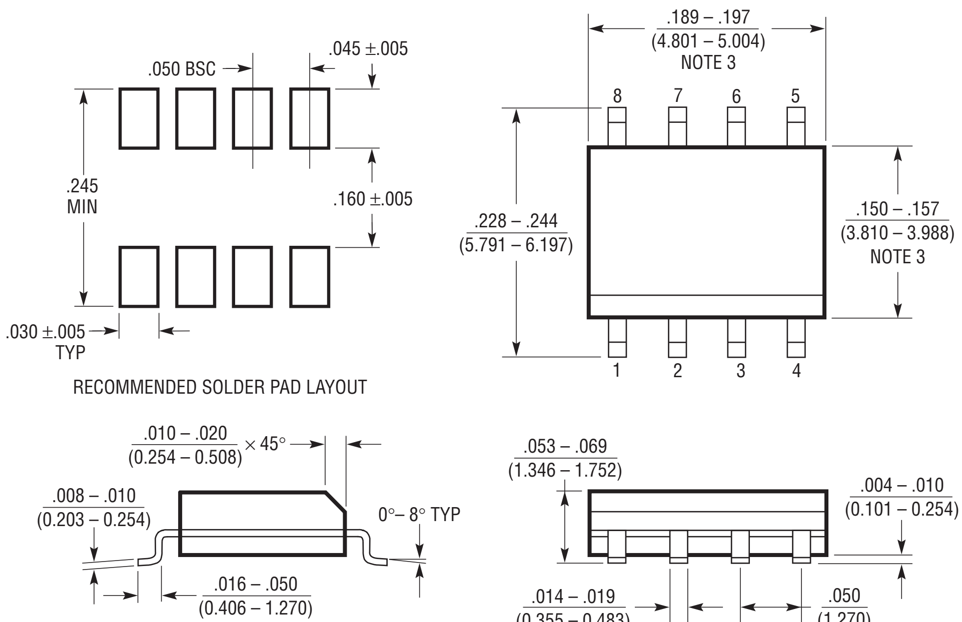
N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

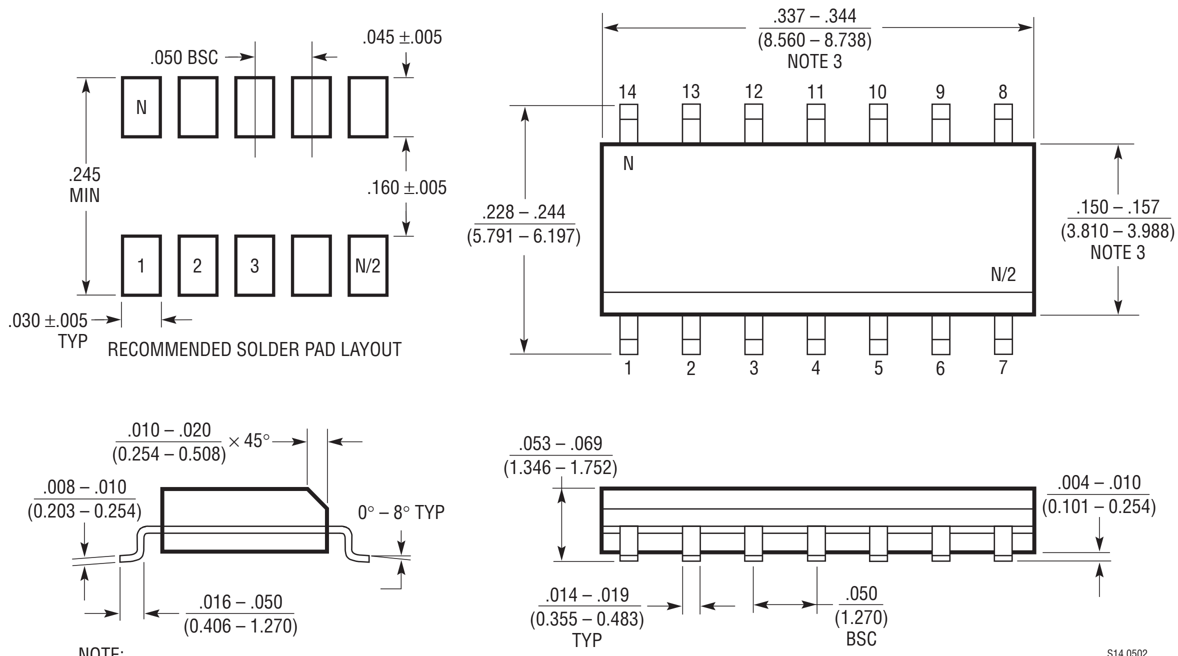
S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

PACKAGE DESCRIPTION

S Package
14-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

REVISION HISTORY (Revision history begins at Rev E)

REV	DATE	DESCRIPTION	PAGE NUMBER
E	10/09	Edit in Absolute Maximum Ratings	2
F	01/10	Added LT1498H/LT1499H (H-Grade) Parts. Reflected throughout the data sheet.	2-24
G	03/10	Updated Part Markings in Order Information Section	2
		Updated Conditions for A_{VOL} in Electrical Characteristics Section	6, 7

TYPICAL APPLICATION

Bidirectional Current Sensor

A bidirectional current sensor for battery-powered systems is shown in Figure 3. Two outputs are provided: one proportional to charge current, the other proportional to discharge current. The circuit takes advantage of the LT1498's rail-to-rail input range and its output phase reversal protection. During the charge cycle, the op amp A1 forces a voltage equal to $(I_L)(R_{SENSE})$ across R_A. This voltage is then amplified at the Charge Out by the ratio of R_B over R_A. In this mode, the output of A2 remains high, keeping Q2 off and the Discharge Out low, even though the (+) input of A2 exceeds the positive power supply. During the discharge cycle, A2 and Q2 are active and the operation is similar to the charge cycle.

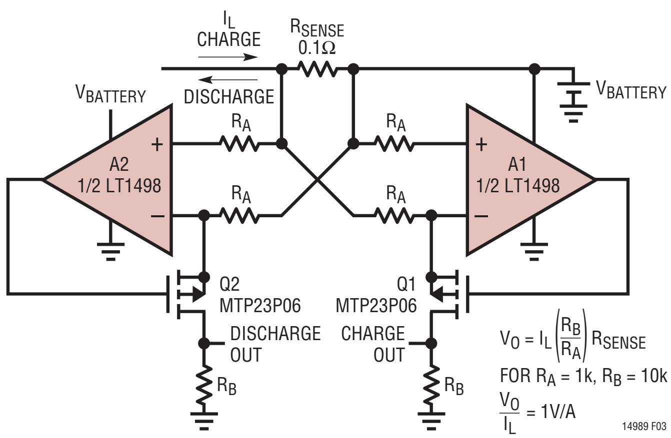


Figure 3. Bidirectional Current Sensor

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC®1152	Rail-to-Rail Input and Output, Zero-Drift Op Amp	High DC Accuracy, 10μV $V_{OS(MAX)}$, 100nV/°C Drift, 1MHz GBW, 1V/μs Slew Rate, Max Supply Current 2.2mA
LT1211/LT1212	Dual/Quad 14MHz, 7V/μs, Single Supply Precision Op Amps	Input Common Mode Includes Ground, 275μV $V_{OS(MAX)}$, 6μV/°C Max Drift, Max Supply Current 1.8mA per Op Amp
LT1213/LT1214	Dual/Quad 28MHz, 12V/μs, Single Supply Precision Op Amps	Input Common Mode Includes Ground, 275μV $V_{OS(MAX)}$, 6μV/°C Max Drift, Max Supply Current 3.5mA per Op Amp
LT1215/LT1216	Dual/Quad 23MHz, 50V/μs, Single Supply Precision Op Amps	Input Common Mode Includes Ground, 450μV $V_{OS(MAX)}$, Max Supply Current 6.6mA per Op Amp
LT1366/LT1367	Dual/Quad Precision, Rail-to-Rail Input and Output Op Amps	475μV $V_{OS(MAX)}$, 400kHz GBW, 0.13V/μs Slew Rate, Max Supply Current 520μA per Op Amp
LT1490/LT1491	Dual/Quad Micropower, Rail-to-Rail Input and Output Op Amps	Max Supply Current 50μA per Op Amp, 200kHz GBW, 0.07V/μs Slew Rate, Operates with Inputs 44V Above V^- Independent of V^+
LT1884/LT1885	Dual/Quad, Rail-to-Rail Output Picoamp Input Precision Op Amps	I_{CC} = 650μA, V_{OS} < 50μV, I_B < 400pA

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