TS1100/01/02/03 Data Sheet

TS1100/01/02/03 Uni- and Bidirectional Current-Sense Amplifiers

The TS1100/01/02/03 Unidirectional and Bidirectional Current Sense Amplifiers consume a very low 0.68 µA supply current.

The TS1100 and TS1101 high-side current sense amplifiers (CSA) combine a 100 µV (max) input offset voltage (V_{OS}) and a 0.6% (max) gain error (GE), with both specifications optimized for any precision current measurement.

The TS1102 and TS1103 CSAs combine a 200 µV (max) V_{OS} and a 0.6% (max) GE for cost-sensitive applications.

For all high-side current sensing applications, the TS1100/01/02/03 CSAs are self-powered and feature a wide input common-mode voltage range from 2 to 27 V.

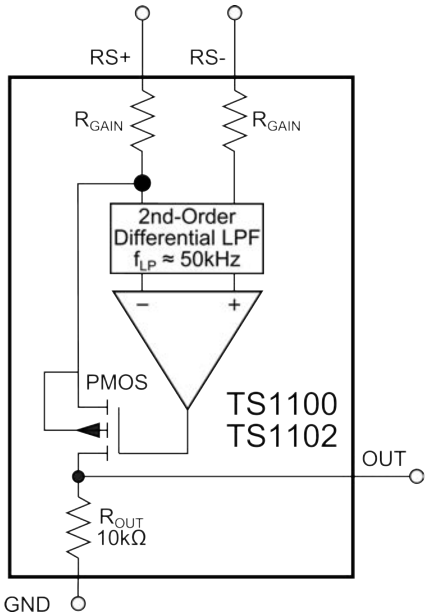
For the bidirectional CSAs, TS1101 and TS1103, a SIGN comparator digital output is provided that indicates the direction of current flow. All CSAs are specified for operation over the –40 °C to +105 °C temperature range.

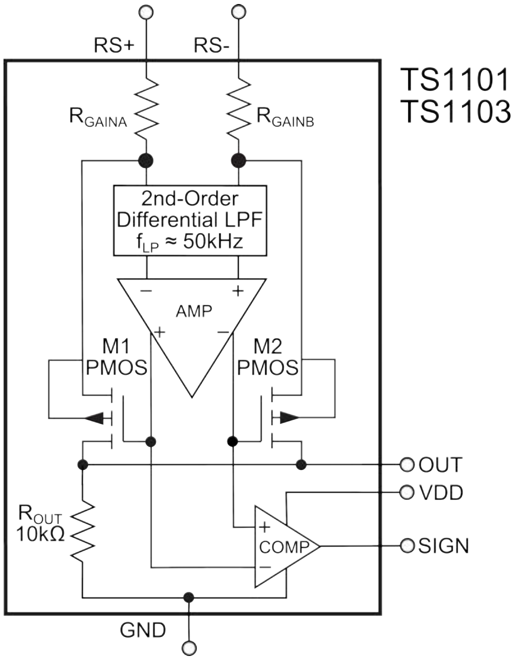
Applications

- Power Management Systems
- Portable/Battery-Powered Systems
- Smart Chargers
- Battery Monitoring
- Overcurrent and Undercurrent Detection
- Remote Sensing
- Industrial Control

KEY FEATURES

- Low Supply Current
  - Current Sense Amplifier: 0.68 µA
  - I_{VDD}: 0.02 µA
- High Side Bidirectional and Unidirectional Current Sense Amplifier
- Wide CSA Input Common Mode Range: +2 V to +27 V
- Low CSA Input Offset Voltage: 100 µV (max) (TS1100 and TS1101 Only)
- Low Gain Error: 0.6% (max)
- Four Gain Options Available:
  - 25 V/V
  - 50 V/V
  - 100 V/V
  - 200 V/V
- 5-Lead and 6-Lead SOT23 Packaging





1. Ordering Information

Ordering Number[1]	Part Marking	Description	Gain V/V
TS1100-25EG5	TADJ	Unidirectional current sense amplifier ($V_{OS(MAX)}$ = 200 μV)	25
TS1100-50EG5	TADK		50
TS1100-100EG5	TADL		100
TS1100-200EG5	TADM		200
TS1101-25EG6	TADN	Bidirectional current sense amplifier ($V_{OS(MAX)}$ = 200 μV)	25
TS1101-50EG6	TADP		50
TS1101-100EG6	TADQ		100
TS1101-200EG6	TADR		200
TS1102-25EG5	TADS	Unidirectional current sense amplifier ($V_{OS(MAX)}$ = 300 μV)	25
TS1102-50EG5	TADT		50
TS1102-100EG5	TADU		100
TS1102-200EG5	TADV		200
TS1101-25EG6	TADW	Bidirectional current sense amplifier ($V_{OS(MAX)}$ = 300 μV)	25
TS1101-50EG6	TADX		50
TS1101-100EG6	TADY		100
TS1101-200EG6	TADZ		200

Note:

1. Adding the suffix, "T", to the part number (e.g., TS1101-25EG6T) denotes tape and reel.

2. System Overview

2.1 Typical Application Circuits

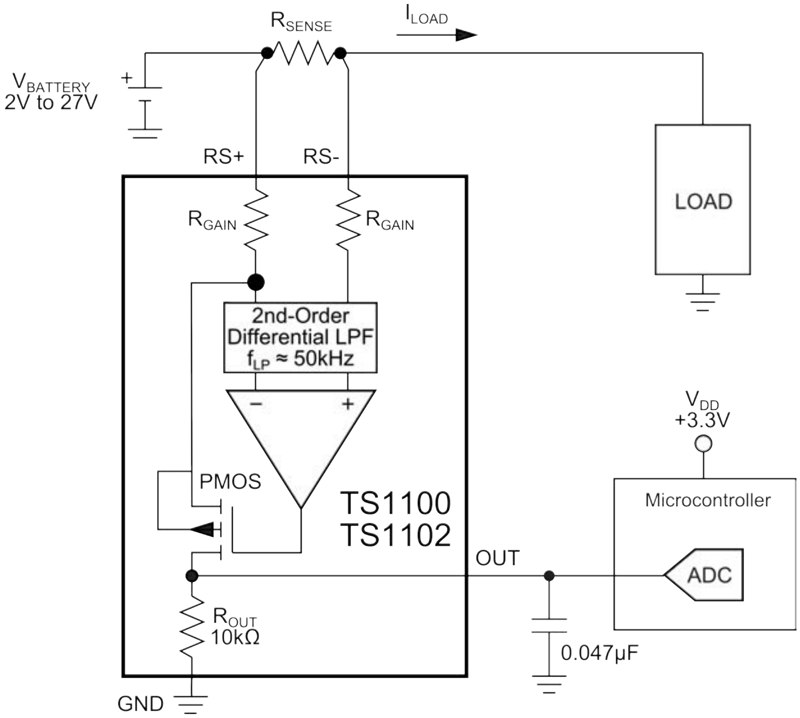


Figure 2.1. TS1100 and TS1102 Typical Application Circuit

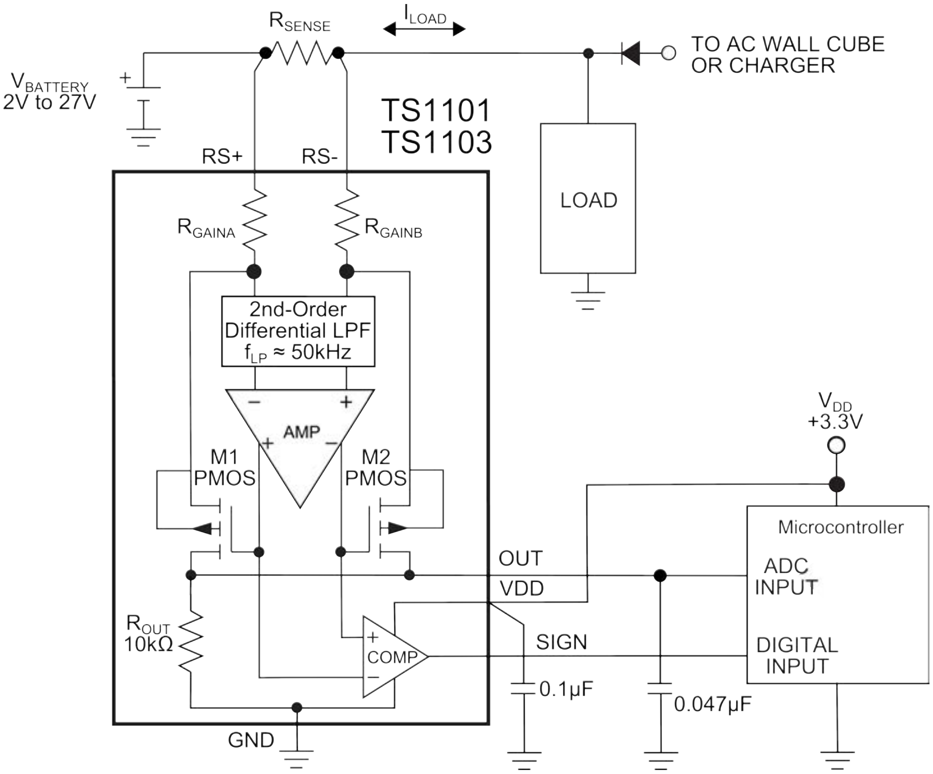


Figure 2.2. TS1101 and TS1103 Typical Application Circuit

2.2 Theory of Operation

The internal configuration of the TS1100/02 (a unidirectional high-side, current-sense amplifier) is based on a common operational amplifier circuit used for measuring load currents (in one direction) in the presence of high common-mode voltages. In the general case, a current-sense amplifier monitors the voltage caused by a load current through an external sense resistor and generates an output voltage as a function of that load current.

The internal configuration of the TS1101/03 (a bidirectional high-side, current-sense amplifier) is a variation of the TS1100/02 unidirectional current-sense amplifier. In the design of the TS1101/03, the input amplifier was reconfigured for fully differential input/output operation and a second low-threshold p-channel FET (M2) was added where the drain terminal of M2 is also connected to R_{OUT}. Therefore, the behavior of the TS1101/03 for when $V_{RS-} > V_{RS+}$ is identical for when $V_{RS+} > V_{RS-}$.

Referring to the typical application circuit, the inputs of the op-amp based circuit are connected across an external R_{SENSE} resistor that is used to measure load current. At the non-inverting input of the current-sense amplifier (the RS+ terminal), the applied voltage is $I_{LOAD} \times R_{SENSE}$. Since the RS– terminal is the non-inverting input of the internal op-amp, op-amp feedback action forces the inverting input of the internal op-amp to the same potential. Therefore, the voltage drop across R_{SENSE} (V_{SENSE}) and the voltage drop across R_{GAINA} (at the RS+ terminal) are equal. Necessary for gain ratio matched, both R_{GAINA} and R_{GAINB} are the same value.

Since p-channel M1's source is connected to the inverting input of the internal op amp and since the voltage drop across R_{GAINA} is the same as the external V_{SENSE}, op amp feedback action drives the gate of M1 such that M1's drain-source current is equal to:

$$I_{DS(M1)} = \frac{V_{SENSE}}{R_{GAINA}}$$

or

$$I_{DS(M1)} = \frac{I_{LOAD} \times R_{SENSE}}{R_{GAINA}}$$

Since M1's drain terminal is connected to R_{OUT}, the output voltage of the current-sense amplifier at the OUT terminal is, therefore:

$$V_{OUT} = I_{LOAD} \times R_{SENSE} \times \frac{R_{OUT}}{R_{GAINA}}$$

For the TS1101 and TS1103, when the voltage at the RS– terminal is greater than the voltage at the RS+ terminal, the external VSENSE voltage drop is impressed upon R_{GAINB}. The voltage drop across R_{GAINB} is then converted into a current by M2 that then produces an output voltage across R_{OUT}. In this design, when M1 is conducting current ($V_{RS+} > V_{RS-}$), the TS1101/03's internal amplifier holds M2 OFF. When M2 is conducting current ($V_{RS-} > V_{RS+}$), the internal amplifier holds M1 OFF. In either case, the disabled FET does not contribute to the resultant output voltage.

The current-sense amplifier's gain accuracy is therefore the ratio match of R_{OUT} to $R_{GAIN[A/B]}$. For each of the four gain options available, Table 1 lists the values for R_{OUT} and $R_{GAIN[A/B]}$. The TS1101's output stage is protected against input overdrive by use of an output current-limiting circuit of 3 mA (typical) and a 7 V internal clamp protection circuit.

2.3 SIGN Comparator Output

As shown in the TS1101/03's block diagram, the design of the TS1101/03 incorporated one additional feature: an analog comparator whose inputs monitor the internal amplifier's differential output voltage. While the voltage at the TS1101/03's OUT terminal indicates the magnitude of the load current, the TS1101/03's SIGN output indicates the load current's direction. The SIGN output is a logic high when M1 is conducting current ($V_{RS+} > V_{RS-}$). Alternatively, the SIGN output is a logic low when M2 is conducting current ($V_{RS+} < V_{RS-}$). The SIGN comparator's transfer characteristic is illustrated in the figure below. Unlike other current-sense amplifiers that implement a OUT/ SIGN arrangement, the TS1101/03 exhibits no "dead zone" at I_{LOAD} switchover. The other attribute of the SIGN comparator's behavior is its propagation delay as a function of applied V_{SENSE} [($V_{RS+} - V_{RS-}$) or ($V_{RS-} - V_{RS+}$)]. As shown below, the SIGN comparator's propagation delay behavior is symmetric regardless of current-flow direction and is inversely proportional to V_{SENSE}.

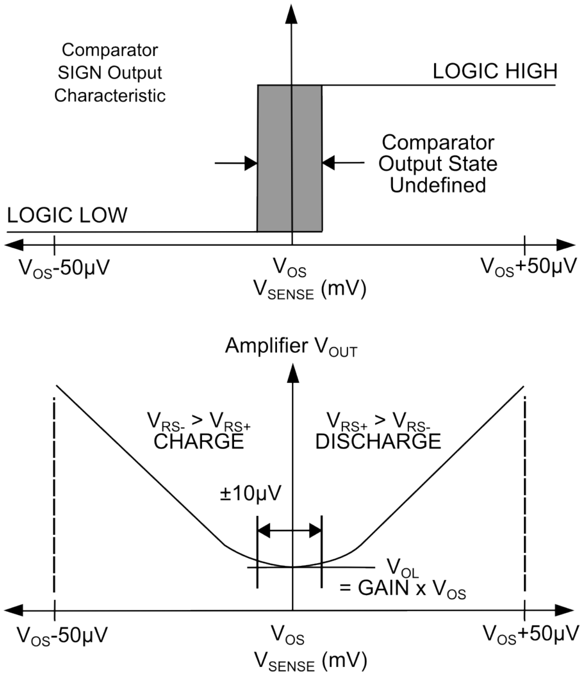


Figure 2.3. SIGN Comparator Transfer Characteristic and Propagation Delay

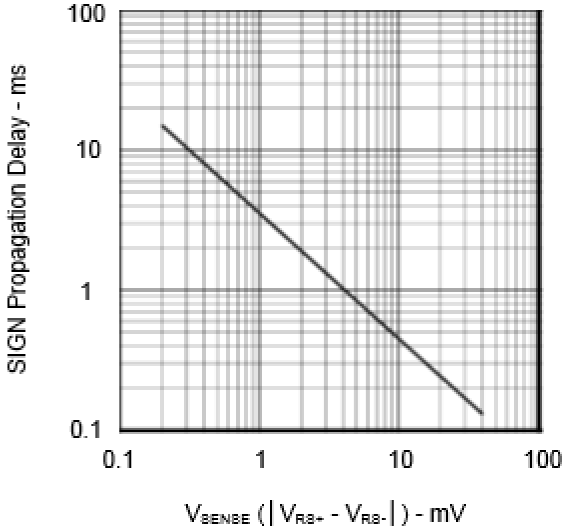


Figure 2.4. SIGN Comparator Propagation Delay vs. V_{SENSE}

2.4 Choosing the Sense Resistor

Selecting the optimal value for the external RSENSE is based on the following criteria and for each commentary follows:

1. R_{SENSE} Voltage Loss
2. V_{OUT} Swing vs. Applied Input Voltage at V_{RS+} and Desired V_{SENSE}
3. Total I_{LOAD} Accuracy
4. Circuit Efficiency and Power Dissipation
5. R_{SENSE} Kelvin Connections

2.4.1 R_{SENSE} Voltage Loss

For the lowest IR power dissipation in R_{SENSE}, the smallest usable resistor value for R_{SENSE} should be selected.

2.4.2 V_{OUT} Swing vs. Applied Input Voltage at V_{RS+} and Desired V_{SENSE}

As there is no separate power supply pin for the current-sense amplifiers, the circuit draws its power from the voltage at its RS+ and RS- terminals. Therefore, the signal voltage at the OUT terminal is bounded by the minimum voltage applied at the RS+ terminal.

Therefore:

$$V_{OUT}(\max) = V_{RS+}(\min) - V_{SENSE}(\max) - V_{OH}(\max)$$

and

$$R_{SENSE} < \frac{V_{OUT}(\max)}{GAIN \times I_{LOAD}(\max)}$$

where the full-scale V_{SENSE} should be less than $V_{OUT(MAX)}$/GAIN at the application's minimum RS+ terminal voltage. For best performance with a 3.6 V power supply, R_{SENSE} should be chosen to generate a V_{SENSE} of: a) 120 mV (for the 25 V/V GAIN option), b) 60 mV (for the 50 V/V GAIN option), c) 30 mV (for the 100 V/V GAIN option), or d) 15 mV (for the 200 V/V GAIN option) at the full-scale I_{LOAD} current in each application. For the case where the minimum power supply voltage is higher than 3.6 V, each of the four full-scale V_{SENSE}s above can be increased.

2.4.3 Total Load Current Accuracy

In the current-sense amplifiers' linear region where $V_{OUT} < V_{OUT(max)}$, there are two specifications related to the circuit's accuracy: a) the input offset voltage and b) gain error (GE(max) = 0.6%). An expression for the current sense amplifiers' total error is given by:

$$V_{OUT} = \left[GAIN \times (1 \pm GE) \times V_{SENSE}\right] \pm (GAIN \times V_{OS})$$

A large value for R_{SENSE} permits the use of smaller load currents to be measured more accurately because the effects of offset voltages are less significant when compared to larger V_{SENSE} voltages. Due care though should be exercised as previously mentioned with large values of R_{SENSE}.

2.4.4 Circuit Efficiency and Power Dissipation

IR losses in R_{SENSE} can be large especially at high load currents. It is important to select the smallest, usable R_{SENSE} value to minimize power dissipation and to keep the physical size of R_{SENSE} small. If the external R_{SENSE} is allowed to dissipate significant power, then its inherent temperature coefficient may alter its design center value, thereby reducing load current measurement accuracy. Precisely because the current-sense amplifiers input stages were designed to exhibit a very low input offset voltage, small R_{SENSE} values can be used to reduce power dissipation and minimize local hot spots on the PCB.

2.4.5 R_{SENSE} Kelvin Connections

For optimal V_{SENSE} accuracy in the presence of large load currents, parasitic PCB track resistance should be minimized. Kelvin-sense PCB connections between R_{SENSE} and the current-sense amplifier's RS+ and RS– terminals are strongly recommended. The drawing below illustrates the connections between the current-sense amplifier and the current-sense resistor. The PCB layout should be balanced and symmetrical to minimize wiring-induced errors. In addition, the pcb layout for R_{SENSE} should include good thermal management techniques for optimal R_{SENSE} power dissipation.

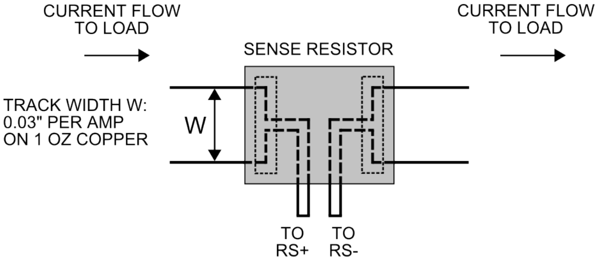


Figure 2.5. Making PCB Connections to R_{SENSE}

2.4.6 R_{SENSE} Composition

Current-shunt resistors are available in metal film, metal strip, and wire-wound constructions. Wire-wound current-shunt resistors consist of a wire spirally wound onto a core. As a result, these types of current shunt resistors exhibit the largest self inductance. In applications where the load current contains high-frequency transients, metal film or metal strip current-sense resistors are recommended.

2.4.7 Internal Noise Filter

In power management and motor control applications, current-sense amplifiers are required to measure load currents accurately in the presence of both externally-generated differential and common-mode noise. An example of differential-mode noise that can appear at the inputs of a current-sense amplifier is high-frequency ripple. High-frequency ripple (whether introduced into the circuit inductively or capacitively) can produce a differential-mode voltage drop across the external current-shunt resistor (R_{SENSE}). An example of externally-generated, common-mode noise is the high-frequency output ripple of a switching regulator that can result in the injection of common-mode noise into both inputs of a current-sense amplifier.

Even though the load current signal bandwidth is dc, the input stage of any current-sense amplifier can rectify unwanted out-of-band noise that can result in an apparent error voltage at its output. This rectification of noise signals occurs because all amplifier input stages are constructed with transistors that can behave as high-frequency signal detectors in the same way P–N junction diodes were used as RF envelope detectors in early radio designs. The amplifier's internal common-mode rejection is usually sufficient to defeat injected common-mode noise.

To counter the effects of externally-injected noise, it has always been good engineering practice to add external low-pass filters in series with the inputs of a current-sense amplifier. In the design of discrete current-sense amplifiers, resistors used in the external low-pass filters were incorporated into the circuit's overall design to compensate for any input-bias-current-generated offset voltage and gain errors.

With the advent of monolithic current-sense amplifiers, the addition of external low-pass filters in series with the current-sense amplifier's inputs only introduces additional offset voltage and gain errors. To minimize or altogether eliminate the need for external low-pass filters and to maintain low input offset voltage and gain errors, the current-sense amplifiers incorporate a 50 kHz (typ) 2nd-order differential low-pass filter as shown in the Block Diagrams.

2.4.8 Output Filter Capacitor

If the current-sense amplifiers are a part of a signal acquisition system in which their OUT terminal is connected to the input of an ADC with an internal, switched-capacitor track-and-hold circuit, the internal track-and-hold's sampling capacitor can cause voltage droop at V_{OUT}. A good-quality 22 to 100 nF ceramic capacitor from the OUT terminal to GND forms a low-pass filter with the current-sense amplifier's R_{OUT} and should be used to minimize voltage droop (holding VOUT constant during the sample interval. Using a capacitor on the OUT terminal will also reduce the small-signal bandwidth as well as band-limiting amplifier noise.

2.4.9 PC Board Layout and Power Supply Bypassing

For optimal circuit performance, the current-sense amplifiers should be in very close proximity to the external current-sense resistor, and the PCB tracks from R_{SENSE} to the RS+ and the RS– input terminals should be short and symmetric. Also recommended are a ground plane and surface mount resistors and capacitors.

3. Electrical Characteristics

Table 3.1. Recommended Operating Conditions[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
System Specifications						
Operating Voltage Range	VDD		1.25		5.5	V
Common-Mode Input Range	V_{CM}	V_{RS+}, Guaranteed by CMRR	2		27	V

Note:

1. All devices 100% production tested at T_A = +25 °C. Limits over Temperature are guaranteed by design and characterization.

Table 3.2. DC Characteristics[1]

Parameter	Symbol	Conditions		Min	Typ	Max	Units
System Specifications							
No Load Input Supply Current	$I_{RS+} + I_{RS-}$[2]	T_A = +25 °C		—	0.68	0.85	µA
				—	—	1.0	
		V_{RS+} = 25 V	T_A = +25 °C	—	—	1.0	
				—	—	1.2	
	I_{VDD}			—	0.02	0.2	
Current Sense Amplifier							
Common Mode Rejection Ratio	CMRR	2 V < V_{RS+} < 27 V		120	130	—	dB
Input Offset Voltage[3]	V_{OS}	TS1100 and TS1101	T_A = +25 °C	—	±30	±100	µV
			–40 °C < TA < +85 °C	—	—	±200	
		TS1102 and TS1103	T_A = +25 °C	—	±30	±200	
			–40 °C < T_A < + 85 °C	—	—	±300	
V_{OS} Hysteresis[4]	V_{HYS}	T_A = +25 °C		—	10	—	µV
Gain	G	TS1100, TS1101, TS1102, TS1103	TS110x-25	—	25	—	V/V
			TS110x-50	—	50	—	
			TS110x-100	—	100	—	
			TS110x-200	—	200	—	
Gain Error[5]	GE	T_A = +25 °C		—	±0.1	±0.6	%
		–40 °C < T_A < +85 °C		—		±1	%
Gain Match[5]	GM	T_A = +25 °C		—	±0.2	±0.6	%
		–40 °C < T_A < +85 °C		—		±1	%
Output Resistance[6]	R_{OUT}	TS110x-25/50/100		28.0	40.0	52	kΩ
		TS110x-200		14.0	20.0	26.4	

Parameter	Symbol	Conditions		Min	Typ	Max	Units
OUT Low Voltage	V_{AOL}	TS1100 and TS1101	Gain = 25	—	—	5	mV
			Gain = 50	—	—	10	
			Gain = 100	—	—	20	
			Gain = 200	—	—	40	
		TS1102 and TS1103	Gain = 25	—	—	7.5	
			Gain = 50	—	—	15	
			Gain = 100	—	—	30	
			Gain = 200	—	—	60	
OUT High Voltage	V_{AOH}	$V_{OH} = V_{RS-} – V_{OUT}$		—	0.05	0.2	V
Sign Comparator Parameters (TS1106 Only)							
Output Low Voltage	V_{COL}	VDD = 1.25 V, I_{SINK} = 5 µA		—		0.2	V
		VDD = 1.8 V, I_{SINK} = 35 µA		—	—		
Output High Voltage	V_{COH}	VDD = 1.25 V, I_{SOURCE} = 5 µA		VDD – 0.2	—	—	V
		VDD = 1.8 V, I_{SOURCE} = 35 µA			—	—	

Notes:

1. V_{RS+} = 3.6 V; V_{SENSE} = (V_{RS+} – $V_{RS–}$) = 0 V; C_{OUT} = 47 nF; V_{DD} = 1.8 V; T_A = –40 °C to +105 °C, unless otherwise noted. Typical values are at T_A = +25 °C.
2. Extrapolated to VOUT=0V. IRS++IRS- is the total current into the RS+ and the RS– pins.
3. Input offset voltage V_{OS} is extrapolated from a $V_{OUT(+)}$ measurement with V_{SENSE} set to +1 mV and a $V_{OUT(–)}$ measurement with VSENSE set to -1mV; vis-a-viz, Average V_{OS} = ($V_{OUT(–)}$ – $V_{OUT(+)}$)/(2 x GAIN).
4. Amplitude of V_{SENSE} lower or higher than V_{OS} required to cause the comparator to switch output states.
5. Gain error is calculated by applying two values for V_{SENSE} and then calculating the error of the actual slope vs. the ideal transfer characteristic. TS1100 and TS1102 only applies positive V_{SENSE} values.

   For GAIN = 25, the applied V_{SENSE} is 20 mV and 120 mV.

   For GAIN = 50, the applied V_{SENSE} is 10 mV and 60 mV.

   For GAIN = 100, the applied V_{SENSE} is 5 mV and 30 mV.

   For GAIN = 200, the applied V_{SENSE} is 2.5 mV and 15 mV.
6. The device is stable for any capacitance load at V_{OUT}.

Table 3.3. AC Characteristics[1]

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Current Sense Amplifier							
Output Settling time	t_{OUT_s}	1% Final value, VOUT = 3 V	Gain = 25, 50, 100	—	2.2	—	msec
			Gain = 200	—	4.3	—	msec
Sign Comparator Parameters (TS1101 and TS1103 Only)							
Propagation Delay	t_{SIGN_PD}	V_{SENSE} = ±1 mV		—	3	—	msec
		V_{SENSE} = ±10 mV		—	0.4	—	msec

Notes:

1. V_{RS+} = 3.6 V; V_{SENSE} = (V_{RS+} – $V_{RS–}$) = 0 V; C_{OUT} = 47 nF; V_{DD} = 1.8 V; T_A = –40 °C to +105 °C, unless otherwise noted. Typical values are at T_A = +25 °C.

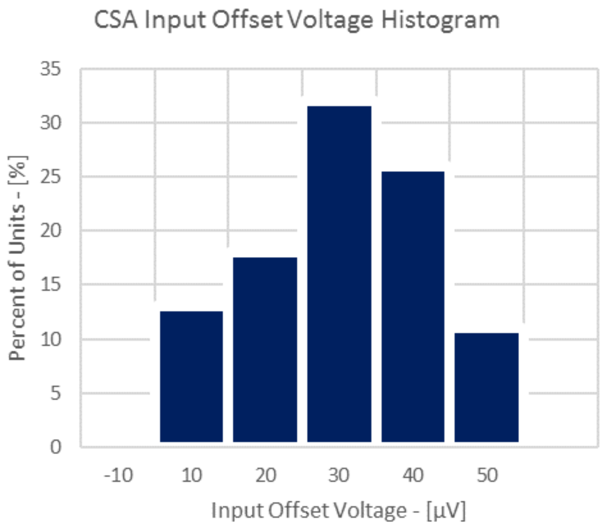
Table 3.4. Thermal Conditions

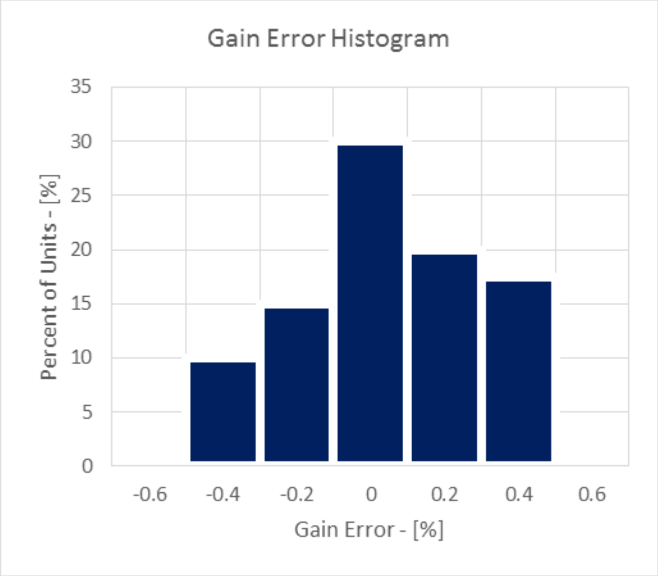
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Temperature Range	T_{OP}		–40	—	+105	°C

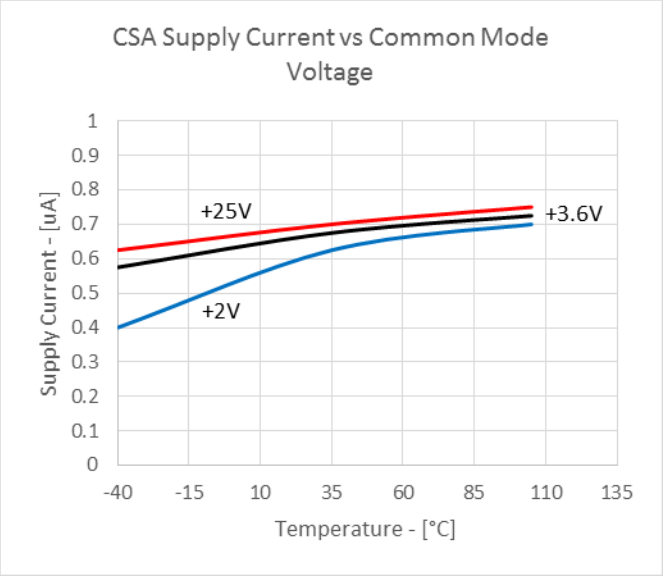
Table 3.5. Absolute Maximum Limits

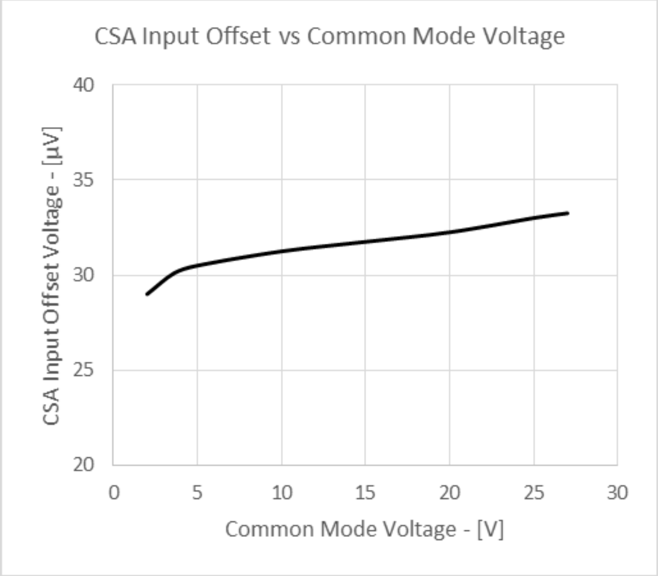
Parameter	Symbol	Conditions	Min	Typ	Max	Units
RS+ Voltage	V_{RS+}		–0.3	—	27	V
RS– Voltage	$V_{RS–}$		–0.3	—	27	V
Supply Voltage	VDD		–0.3	—	6	V
OUT Voltage	V_{OUT}		–0.3	—	6	V
SIGN Voltage (TS1106 Only)	V_{SIGN}		–0.3	—	6	V
RS+ to RS– Voltage	V_{RS+} – $V_{RS–}$		—	—	28	V
Short Circuit Duration: OUT to GND			—	—	Continuous	
Continuous Input Current (Any Pin)			–20	—	20	mA
Junction Temperature			—	—	150	°C
Storage Temperature Range			–65	—	150	°C
Lead Temperature (Soldering, 10 s)			—	—	300	°C
Soldering Temperature (Reflow)			—	—	260	°C
ESD Tolerance						
Human Body Model			—	—	2000	V
Machine Model			—	—	200	V

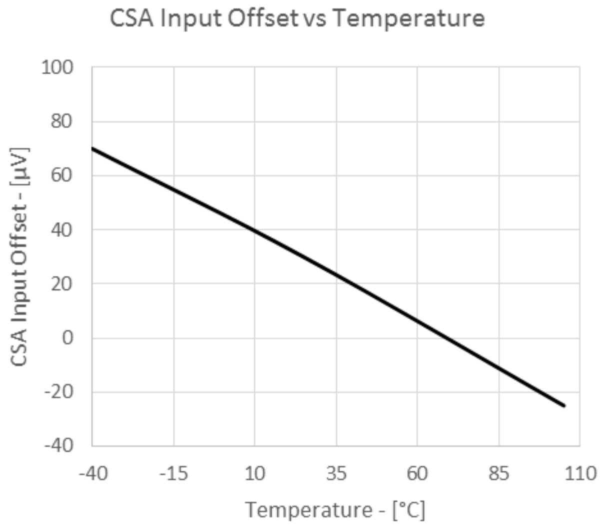
For the following graphs, $V_{RS+} = V_{RS-} = 3.6$ V; $T_A = +25$ C unless otherwise noted.

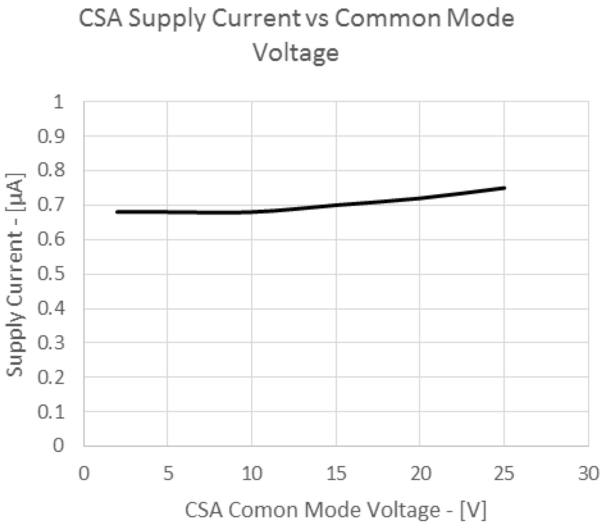


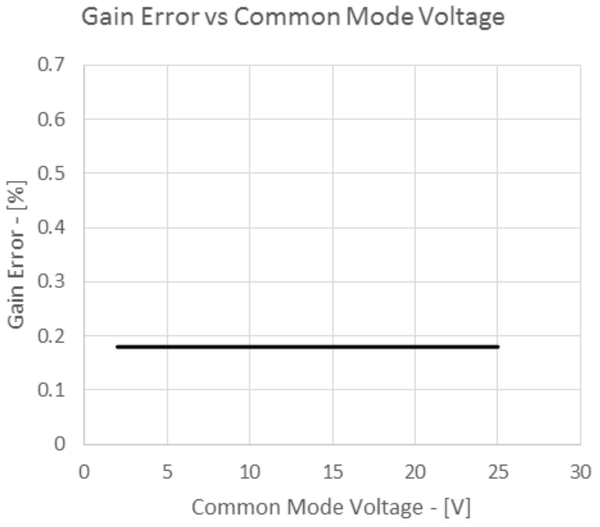


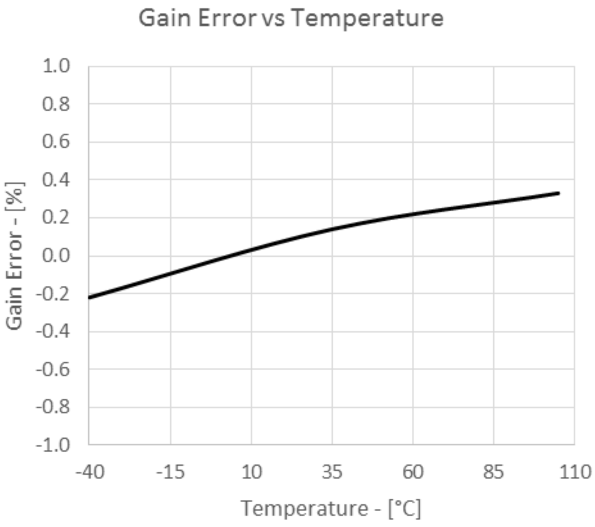


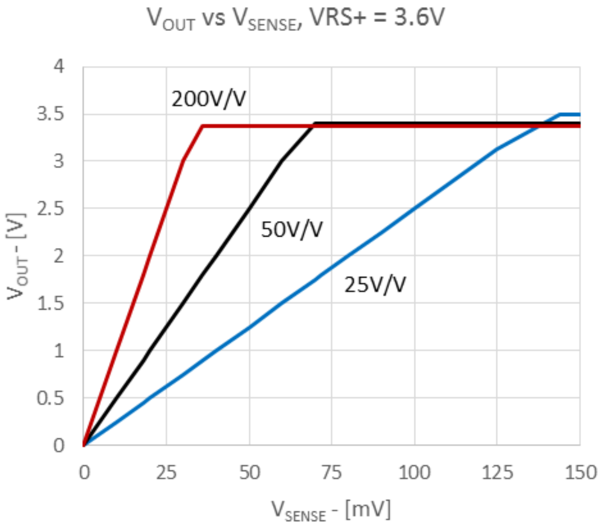


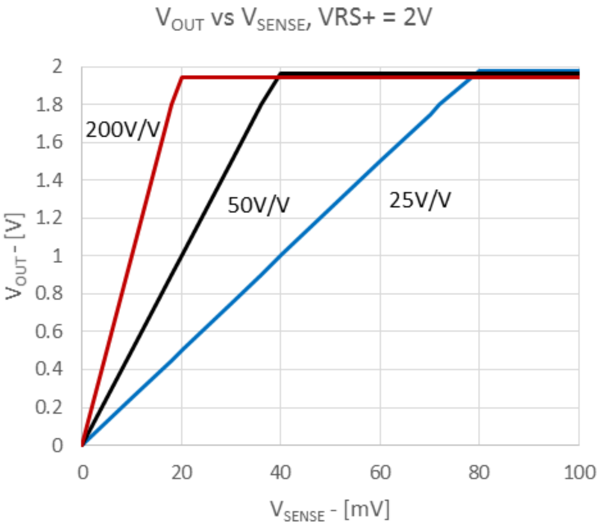


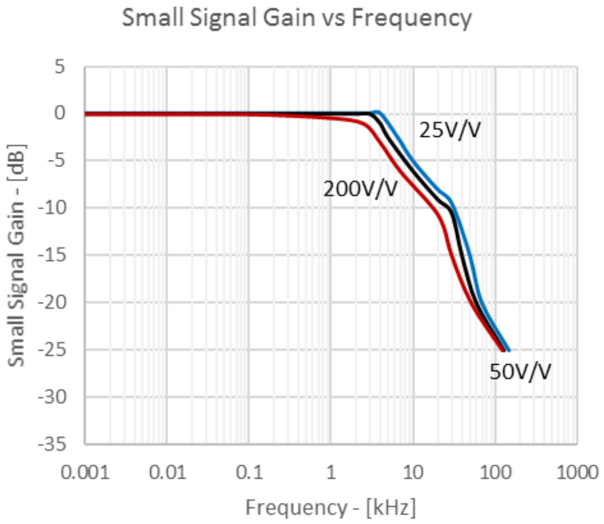


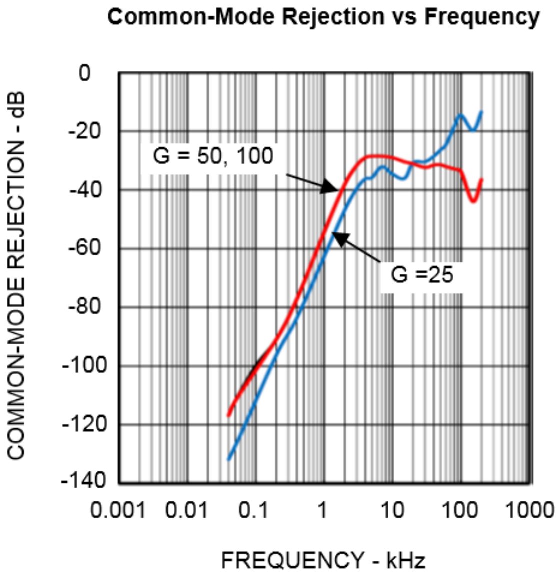

Gain Error vs Common Mode Voltage


Gain Error vs Temperature

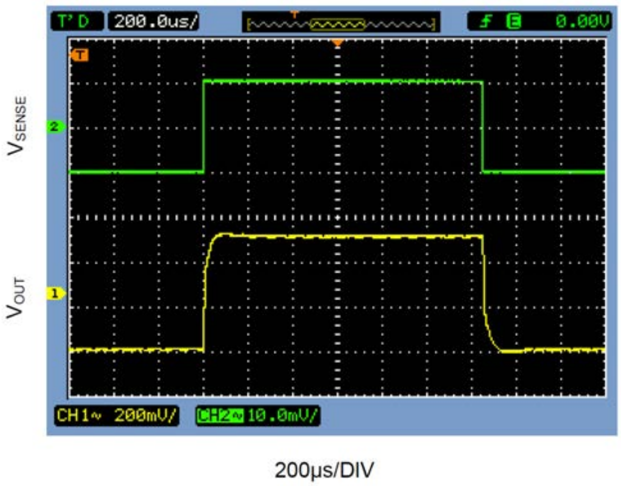

V_{OUT} vs V_{SENSE}, VRS+ = 3.6V


V_{OUT} vs V_{SENSE}, VRS+ = 2V

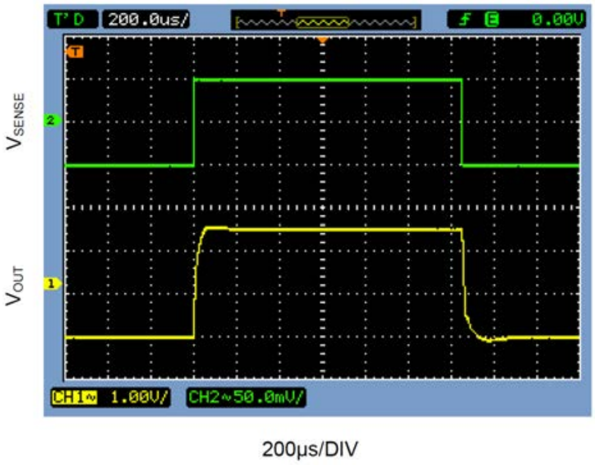

Small Signal Gain vs Frequency


Common-Mode Rejection vs Frequency

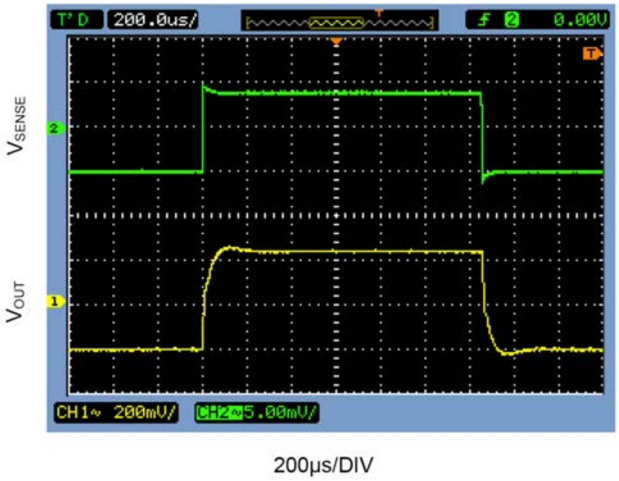
Small-Signal Pulse Response, Gain = 25



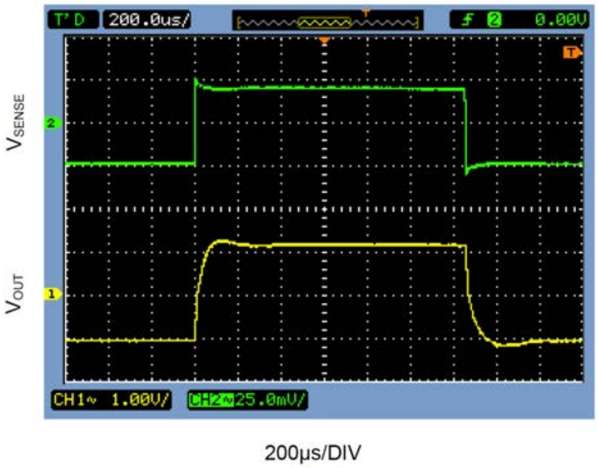
Large-Signal Pulse Response, Gain = 25



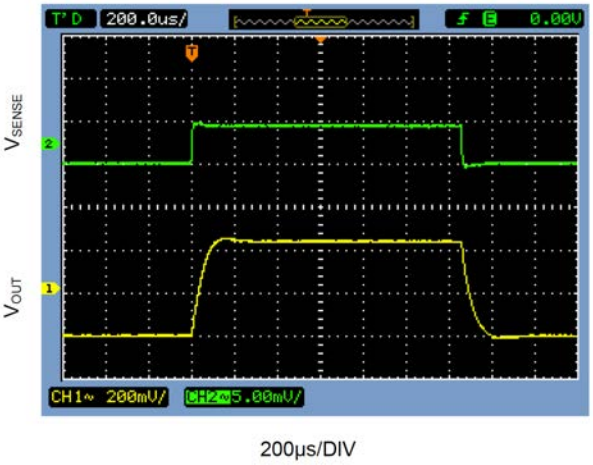
Small-Signal Pulse Response, Gain = 50



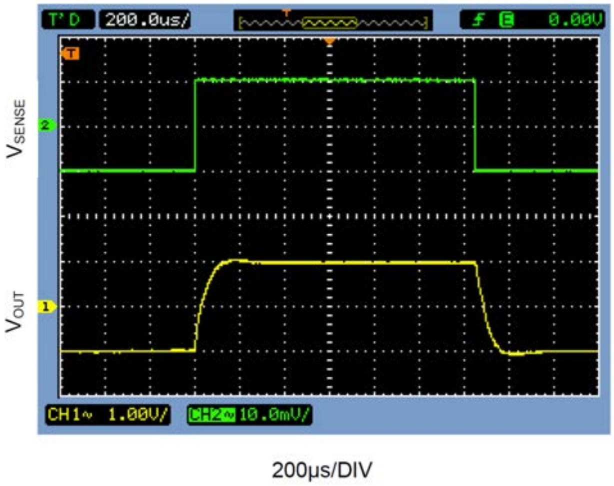
Large-Signal Pulse Response, Gain = 50



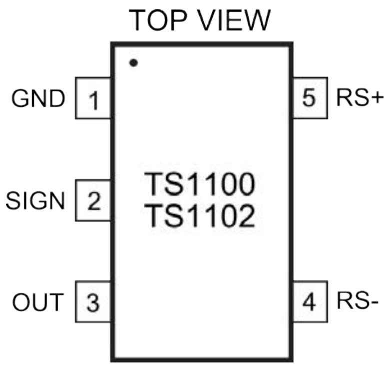
Small-Signal Pulse Response, Gain = 100



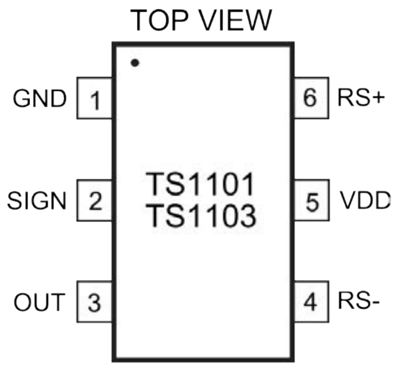
Large-Signal Pulse Response, Gain = 100



4. Pin Descriptions



SOT23-5
G6 Package



SOT23-6
G6 Package

Table 4.1. Pin Descriptions

Pin	Part Number	Label	Function
1	TS1100 TS1101 TS1102 TS1103	GND	Ground. Connect this pin to analog ground.
2	TS1100 TS1102	GND	Ground. Connect this pin to analog ground.
	TS1101 TS1103	SIGN	Comparator Output, push-pull; SIGN is HIGH for ($V_{RS+} > V_{RS-}$) and LOW for ($V_{RS-} > V_{RS+}$).
3	TS1100 TS1101 TS1102 TS1103	OUT	Output Voltage. V_{OUT} is proportional to $V_{SENSE} = (V_{RS+} - V_{RS-})$ or ($V_{RS-} - V_{RS+}$).
4	TS1100 TS1101 TS1102 TS1103	RS–	External Sense Resistor Load-Side Connection
5	TS1100 TS1102	RS+	External Sense Resistor Power-Side Connection
	TS1101 TS1103	VDD	SIGN Comparator External Power Supply Pin; Connect this pin to system's logic VDD supply.
6	TS1100 TS1102	N/A	N/A
	TS1101 TS1103	RS+	External Sense Resistor Power-Side Connection

5. Packaging

5.1 TS1100 and TS1102 Package Dimensions

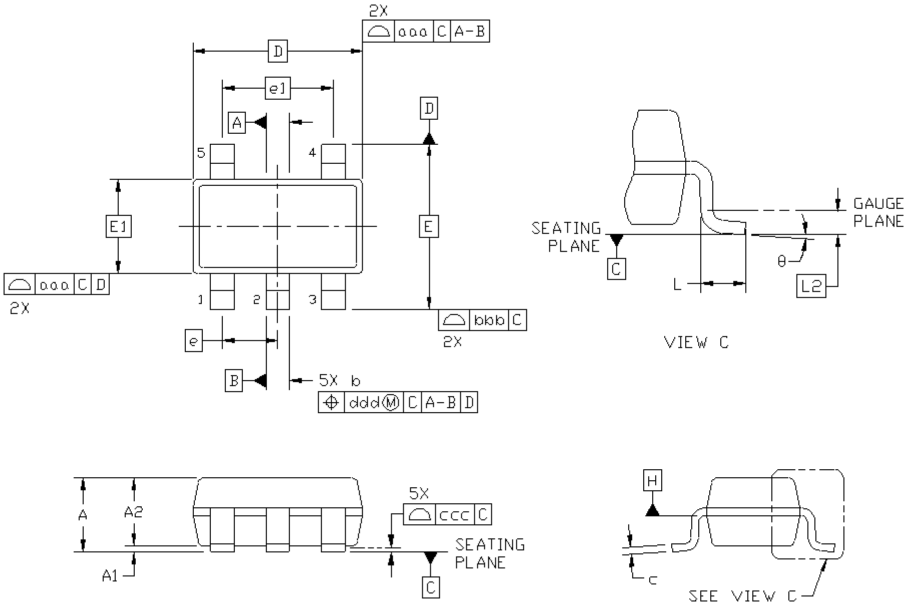


Figure 5.1. TS1100 and TS1102 Package Diagram

Table 5.1. TS1100 and TS1102 Package Dimensions

Dimension	Min	Max
A	—	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.30	0.50
c	0.09	0.20
D	2.90 BSC	
E	2.80 BSC	
E1	1.60 BSC	
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
L2	0.25 BSC	
θ	0°	8°
aaa	0.15	
bbb	0.20	
ccc	0.10	
ddd	0.20	

Dimension	Min	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.
4. This drawing conforms to the JEDEC Solid State Outline MO-178, Variation AA.

5.2 TS1101 and TS1103 Package Dimensions

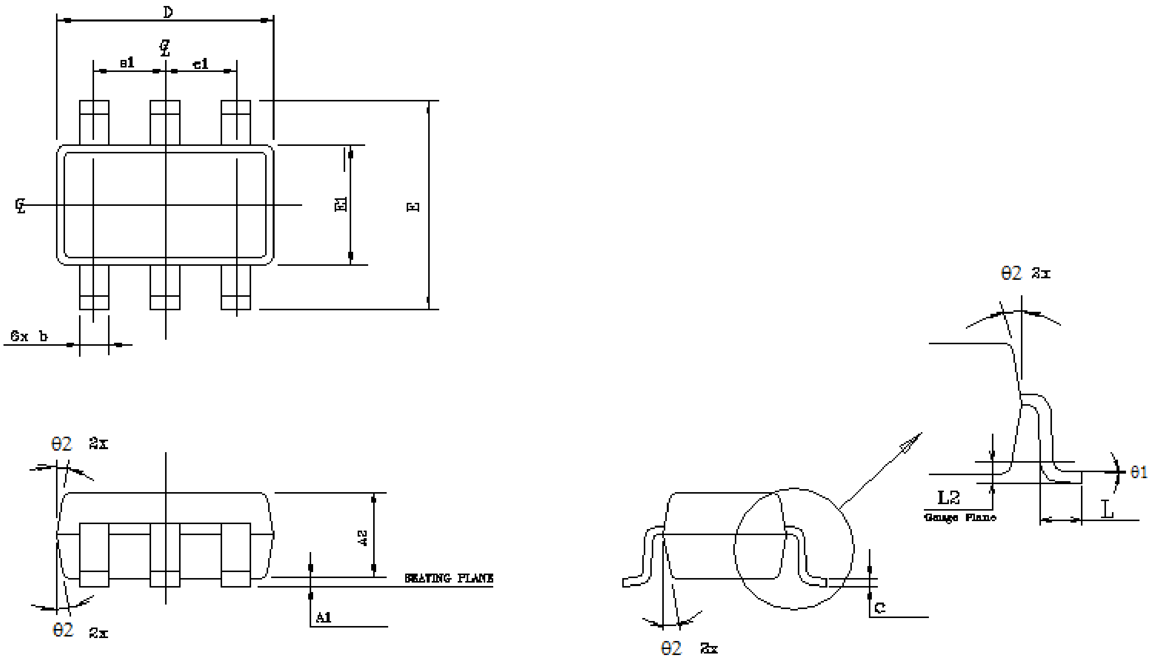


Figure 5.2. TS1101 and TS1103 Package Diagram

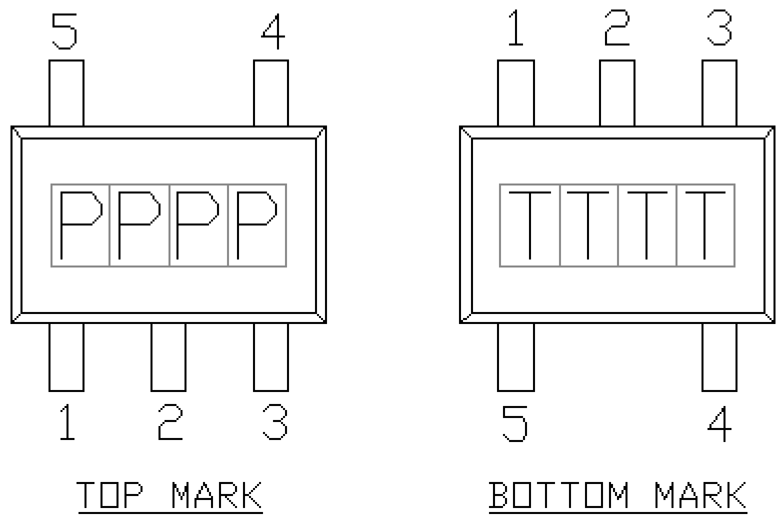
Table 5.2. TS1101 and TS1103 Package Dimensions

Dimension	Min	Max
A1	0.06	0.15
A2	1.00	1.30
b	0.35	0.50
c	0.127	
D	2.80	2.90
E	2.60	3.00
E1	1.50	1.70
e1	0.950 TYP	
L	0.35	0.55
L2	0.20 BSC	
θ1	0°	3°
θ2	10° TYP	

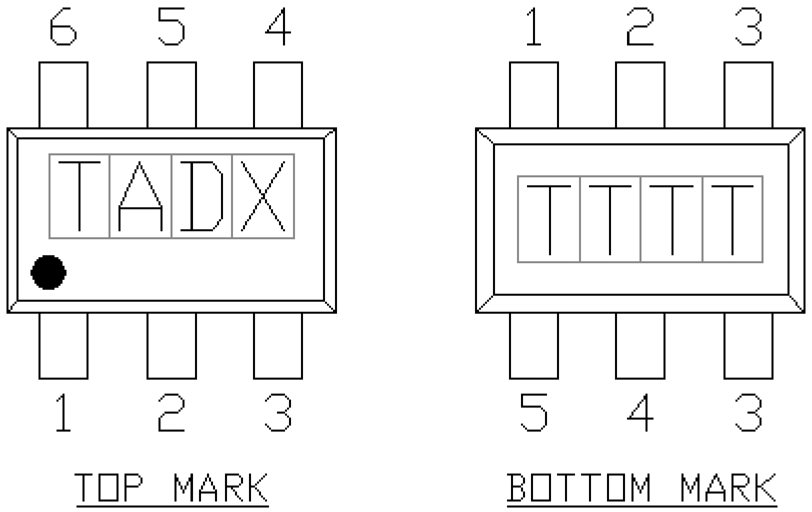
Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.
4. This drawing conforms to the JEDEC Solid State Outline MO-178, Variation AA.

6. Top and Bottom Marking: 5 and 6-Pin Packages



Mark Method:	Laser	
Font Size:	0.60 mm (24 mils)	
Line 1 Mark Format:	Device Identifier	TADT
Line 5 Backside:	TTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order Form



Mark Method:	Laser	
Font Size:	0.60 mm (24 mils)	
Line 1 Mark Format:	Device Identifier	TADT
Line 5 Backside:	TTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order Form

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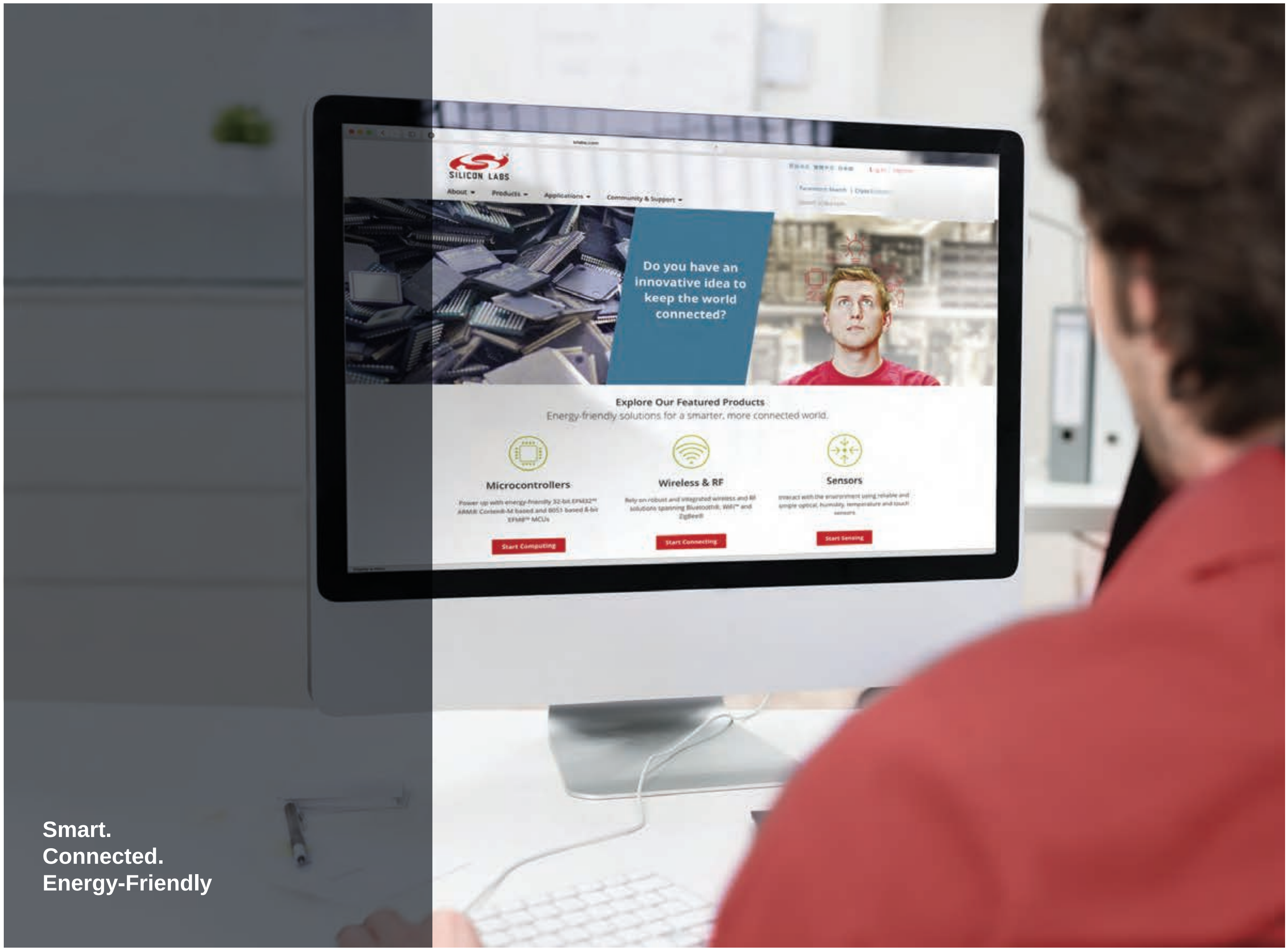

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